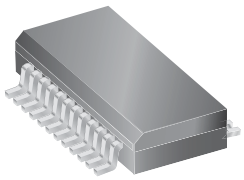
High Bandwidth, Fast Fault Response Current Sensor IC In Thermally Enhanced Package

Features and Benefits

- Industry-leading noise performance with 120 kHz bandwidth through proprietary amplifier and filter design techniques
- Integrated shield greatly reduces capacitive coupling from current conductor to die due to high dV/dt, and prevents offset drift in high-side applications
- Small footprint surface mount QSOP24 package
- 2100 VRMS isolation voltage between primary current path and sensor IC electronics
- 1.1 mΩ primary conductor resistance for low power loss
- User-settable Overcurrent Fault level
- Overcurrent Fault signal typically responds to an overcurrent condition in < 2 µs
- Filter pin capacitor sets analog signal bandwidth
- ±2% typical output error
- 3 to 5.5 V, single supply operation
- Factory trimmed sensitivity, quiescent output voltage, and associated temperature coefficients
- Chopper stabilization results in extremely stable quiescent output voltage
- Ratiometric output from supply voltage

Package: 24 pin QSOP (suffix LF)

Approximate Scale



Description

The Allegro™ ACS709 current sensor IC provides economical and precise means for current sensing applications in industrial, automotive, commercial, and communications systems. The device is offered in a small footprint surface mount package that allows easy implementation in customer applications.

The ACS709 consists of a precision linear Hall sensor integrated circuit with a copper conduction path located near the surface of the silicon die. Applied current flows through the copper conduction path, and the analog output voltage from the Hall sensor IC linearly tracks the magnetic field generated by the applied current. The accuracy of the ACS709 is maximized with this patented packaging configuration because the Hall element is situated in extremely close proximity to the current to be measured.

High level immunity to current conductor dV/dt and stray electric fields, offered by Allegro proprietary integrated shield technology, guarantees low output ripple and low offset drift in high-side applications.

The voltage on the Overcurrent Input (VOC pin) allows customers to define an overcurrent fault threshold for the device. When the current flowing through the copper conduction path (between the IP+ and IP– pins) exceeds this threshold,

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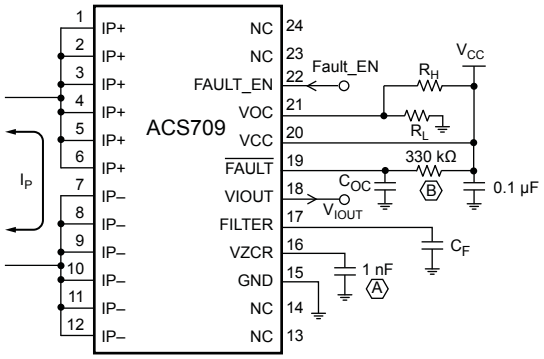
Typical Application



R_H, R_L	Sets resistor divider reference for V_{OC}
C_F	Noise and bandwidth limiting filter capacitor
C_{OC}	Fault delay setting capacitor, 22 nF maximum
(A)	Use of capacitor required
(B)	Use of resistor optional

Description (continued)

the open drain Overcurrent Fault pin will transition to a logic low state. Factory programming of the linear Hall sensor IC inside of the ACS709 results in exceptional accuracy in both analog and digital output signals.

The internal resistance of the copper path used for current sensing is typically 1.1 mΩ, for low power loss. Also, the current conduction path is electrically isolated from the low voltage device inputs and outputs. This allows the ACS709 family of sensor ICs to be used in applications requiring electrical isolation, without the use of opto-isolators or other costly isolation techniques.

Applications include:

- Motor control and protection
- Load management and overcurrent detection
- Power conversion and battery monitoring / UPS systems

Selection Guide

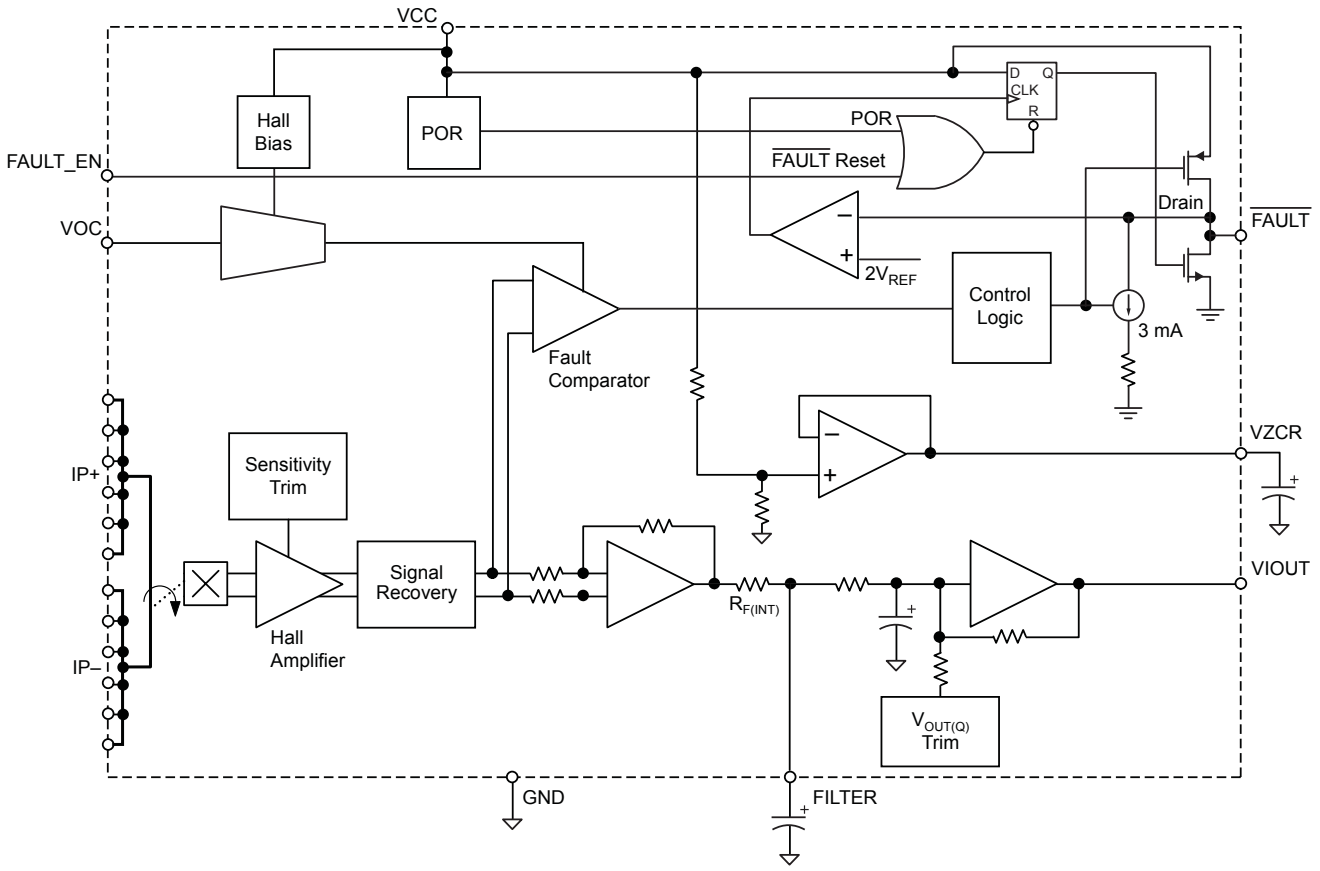
Part Number	$I_{P(LIN)}$ (A)	Sens (Typ at V_{CC} = 5 V) (mV/A)	T_A (°C)	Packing*
ACS709LLFTR-35BB-T	75	28	–40 to 150	Tape and Reel, 2500 pieces per reel
ACS709LLFTR-20BB-T	37.5	56		

*Contact Allegro for packing options.

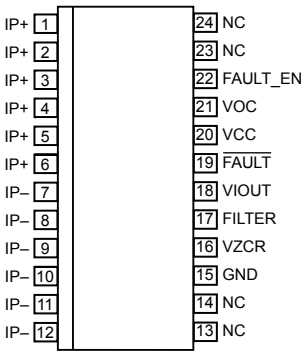
Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		8	V
Filter Pin	V_{FILTER}		8	V
Analog Output Pin	V_{IOUT}		32	V
Overcurrent Input Pin	V_{OC}		8	V
Overcurrent $\overline{\text{FAULT}}$ Pin	$V_{\overline{FAULT}}$		8	V
Fault Enable (FAULT_EN) Pin	$V_{FAULTEN}$		8	V
Voltage Reference Output Pin	V_{ZCR}		8	V
DC Reverse Voltage: Supply Voltage, Filter, Analog Output, Overcurrent Input, Overcurrent Fault, Fault Enable, and Voltage Reference Output Pins	V_{Rdcx}		–0.5	V
Rated Dielectric Insulation Voltage	V_{ISO}	60 Hz AC, 1 minute at T_A = 25°C	2100	VAC
Rated Continuous Voltage on Primary Leads (IP+ and IP–)	$V_{WORKING}$	For single protection according to UL 1577 standard; for higher continuous voltage ratings, please contact Allegro	277	VAC
Output Current Source	$I_{IOUT(Source)}$		3	mA
Output Current Sink	$I_{IOUT(Sink)}$		1	mA
Operating Ambient Temperature	T_A	Range L	–40 to 150	°C
Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

Functional Block Diagram



Pin-out Diagram



Terminal List Table

Number	Name	Description
1 through 6	IP+	Sensed current copper conduction path pins. Terminals for current being sensed; fused internally, loop to IP– pins; unidirectional or bidirectional current flow.
7 through 12	IP–	Sensed current copper conduction path pins. Terminals for current being sensed; fused internally, loop to IP+ pins; unidirectional or bidirectional current flow.
13, 14, 23, 24	NC	No connection
15	GND	Device ground connection.
16	VZCR	Voltage Reference Output pin. Zero current (0 A) reference; output voltage on this pin scales with V_{CC}.
17	FILTER	Filter pin. Terminal for an external capacitor connected from this pin to GND to set the device bandwidth.
18	VIOUT	Analog Output pin. Output voltage on this pin is proportional to current flowing through the loop between the IP+ pins and IP– pins.
19	$\overline{\text{FAULT}}$	Overcurrent Fault pin. When current flowing between IP+ pins and IP– pins exceeds the overcurrent fault threshold, this pin transitions to a logic low state.
20	VCC	Supply voltage.
21	VOC	Overcurrent Input pin. Analog input voltage on this pin sets the overcurrent fault threshold.
22	FAULT_EN	Enables overcurrent faulting when high. Resets $\overline{\text{FAULT}}$ when low.

COMMON OPERATING CHARACTERISTICS Valid at T_A = –40°C to 150°C, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
ELECTRICAL CHARACTERISTICS						
Supply Voltage[1]	V_{CC}		3	–	5.5	V
Nominal Supply Voltage	V_{CCN}		–	5	–	V
Supply Current	I_{CC}	VIOUT open, $\overline{\text{FAULT}}$ pin high	–	11	14.5	mA
Output Capacitance Load	C_{LOAD}	VIOUT pin to GND	–	–	10	nF
Output Resistive Load	R_{LOAD}	VIOUT pin to GND	10	–	–	kΩ
Magnetic Coupling from Device Conductor to Hall Element	MC_{HALL}	Current flowing from IP+ to IP– pins	–	9.5	–	G/A
Internal Filter Resistance[2]	$R_{F(INT)}$		–	1.7	–	kΩ
Primary Conductor Resistance	$R_{PRIMARY}$	T_A = 25°C	–	1.1	–	mΩ
ANALOG OUTPUT SIGNAL CHARACTERISTICS						
Full Range Linearity[3]	E_{LIN}	$I_P = \pm I_{P0A}$	–0.75	±0.25	0.75	%
Symmetry[4]	E_{SYM}	$I_P = \pm I_{P0A}$	99.1	100	100.9	%
Bidirectional Quiescent Output	$V_{OUT(QBI)}$	I_P = 0 A, T_A = 25°C	–	V_{CC}×0.5	–	V
TIMING PERFORMANCE CHARACTERISTICS						
VIOUT Signal Rise Time	t_r	T_A = 25°C, Swing I_P from 0 A to I_{P0A}, no capacitor on FILTER pin, 100 pF from VIOUT to GND	–	3	–	µs
VIOUT Signal Propagation Time	t_{PROP}	T_A = 25°C, no capacitor on FILTER pin, 100 pF from VIOUT to GND	–	1	–	µs
VIOUT Signal Response Time	$t_{RESPONSE}$	T_A = 25°C, Swing I_P from 0 A to I_{P0A}, no capacitor on FILTER pin, 100 pF from VIOUT to GND	–	4	–	µs
VIOUT Large Signal Bandwidth[5]	f_{3dB}	–3 dB, T_A = 25°C, no capacitor on FILTER pin, 100 pF from VIOUT to GND	–	120	–	kHz
Power-On Time	t_{PO}	Output reaches 90% of steady-state level, no capacitor on FILTER pin, T_A = 25°C	–	35	–	µs
OVERCURRENT CHARACTERISTICS						
Setting Voltage for Overcurrent Switchpoint[6]	V_{OC}		V_{CC}×0.25	–	V_{CC}×0.4	V
Signal Noise at Overcurrent Comparator Input	I_{NCOMP}		–	±1	–	A
Overcurrent Fault Switchpoint Error[7,8]	E_{OC}	Switchpoint in V_{OC} safe operating area; assumes I_{NCOMP} = 0 A	–	±5	–	%
Overcurrent $\overline{\text{FAULT}}$ Pin Output Voltage	$V_{\overline{FAULT}}$	1 mA sink current at $\overline{\text{FAULT}}$ pin	–	–	0.4	V
Fault Enable (FAULT_EN Pin) Input Low Voltage Threshold	V_{IL}		–	–	0.1 × V_{CC}	V
Fault Enable (FAULT_EN Pin) Input High Voltage Threshold	V_{IH}		0.8 × V_{CC}	–	–	V
Fault Enable (FAULT_EN Pin) Input Resistance	R_{FEI}		–	1	–	MΩ

Continued on the next page…

COMMON OPERATING CHARACTERISTICS (continued) Valid at T_A = –40°C to 150°C, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
OVERCURRENT CHARACTERISTICS (continued)						
Fault Enable (FAULT_EN Pin) Delay[9]	t_{FED}	Set FAULT_EN to low, V_{OC} = 0.25 × V_{CC}, C_{OC} = 0 F; then run a DC I_P exceeding the corresponding overcurrent threshold; then reset FAULT_EN from low to high and measure the delay from the rising edge of FAULT_EN to the falling edge of $\overline{FAULT}$	–	15	–	µs
Overcurrent Fault Response Time	t_{OC}	FAULT_EN set to high for a minimum of 20 µs before the overcurrent event; switchpoint set at V_{OC} = 0.25 × V_{CC}; delay from I_P exceeding overcurrent fault threshold to $V_{\overline{FAULT}}$ < 0.4 V, without external C_{OC} capacitor	–	1.9	–	µs
Overcurrent Fault Reset Delay	t_{OCR}	Time from $V_{FAULTEN}$ < V_{IL} to V_{FAULT} > 0.8 × V_{CC} , R_{PU} = 330 kΩ	–	500	–	ns
Overcurrent Fault Reset Hold Time	t_{OCH}	Time from $V_{FAULTEN}$ pin < V_{IL} to reset of fault latch; see Functional Block Diagram	–	250	–	ns
Overcurrent Input Pin Resistance	R_{OC}	T_A = 25°C, VOC pin to GND	2	–	–	MΩ
VOLTAGE REFERENCE CHARACTERISTICS						
Voltage Reference Output	V_{ZCR}	T_A = 25 °C	–	0.5 × V_{CC}	–	V
Voltage Reference Output Load Current	I_{ZCR}	Source current	3	–	–	mA
		Sink current	50	–	–	µA
Voltage Reference Output Drift	ΔV_{ZCR}		–	±10	–	mV

[1]Devices are trimmed for maximum accuracy at V_{CC} = 5 V. The ratiometry feature of the device allows operation over the full V_{CC} range; however, accuracy may be slightly degraded for V_{CC} values other than 5 V. Contact the Allegro factory for applications that require maximum accuracy for V_{CC} = 3.3 V.
[2]$R_{F(INT)}$ forms an RC circuit via the FILTER pin.
[3]This parameter can drift by as much as 0.25% over the lifetime of this product.
[4]This parameter can drift by as much as 0.3% over the lifetime of this product.
[5]Calculated using the formula f_{3dB} = 0.35 / t_r.
[6]See page 8 on how to set overcurrent fault switchpoint.
[7]Switchpoint can be lower at the expense of switchpoint accuracy.
[8]This error specification does not include the effect of noise. See the I_{NCOMP} specification in order to factor in the additional influence of noise on the fault switchpoint.
[9]Fault Enable Delay is designed to avoid false tripping of an Overcurrent (OC) fault at power-up. A 15 µs (typical) delay will always be needed, every time FAULT_EN is raised from low to high, before the device is ready for responding to any overcurrent event.

X20B PERFORMANCE CHARACTERISTICS, T_A Range L, valid at T_A = –40°C to 150°C, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	$I_{P(OA)}$		–20	–	20	A
Linear Sensing Range	$I_{P(LIN)}$		–37.5	–	37.5	A
Performance Characteristics at V_{CC} = 5 V						
Noise[1]	$V_{NOISE(rms)}$	T_A = 25°C, Sens = 56 mV/A, C_f = 0, C_{LOAD} = 4.7 nF, R_{LOAD} open	–	1.50	–	mV
Sensitivity[2,3]	Sens	I_P = 12.5 A, T_A = 25°C	–	56	–	mV/A
		I_P = 12.5 A, T_A = 25°C to 150°C	54.5	–	58	mV/A
		I_P = 12.5 A, T_A = –40°C to 25°C	54.5	–	58.5	mV/A
Electrical Offset Voltage[2]	V_{OE}	I_P = 0 A, T_A = 25°C	–	±5	–	mV
		I_P = 0 A, T_A = 25°C to 150°C	–25	–	25	mV
		I_P = 0 A, T_A = –40°C to 25°C	–40	–	40	mV
Total Output Error[2,4]	E_{TOT}	Tested at I_P =12.5 A, I_P applied for 5 ms, T_A = 25°C to 150°C	–	±2	–	%
		Tested at I_P =12.5 A, I_P applied for 5 ms, T_A = –40°C to 25°C	–	±3	–	%

[1]V_{pk-pk} noise (6 sigma noise) is equal to 6 × $V_{NOISE(rms)}$. Lower noise levels than this can be achieved by using C_f for applications requiring narrower bandwidth. See Characteristic Performance page for graphs of noise versus C_f and bandwidth versus C_f.
[2]See Characteristic Performance Data graphs for parameter distribution over ambient temperature range.
[3]This parameter can drift by as much as 1.75% over lifetime of the product.
[4]This parameter can drift by as much as 2.5% over lifetime of the product.

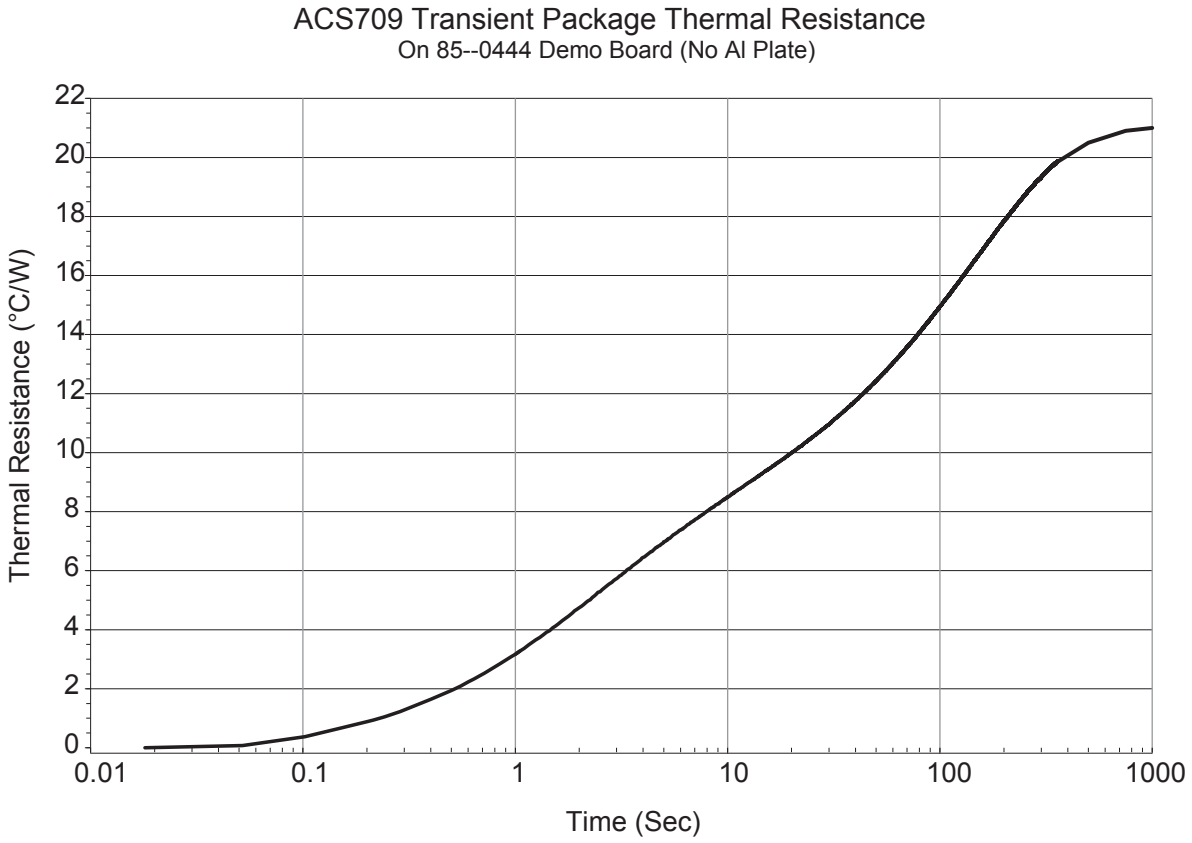
X35B PERFORMANCE CHARACTERISTICS, T_A Range L, valid at T_A = –40°C to 150°C, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	$I_{P(OA)}$		–37.5	–	37.5	A
Linear Sensing Range	$I_{P(LIN)}$		–75	–	75	A
Performance Characteristics at V_{CC} = 5 V						
Noise[1]	$V_{NOISE(rms)}$	T_A = 25°C, Sens = 28 mV/A, C_f = 0, C_{LOAD} = 4.7 nF, R_{LOAD} open	–	1	–	mV
Sensitivity[2,3]	Sens	I_P = 25 A, T_A = 25°C	–	28	–	mV/A
		I_P = 25 A, T_A = 25°C to 150°C	27	–	29.5	mV/A
		I_P = 25 A, T_A = –40°C to 25°C	27	–	29.5	mV/A
Electrical Offset Voltage[2]	V_{OE}	I_P = 0 A, T_A = 25°C	–	±5	–	mV
		I_P = 0 A, T_A = 25°C to 150°C	–25	–	25	mV
		I_P = 0 A, T_A = –40°C to 25°C	–40	–	40	mV
Total Output Error[2,4]	E_{TOT}	Tested at I_P = 25 A, I_P applied for 5 ms, T_A = 25°C to 150°C	–	±3	–	%
		Tested at I_P = 25 A, I_P applied for 5 ms, T_A = –40°C to 25°C	–	±3	–	%

[1]V_{pk-pk} noise (6 sigma noise) is equal to 6 × $V_{NOISE(rms)}$. Lower noise levels than this can be achieved by using C_f for applications requiring narrower bandwidth. See Characteristic Performance page for graphs of noise versus C_f and bandwidth versus C_f.
[2]See Characteristic Performance Data graphs for parameter distribution over ambient temperature range.
[3]This parameter can drift by as much as 1.75% over lifetime of the product.
[4]This parameter can drift by as much as 2.5% over lifetime of the product.

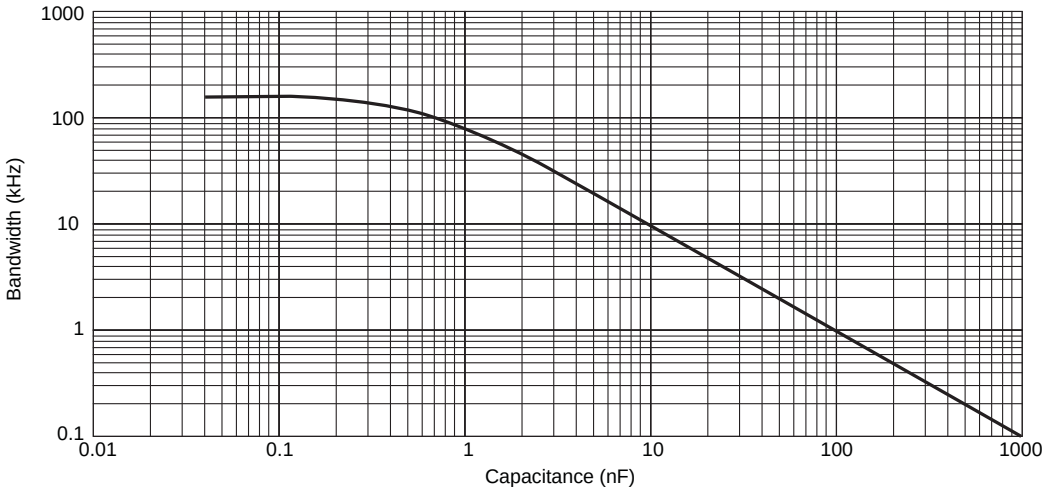
Thermal Characteristics

Characteristic	Symbol	Test Conditions	Value	Units
Steady State Package Thermal Resistance	$R_{\theta JA}$	Tested with 30 A DC current and based on ACS709 demo board in 1 cu. ft. of still air. Please refer to product FAQs page on Allegro web site for detailed information on ACS709 demo board.	21	°C/W
Transient Package Thermal Resistance	$R_{T\theta JA}$	Tested with 30 A DC current and based on ACS709 demo board in 1 cu. ft. of still air. Please refer to product FAQs page on Allegro web site for detailed information on ACS709 demo board.	See graph	°C/W

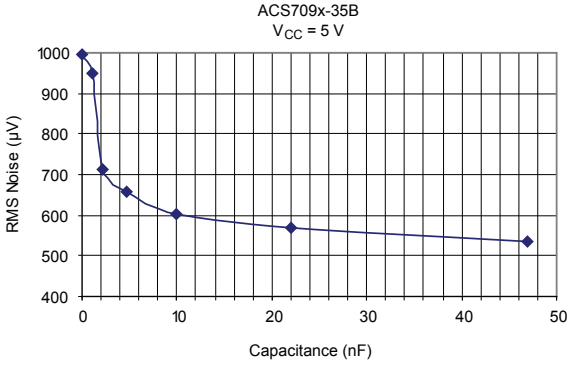


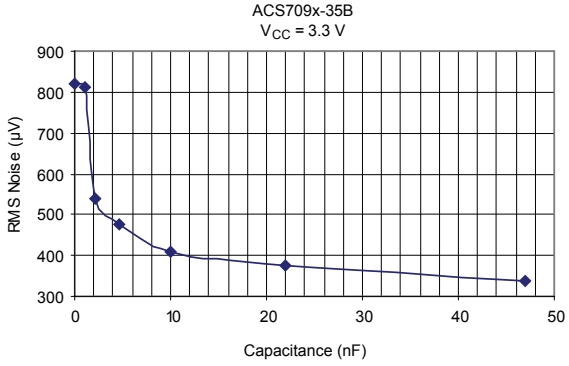
Characteristic Performance

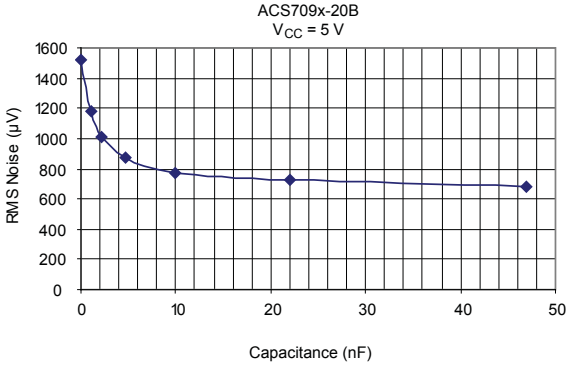
ACS709 Bandwidth versus External Capacitor Value, C_F
Capacitor connected between FILTER pin and GND

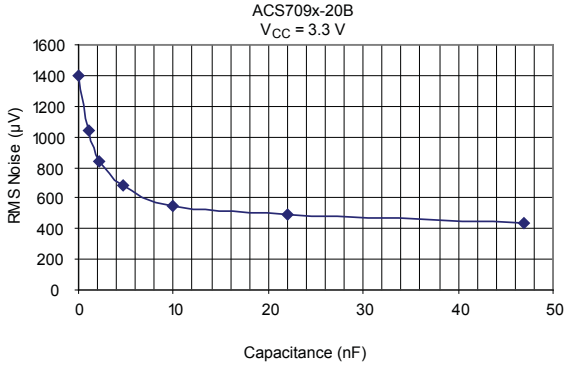


ACS709 Noise versus External Capacitor Value, C_F
Capacitor connected between FILTER pin and GND







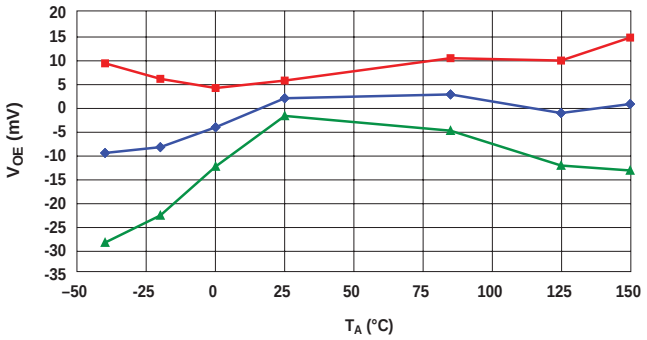


Characteristic Performance Data

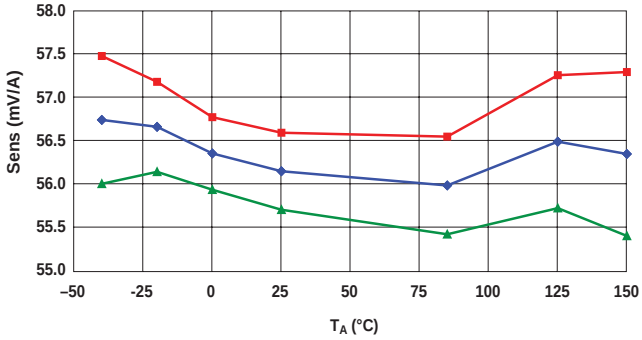
Data taken using the ACS709-20BB, V_{CC} = 5 V

Accuracy Data

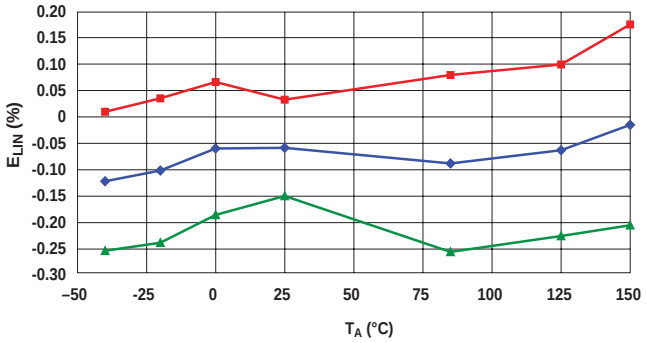
Electrical Offset Voltage versus Ambient Temperature



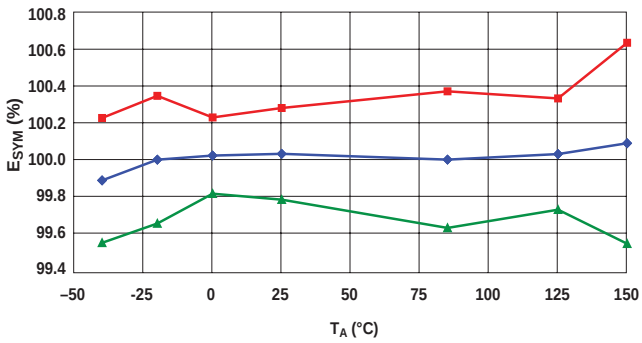
Sensitivity versus Ambient Temperature



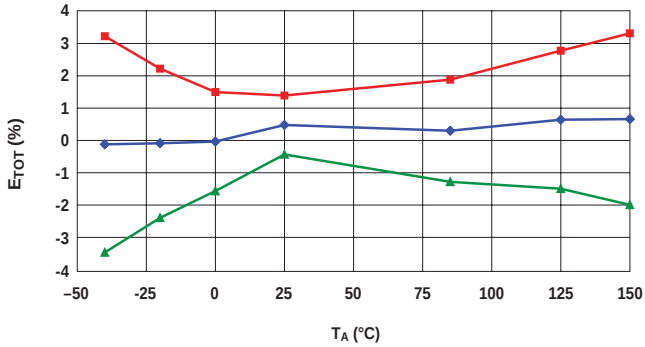
Nonlinearity versus Ambient Temperature

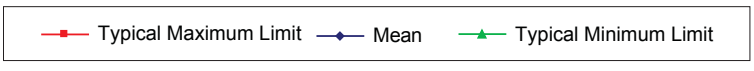


Symmetry versus Ambient Temperature



Total Output Error versus Ambient Temperature



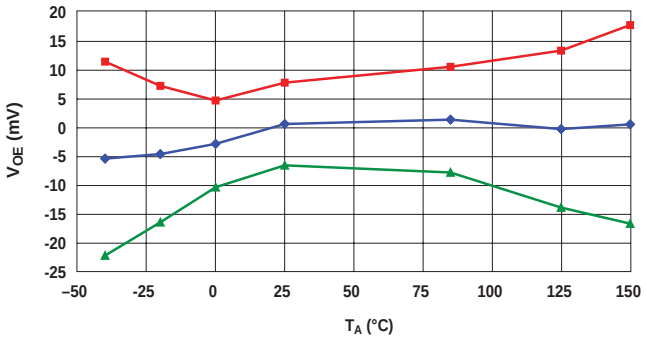


Characteristic Performance Data

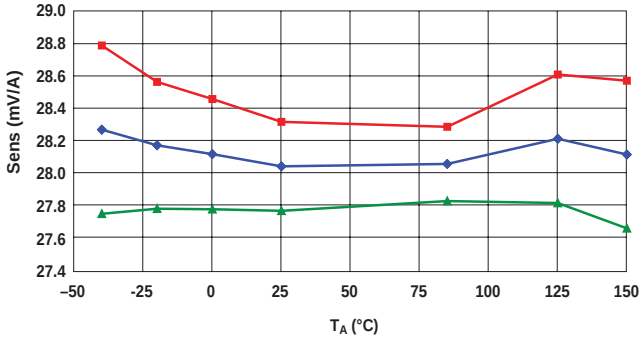
Data taken using the ACS709-35BB, V_{CC} = 5 V

Accuracy Data

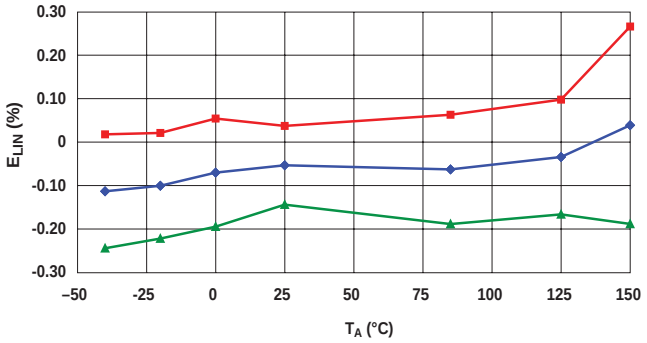
Electrical Offset Voltage versus Ambient Temperature



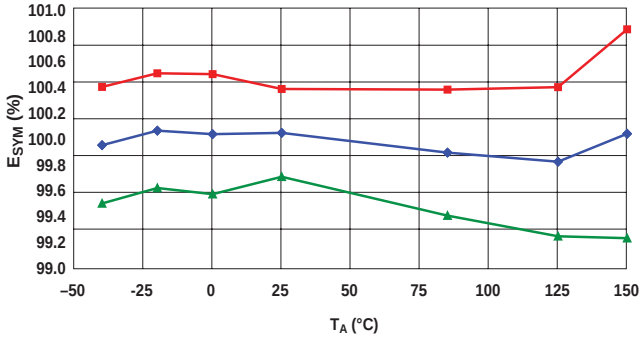
Sensitivity versus Ambient Temperature



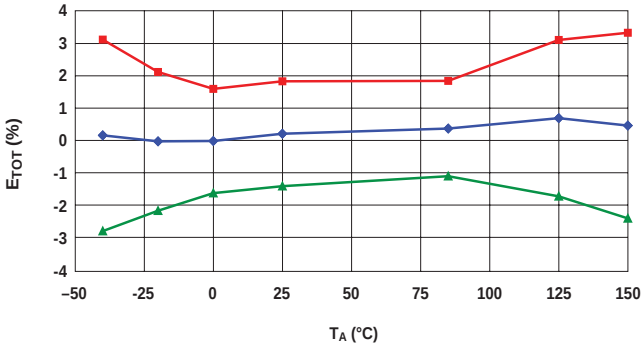
Nonlinearity versus Ambient Temperature

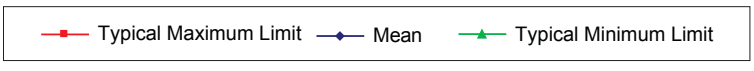


Symmetry versus Ambient Temperature



Total Output Error versus Ambient Temperature





Setting Overcurrent Fault Switchpoint

The V_{OC} needed for setting the overcurrent fault switchpoint can be calculated as follows:

$$V_{OC} = \text{Sens} \times |I_{OC}| \ ,$$

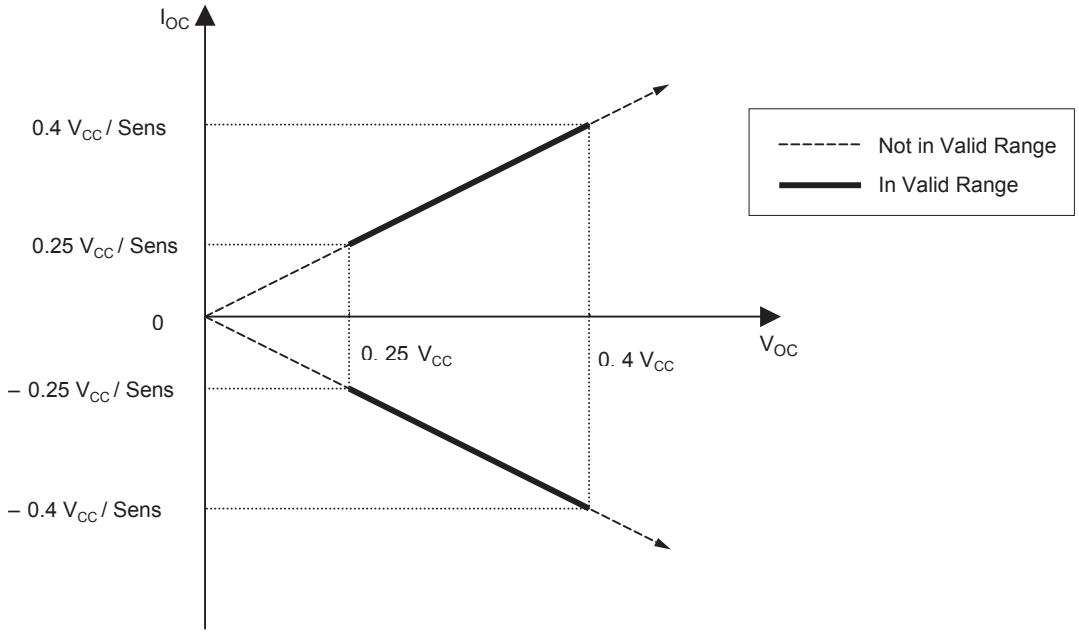
where V_{OC} is in mV, Sens in mV/A, and I_{OC} (overcurrent fault switchpoint) in A.

|Ioc | is the overcurrent fault switchpoint for a bi-directional (AC) current, which means a bi-directional device will have two symmetrical overcurrent fault switchpoints, $+I_{OC}$ and $-I_{OC}$.

See the following graph for I_{OC} and V_{OC} ranges.

I_{OC} versus V_{OC}

(20BB and 35BB Versions)



Example: For ACS709LLFTR-35BB-T, if required overcurrent fault switchpoint is 50 A, and V_{CC} = 5 V, then the required V_{OC} can be calculated as follows:

$$V_{OC} = \text{Sens} \times I_{OC} = 28 \times 50 = 1400 \text{ (mV)}$$

Functional Description

Overcurrent Fault Operation

The primary concern with high-speed fault detection is that noise may cause false tripping. Various applications have or need to be able to ignore certain faults that are due to switching noise or other parasitic phenomena, which are application dependant. The problem with simply trying to filter out this noise up front is that in high-speed applications, with asymmetric noise, the act of filtering introduces an error into the measurement. To get around this issue, and allow the user to prevent the fault signal from being latched by noise, a circuit was designed to slew the $\overline{\text{FAULT}}$ pin voltage based on the value of the capacitor from that pin to ground. Once the voltage on the pin falls below 2 V, as established by an internal reference, the fault output is latched and pulled to ground quickly with an internal N-channel MOSFET.

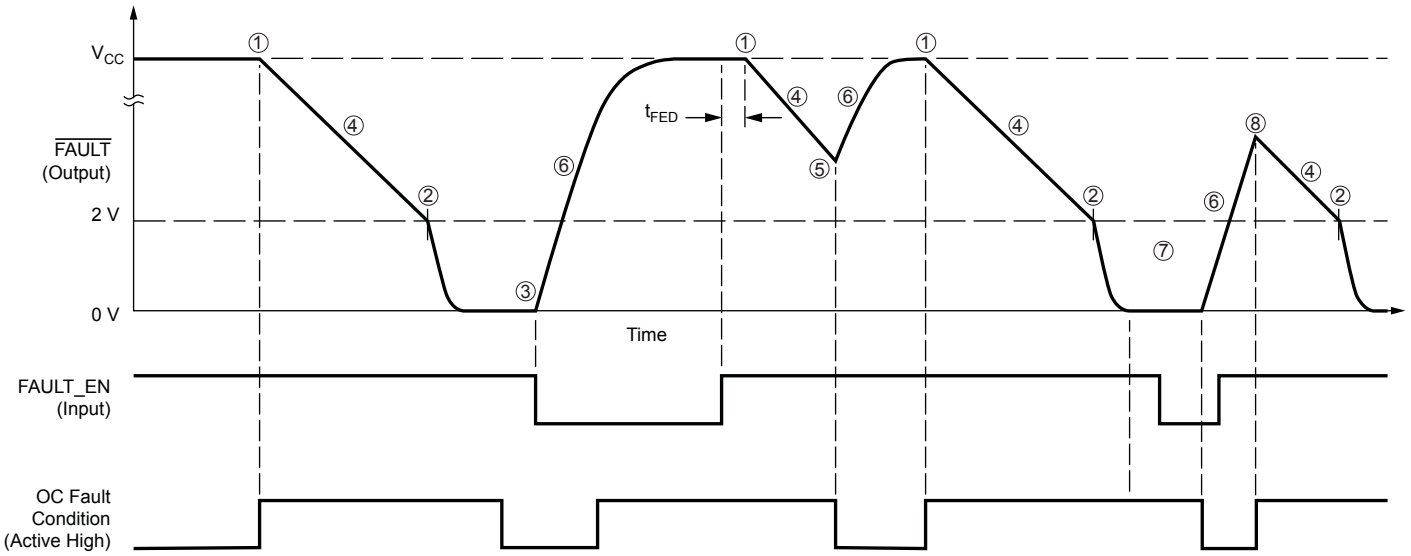
Fault Walk-through

The following walk-through references various sections and attributes in the figure below. This figure shows different fault set/reset scenarios and how they relate to the voltages on the $\overline{\text{FAULT}}$ pin, FAULT_EN pin, and the internal Overcurrent (OC) Fault node, which is invisible to the customer.

1. Because the device is enabled (FAULT_EN is high for a minimum period of time, the Fault Enable Delay, t_{FED}, 15 µs typical) and there is an OC fault condition, the device $\overline{\text{FAULT}}$ pin starts discharging.
2. When the $\overline{\text{FAULT}}$ pin voltage reaches approximately 2 V, the fault is latched, and an internal NMOS device pulls the $\overline{\text{FAULT}}$ pin voltage to approximately 0 V. The rate at which the $\overline{\text{FAULT}}$ pin slews downward (see [4] in the figure) is dependent on the external capacitor, C_{OC}, on the $\overline{\text{FAULT}}$ pin.
3. When the FAULT_EN pin is brought low, the $\overline{\text{FAULT}}$ pin starts resetting if no OC Fault condition exists. The internal NMOS pull-down turns off and an internal PMOS pull-up turns on (see [7] if the OC Fault condition still exists).
4. The slope, and thus the delay, on the fault is controlled by the capacitor, C_{OC}, placed on the $\overline{\text{FAULT}}$ pin to ground. During this portion of the fault (when the $\overline{\text{FAULT}}$ pin is between V_{CC} and 2 V), there is a 3 mA constant current sink, which discharges C_{OC}. The length of the fault delay, t, is equal to:

$$t = \frac{C_{OC} \times (V_{CC} - 2\text{ V})}{3\text{ mA}} \quad (1)$$

   where V_{CC} is the device power supply voltage.
5. The $\overline{\text{FAULT}}$ pin did not reach the 2 V latch point before the OC fault condition cleared. Because of this, the fixed 3 mA current sink turns off, and the internal PMOS pull-up turns on to recharge C_{OC} through the $\overline{\text{FAULT}}$ pin.

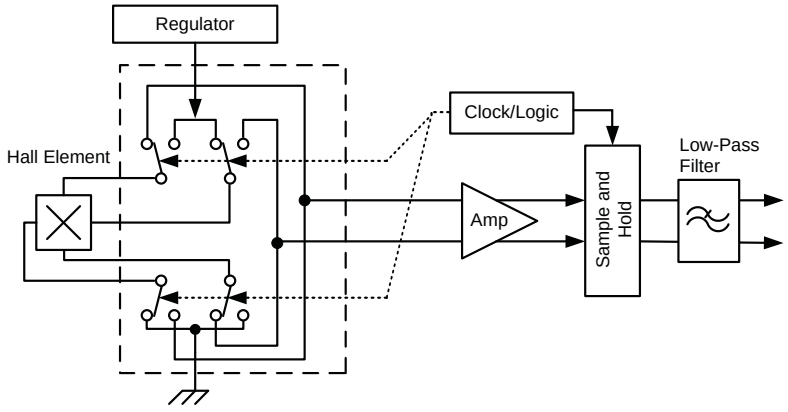


6. This curve shows V_{CC} charging external capacitor C_{OC} through the internal PMOS pull-up. The slope is determined by C_{OC}.
7. When the FAULT_EN pin is brought low, if the fault condition still exists, the latched $\overline{FAULT}$ pin will stay low until the fault condition is removed, then it will start resetting.
8. At this point there is a fault condition, and the part is enabled before the $\overline{FAULT}$ pin can charge to V_{CC}. This shortens the user-set delay, so the fault is latched earlier. The new delay time can be calculated by equation 1, after substituting the voltage seen on the $\overline{FAULT}$ pin for V_{CC}.

Chopper Stabilization Technique

Chopper Stabilization is an innovative circuit technique that is used to minimize the offset voltage of a Hall element and an associated on-chip amplifier. Allegro patented a Chopper Stabilization technique that nearly eliminates Hall IC output drift induced by temperature or package stress effects. This offset reduction technique is based on a signal modulation-demodulation process. Modulation is used to separate the undesired dc offset signal from the magnetically induced signal in the frequency domain. Then, using a low-pass filter, the modulated DC offset is suppressed while the magnetically induced signal passes through the filter. As a result of this chopper stabilization approach, the output voltage from the Hall IC is desensitized to the effects of temperature and mechanical stress. This technique produces devices that have an extremely stable Electrical Offset Voltage, are immune to thermal stress, and have precise recoverability after temperature cycling.

This technique is made possible through the use of a BiCMOS process that allows the use of low-offset and low-noise amplifiers in combination with high-density logic integration and sample and hold circuits.



Concept of Chopper Stabilization Technique

Definitions of Accuracy Characteristics

Sensitivity (Sens). The change in device output in response to a 1 A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the full-scale current of the device.

Noise (V_{NOISE}). The product of the linear IC amplifier gain (mV/G) and the noise floor for the Allegro Hall effect linear IC (≈1 G). The noise floor is derived from the thermal and shot noise observed in Hall elements. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

Linearity (E_{LIN}). The degree to which the voltage output from the device varies in direct proportion to the primary current through its full-scale amplitude. Nonlinearity in the output can be attributed to the saturation of the flux concentrator approaching the full-scale current. The following equation is used to derive the linearity:

$$100\left\{1-\left[\frac{V_{\text{IOUT_full-scale amperes}}-V_{\text{IOUT(Q)}}}{2\,(V_{\text{IOUT_1/2 full-scale amperes}}-V_{\text{IOUT(Q)}})}\right]\right\}$$

where $V_{\text{IOUT_full-scale amperes}}$ = the output voltage (V) when the sensed current approximates full-scale $\pm I_P$.

Symmetry (E_{SYM}). The degree to which the absolute voltage output from the device varies in proportion to either a positive or negative full-scale primary current. The following formula is used to derive symmetry:

$$100\left(\frac{V_{\text{IOUT_+ full-scale amperes}}-V_{\text{IOUT(Q)}}}{V_{\text{IOUT(Q)}}-V_{\text{IOUT_–full-scale amperes}}}\right)$$

Quiescent output voltage ($V_{IOUT(Q)}$). The output of the device when the primary current is zero. For a unipolar supply voltage, it nominally remains at $0.5\times V_{CC}$. For example, in the case of a bidirectional output device, V_{CC} = 5 V translates into $V_{IOUT(Q)}$ = 2.5 V. Variation in $V_{IOUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

Electrical offset voltage (V_{OE}). The deviation of the device output from its ideal quiescent voltage due to nonmagnetic causes. To convert this voltage to amperes, divide by the device sensitivity, Sens.

Accuracy (E_{TOT}). The accuracy represents the maximum deviation of the actual output from its ideal value. This is also known as the total ouput error. The accuracy is illustrated graphically in the output voltage versus current chart at right. Note that error is directly measured during final test at Allegro.

Accuracy is divided into four areas:

- **0 A at 25°C.** Accuracy of sensing zero current flow at 25°C, without the effects of temperature.
- **0 A over Δ temperature.** Accuracy of sensing zero current flow including temperature effects.
- **Full-scale current at 25°C.** Accuracy of sensing the full-scale current at 25°C, without the effects of temperature.
- **Full-scale current over Δ temperature.** Accuracy of sensing full-scale current flow including temperature effects.

Ratiometry. The ratiometric feature means that its 0 A output, $V_{IOUT(Q)}$, (nominally equal to $V_{CC}/2$) and sensitivity, Sens, are proportional to its supply voltage, V_{CC}. The following formula is used to derive the ratiometric change in 0 A output voltage, $\Delta V_{IOUT(Q)RAT}$ (%).

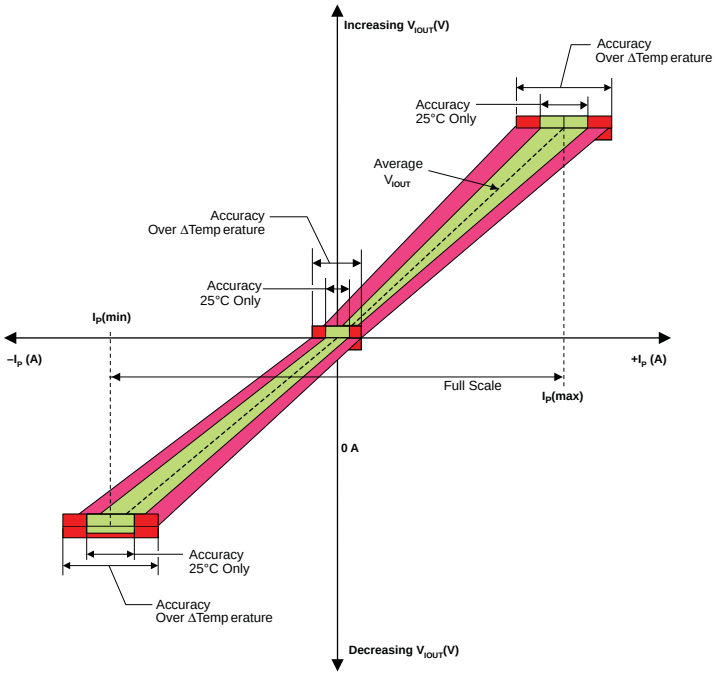
$$100\left(\frac{V_{\text{IOUT(Q)VCC}}/V_{\text{IOUT(Q)5V}}}{V_{CC}/5\text{ V}}\right)$$

The ratiometric change in sensitivity, $\Delta Sens_{RAT}$ (%), is defined as:

$$100\left(\frac{Sens_{VCC}/\ Sens_{5V}}{V_{CC}/5\text{ V}}\right)$$

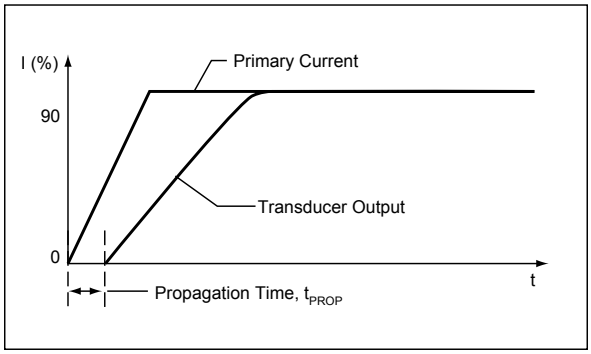
Output Voltage versus Sensed Current

Accuracy at 0 A and at Full-Scale Current

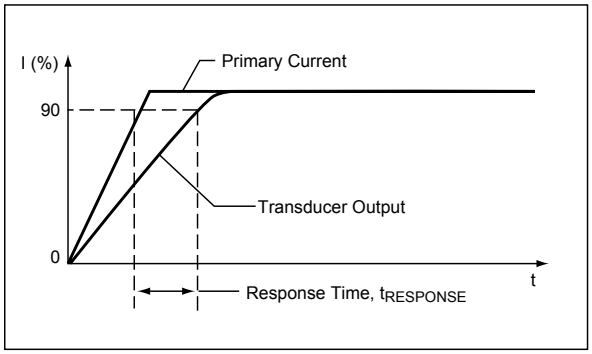


Definitions of Dynamic Response Characteristics

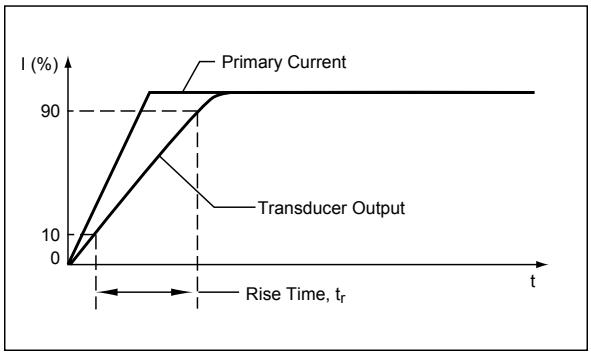
Propagation delay (t_{PROP}). The time required for the device output to reflect a change in the primary current signal. Propagation delay is attributed to inductive loading within the linear IC package, as well as in the inductive loop formed by the primary conductor geometry. Propagation delay can be considered as a fixed time offset and may be compensated.



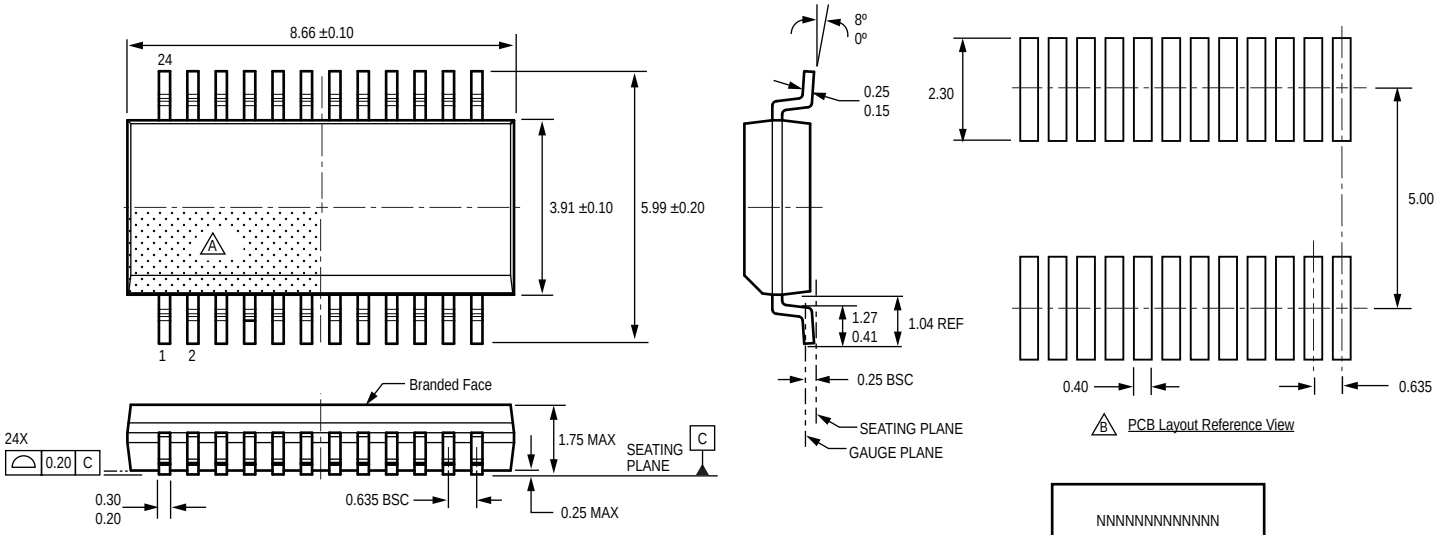
Response time ($t_{RESPONSE}$). The time interval between a) when the primary current signal reaches 90% of its final value, and b) when the device reaches 90% of its output corresponding to the applied current.



Rise time (t_r). The time interval between a) when the device reaches 10% of its full scale value, and b) when it reaches 90% of its full scale value. The rise time to a step response is used to derive the bandwidth of the current sensor IC, in which $f(-3\ dB) = 0.35 / t_r$. Both t_r and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane.



Package LF, 24-pin QSOP



For Reference Only, not for tooling use (reference JEDEC MO-137 AE)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference pad layout (reference IPC7351 SOP63P600X175-24M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

N = Device part number
T = Temperature code
LF = (Literal) Package type
A = Amperage

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