Dual Advanced PWM and Source-Sink Linear Controller

Features

- 3 Regulated Voltages are provided
  - – Standard Buck Converter for VCORE (1.15~1.50V)
  - – Standard Buck Converter for VMEM (2.40~3.15V)
  - –Linear Controller with SOURCE-SINK Regulation for VTT(1.25V)
- Simple Single-Loop Control Design
  - – Voltage-Mode PWM Control
- Excellent Output Voltage Regulation
  - – VCORE Output : ±1% Over Temperature
  - – VMEM Output : ±1.5% Over Temperature
  - – VTT Output : 1/2 VIN ±25mV Over Temperature Min. VIN = 1.7V
- Fast Transient Response
  - – Built-in Feedback Compensation
  - – Full 0% to 100% Duty Ratio
- Over-Voltage and Over-Current Fault Monitor
- Constant Frequency Operation(200kHz)
- 24 pins, SOIC Package

Applications

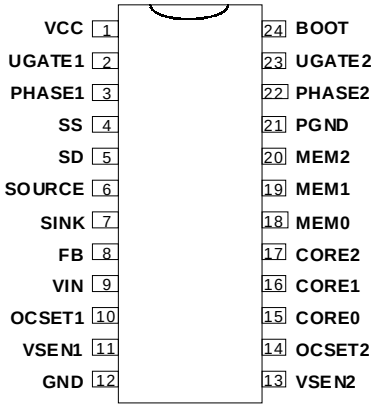
- M/B DDR Power Regulation
- AGP/PCI Graphics Power Regulation
- SSTL-2 Termination

General Description

The APW7046 provides the power controls and protections for three output voltages on AGP/PCI Graphic Card applications. It integrates two PWM controllers , one SOURCE-SINK linear controller, as well as the monitor and protection functions into a single package. One PWM converter (PWM1) supplies the VCORE(1.5V) for the GPU with a standard buck converter. The other standard buck converter (PWM2) regulates the VMEM(2.5V) for the power of DDR memory. The SOURCE-SINK linear controller control two external MOSFETs to be a linear regulator with the capability of sourcing and sinking current. It regulates the VTT (1.25V) power for DDR Termination voltage.

Additional built-in over-voltage protection (OVP) will be started when the VCORE or VMEM output is above 115% of each DAC setting (V_{CORE} and V_{MEM}). OVP function will shutdown the all output voltages until re-powering on the IC. For each PWM converter, the over-current function monitors the output current by sensing the voltage drop across the MOSFET's $r_{DS(ON)}$, eliminating the need for a current sensing resistor.

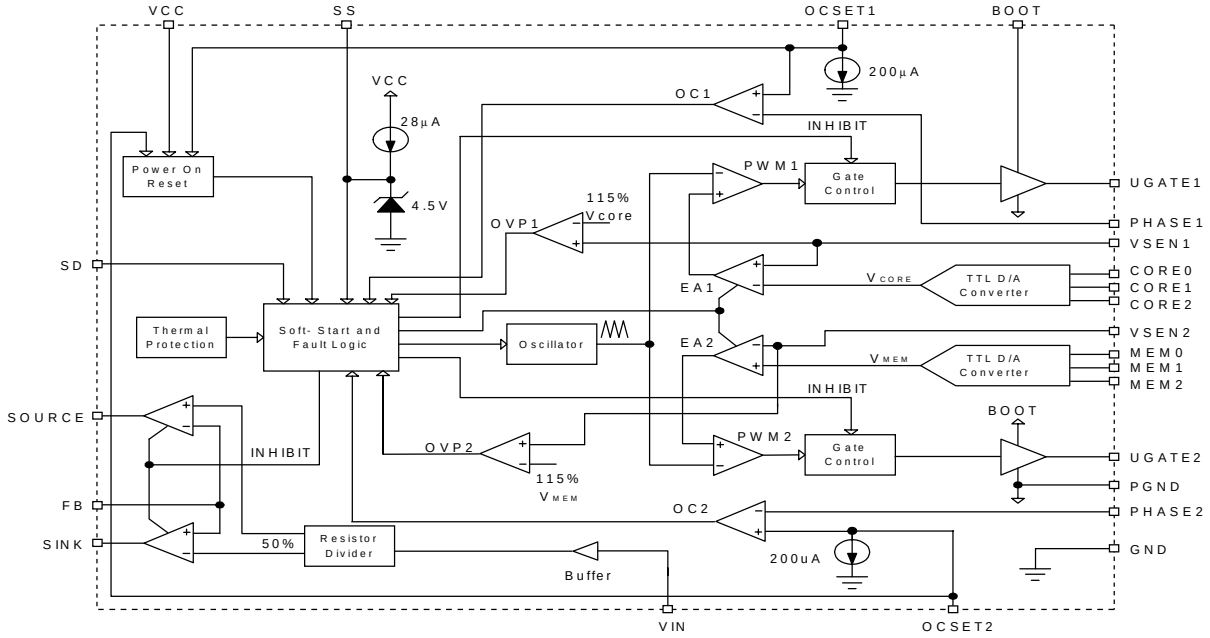
Pin Description



Ordering and Marking Information

APW7046 □ □□-□□□ Lead Free Code Handling Code Temp. Range Package Code Voltage Code	Voltage Code A : VCORE(1.15~1.50V) VMEM(2.40~2.75V) B : VCORE(1.15~1.50V) VMEM(2.80~3.15V) Package Code K : SOP-24 Temp. Range C : 0 to 70° C Handling Code TU : Tube TR : Tape & Reel Lead Free Code L : Lead Free Device Blank : Original Device
APW7046K : 	XXXXX - Date Code

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	15	V
V_I, V_O	Input , Output or I/O Voltage	GND -0.3 V to V_{CC} +0.3	V
T_A	Operating Ambient Temperature	Range 0 to 70	°C
T_J	Junction Temperature	Range 0 to 125	°C
T_{STG}	Storage Temperature	Range -65 to +150	°C
T_S	Soldering Temperature	300 ,10 seconds	°C

Thermal Characteristics

Symbol	Parameter	Value	Unit
R_{JA}	Thermal Resistance in Free Air SOIC SOIC (with 3in^2 of Copper)	 75 65	°C/W

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{CC}=V_{BOOT}=12V and T_A=0~70°C.
Typical values refer to T_A=25°C.

Symbol	Parameter	Test Conditions	APW7046			Unit
			Min.	Typ.	Max.	
Supply Current						
I_{CC}	Nominal Supply Current	SD=0V, UGATE1,UGATE2 , SOURCE, and SINK Open		8		mA
I_{CCSD}	Shutdown Supply Current	SD=5V		2.7		
Power-on Reset						
	Rising VCC Threshold	Vocset=3V		4.2	4.6	V
	Falling VCC Threshold	Vocset=3V	3.6			V
	SD Input High Voltage		2.0			V
	SD Input Low Voltage				0.8	V
Oscillator						
F_{OSC}	Free Running Frequency		185	200	215	kHz
ΔV_{OSC}	Ramp Amplitude			1.9		V
PWM Controller Reference Voltage						
V_{CORE}	PWM1 Reference Voltage Accuracy		-1		+1	%
	CORE0-CORE2 Input High Voltage		2.0			V
	CORE0-CORE2 Input Low Voltage				0.8	V
V_{MEM}	PWM2 Reference Voltage Accuracy		-1.5		+1.5	%
	MEM0-MEM2 Input High Voltage		2.0			V
	MEM0-MEM2 Input Low Voltage				0.8	V
SOURCE-SINK Linear Controller						
V_{FB}	FB Regulation Voltage	Regulator Sourcing or Sinking Current		0.5VIN		V
	V_{FB} accuracy		-25		+25	mV
	Max. SOURCE Pin Drive Current			0.8		mA
	Max. SINK Pin Drive Current			0.8		mA

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{CC}=V_{BOOT}=12V and T_A=0~70°C.
Typical values refer to T_A=25°C.

Symbol	Parameter	Test Conditions	APW7046			Unit
			Min.	Typ.	Max.	
I_{VIN}	VIN Input Bias Current	VIN=2.5V			2	uA
PWM Controllers Gate Drivers						
I_{UGATE}	UGATE1,2 Source	V_{CC}=V_{BOOT}=12V, $V_{UGATE1,2}$=6V		0.74		A
R_{GATE}	UGATE Sink	V_{CC}=12V,$V_{UGATE1,2}$=6V		3	4	Ω
Protection						
	VSEN1,2 OVP trip point (V_{SEN1}/V_{CORE} and V_{SEN2}/V_{MEM})	VSEN Rising		115	120	%
	VSEN1,2 O.V. Hysteresis			2		
I_{OCSET}	Ocset Current Source	Vocset=3V	170	200	230	uA
I_{SS}	Soft start Current			28		

Functional Pin Description

VCC (Pin 1)
Provide a +12V bias supply for the IC to this pin. This pin also provides the gate bias charge for the MOSFETs of the SOURCE-SINK regulator. The voltage at this pin is monitored for Power-On Reset (POR) purposes.

UGATE1 (Pin 2)
Connect this pin to the MOSFET gate of the PWM1 converter. This pin provides the gate drive for the MOSFET.

PHASE1 (Pin 3)
Connect this pin to the PWM1 converter's MOSFET source.This pin is used to monitor the voltage drop across the MOSFET for over-current protection.

SS (Pin 4)
Connect a capacitor from this pin to ground.This capacitor, along with an internal 28uA current source, sets the soft-start interval of all power controls and preventing the outputs from overshoot as well as limiting the input current .

SD (Pin 5)
The pin shuts down all power outputs. A TTL compatible , logic level high signal applied at this pin immediately discharges the soft-start capacitor,disabling all power outputs. When re-enabled, the IC undergoes a new soft-start cycle. Left open, this pin is pulled low by an internal pull-down resistor, enabling operation.

SOURCE (Pin 6)
Connect this pin to the upper MOSFET gate drive of the SOURCE-SINK regulator. This pin drives the upper external MOSFET as a sourcing regulator.

SINK (Pin 7)
Connect this pin to the lower MOSFET gate drive of

Functional Pin Description (Cont.)

the SOURCE-SINK regulator. This pin drives the lower external MOSFET as a sinking regulator.

FB (Pin 8)

Connect this pin to output of the SOURCE-SINK regulator. This pin provides the voltage feedback path for the sourcing and sinking regulators. This pin is internally connected to the negative input of the SOURCE controller, and also connected to the positive input of the SINK controller.

VIN (Pin 9)

Connect this pin to VMEM or a fixed voltage source. Two voltages, about 0.5VIN, are generated by an internal resistor divider as the reference voltages of the sourcing and sinking regulators. The sinking regulation voltage is higher than the sourcing one to prevent a direct current path through the upper and lower MOSFETs.

OCSET1 (Pin 10)

Connect a resistor (R_{OCSET}) from this pin to the drain of the PWM1 converter's MOSFET. R_{OCSET}, an internal 200uA current source (I_{OCSET}), and the MOSFET's on-resistance($r_{DS(ON)}$) set the converter's over-current (OC) trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

An over-current trip cycles the soft-start function. The voltage at this pin is monitored for Power-On Reset (POR) purposes.

VSEN1 (Pin 11)

This pin is connected to the PWM1 converter's output voltage to provide the voltage feedback path. The over-voltage protection(OVP) comparator uses this pin to monitor the output voltage for over- voltage protection

GND (Pin 12)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

VSEN2 (Pin 13)

This pin is connected to the PWM2 converter's output voltage to provide the voltage feedback path. The over-voltage protection(OVP) comparator uses this pin to monitor the output voltage for over- voltage protection.

OCSET2 (Pin 14)

Connect a resistor (R_{OCSET}) from this pin to the drain of the PWM2 converter's MOSFET. The function of this pin is similar to OCSET1(pin 10) for OC detection and POR purposes.

CORE0-2 (Pin 15-17)

CORE0-2 are TTL-compatible logic level input pins to the 3-bit DAC. The states of the three pins set the internal reference voltage (V_{CORE}) for the PWM1 converter and also set the OVP threshold voltage for PWM1 converter.

MEM0-2 (Pin 18-20)

MEM0-2 are TTL-compatible logic level input pins to the other 3-bit DAC. The states of the three pins set the internal reference voltage (V_{MEM}) for the PWM2 converter and also set the OVP threshold voltage for PWM2 converter.

PGND (Pin 21)

Connect this pin to the anode of the flywheel diodes of the two PWM converters.

PHASE2 (Pin 22)

Connect this pin to the PWM2 converter's MOSFET source.This pin is used to monitor the voltage drop across the MOSFET for over-current protection.

Functional Pin Description

UGATE2 (Pin 23)

Connect this pin to the MOSFET gate of the PWM2 converter. This pin provides the gate drive for the MOSFET.

BOOT (Pin 24)

Connect this pin to +12V. This pin provides bias voltage to the MOSFET drivers.

Table 1 DAC Table

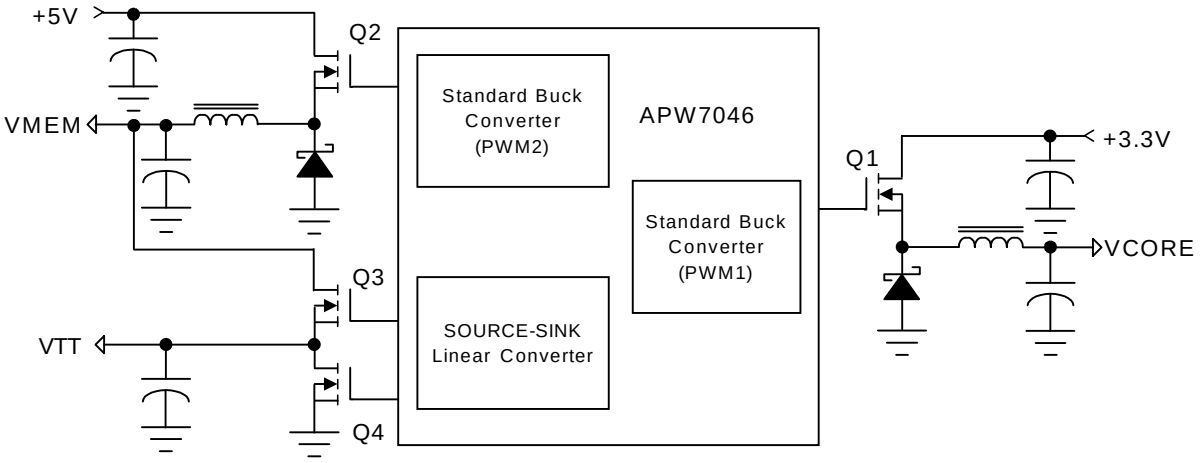
APW7046 - A

Pin Name			V_{CORE} Voltage
CORE2	CORE1	CORE0	
0	0	0	1.15
0	0	1	1.20
0	1	0	1.25
0	1	1	1.30
1	0	0	1.35
1	0	1	1.40
1	1	0	1.45
1	1	1	1.50
Pin Name			V_{MEM} Voltage
MEM2	MEM1	MEM0	
0	0	0	2.40
0	0	1	2.45
0	1	0	2.50
0	1	1	2.55
1	0	0	2.60
1	0	1	2.65
1	1	0	2.70
1	1	1	2.75

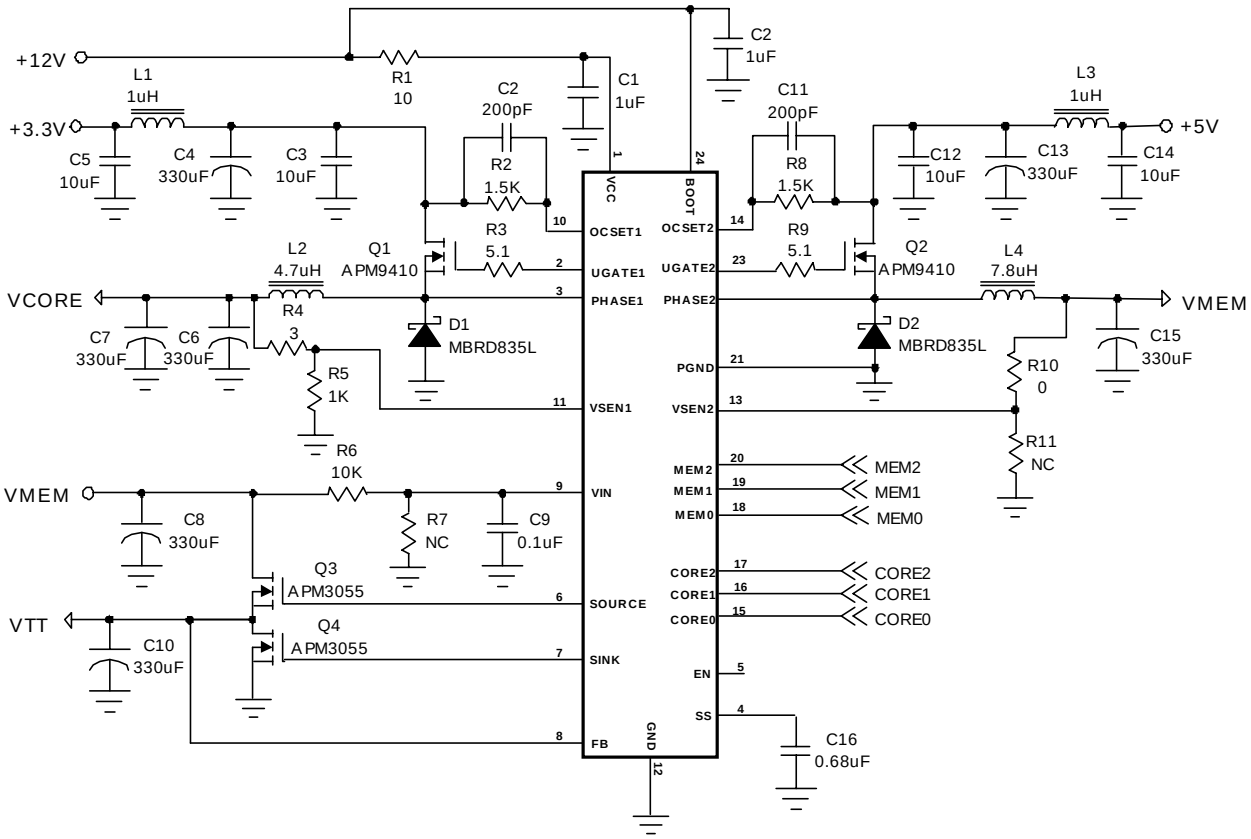
APW7046 - B

Pin Name			V_{CORE} Voltage
CORE2	CORE1	CORE0	
0	0	0	1.15
0	0	1	1.20
0	1	0	1.25
0	1	1	1.30
1	0	0	1.35
1	0	1	1.40
1	1	0	1.45
1	1	1	1.50
Pin Name			V_{MEM} Voltage
MEM2	MEM1	MEM0	
0	0	0	2.80
0	0	1	2.85
0	1	0	2.90
0	1	1	2.95
1	0	0	3.00
1	0	1	3.05
1	1	0	3.10
1	1	1	3.15

Simplified Power System Diagram



Typical Application Circuit



C4, C6, C7, C8 , C10, C13, C15 : 330uF/6.3V
SMD Low ESR tantalum Capacitor

Typical Performance

1. SOURCE-SINK Linear Regulator Transient Response
   - The output capacitor is 330uF (Low ESR tantalum capacitor)
   - Define the output cerrent (IVTT) sourcing from the regulator to be positive.
   - The interval of current transitions in figures 1 and 2 are all smaller than 1uS.
   - In figure 1, the IVTT transition is from -0.2A to 4A.
   - In figure 2, the IVTT transition is from 0.2A to -4A.

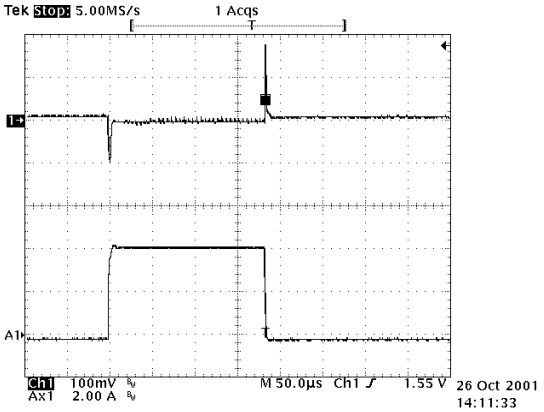


Figure 1

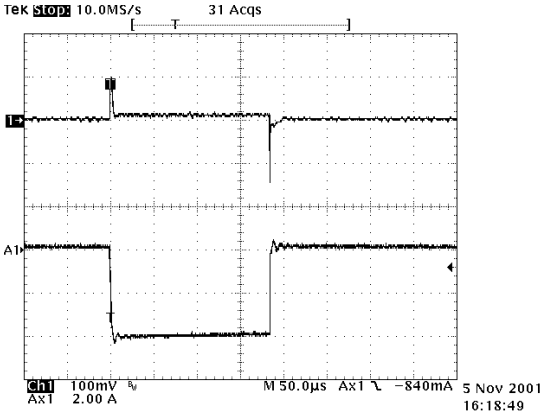
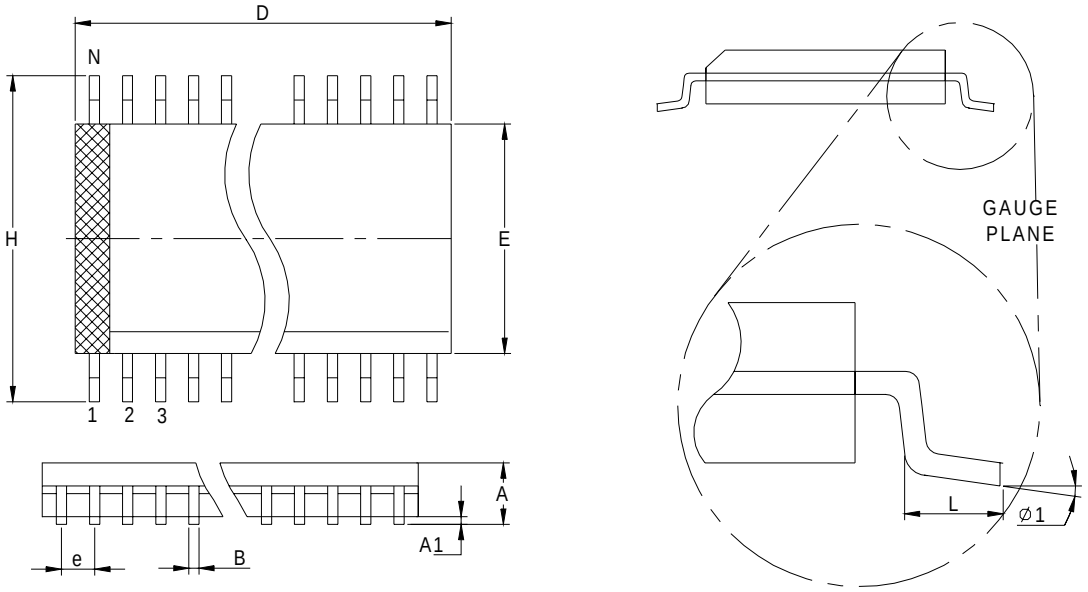


Figure 2

Packaging Information

SO – 300mil (Reference JEDEC Registration MS-013)

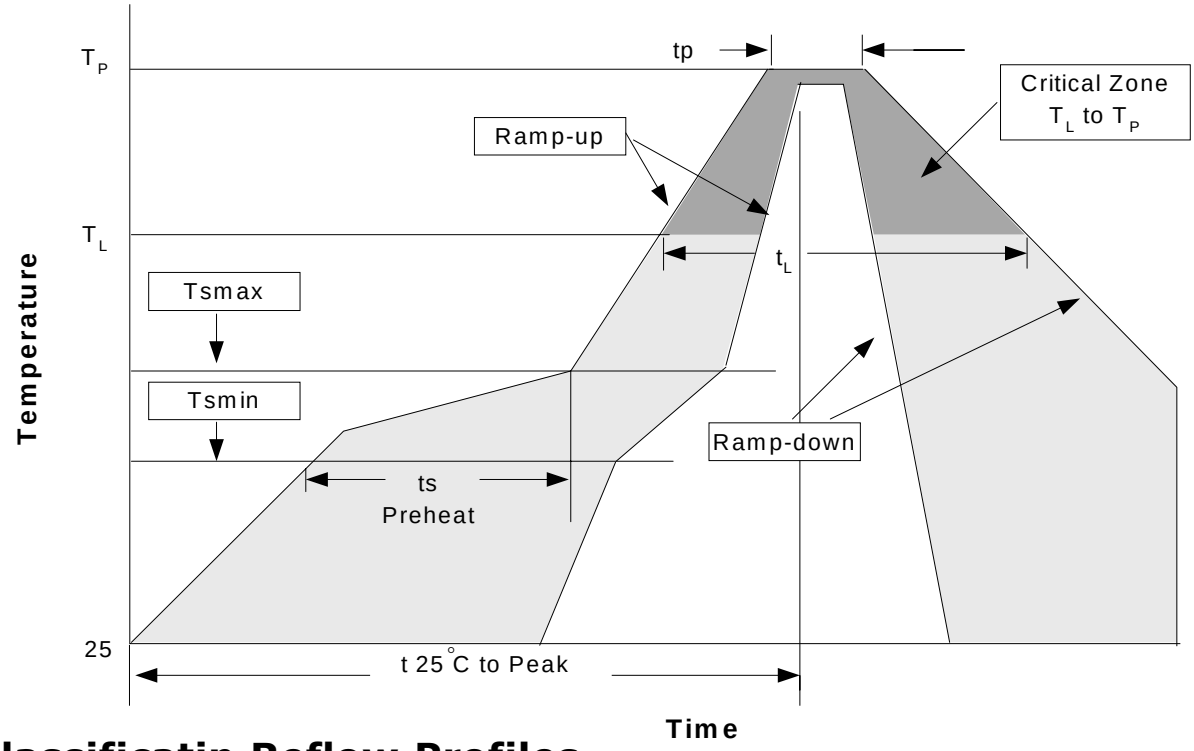


Dim	Millimeters		Variations- D			Dim	Inches		Variations- D		
	Min.	Max.	Variations	Min.	Max.		Min.	Max.	Variation	Min.	Max.
A	2.35	2.65	SO-16	10.10	10.50	A	0.093	0.1043	SO-16	0.398	0.413
A1	0.10	0.30	SO-18	11.35	11.76	A1	0.004	0.0120	SO-18	0.447	0.463
B	0.33	0.51	SO-20	12.60	13	B	0.013	0.020	SO-20	0.496	0.512
D	See variations		SO-24	15.20	15.60	D	See variations		SO-24	0.599	0.614
E	7.40	7.60	SO-28	17.70	18.11	E	0.2914	0.2992	SO-28	0.697	0.713
e	1.27BSC		SO-14	8.80	9.20	e	0.050BSC		SO-14	0.347	0.362
H	10	10.65				H	0.394	0.419			
L	0.40	1.27				L	0.016	0.050			
N	See variations					N	See variations				
ϕ 1	0°	8°				ϕ 1	0°	8°			

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.
Packaging	1000 devices per reel for SO-16 , 2500 devices per reel for SSOP-16.

Reflow Condition (IR/Convection or VPR Reflow)



Classificatin Reflow Profiles

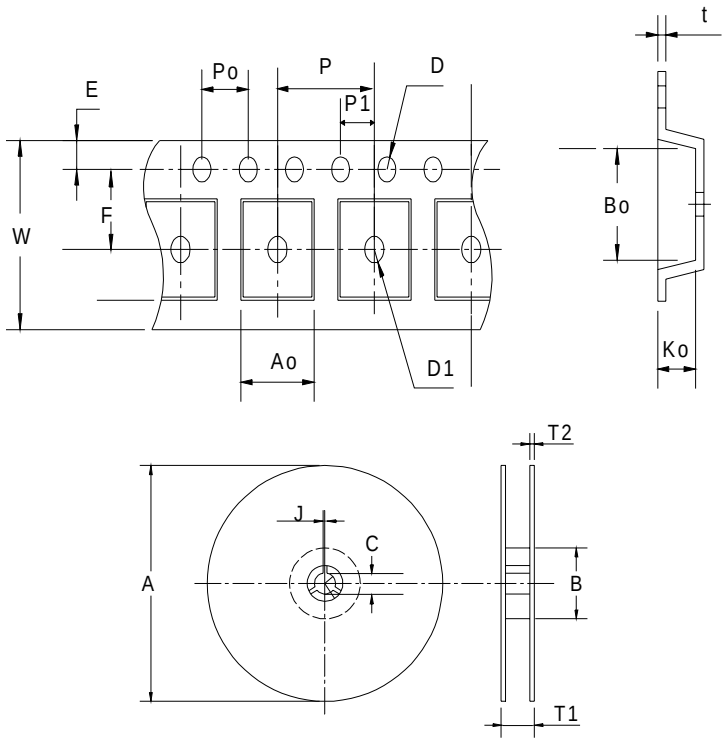
Profile Feature	Sn-Pb Eutectic Assembly		Pb-Free Assembly	
	Large Body	Small Body	Large Body	Small Body
Average ramp-up rate (T_L to T_P)	3°C/second max.		3°C/second max.	
Preheat - Temperature Min (Tsmin) - Temperature Mix (Tsmax) - Time (min to max)(ts)	100°C 150°C 60-120 seconds		150°C 200°C 60-180 seconds	
Tsmax to T_L - Ramp-up Rate			3°C/second max	
Tsmax to T_L - Temperature(T_L) - Time (t_L)	183°C 60-150 seconds		217°C 60-150 seconds	
Peak Temperature(Tp)	225 +0/-5°C	240 +0/-5°C	245 +0/-5°C	250 +0/-5°C
Time within 5°C of actual Peak Temperature(tp)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.		6°C/second max.	
Time 25°C to Peak Temperature	6 minutes max.		8 minutes max.	

Note: All temperatures refer to topside of the package. Measured on the body surface.

Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I_{tr} > 100mA

Carrier Tape & Reel Dimensions



Application	A	B	C	J	T1	T2	W	P	E
SOP- 24	330±1	62 ±1.5	12.75 ± 0.15	2 ± 0.6	24.4 ± 0.2	2± 0.2	24 ± 0.3	12 ± 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	11.5 ± 0.1	1.55 +0.1	1.5+ 0.25	4.0 ± 0.1	2.0 ± 0.1	10.9 ± 0.1	15.9± 0.1	3.1± 0.1	0.35±0.05

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 16 / 20 / 24 / 28	24	21.3	1000

Customer Service

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