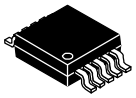


800-mA SYNCHRONOUS STEP-DOWN CONVERTER

FEATURES

- **High-Efficiency Synchronous Step-Down Converter With up to 95% Efficiency**
- **12-µA Quiescent Current (Typ)**
- **2.7-V to 10-V Operating Input Voltage Range**
- **Adjustable Output Voltage Range From 0.7 V to 6 V**
- **Fixed Output Voltage Options Available in 1.5 V, 1.8 V, and 3.3 V**
- **Synchronizable to External Clock Signal up to 1.2 MHz**
- **High Efficiency Over a Wide Load Current Range in Power-Save Mode**
- **100% Maximum Duty Cycle for Lowest Dropout**
- **Low Noise Operation in Forced Fixed Frequency PWM Operation Mode**
- **Internal Softstart**
- **Overtemperature and Overcurrent Protected**
- **Available in 10-Pin Microsmall Outline Package MSOP**

APPLICATIONS

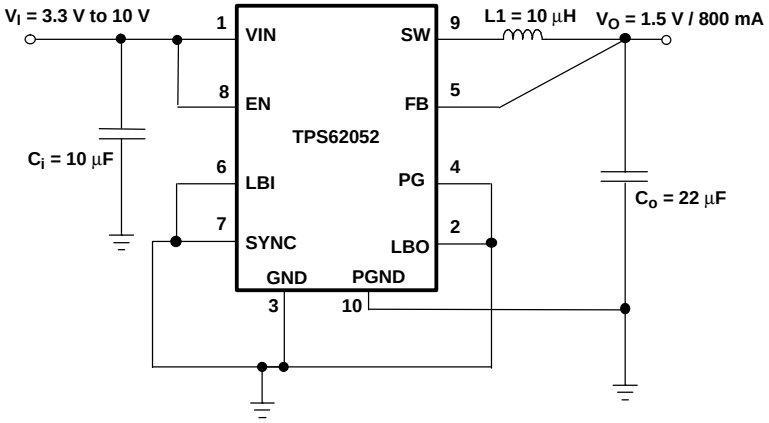
- **Cellular Phones**
- **Organizers, PDAs, and Handheld PCs**
- **Low Power DSP Supply**
- **Digital Cameras and Hard Disks**

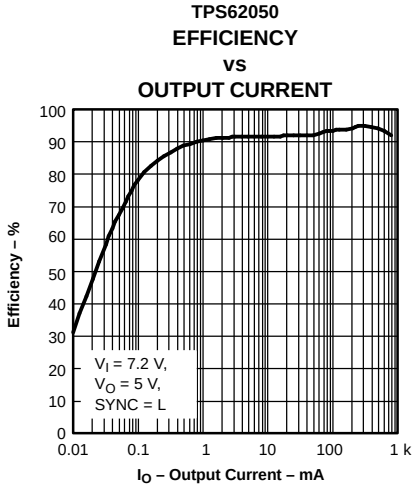
DESCRIPTION

The TPS6205x devices are a family of high-efficiency synchronous step-down dc/dc converters ideally suited for systems powered from a 1-cell or 2-cell Li-Ion battery or from a 3-cell to 5-cell NiCd, NiMH, or alkaline battery.

The TPS62050 is a synchronous PWM converter with integrated N-channel and P-channel power MOSFET switches. Synchronous rectification increases efficiency and reduces external component count. To achieve highest efficiency over a wide load current range, the converter enters a power-saving pulse-frequency modulation (PFM) mode at light load currents. Operating frequency is typically 850 kHz, allowing the use of small inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 600 kHz to 1.2 MHz. For low noise operation, the converter can be programmed into forced-fixed frequency in PWM mode. In shutdown mode, the current consumption is reduced to less than 2 µA. The TPS6205x is available in the 10-pin (DGS) micro-small outline package (MSOP) and operates over an free air temperature range of -40°C to 85°C.

TYPICAL APPLICATION CIRCUIT





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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PACKAGED DEVICES PLASTIC MSOP (1) (DGS)	OUTPUT VOLTAGE	LBI/LBO FUNCTIONALITY	PACKAGE MARKING
TPS62050DGS	Adjustable 0.7 V to 6 V	Standard	BFM
TPS62051DGS	Adjustable 0.7 V to 6 V	Enhanced	BGB
TPS62052DGS	1.5 V	Standard	BGC
TPS62054DGS	1.8 V	Standard	BGE
TPS62056DGS	3.3 V	Standard	BGG

(1) The DGS packages are available taped and reeled. Add an R suffix to the device type (i.e., TPS62050DGSR) to order quantities of 2500 devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted (1)

	TPS6205x
Supply voltage, V_I	-0.3 V to 11 V
Voltage at EN, SYNC	-0.3 V to V_I
Voltage at LBI, FB, LBO, PG	-0.3 V to 7 V
Voltage at SW	-0.3 V to 11 V (2)
Output current, I_O	850 mA
Maximum junction temperature, T_J	150°C
Operating free-air temperature range, T_A	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) The voltage at the SW pin is sampled in PFM mode 15 µs after the PMOS has switched off. During this time the voltage at SW is limited to 7 V maximum. Therefore, the output voltage of the converter is limited to 7 V maximum.

PACKAGE DISSIPATION RATING

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR $T_A \leq 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
10-PIN MSOP (1)	555 mW	5.56 mW/°C	305 mW	221 mW

(1) The thermal resistance junction to ambient soldered onto a PCB of the 10-pin MSOP is 180°C/W.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage at V_I	2.7		10	V
Voltage at PG, LBO			6	V
Maximum output current			800 (1)	mA
Operating junction temperature	-40		125	°C

(1) Assuming no thermal limitation

ELECTRICAL CHARACTERISTICS

V_I =7.2 V, V_O = 3.3 V, I_O = 300 mA, EN = V_I, T_A =-40°C to 85°C unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
V_I	Input voltage range			2.7		10	V
$I_{(Q)}$	Operating quiescent current		I_O = 0 mA, SYNC = GND, V_I = 7.2 V		12	20	µA
$I_{(SD)}$	Shutdown current		EN = GND		1.5	5	µA
			EN = GND, T_A=25°C		1.5	3	
$I_{Q(LBI)}$	Quiescent current with enhanced LBI comparator version.		EN = V_I, LBI=GND, TPS62051 only		5		µA
ENABLE							
V_{IH}	EN high level input voltage			1.3			V
V_{IL}	EN low level input voltage					0.3	V
	EN trip point hysteresis				100		mV
I_{lkg}	EN input leakage current		EN = GND or VIN, V_I=7.2 V		0.01	0.2	µA
$I_{(EN)}$	EN input current		0.6 V ≤ $V_{(EN)}$≤ 4 V		2		µA
$V_{(UVLO)}$	Undervoltage lockout threshold				1.6		V
POWER SWITCH							
$r_{DS(on)}$	P-channel MOSFET on-resistance		V_I ≥ 5.4 V; I_O = 300 mA		400	650	mΩ
			V_I = 2.7 V; I_O = 300 mA		600	850	
	P-channel MOSFET leakage current		V_{DS} = 10 V			1	µA
	P-channel MOSFET current limit		V_I = 7.2V, V_O = 3.3 V	1000	1200	1400	mA
$r_{DS(on)}$	N-channel MOSFET on-resistance		V_I ≥ 5.4 V; I_O = 300 mA		300	450	mΩ
			V_I = 2.7 V; I_O = 300 mA		450	550	
	N-channel MOSFET leakage current		V_{DS} = 6 V			1	µA
POWER GOOD OUTPUT, LBI, LBO							
$V_{(PG)}$	Power good trip voltage				VmI -2%		V
	Power good delay time		V_O ramping positive		50		µs
			V_O ramping negative		200		
V_{OL}	PG, LBO output low voltage		$V_{(FB)}$ = 0.8 x V_O nominal, $I_{(sink)}$ = 1 mA			0.3	V
	PG, LBO output leakage current		$V_{(FB)}$ = V_O nominal, $V_{(LBI)}$ = V_I		0.01	0.25	µA
	Minimum supply voltage for valid power good, LBO signal				2.3		V
$V_{(LBI)}$	Low battery input trip voltage		Input voltage falling		1.21		V
	Low battery input trip point accuracy					1.5%	
$V_{(LBI,HYS)}$	Low battery input hysteresis				15		mV
$I_{lkg(LBI)}$	LBI leakage current				0.01	0.1	µA
OSCILLATOR							
f_S	Oscillator frequency			600	850	1000	kHz
$f_{(SYNC)}$	Synchronization range			600		1200	kHz
V_{IH}	SYNC high level input voltage			1.5			V
V_{IL}	SYNC low level input voltage					0.3	V
I_{lkg}	SYNC input leakage current		SYNC = GND or VIN		0.01	0.1	µA
	SYNC trip point hysteresis				100		mV
	Duty cycle of external clock signal			20%		90%	
OUTPUT							
V_O	Adjustable output voltage range	TPS62050, TPS62051		0.7		6.0	V
$V_{(FB)}$	Feedback voltage	TPS62050, TPS62051		0.5			V
	FB leakage current	TPS62050, TPS62051			0.02	0.1	µA

ELECTRICAL CHARACTERISTICS (continued)

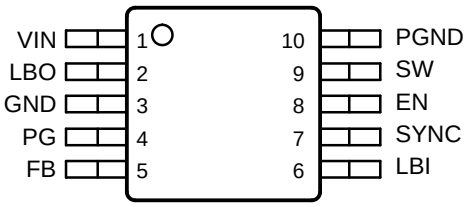
V_I =7.2 V, V_O = 3.3 V, I_O = 300 mA, EN = V_I, T_A =-40°C to 85°C unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Feedback voltage tolerance	TPS62050, TPS62051	V_I = 2.7 V to 10 V, 0 mA< I_O< 600 mA	-3%		3%	
	Fixed output voltage tolerance (1)	TPS62052	V_I = 2.7 V to 10 V, 0 mA< I_O< 600 mA	-3%		3%	
		TPS62054	V_I = 2.7 V to 10 V, 0 mA< I_O< 600 mA	-3%		3%	
		TPS62056	V_I = 3.75 V to 10 V, 0 mA< I_O< 600 mA	-3%		3%	
	Resistance of internal voltage divider forfixed-voltage versions			700	1000	1300	kΩ
	Line regulation		V_O = 3.3 V, V_I = 5 V to 10 V, I_O = 600 mA		5.2		mV/V
	Load regulation		V_I = 7.2 V; I_O = 10 mA to 600 mA		0.0045		%/mA
η	Efficiency		V_I = 5 V; V_O = 3.3 V; I_O = 300 mA		93%		
			V_I = 3.6 V; V_O = 2.5 V; I_O = 200 mA		93%		
	Duty cycle range for main switches					100%	
	Minimum t_{on} time for main switch				100		ns
	Shutdown temperature				145		°C
	Start-up time		I_O = 200 mA, V_I = 5 V, V_o = 3.3 V, C_o = 22 µF, L = 10 µH		1		ms

(1) The worst case $r_{DS(on)}$ of the PMOS in 100% mode for an input voltage of 3.3 V is 0.75 Ω. This value can be used to determine the minimum input voltage if the output current is less than 600 mA with the TPS62056.

PIN ASSIGNMENTS

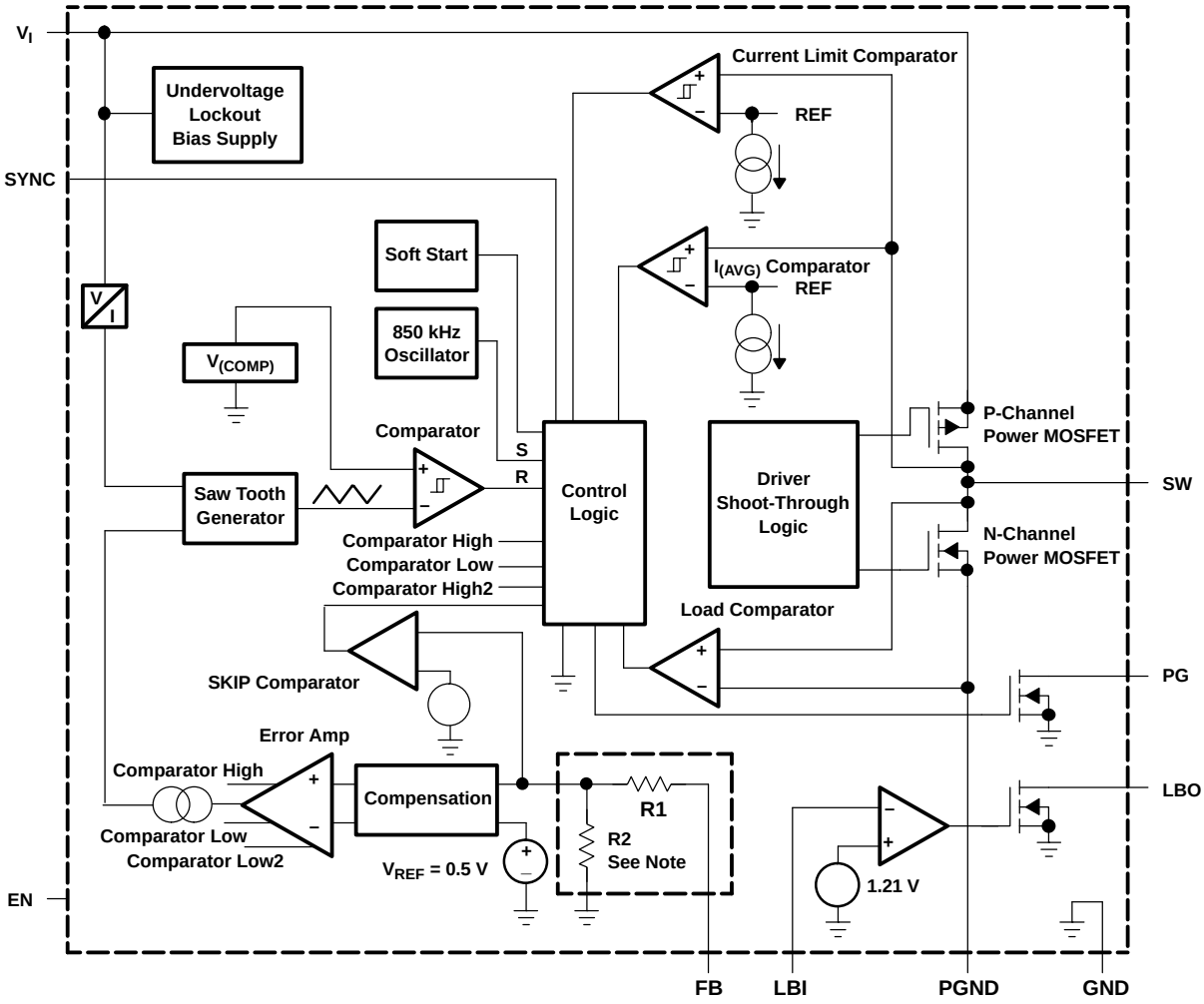
DGS PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
EN	8	I	Enable. A logic high enables the converter, logic low forces the device into shutdown mode, reducing the supply current to less than 2 µA.
FB	5	I	Feedback pin for the fixed output voltage option. For the adjustable version, an external resistive divider is connected to this pin. The internal voltage divider is disabled for the adjustable version.
GND	3	I	Ground
LBO	2	O	Open drain low battery output. Logic low signal indicates a low battery voltage.
LBI	6	I	Low battery input
PG	4	O	Power good comparator output. This is an open-drain output. A pullup resistor should be connected between PG and VOUT. The output goes active high when the output voltage is greater than 95% of the nominal value.
PGND	10	I	Power ground. Connect all power grounds to this pin.
SW	9	O	Connect the inductor to this pin. This pin is the switch pin and connected to the drain of the internal power MOSFETS.
SYNC	7	I	Input for synchronization to the external clock signal. This input can be connected to an external clock or pulled to GND or V_I. When an external clock signal is applied, the device synchronizes to this external clock and the device operates in fixed PWM mode. When the pin is pulled to either GND or V_I, the internal oscillator is used and the logic level determines if the device operates in fixed PWM or PWM/PFM mode.SYNC = HIGH: Low-noise mode enabled, fixed frequency PWM operation is forcedSYNC = LOW (GND): Power-save mode enabled, PFM/PWM mode enabled.
VIN	1	I	Supply voltage input

FUNCTIONAL BLOCK DIAGRAM

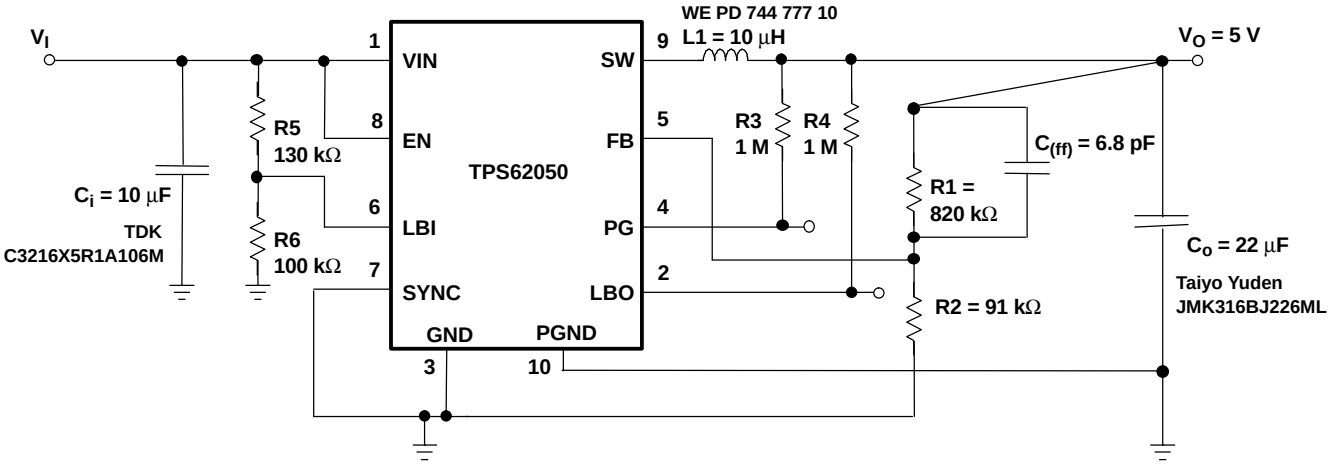


NOTE: For the adjustable versions (TPS62050, TPS62051), the internal feedback driver is disabled and the FB pin is directly connected to the GM amplifier.

PARAMETER MEASUREMENT INFORMATION

All graphs were generated using the circuit as shown unless otherwise noted. For output voltages other than 5 V, the fixed voltage versions are used. The resistors R1, R2, and the feedforward capacitor (Cff) are removed and the feedback pin is directly connected to the output.

STANDARD CIRCUIT FOR ADJUSTABLE VERSION



Quiescent Current Measurements and Efficiency Were Taken
With: R5 = Open, R4 = Open, LBI Connected to GND.

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

	FIGURE
Efficiency vs load current	1 - 8
Switching frequency vs temperature	9
Output voltage ripple in SKIP mode	10
Output voltage ripple in PWM mode	11
Line transient response in PWM mode	12
Load transient	13
$V_{(switch)}$ and I_L (inductor current) in skip mode	14
Start-up timing	15

TPS62050 EFFICIENCY vs LOAD CURRENT

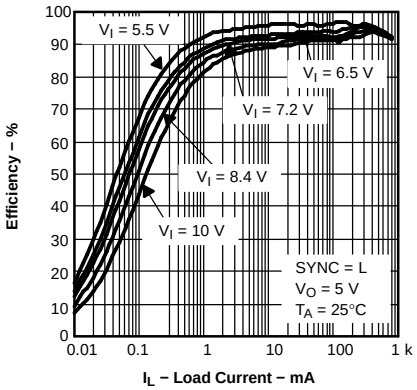


Figure 1.

TPS62052 EFFICIENCY vs LOAD CURRENT

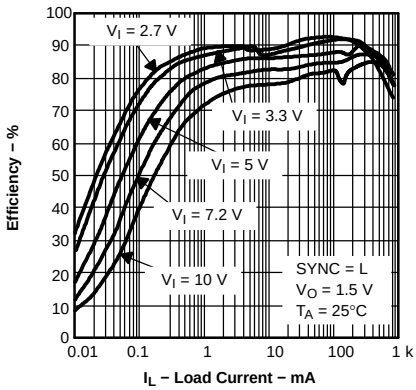


Figure 2.

TPS62054 EFFICIENCY vs LOAD CURRENT

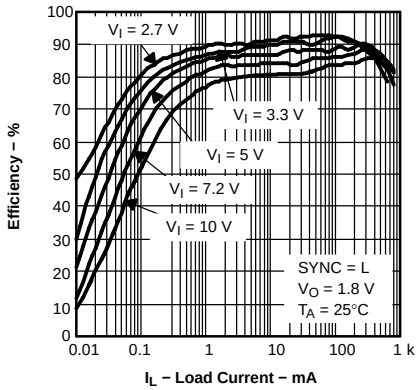


Figure 3.

TPS62056 EFFICIENCY vs LOAD CURRENT

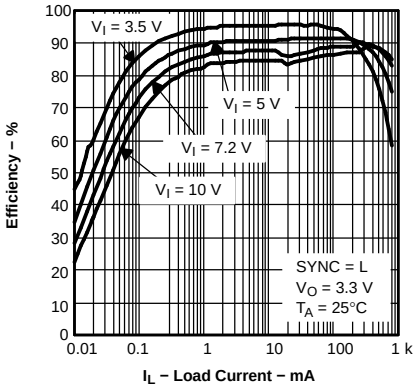


Figure 4.

TPS62050 EFFICIENCY vs LOAD CURRENT

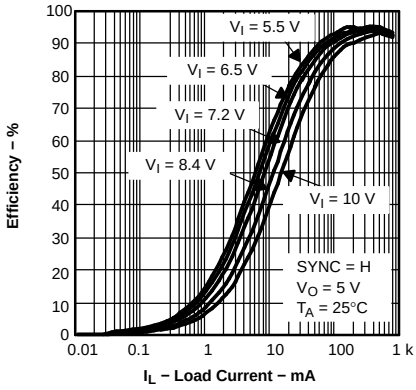


Figure 5.

TPS62052 EFFICIENCY vs LOAD CURRENT

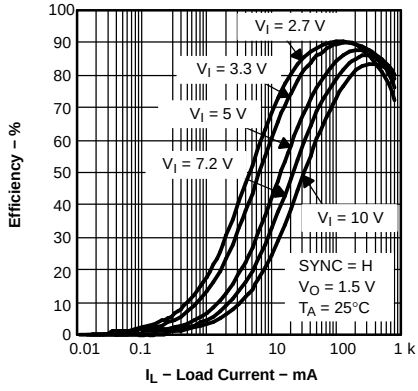


Figure 6.

TYPICAL CHARACTERISTICS (continued)

TPS62054 EFFICIENCY vs LOAD CURRENT

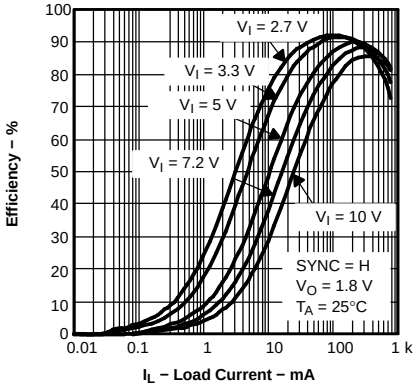


Figure 7.

TPS62056 EFFICIENCY vs LOAD CURRENT

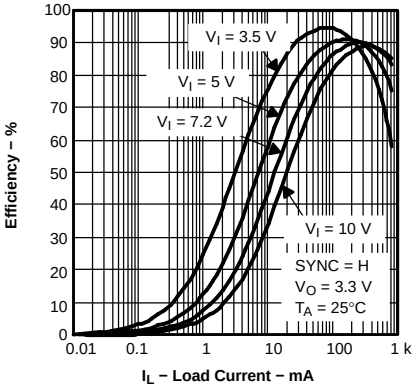


Figure 8.

SWITCHING FREQUENCY vs FREE-AIR TEMPERATURE

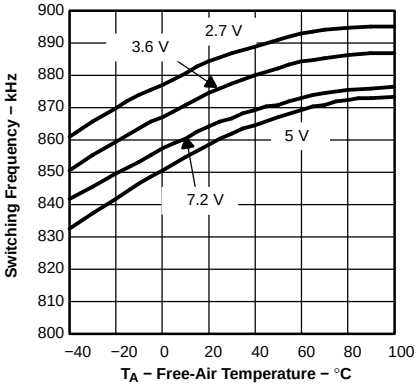


Figure 9.

OUTPUT VOLTAGE RIPPLE IN SKIP MODE

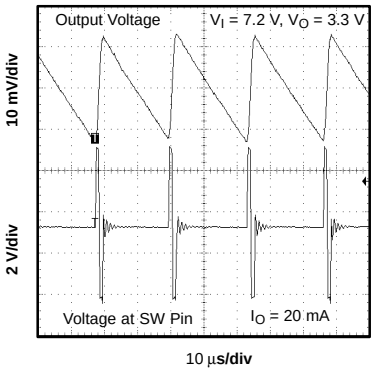


Figure 10.

OUTPUT VOLTAGE RIPPLE IN PWM MODE

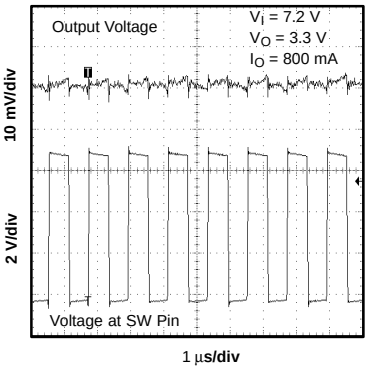


Figure 11.

LINE TRANSIENT RESPONSE IN PWM MODE

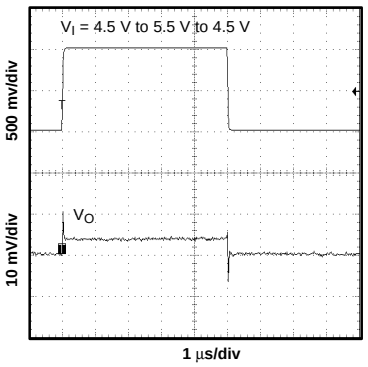


Figure 12.

LOAD TRANSIENT

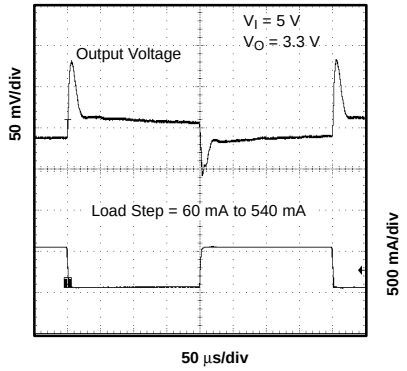


Figure 13.

$V_{(SWITCH)}$ AND I_L (INDUCTOR CURRENT) IN SKIP MODE

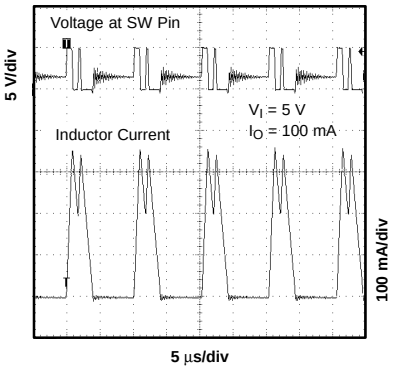


Figure 14.

START-UP TIMING

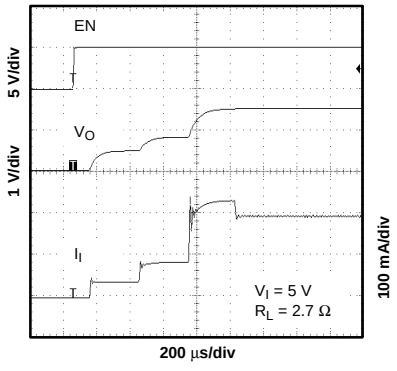


Figure 15.

APPLICATION INFORMATION

Operation

The TPS6205x is a synchronous step-down converter that operates with a 850-kHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents and enters the power-save mode at light load current.

During PWM operation the converter uses a unique fast response voltage mode control scheme with input voltage feed forward to achieve good line and load regulation with the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal (S), the P-channel MOSFET switch is turned on and the inductor current ramps up until the voltage-comparator trips and the control logic turns the switch off. Also the switch is turned off by the current limit comparator in case the current limit of the P-channel switch is exceeded. After the dead time preventing current shoot through, the N-channel MOSFET rectifier is turned on and the inductor current ramps down. The next cycle is initiated by the clock signal again, turning off the N-channel rectifier and turning on the P-channel switch.

The error amplifier as well as the input voltage determines the rise time of the saw tooth generator; therefore, any change in input voltage or output voltage directly controls the duty cycle of the converter giving a very good line and load transient regulation.

Constant Frequency Mode Operation (SYNC = HIGH)

In the constant frequency mode, the output voltage is regulated by varying the duty cycle of the PWM signal in the range of 100% to 10%. Connecting the SYNC pin to a voltage greater than 1.5 V forces the converter to operate permanently in the PWM mode even at light or no load currents. The advantage is the converter operates with a fixed switching frequency that allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads (see Figure 16). The N-MOSFET of the devices stays on even when the current into the output drops to zero. This prevents the device from going into discontinuous mode. The device transfers unused energy back to the input. Therefore, there is no ringing at the output that usually occurs in the discontinuous mode. The duty cycle range in constant frequency mode is 100% to 10%.

It is possible to switch from forced PWM mode to the power-save mode during operation by pulling the SYNC pin low. The flexible configuration of the SYNC pin during operation of the device allows efficient power management by adjusting the operation of the TPS6205x to the specific system requirements.

Power-Save Mode Operation (SYNC = LOW)

As the load current decreases, the converter enters the power-save mode operation. During power-save mode the converter operates with reduced switching frequency in PFM and with a minimum quiescent current to maintain high efficiency. Whenever the average output current goes below the skip threshold, the converter enters the power-save mode. The average current depends on the input voltage. It is 100 mA at low input voltages and up to 200 mA with maximum input voltage. The average output current must be below the threshold for at least 32 clock cycles (t_{cy}) to enter the power-save mode. During the power-save mode the output voltage is monitored with a comparator. When the output voltage falls below the comp low threshold set to 0.8% above V_O nominal, the P-channel switch turns on. The P-channel switch turns off as the peak switch current of typically 200 mA is reached. The N-channel rectifier turns on and the inductor current ramps down. As the inductor current approaches zero, the N-channel rectifier is turned off and the switch is turned on starting the next pulse. When the output voltage can not be reached with a single pulse, the device continues to switch with its normal operating frequency, until the comparator detects the output voltage to be 1.6% above the nominal output voltage. The converter wakes up again when the output voltage falls below the comp low threshold. This control method reduces the quiescent current to typically to 12 µA and the switching frequency to a minimum achieving the highest converter efficiency. Having these skip current thresholds 0.8% and 1.6% above the nominal output voltage gives a lower absolute voltage drop during a load transient as anticipated with a standard converter operating in this mode.

APPLICATION INFORMATION (continued)

Feedforward Capacitor

The feedforward capacitor, $C_{(ff)}$ shown in Figure 20, improves the performance in SKIP mode. The comparator is faster, therefore, there is less voltage ripple at the output in SKIP mode. Use the values listed in Table 1. Larger values decrease stability in fixed frequency PWM mode. If the TPS6205x is only operated in fixed frequency PWM mode, the feedforward capacitor is not needed.

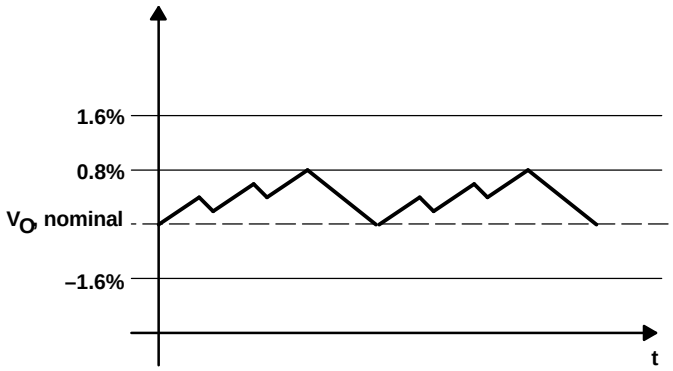


Figure 16. Power-Save Mode Output Voltage Thresholds

The converter enters the fixed frequency PWM mode again as soon as the output voltage falls below the comp low 2 threshold set to 1.6% below V_O, nominal.

Soft-Start

The TPS6205x has an internal soft-start circuit that limits the inrush current during start-up. This prevents possible voltage drops of the input voltage if a battery or a high impedance power source is connected to the input of the TPS6205x.

The soft-start is implemented as a digital circuit increasing the switch current in steps of 200 mA, 400 mA, 800 mA and then the typical switch current limit of 1.2 A. Therefore the start-up time mainly depends on the output capacitor and load current. Typical start-up time with a 22-µF output capacitor and a 200-mA load current is 1 ms.

100% Duty Cycle Low Dropout Operation

The TPS6205x offers the lowest possible input to output voltage difference while still maintaining operation with the use of the 100% duty cycle mode. In this mode, the P-channel switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range, i.e. The minimum input voltage to maintain regulation depends on the load current and output voltage and can be calculated as:

APPLICATION INFORMATION (continued)

$$V_I(min) = V_O(max) + I_O(max) \times \left(r_{DS(on)}(max) + R_L \right)$$

$I_O(max)$ = Maximum output current plus inductor ripple current
$r_{DS(on)}(max)$ = Maximum P-Channel switch $r_{DS(on)}$
R_L = DC resistance of the inductor
$V_O(max)$ = Nominal output voltage plus maximum output voltage tolerance

Enable and Overtemperature Protection

Logic low on EN forces the TPS6205x into shutdown. In shutdown, the power switch, drivers, voltage reference, oscillator, and all other functions are turned off. The supply current is reduced to less than 2 µA in the shutdown mode. When the device is in thermal shutdown, the bandgap is forced to stay on even if the device is set into shutdown by pulling EN to GND. As soon as the temperature drops below the threshold, the device automatically starts again.

If an output voltage is present when the device is disabled, which could be an external voltage source or super cap, the reverse leakage current is specified under electrical characteristics. Pulling the enable pin high starts up the TPS6205x with the soft-start as described under the paragraph soft-start. If the EN pin is connected to any voltage other than V_I or GND, an increased leakage current of typically 10 µA and up to 20 µA can occur.

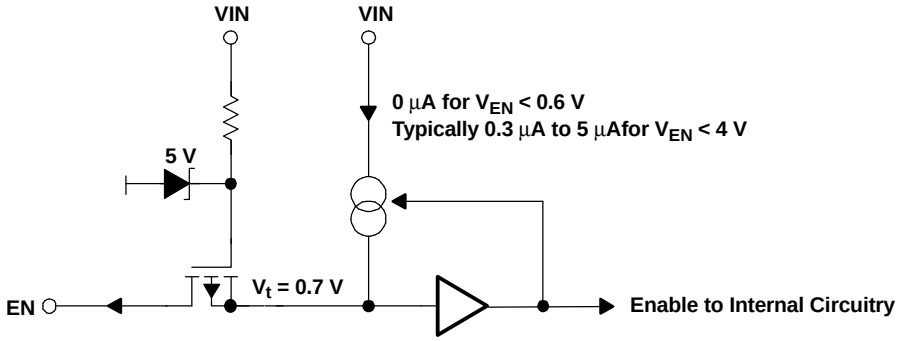


Figure 17. Internal Circuit of the ENABLE Pin

The EN pin can be used in a pushbutton configuration as shown in Figure 18. The external resistor to GND must be capable of sinking 0.3 µA with a minimum voltage drop of 1.3 V to keep the system enabled when both switches are open. When the ON-button is pressed, the device is enabled and the current through the external resistor keeps the voltage level high to ensure that the device stays on when the ON-button is released. When the OFF-button is pressed, the device is switched off and the current through the external resistor is zero. The device therefore stays off even when the OFF-button is released.

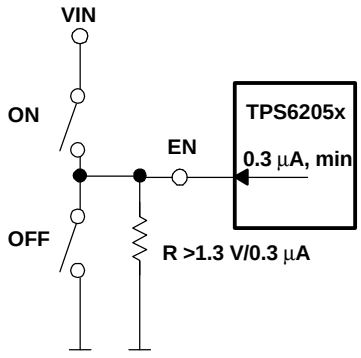


Figure 18. Pushbutton Configuration for the EN-Pin

APPLICATION INFORMATION (continued)

Undervoltage Lockout

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions.

Synchronization

If no clock signal is applied, the converter operates with a typical switching frequency of 850 kHz. It is possible to synchronize the converter to an external clock within a frequency range from 600 kHz to 1200 kHz. The device automatically detects the rising edge of the first clock and synchronizes to the external clock. If the clock signal is stopped, the converter automatically switches back to the internal clock and continues operation. The switchover is initiated if no rising edge on the SYNC pin is detected for a duration of four clock cycles. Therefore, the maximum delay time can be 8.3 µs if the internal clock has its minimum frequency of 600 kHz. During this time, there is no clock signal available. The device stops switching until the internal circuitry is switched to the internal clock source.

When the device is switched between internal synchronization and external synchronization during operation, the output voltage may show transient over/undershoot during switchover. The voltage transients are minimized by using 850 kHz as an initial external frequency, and changing the frequency slowly (>1 ms) to the value desired. The voltage drop at the output when the device is switched from external synchronization to internal synchronization can be reduced by increasing the output capacitor value.

If the device is synchronized to an external clock, the power-save mode is disabled and the device stays in forced PWM mode.

Connecting the SYNC pin to the GND pin enables the power-save mode. The converter operates in the PWM mode at moderate to heavy loads and in the PFM mode during light loads maintaining high efficiency over a wide load current range.

Power Good Comparator

The power good (PG) comparator has an open drain output capable of sinking typically 1 mA. The PG function is only active when the device is enabled (EN = high). When the device is disabled (EN = low), the PG pin is pulled to GND.

The PG output is only valid after a 250 µs delay after the device is enabled and the supply voltage is greater than 2.7 V. Power good is low during the first 250 µs after shutdown and in shutdown.

The PG pin becomes active high when the output voltage exceeds typically 98.5% of its nominal value. Leave the PG pin unconnected, or connect to GND when not used.

Low-Battery Detector (Standard Version)

The low-battery output (LBO) is an open drain type which goes low when the voltage at the low battery input (LBI) falls below the trip point of 1.21 V ±1.5%. The voltage at which the low-battery warning is issued is adjusted with a resistive divider as shown in Figure 20. The sum of the resistors R1 and R2 is recommended to be in the 100-kΩ to 1-MΩ range for high efficiency at low output current. An external pullup resistor at LBO can either be connected to OUT, or any other voltage rail in the voltage range of 0 V to 6 V. During start-up, the LBO output signal is invalid for the first 500 µs. LBO is high impedance when the device is disabled. If the low-battery comparator function is not used, connect LBI to ground. The low-battery detector is disabled when the device is disabled. Leave the LBO pin unconnected, or connect to GND when not used.

APPLICATION INFORMATION (continued)

ENABLE/Low-Battery Detector (Enhanced Version) TPS62051 Only

The TPS62051 offers an enhanced LBI functionality to provide a precise, user programmable undervoltage shutdown. No additional supply voltage supervisor (SVS) is needed to provide this function.

When the enable (EN) pin is pulled high, only the internal bandgap voltage reference is switched on to provide a reference source for the LBI comparator. As long as the voltage at LBI is less than the LBI trip point, all other internal circuits are shut down, reducing the supply current to 5 µA. As soon as input voltage at LBI rises above the LBI trip point of 1.21 V, the device is completely enabled and starts switching.

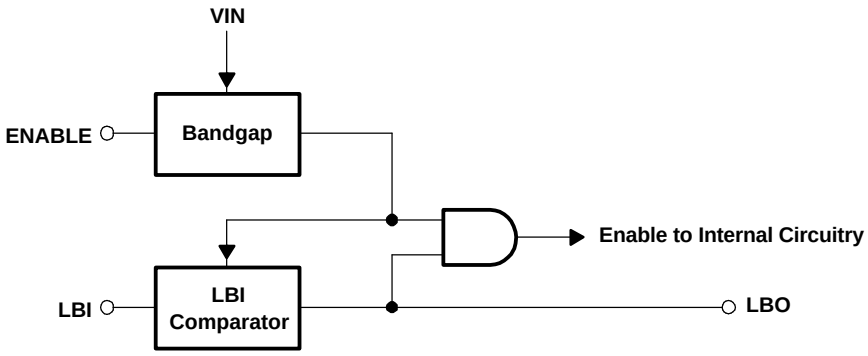


Figure 19. Block Diagram of ENABLE/LBI Functionality for TPS62051

The logic level of the LBO pin is not defined for the first 500 µs after EN is pulled high.

When the enhanced LBI is used to supervise the battery voltage and shut down the TPS62051 at low input voltages, the battery voltage rises again when the current drops to zero. The implemented hysteresis on the LBI pin may not be sufficient for all types of batteries. Figure 20 shows how an additional external hysteresis can be implemented.

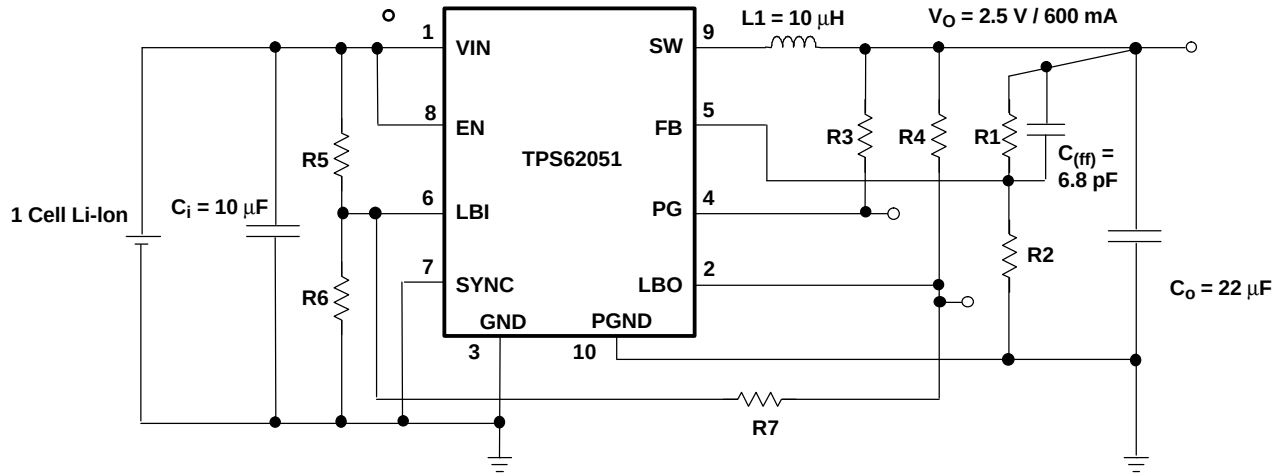


Figure 20. Enhanced LBI With Increased Hysteresis

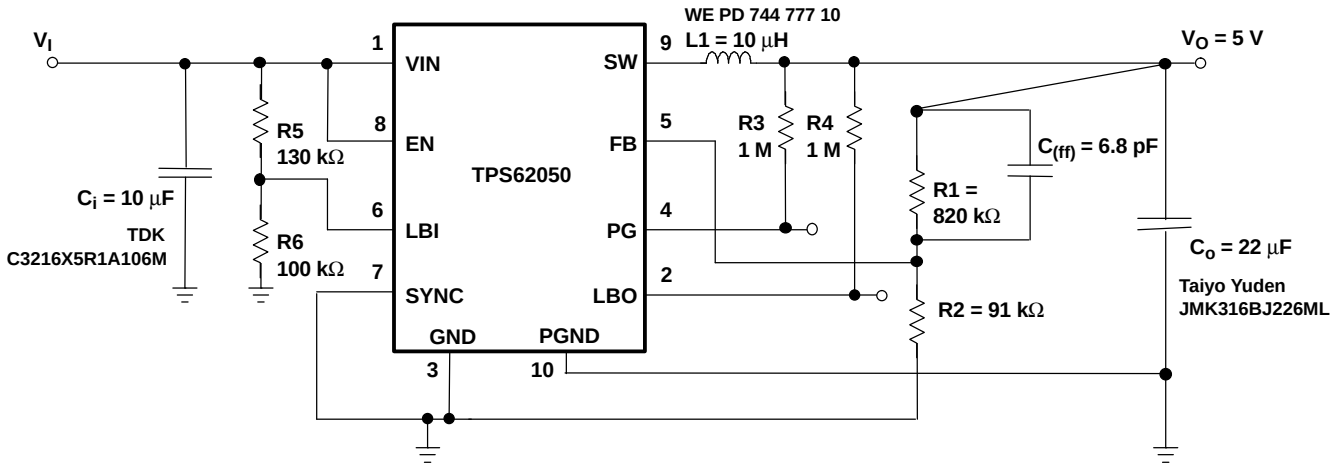
A MATHCAD™ file to calculate R7 can be downloaded from the product folder on the TI web.

APPLICATION INFORMATION (continued)

No Load Operation

If the converter operates in the forced PWM mode and there is no load connected to the output, the converter regulates the output voltage by allowing the inductor current to reverse for a short period of time.

STANDARD CIRCUIT FOR ADJUSTABLE VERSION



Quiescent Current Measurements and Efficiency Were Taken
With: R5 = Open, R4 = Open, LBI Connected to GND.

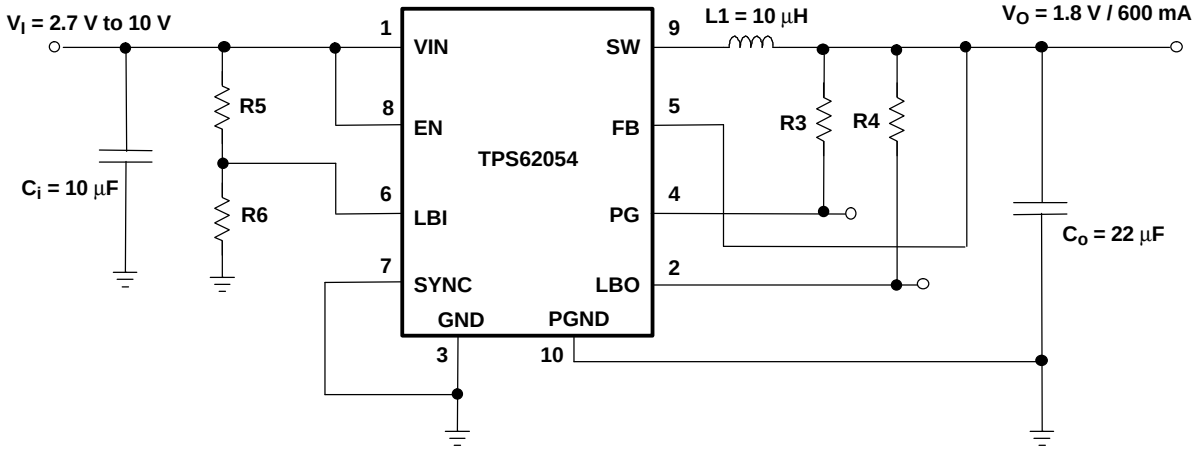
$$V_O = V_{FB} \times \frac{R1 + R2}{R2} \qquad R1 = R2 \times \left(\frac{V_O}{V_{FB}}\right) - R2 \qquad V_{FB} = 0.5V$$

Table 1. Values

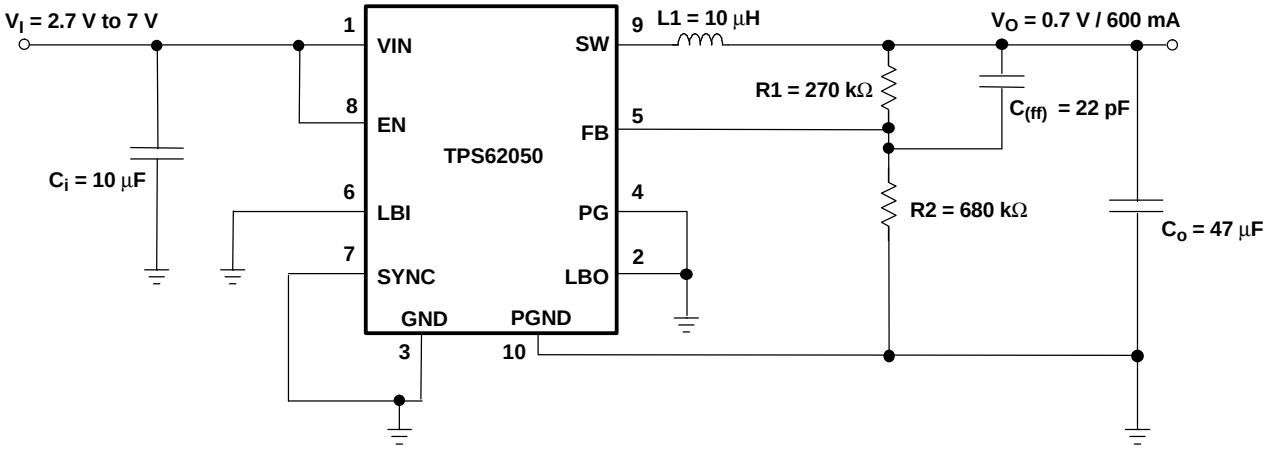
NOMINAL OUTPUT VOLTAGE	EQUATION	POSSIBLE RESISTOR COMBINATION	TYPICAL FEEDBACK CAPACITOR
0.7 V	R1 = 0.4 x R2	R1 = 270 k, R2 = 680 k	$C_{(ff)}$ = 22 pF
1.2 V	R1 = 1.4 x R2	R1 = 510 k, R2 = 360 k (1.21 V)	$C_{(ff)}$ = 6.8 pF
1.5 V	R1 = 2 x R2	R1 = 300 k, R2 = 150 k (1.50 V)	$C_{(ff)}$ = 6.8 pF
1.8 V	R1 = 2.6 x R2	R1 = 390 k, R2 = 150 k (1.80 V)	$C_{(ff)}$ = 6.8 pF
2.5 V	R1 = 4 x R2	R1 = 680 k, R2 = 169 k (2.51 V)	$C_{(ff)}$ = 6.8 pF
3.3 V	R1 = 5.6 x R2	R1 = 560 k, R2 = 100 k (3.30 V)	$C_{(ff)}$ = 6.8 pF
5 V	R1 = 9 x R2	R1 = 820 k, R2 = 91 k (5.0 V)	$C_{(ff)}$ = 6.8 pF

APPLICATION INFORMATION (continued)

STANDARD CIRCUIT FOR FIXED VOLTAGE VERSION



CONVERTER FOR 0.7-V OUTPUT VOLTAGE



The TPS62050 is used to generate output voltages as low as 0.7 V. With such low output voltages, the inductor discharges very slowly. This leads to a high output voltage ripple in power-save mode (SYNC = GND). It is therefore recommended to use a larger output capacitor to keep the output ripple low. With an output capacitor of 47 µF, the output voltage ripple is less than 40 mV_{PP}.

LAYOUT AND BOARD SPACE

All capacitors should be soldered as close as possible to the IC.

For information on the PCB layout see the user's guideSLVU081.

Keep the feedback track as short as possible. Any coupling to the FB pin may cause additional output voltage ripple.

APPLICATION INFORMATION (continued)

INDUCTOR SELECTION

A 10-µH minimum inductor should be used with the TPS6205x. Values larger than 22 µH or smaller than 10 µH may cause stability problems due to the internal compensation of the regulator. After choosing the inductor value of typically 10 µH, two additional inductor parameter should be considered: the current rating of the inductor and the dc resistance. The dc resistance of the inductance directly influences the efficiency of the converter. Therefore, an inductor with lowest dc resistance should be selected for highest efficiency. In order to avoid saturation of the inductor, the inductor should be rated at least for the maximum output current plus half the inductor ripple current which is calculated as:

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \qquad I_L(\max) = I_O(\max) + \frac{\Delta IL}{2}$$

f = Switching frequency (850 kHz typical)
L = Inductor value
ΔIL = Peak-to-peak inductor ripple current
I_L(max) = Maximum inductor current

The highest inductor current occurs at maximum VIN . A more conservative approach is to select the inductor current rating just for the maximum switch current of the TPS6205x which is 1.4 A maximum. See Table 2 for inductors that have been tested for operation with the TPS6205x.

Table 2. Inductors

MANUFACTURER	TYPE	INDUCTANCE	DC RESISTANCE	SATURATION CURRENT
TDK	SLF7032T-100M1R4SLF7032T-220M96SLF7045T-100M1R3SLF7045T-100MR90	10 µH ±20%22 µH ±20%10 µH ±20%22 µH ±20%	53 mΩ±20%110 mΩ±20%36 mΩ±20%61 mΩ±20%	1.4 A0.96 A1.3 A0.9 A
Sumida	CDR74B	10 µH	70 mΩ	1.65 A
	CDR74B	22 µH	130 mΩ	1.12 A
	CDH74	10 µH	49 mΩ	1.8 A
	CDH74	22 µH	110 mΩ	1.23 A
	CDR63B	10 µH	140 mΩ	1 A
	CDRH4D28	10 µH	128 mΩ	1 A
	CDRH5D28	10 µH	48 mΩ	1.3 A
	CDRH5D18	10 µH	92 mΩ	1.2 A
Coilcraft	DT3316P-153	15 µH	60 mΩ	1.8 A
	DT3316P-223	22 µH	84 mΩ	1.5 A
Wuerth	WE-PD 744 778 10	10 µH	72 mΩ	1.68 A
	WE-PD 744 777 10	10 µH	49 mΩ	1.84 A
	WE-PD 744 778 122	22 µH	190 mΩ	1.07A
	WE-PD 744 777 122	22 µH	110 mΩ	1.23 A

APPLICATION INFORMATION (continued)

OUTPUT CAPACITOR SELECTION

The output capacitor should have a minimum value of 22µF. For best performance, a low ESR ceramic output capacitor is needed.

For completeness, the RMS ripple current is calculated as:

$$I_{RMS(Co)} = V_O \times \frac{1-\frac{V_O}{V_I}}{L \times f} \times \frac{1}{2 \times \sqrt{3}}$$

The overall output ripple voltage is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charge and discharging the output capacitor:

$$\Delta V_O = V_O \times \frac{1-\frac{V_O}{V_I}}{L \times f} \times \left(\frac{1}{8 \times C_O \times f} + R_{ESR} \right)$$

The highest output voltage ripple occurs at the highest input voltage V_I.

INPUT CAPACITOR SELECTION

Because the buck converter has a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. The input capacitor should have a minimum value of 10 µF and can be increased without any limit for better input voltage filtering. The input capacitor should be rated for the maximum input ripple current calculated as:

$$I_{RMS} = I_O(max) \times \sqrt{\frac{V_O}{V_I} \times \left(1 - \frac{V_O}{V_I}\right)}$$

The worst case RMS ripple current occurs at D = 0.5 and is calculated as: $I_{RMS} = I_O/2$. Ceramic capacitors have a good performance because of their low ESR value and they are less sensitive to voltage transients compared to tantalum capacitors. Place the input capacitor as close as possible to the input pin of the IC for best performance.

Table 3. Capacitors

MANUFACTURER	PART NUMBER	SIZE	VOLTAGE	CAPACITANCE	TYPE
Taiyo Yuden	JMK212BJ106MG	0805	6.3 V	10 µF	Ceramic
	JMK316BJ106ML	1206	6.3 V	10 µF	Ceramic
	JMK316BJ226ML	1206	6.3 V	22 µF	Ceramic
	LMK316BJ475ML	1206	10 V	4.7 µF (1)	Ceramic
	EMK316BJ475ML	1206	16 V	4.7 µF (1)	Ceramic
	EMK325BJ106KN-T	1210	16 V	10 µF	Ceramic
Kemet	C1206C106M9PAC	1206	6.3 V	10 µF	Ceramic
TDK	C2012X5R0J106M	0805	6.3 V	10 µF	Ceramic
	C3216X5R0J226M	1206	6.3 V	22 µF	Ceramic
	C3216X5R1A106M	1206	10 V	10 µF	Ceramic

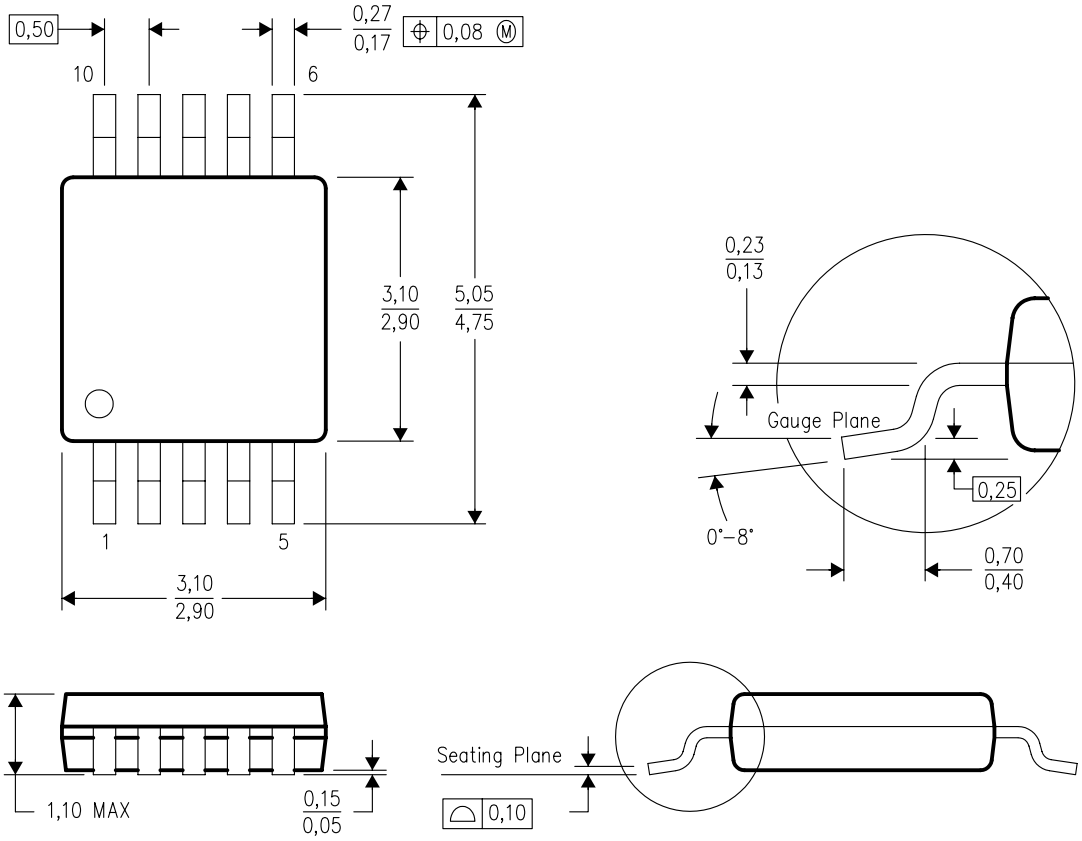
(1) Connect two in parallel.

APPLICATION INFORMATION (continued)

Table 4. Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE	INTERNET
Taiyo Yuden	X7R/X5R ceramic	www.t-yuden.com
TDK	X7R/X5R ceramic	www.component.tdk.com
Vishay	X7R/X5R ceramic	www.vishay.com
Kemet	X7R/X5R ceramic	www.kemet.com

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

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