

CSD83325L 12 V Dual N-Channel NexFET™ Power MOSFET

1 Features

- Common Drain Configuration
- Low On Resistance
- Small Footprint of 2.2 mm × 1.15 mm
- Pb-Free
- RoHS Compliant
- Halogen Free
- Gate ESD Protection

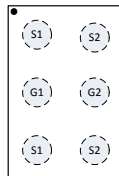
2 Applications

- Battery Management
- Battery Protection

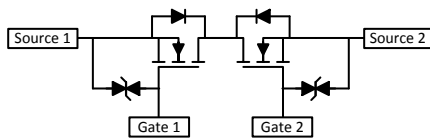
3 Description

This 12 V, 9.9 mΩ, 2.2 mm × 1.15 mm LGA Dual NexFET™ power MOSFET is designed to minimize resistance and gate charge in a small footprint. Its small footprint and common drain configuration make the device ideal for battery pack applications in small handheld devices.

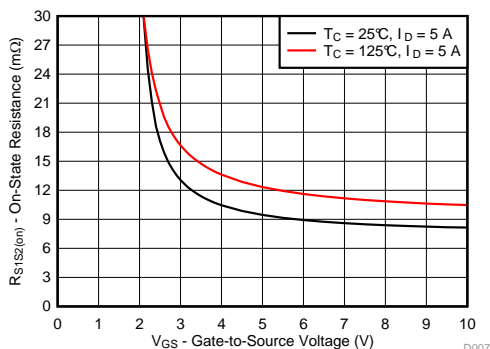
Top View



Configuration



$R_{DS(on)}$ vs V_{GS}



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{S1S2}	Source-to-Source Voltage	12		V
Q_g	Gate Charge Total (4.5 V)	8.4		nC
Q_{gd}	Gate Charge Gate-to-Drain	1.9		nC
$R_{S1S2(on)}$	Source-to-Source On-Resistance	$V_{GS} = 2.5\text{ V}$	17.5	mΩ
		$V_{GS} = 3.8\text{ V}$	10.9	mΩ
		$V_{GS} = 4.5\text{ V}$	9.9	mΩ
$V_{GS(th)}$	Threshold Voltage	0.95		V

Ordering Information⁽¹⁾

Device	Qty	Media	Package	Ship
CSD83325L	3000	7-Inch Reel	2.2 × 1.15 mm Land Grid Array (LGA) Package	Tape and Reel
CSD83325LT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{S1S2}	Source-to-Source Voltage	12	V
V_{GS}	Gate-to-Source Voltage	±10	V
I_S	Continuous Source Current ⁽¹⁾	8	A
I_{SM}	Pulsed Source Current ⁽²⁾	52	A
P_D	Power Dissipation	2.3	W
$V_{(ESD)}$	Human Body Model (HBM)	2	kV
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150	°C

(1) Device operating at a temperature of 105°C.

(2) Typical min Cu $R_{\theta JA} = 150^\circ\text{C}/\text{W}$, pulse duration $\leq 100\ \mu\text{s}$, duty cycle $\leq 1\%$

Gate Charge

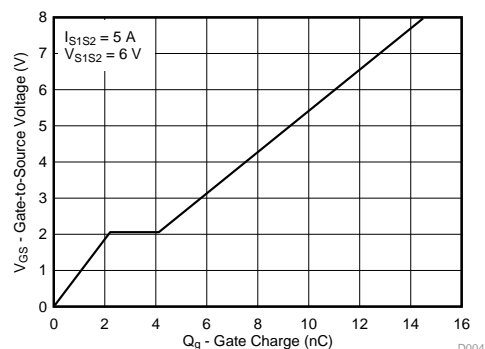


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4 Revision History

DATE	REVISION	NOTES
November 2014	*	Initial release.

5 Specifications

5.1 Electrical Characteristics

 $(T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{S1S2}	Source-to-Source Voltage	$V_{GS} = 0\text{ V}, I_S = 250\ \mu\text{A}$	12			V
I_{S1S2}	Source-to-Source Leakage Current	$V_{GS} = 0\text{ V}, V_{S1S2} = 9.6\text{ V}$			1	μA
I_{GSS}	Gate-to-Source Leakage Current	$V_{S1S2} = 0\text{ V}, V_{GS} = 10\text{ V}$			10	μA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{S1S2} = V_{GS}, I_S = 250\ \mu\text{A}$	0.75	0.95	1.25	V
$R_{S1S2(on)}$	Source-to-Source On-Resistance	$V_{GS} = 2.5\text{ V}, I_S = 5\text{ A}$	14.0	17.5	23.0	m Ω
		$V_{GS} = 3.8\text{ V}, I_S = 5\text{ A}$	8.8	10.9	13.0	m Ω
		$V_{GS} = 4.5\text{ V}, I_S = 5\text{ A}$	7.9	9.9	11.9	m Ω
g_{fs}	Transconductance	$V_{S1S2} = 1.2\text{ V}, I_S = 5\text{ A}$		36		S
DYNAMIC CHARACTERISTICS⁽¹⁾						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{S1S2} = 6\text{ V}, f = 1\text{ MHz}$		902	1170	pF
C_{oss}	Output Capacitance			187	243	pF
C_{rss}	Reverse Transfer Capacitance			111	144	pF
Q_g	Gate Charge Total (4.5 V)	$V_{S1S2} = 6\text{ V}, I_S = 5\text{ A}$		8.4	10.9	nC
Q_{gd}	Gate Charge Gate-to-Drain			1.9		nC
Q_{gs}	Gate Charge Gate-to-Source			2.2		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.6		nC
Q_{oss}	Output Charge	$V_{S1S2} = 6\text{ V}, V_{GS} = 0\text{ V}$		2.9		nC
$t_{d(on)}$	Turn On Delay Time	$V_{S1S2} = 6\text{ V}, V_{GS} = 4.5\text{ V},$ $I_{S1S2} = 5\text{ A}, R_G = 0\ \Omega$		205		ns
t_r	Rise Time			353		ns
$t_{d(off)}$	Turn Off Delay Time			711		ns
t_f	Fall Time			589		ns

(1) Dynamic Characteristics values specified are per single FET.

5.2 Thermal Information

 $(T_A = 25^\circ\text{C}$ unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ⁽¹⁾		150		$^\circ\text{C/W}$
	Junction-to-Ambient Thermal Resistance ⁽²⁾		55		

(1) Device mounted on FR4 material with minimum Cu mounting area.

(2) Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

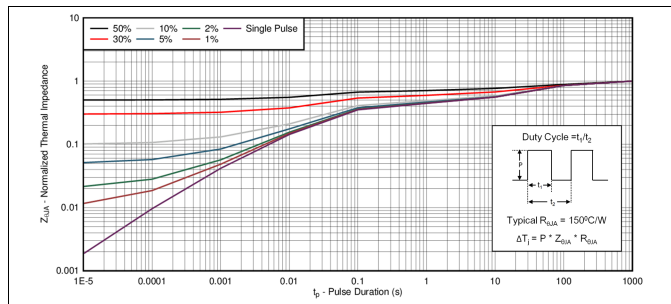


Figure 1. Transient Thermal Impedance

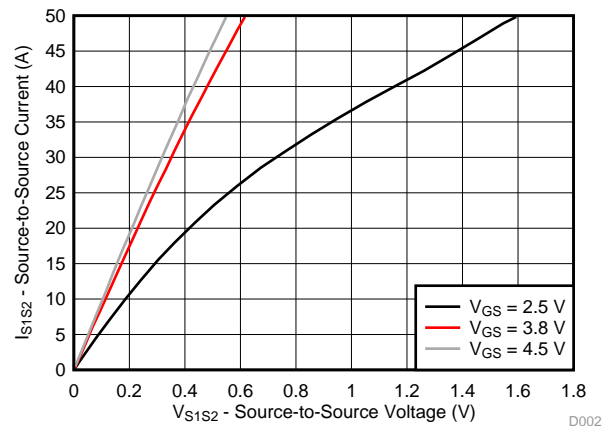


Figure 2. Saturation Characteristics

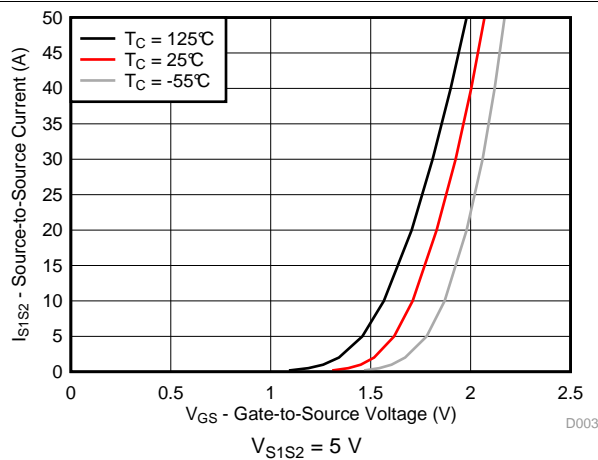


Figure 3. Transfer Characteristics

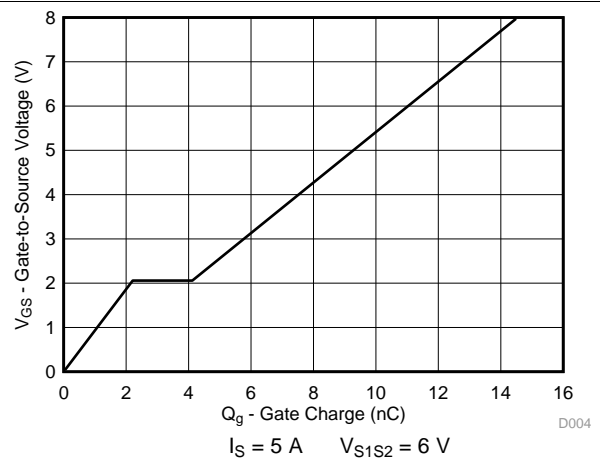
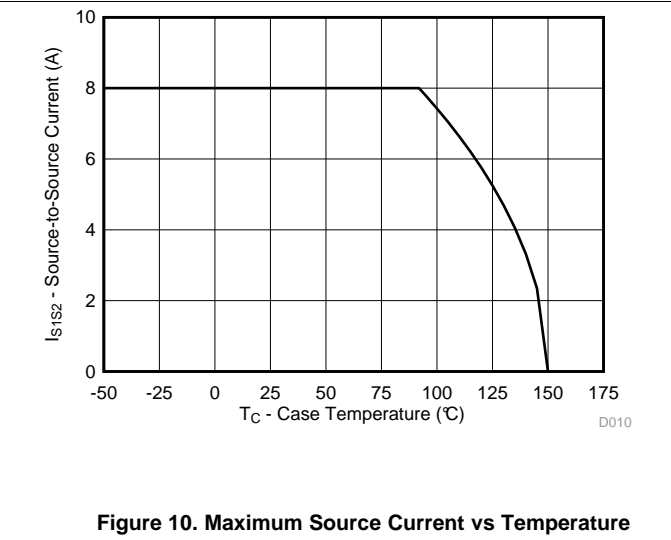
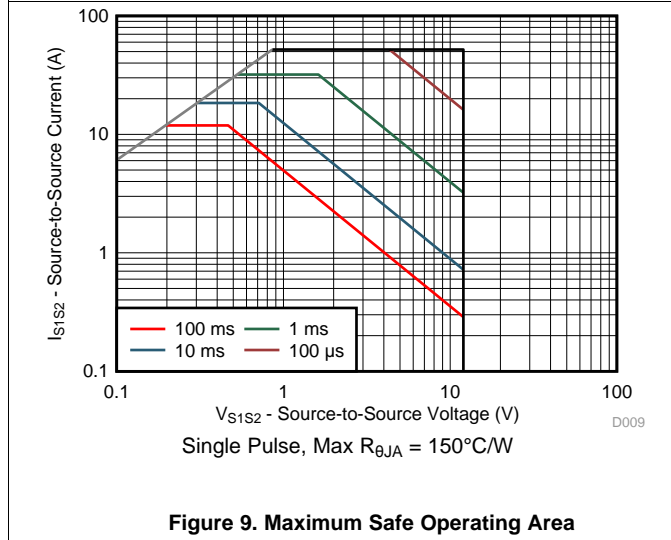
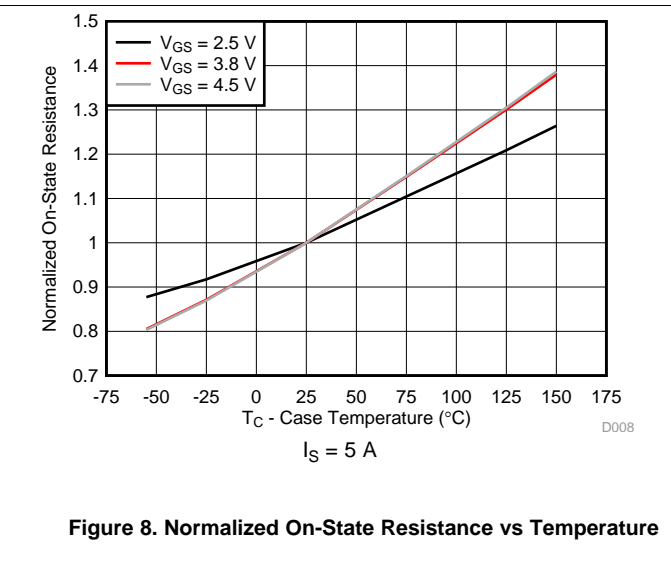
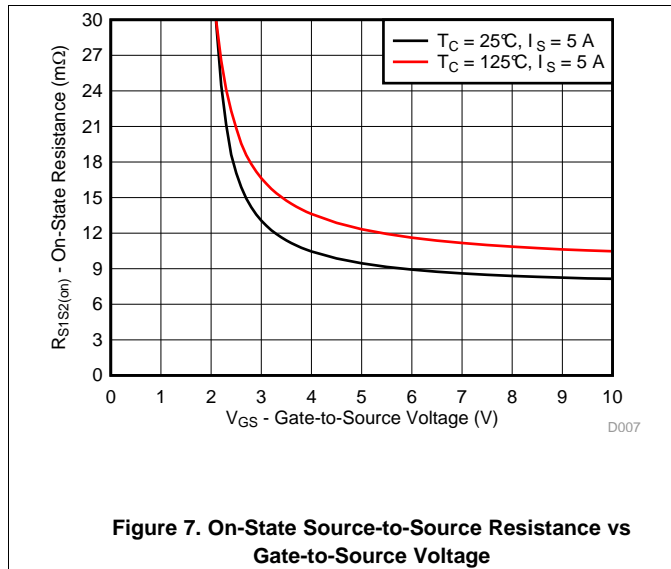
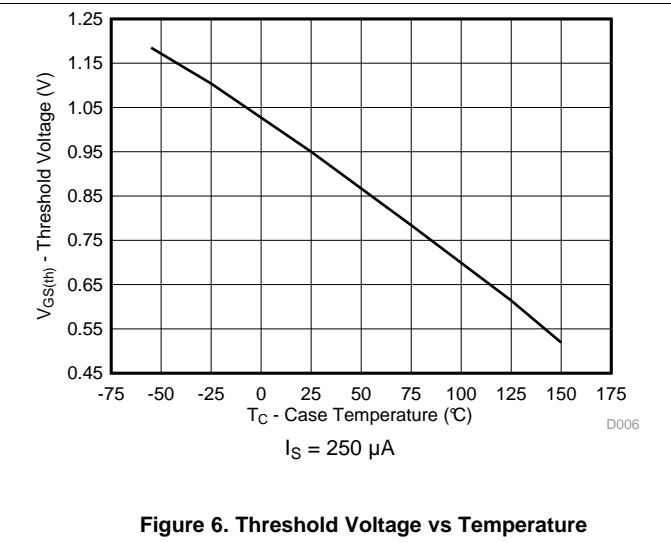
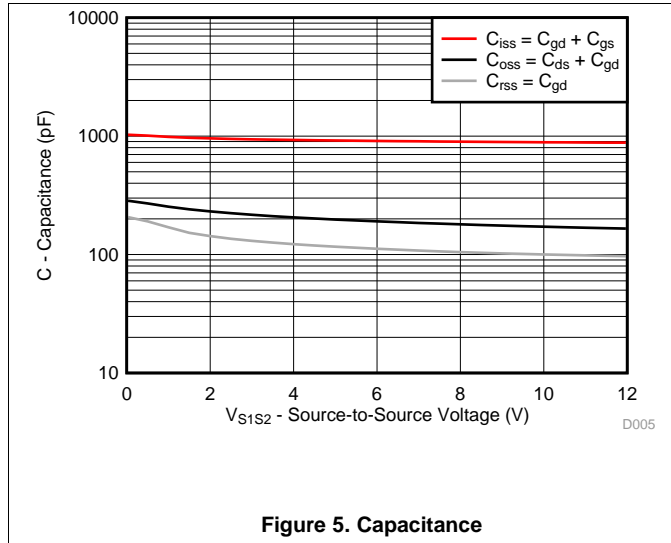


Figure 4. Gate Charge

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)



6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

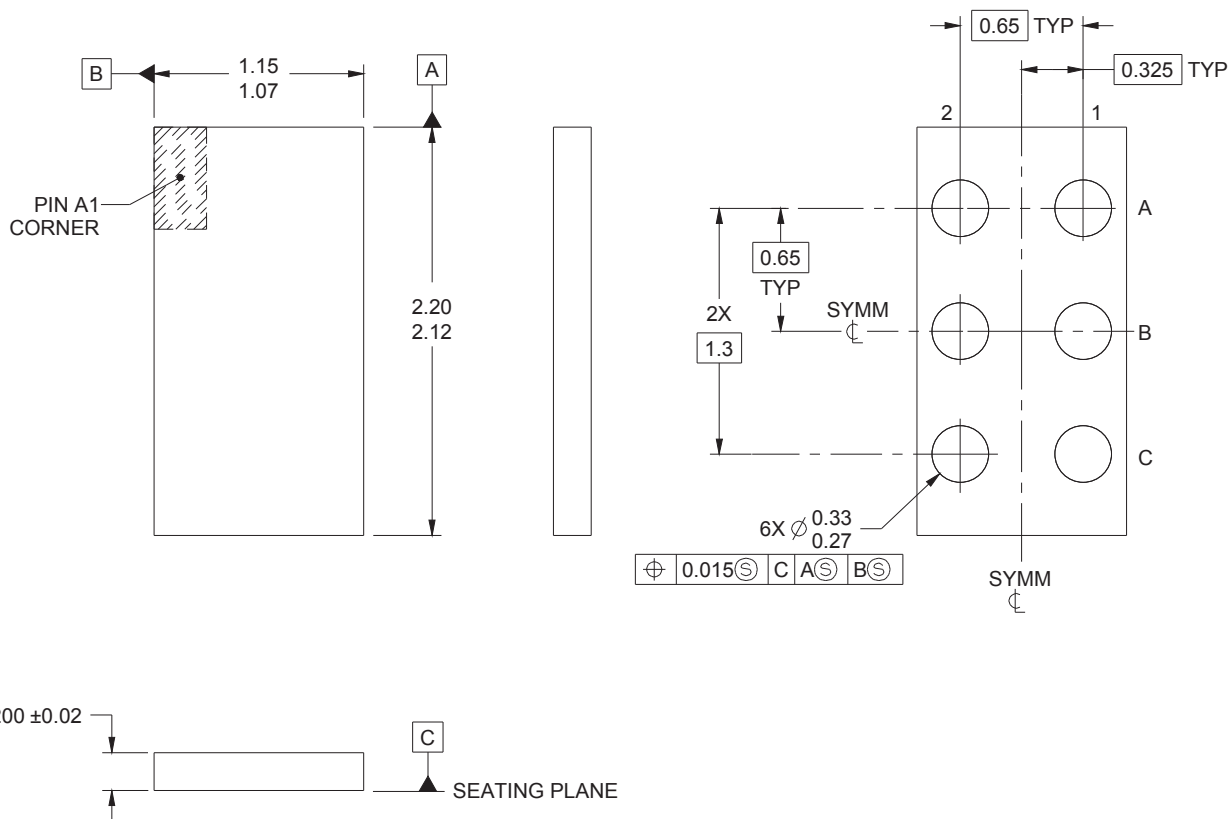
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

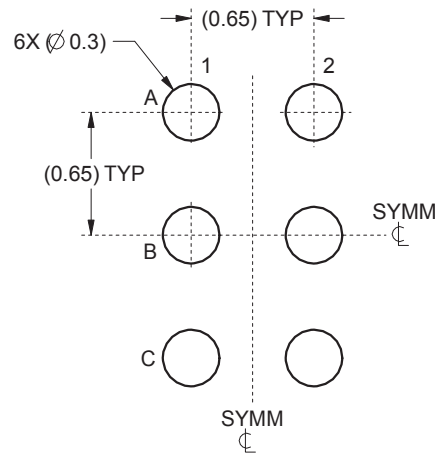
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Package Dimensions

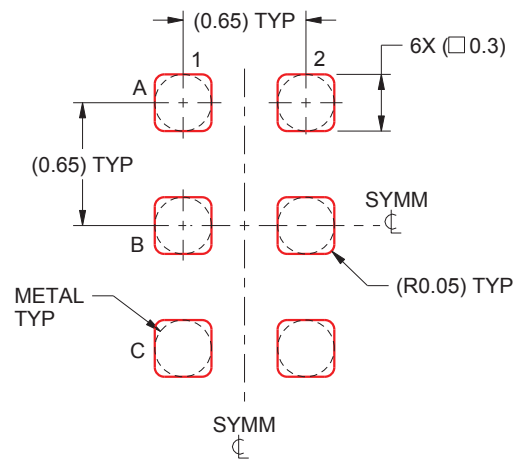


All dimensions in millimeters

7.2 Recommended PCB Pattern



7.3 Recommended Stencil Pattern



All dimensions are in millimeters

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD83325L	ACTIVE	PICOSTAR	YJE	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM		83325L	Samples
CSD83325LT	ACTIVE	PICOSTAR	YJE	6	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM		83325L	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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