Radiation Hardened 3.3V Quad Differential Line Receiver

HS-26CLV32RH, HS-26CLV32EH

The Intersil HS-26CLV32RH, HS-26CLV32EH are radiation hardened 3.3V quad differential line receiver designed for digital data transmission over balanced lines, in low voltage, RS-422 protocol applications. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26CLV32RH, HS-26CLV32EH have an input sensitivity of 200mV (Typ) over a common mode input voltage range of -4V to +7V. The receivers are also equipped with input fail safe circuitry, which causes the outputs to go to a logic "1" when the inputs are open. The device has unique inputs that remain high impedance when the receiver is disabled or powered-down, maintaining signal integrity in multi-receiver applications.

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95689. A "hot-link" is provided on our homepage for downloading.

Features

- Electrically screened to SMD # 5962-95689
- QML qualified per MIL-PRF-38535 requirements
- 1.2 micron radiation hardened CMOS
  - Total dose . . . . . 300 krad(Si)(max)
  - Single event upset LET . . . . . 100MeV/mg/cm^2)
  - Single event latch-up immune
- Low stand-by current . . . . . 13mA(max)
- Operating supply range . . . . . 3.0V to 3.6V
- Enable input levels. . . . . V_{IH} > (0.7)(V_{DD}); V_{IL} < (0.3)(V_{DD})
- CMOS output levels . . . . . V_{OH} > 2.55V; V_{OL} < 0.4V
- Input fail safe circuitry
- High impedance inputs when disabled or powered-down
- Full -55°C to +125°C military temperature range
- Pb-free (RoHS compliant)

Applications

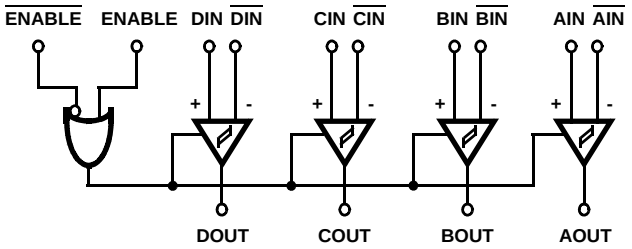
- Line receiver for MIL-STD-1553 serial data bus

Ordering Information

PART NUMBER (Note)	INTERNAL MKT. NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
5962F9568902QEC	HS1-26CLV32RH-8	Q 5962F95 68902QEC	-55 to +125	16 Ld SBDIP	D16.3
5962F9568902QXC	HS9-26CLV32RH-8	Q 5962F95 68902QXC	-55 to +125	16 Ld FLATPACK	K16.A
5962F9568902VEC	HS1-26CLV32RH-Q	Q 5962F95 68902VEC	-55 to +125	16 Ld SBDIP	D16.3
5962F9568902VXC	HS9-26CLV32RH-Q	Q 5962F95 68902VXC	-55 to +125	16 Ld FLATPACK	K16.A
5962F9666302V9A	HS0-26CLV31RH-Q		-55 to +125	Die	
HS0-26CLV31RH/SAMPLE	HS0-26CLV31RH/SAMPLE		-55 to +125	Die	
HS1-26CLV32RH/PROTO	HS1-26CLV32RH/PROTO	HS1- 26CLV32RH /PROTO	-55 to +125	16 Ld SBDIP	D16.3
HS9-26CLV32RH/PROTO	HS9-26CLV32RH/PROTO	HS9- 26CLV32RH /PROTO	-55 to +125	16 Ld FLATPACK	K16.A
5962F9568904VEC	HS1-26CLV32EH-Q	Q 5962F95 68904VEC	-55 to +125	16 Ld SBDIP	D16.3
5962F9568904VXC	HS9-26CLV32EH-Q	Q 5962F95 68904VXC	-55 to +125	16 Ld FLATPACK	K16.A
5962F9568904V9A	HS0-26CLV32EH-Q		-55 to +125	Die	

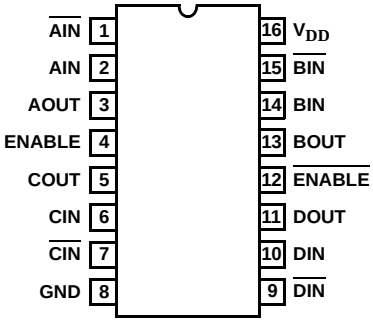
NOTE: These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Logic Diagram

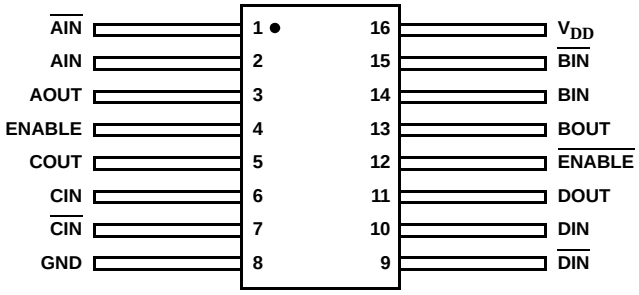


Pin Configurations

HS1-26CLV32RH, HS1-26CLV32EH
(16 LD SBDIP)
MIL-STD-1835: CDIP2-T16
TOP VIEW



HS9-26CLV32RH, HS9-26CLV32EH
(16 LD FLATPACK)
MIL-STD-1835: CDFP4-F16
TOP VIEW



NOTES:

1. For details on input output structures refer to application note AN9520.
2. For details on package dimensions refer MIL STD 1835.

Die Characteristics

DIE DIMENSIONS:

78 mils x 123 mils x 21 mils
(1970µm x 3120µm)

INTERFACE MATERIALS:

Glassivation:

Type: PSG (Phosphorus Silicon Glass)
Thickness: 8kÅ ±1kÅ

Substrate:

AVLSI1RA, Silicon backside, V_{DD} backside potential

Metallization:

Bottom: Mo/TiW
Thickness: 5800Å ±1kÅ
Top: Al/Si/Cu
Thickness: 10kÅ ±1kÅ

Worst Case Current Density:

$<2.0 \times 10^5 A/cm^2$

Bond Pad Size:

110µm x 100µm

Metallization Mask Layout

HS-26CLV32RH, HS-26CLV32EH

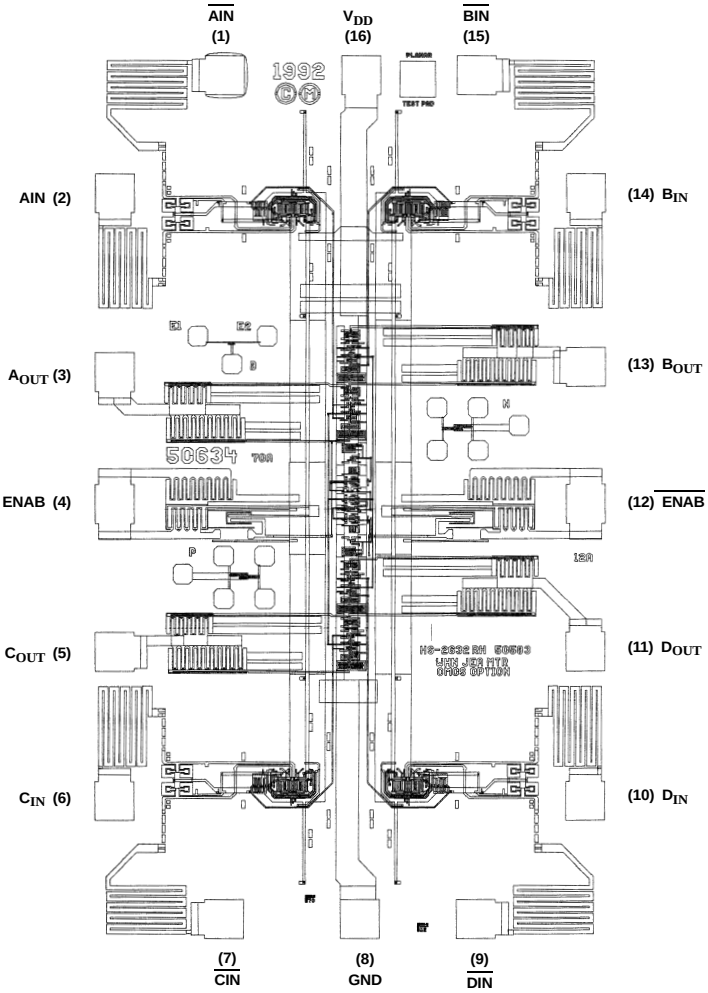


TABLE 1. HS-26CLV32RH, HS-26CLV32EH PAD COORDINATES

PIN NUMBER	PAD NAME	RELATIVE TO PIN 1	
		X COORDINATES	Y COORDINATES
1	$\overline{AIN}$	0	0
2	AIN	-337.1	-362
3	A_{OUT}	-337.1	-912.5
4	ENABLE	-337.1	-1319.3
5	C_{OUT}	-337.1	-1774.4
6	CIN	-337.1	-2233.7
7	$\overline{CIN}$	0	-2595.7
8	GND	418.4	-2596.7
9	$\overline{DIN}$	776.4	-2595.7
10	DIN	1113.5	-2233.7
11	D_{OUT}	1113.5	-1774.4
12	$\overline{ENABLE}$	1113.5	-1319.3
13	B_{OUT}	1113.5	-898.4
14	BIN	1113.5	-362
15	$\overline{BIN}$	776.4	0
16	VDD	420.2	1

NOTE: Dimensions in microns