MCRF450/451/452/455

13.56 MHz Read/Write Passive RFID Device

Features

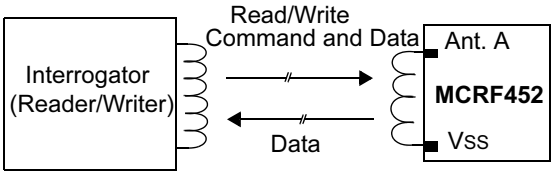
- Contactless read and write with anti-collision algorithm
- 1024 bits (32 blocks) of total memory
- 928 bits (29 blocks) of user programmable memory
- Unique 32-bit tag ID (factory programmed)
- 32 bits for data and 16 bits for CRC per block
- Block write protection
- 70 Kbit/s read data rate (Manchester format)
- Special bit (Fast Read) for fast identification and anti-counterfeit applications (EAS)
- 1-of-16 PPM encoding for writing data
- Interrogator-Talks-First (ITF) or Tag-Talks-First (TTF) operation
- Long range for reading and writing
- High-speed anti-collision algorithm for reading and writing
- Fast and Normal modes for write data speed
- Anti-tearing feature for secure write transactions
- Asynchronous operation for low power consumption and flexible choice of carrier frequency bands
- Internal resonance capacitors (MCRF451/452/ 455)
- Two pad connections for external antenna circuit (MCRF452)
- Three pad connections for external antenna circuit (MCRF450, 451, 455)
- Very low power CMOS design
- Die in waffle pack, wafer, wafer on frame, bumped wafer, COB, PDIP or SOIC package options

Applications

- **Item Level Tagging:** To read and write multiple items in long read range environment.
- **Anti-Counterfeit:** The device has a unique feature to distinguish between paid, unpaid or returned merchandise.
- **Inventory Management:** Tag's data can be read or updated (written) in multiple tags and long range environment. Its memory (32 blocks, 1 Kbit, each block = 32 bits) is well organized for the inventory management applications.
- **Product Identification**s
- Airline Baggage Tracking
- Book Store and Library Book ID
- **Low Cost Animal Ear Tags:** The device's long range reading performance combined with 1 Kbit of memory is suitable for animal tagging applications. Tag cost can be cheaper and read range is much longer than existing 125 kHz conventional animal ear tags.
- **Toys and Gaming Tools:** Device's anti-collision feature for reading and writing allows to make intelligent interactive toys and gaming tools.
- **Access Control and Time Attendance Cards:** Device's long range performance allows to make long range access control, parking lot entry, and time attendance cards.

Inexpensive finished tags and readers are available from Microchip's worldwide OEM partners. Please contact Microchip Technology Inc. near you or visit http://www.microchip.com for further product information and inquiries for your applications.

Typical Configuration for Applications

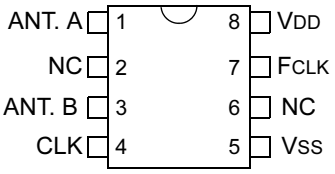


Read/Write Range:~ up to 1.5 meters depending on tag size and system requirements.

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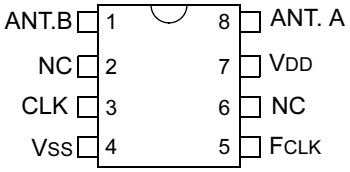
Package Types

PDIP ("P")



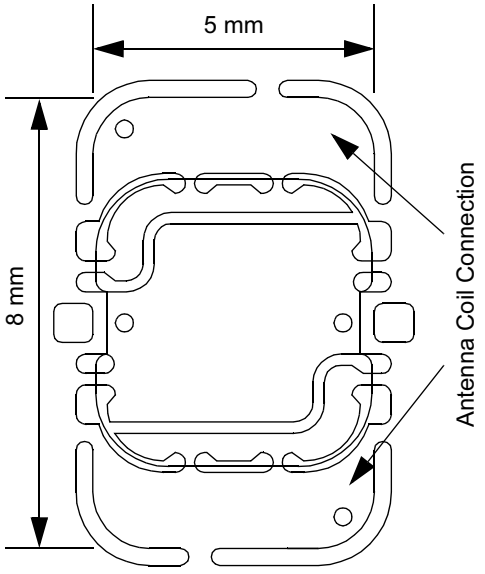
Note: Pins 4, 7 and 8 are for device test purposes only
NC = Not Connected
MCRF450/451/455: Antenna connections = pins 1, 3 and 5
MCRF452: Antenna connections = pins 1 and 5

ROTATED SOIC ("X/SN")



Note: Pins 3, 5 and 7 are for device test purposes only
NC = Not Connected
MCRF450/451/455: Antenna connections = pins 1, 4 and 8
MCRF452: Antenna connections = pins 4 and 8

MCRF450 COB ("7M")



Thickness = 0.4 mm

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1.0 DESCRIPTION OF DEVICE FEATURES

The MCRF450/451/452/455 is a contactless read/write passive RFID device that is optimized for 13.56 MHz RF carrier signal. The device needs an external LC resonant circuit to communicate wirelessly with the Interrogator. The device is powered remotely by rectifying an RF signal that is transmitted from the Interrogator and transmits or updates its contents from memory-based on commands from the Interrogator.

The device is engineered to be used effectively for item level tagging applications, such as retail and inventory management, where a large volume of tags are read and written in the same Interrogator field.

The device contains 32 blocks (B0-B31) of EEPROM memory. Each block consists of 32 bits. The first three blocks (B0-B2) are allocated for device operation, while the remaining 29 blocks (B3-B31: 928 bits) are for user data. Block 1 contains unique 32 bits of Tag ID. The Tag ID is preprogrammed at the factory and write protected.

All blocks, except for the Tag ID (Block 1), are contactlessly writable block-wise by Interrogator commands. All data blocks, with the exception of bits 30 and 31 in Block 0, are write-protectable.

The device can be configured as either Tag-Talks-First (TTF) or Interrogator-Talks-First (ITF). In TTF mode, the device transmits its fast response data (160 bits max., see Example 9-1) as soon as it is energized, then waits for the next command. In ITF mode, the device requires an Interrogator command before it sends any data. The control bits for TTF and ITF modes are bits 30 and 31 in Block 0.

All downlink commands from the Interrogator are encoded using 1-of-16 Pulse Position Modulation (PPM) and specially timed gap pulses. This encoded information amplitude modulates the Interrogator's RF carrier signal.

At the other end, the MCRF450/451/452/455 device demodulates the received RF signal and then sends data (from memory) at 70 Kbit/s back to the Interrogator in Manchester format.

The communication between Interrogator and device takes place asynchronously. Therefore, to enhance the detection accuracy of the device, the Interrogator sends a time reference signal (time calibration pulse) to the device, followed by the command and programming data. The time reference signal is used to calibrate timing of the internal decoder of the device.

There are device options for the internal resonant capacitor between antenna A and VSS: (a) no internal resonant capacitor for the MCRF450, (b) 100 pF for the MCRF451, (c) two 50 pF in series (25 pF in total) for the MCRF452 and (d) 50 pF for the MCRF455. The internal resonant capacitors for each device are shown in Figures 2-2 through 2-5.

The MCRF450 needs an external LC resonant circuit connected between antenna A, antenna B and VSS pads. See Figure 2-2 for the external circuit configuration. The MCRF452 needs a single external antenna coil only between antenna A and VSS pads, as shown in Figure 2-4.

This external circuit, along with the internal resonant capacitor, must be tuned to the carrier frequency of the Interrogator for maximum performance.

When a tag (device with the external LC resonant circuit) is brought to the Interrogator's RF field, it develops an RF voltage across the external circuit. The device rectifies the RF voltage and develops a DC voltage (VDD). The device becomes functional as soon as VDD reaches the operating voltage level.

The device then sends data stored in memory to the Interrogator by turning on/off the internal modulation transistor. This internal modulation transistor is located between antenna B and VSS. The modulation transistor has a very small turn-on resistance between Drain (antenna B) and Source (VSS) terminals during its turn-on time.

When the modulation transistor turns on, the resonant circuit component between antenna B and VSS, which is in parallel with the modulation transistor, is shorted due to the low turn-on resistance. This results in a change in the LC value of the circuit. As a result, the circuit no longer resonates at the carrier frequency of the Interrogator. Therefore, the voltage across the circuit is minimized. This condition is called "cloaking".

When the modulation transistor turns off, the circuit resonates at the carrier frequency of the Interrogator and develops maximum voltage. This condition is called "uncloaking". Therefore, the data is sent to the Interrogator by turning on (cloaking) and off (uncloaking) the modulation transistor.

The voltage amplitude of the carrier signal across the LC resonant circuit changes depending on the amplitude of modulation data. This is called an amplitude modulation signal. The receiver channel in the Interrogator detects this amplitude modulation signal and reconstructs the modulation data for decoding.

The device includes a unique anti-collision algorithm to be read or written effectively in multiple tag environments. To minimize data collision, the algorithm utilizes time division multiplexing of the device response. Each device can communicate with the Interrogator in a different time slot. The devices in the Interrogator's RF field remain in a nonmodulating condition if they are not in the given time slot. This enables the Interrogator to communicate with the multiple devices one at a time without data collision. The details of the algorithm are described in **Section 6.0 "Read/Write Anti-Collision Logic"**.

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To enhance data integrity for writing, the device includes an anti-tearing feature. This anti-tearing feature provides verification of data integrity for incomplete write cycles due to failed communication between the Interrogator and the device during the write sequences.

1.1 Device's Communication with Interrogator

The device can be operated in either Fast Read Request (FRR) or Fast Read Bypass (FRB) mode, depending on the status of bit 31 (FR: bit) of Block 0. If the FR bit is set, the device is operated in FRR mode, and FRB mode, if the FR bit is cleared. The FR bit is always reprogrammable and not write-protectable. The FRR mode is a default setting. The communication between the Interrogator and tag starts with a FRR or FRB command.

In FRR mode, the device sends a response only when it receives the FRR command, not the FRB command.

Conversely, the device in FRB mode sends a response when it receives the FRB command only, not the FRR command.

If the device is set to FRR mode and also set to TTF mode (TF bit = set), the device can send the FRR response as soon as it is energized.

One of the main purposes of using the two different modes (FRR and FRB) is to use the device effectively in the item level supply-chain application, where a rapid identification and an effective anti-collision read/write process is needed (i.e., to identify whether it is a paid or unpaid item, or whether it passed one particular point of interest or not). This can be done by either checking the status of the FR bit or by checking the response of the tag to the command. For this reason, the FR bit is also called an Electronic Article Surveillance (EAS) bit.

1.1.1 OPERATION OF TAG IN FRR MODE

If the device is in the FRR mode (FR bit = set), the communication between the Interrogator and the device can start in two ways, depending on the status of TF (Bit 30 of Block 0). If the TF bit is cleared, it is called ITF mode. In this case, the tag waits for the Interrogator's FRR command and sends the FRR response data when it sees the FRR command. If the TF bit is set, the device is in a TTF mode. In this case, the tag sends the FRR response as soon as it is energized, even without the FRR command. The tag has a short listening window (1 ms) immediately after the FRR response. The Interrogator sends its next command during this listening window.

The FRR response includes the 32 bits of tag ID and FRF (Blocks 3 -5). See Tables 7-3, 7-4 and 7-6 for data. The Interrogator identifies which tags are in the field by receiving their FRR responses.

Based upon the FRR response, the Interrogator will send Matching Code 1 (MC1) or Matching Code 2 (MC2) during the tag's listening window. The Interrogator sends the MC1 to put the tag into Sleep mode. Tags in Sleep mode never respond to any command. Removal of the Interrogator's RF energy from the device is the only way to wake-up the device.

If the tag needs further read/write processing, the Interrogator sends the MC2, followed by a Read or Write command. After the completion of reading or writing of block data, the Interrogator sends an End command to put the tag into Sleep mode.

The reading and writing of the FRR devices takes place in the Anti-collision mode. For instance, if there are multiple tags in the field, the Interrogator selects one tag at a time by controlling the tag's time slot for the FRR response. The Interrogator repeats this sequence until all tags in its field are processed:

- send FRR command
- receive FRR response
- send Matching Code 1 or 2 at tag's listing window
- send Read Block command/or send Write Block command and data
- verify read/write response
- send End command
- verify the End command response
- look for other tag's FRR responses

1.1.2 OPERATION OF TAG IN FRB MODE

The communication with the device in the FRB mode is initiated by the FRB command only. If the device sees the Interrogator's FRB command, it sends its 32-bit tag ID and waits for the MC2. This is followed by a Read or Write command. Once the device is read or written, the Interrogator sends an End command. Unlike the FRR mode, the reading and writing of the tag are processed in a non Anti-collision mode.

See **Section 6.0 "Read/Write Anti-Collision Logic"**, for the read and write anti-collision algorithm. See Example 9-1 for command sequences and device responses.

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2.0 ELECTRICAL CHARACTERISTICS

TABLE 2-1: ABSOLUTE RATINGS

Parameters	Symbol	Min	Max	Units	Conditions
Coil current into coil pad	I_{PP_AC}	—	40	mA	Peak-to-Peak coil current
Maximum power dissipation	P_{MPD}	—	0.5	W	—
Ambient temperature with power applied	T_{AMB}	-40	+125	°C	—
Assembly temperature	T_{ASM}	—	300	°C	< 10 sec.
Storage temperature	T_{STORE}	-65	150	°C	—

Note: Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 2-2: OPERATING DC CHARACTERISTICS

	Standard Operating Conditions (unless otherwise stated) Operating Temperature = -20°C to +70°C					
Parameters	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Reading voltage	V_{DDR}	2.8	—	—	V	V_{DD} voltage for reading at 25°C
Operating current in Normal mode	I_{OPER_N}	—	20	—	μA	V_{DD} = 2.8V during reading at 25°C
Operating current in Fast mode	I_{OPER_F}	—	45	—	μA	V_{DD} = 2.8V during reading at 25°C
Writing current	I_{WRITE}	—	130	—	μA	At 25°C, V_{DD} = 2.8V
Writing voltage	V_{WRITE}	2.8	—	—	V_{DC}	At 25 °C
Modulation resistance	R_M	—	3.0	5.0	Ω	DC turn-on resistance between Drain and Source terminals of the modulation transistor at V_{DD} = 2.8V
Data retention	—	200	—	—	Years	For T < 120°C
Endurance	—	1.0	—	—	Million Cycles	At 25°C

TABLE 2-3: OPERATING AC CHARACTERISTICS

	Standard Operating Conditions (unless otherwise stated) Operating Temperature = -20°C to +70°C.					
Parameters	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Carrier frequency	FC	2.0	13.56	35	MHz	
Device data rate	FM	58	70	82	kHz	Manchester coding, both Normal and Fast modes, 70 kHz ±17% **(Note 1)**
Pulse width of 1-of-16 PPM for Normal mode	PWPPM_N	145	175	205	µs	See Figure 6-2 and Table 6-7, 175 µs ±17%
Pulse width of 1-of-16 PPM for Fast mode	PWPPM_F	8.3	10	11.7	µs	See Figure 6-2 and Table 6-7
Symbol duration of 1-of-16 PPM for Normal mode	SWPPM_N	2.32	2.8	3.28	ms	See Figure 6-9
Symbol duration of 1-of-16 PPM for Fast mode	SWPPM_F	133	160	187	µs	
Modulation index of gap pulse	MODINDEX_GAP	20	60	100	%	See Figure 6-2
Gap width of Interrogator command and data except Fast mode data	GAPWIDTH_N	20	100	150	µs	See Figure 6-2 and Table 6-7
Gap width of Fast mode data	GAPWIDTH_F	6.0	7.0	8.0	µs	See Figure 6-2 and Table 6-7
Coil voltage during reading	VPP_AC	4.0	—	—	VPP	Peak-to-Peak voltage across the coil during reading
Detuning voltage	VDETUNE	3.0	4.0	—	VDC	VDD voltage at which the input voltage limiting circuit becomes active
EEPROM (Memory) Writing Time	TWRITE	—	5.0	—	ms	Write time for a 32-bit block
Command Decode Time	TDECODE	0.97	1.225	1.48	ms	Time delay between end of command symbol and start of the device response
Time slot	TSLOT	2.1	2.5	2.93	ms	
Listening Window	TLW	0.82	1.0	1.17	ms	
Command Duration of Fast Read command (FRR and FRB)	T_CMD_FRR	1.305	1.575	1.845	ms	175 µs/pulse position x 9 pulse positions = 1.575 ms
Internal Resonant Capacitor	CRES_100	85.5	95	104.5	pF	Between Ant. A and VSS pads at 13.56 MHz and at 25°C (MCRF451) See Figure 2-3
	CRES_2_50	27	30	33	pF	Between Ant. A and VSS pads at 13.56 MHz and at 25°C (MCRF452) See Figure 2-4
	CRES_50	45	50	55	pF	Between Ant. A and VSS pads at 13.56 MHz and at 25°C (MCRF455) See Figure 2-5
Parasitic Input Capacitance of MCRF450	CPARA_IN	—	3.5	—	pF	Between antenna pad A and VSS, at 13.56 MHz with modulation transistor off (no external coils). Not tested in production

Note 1: Tested in production at VDD = 2.8 VDC and 5.0 VDC.

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TABLE 2-4: PAD COORDINATES (MICRONS)

Pad Name	Lower		Upper		Passivation Openings		Pad Center X	Pad Center Y
	Left X	Left Y	Right X	Right Y	Pad Width	Pad Height		
Ant. Pad A	-853.50	-992.10	-764.50	-903.10	89.00	89.00	-809.00	-947.60
Ant. Pad B	759.50	-993.70	848.50	-904.70	89.00	89.00	804.00	-949.20
VSS	769.10	977.90	858.10	1066.90	89.00	89.00	813.60	1022.40
VDD	-839.50	45.50	-750.50	134.50	89.00	89.00	-795.00	90.00
CLK	721.10	77.80	810.10	166.80	89.00	89.00	765.60	122.30
FCLK	-821.50	910.70	-732.50	999.70	89.00	89.00	-777.00	955.20

Note 1: All coordinates are referenced from the center of the die.

TABLE 2-5: DIE MECHANICAL DIMENSIONS

Specifications	Min	Typ	Max	Unit	Comments
Bond pad opening	— —	3.5 x 3.5 89 x 89	— —	mil μm	**Note 1**, **Note 2**
Die backgrind thickness	7.5 190.5	8 203.2	8.5 215.9	mil μm	Sawed 8” wafer on frame (option = WF) **(Note 3)**
	10 254	11 279.4	12 304.8	mil μm	• Bumped, sawed 8” wafer on frame (option = WFB) • Unsawed wafer (option = W) • Unsawed 8” bumped wafer (option = WB), **(Note 3)**
Die passivation thickness (multilayer)	—	1.3	—	μm	**Note 4**
Die Size: Die size X*Y before saw (step size) Die size X*Y after saw	 — —	 1904 x 2340.8 1840.5 x 2277.3	 — —	 μm μm	 — —

Note 1: The bond pad size is that of the passivation opening. The metal overlaps the bond pad passivation by at least 0.1 mil.

2: Metal Pad Composition is 98.5% Aluminum with 1% Si and 0.5% Cu.

3: As the die thickness decreases, susceptibility to cracking increases. It is recommended that the die be as thick as the application will allow.

4: The Die Passivation Thickness (1.3 μm) can vary by device depending on the mask set used. The passivation is formed by:

- Layer 1: Oxide (undoped oxide)
- Layer 2: PSG (doped oxide)
- Layer 3: Oxynitride (top layer)

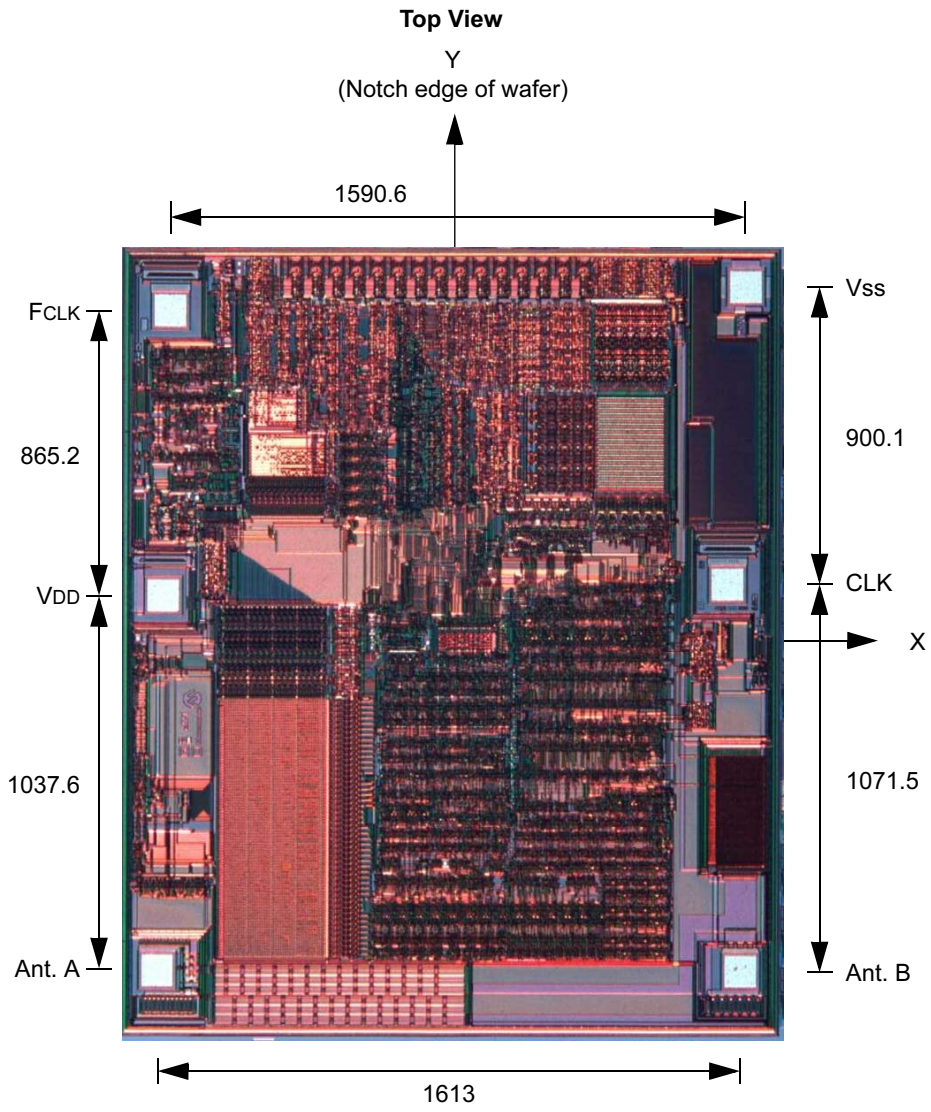
5: The conversion rate is 25.4 μm/mil.

Notice: Extreme care is urged in the handling and assembly of die products since they are susceptible to mechanical and electrostatic damage.

TABLE 2-6: WAFER MECHANICAL SPECIFICATIONS

Specifications	Min	Typ	Max	Unit	Comments
Wafer Diameter	—	8	—	inch	
Die separation line width	—	80	—	μm	
Dice per wafer	—	6,600	—	die	
Batch size	—	24	—	wafer	

FIGURE 2-1: MCRF450/451/452/455 DIE LAYOUT



Note: Coordinate units are in μm.
See Table 2-5 for die mechanical dimensions.

Die size before saw:
1904.0 μm x 2340.8 μm
1.904 mm x 2.3408 mm
74.96 mil x 92.16 mil

Die size after saw:
1840.5 μm x 2277.3 μm
1.8405 mm x 2.2773 mm
72.46 mil x 89.66 mil

Bond pad size:
89 μm x 89 μm
0.089 mm x 0.089 mm
3.5 mil x 3.5 mil

Bumped die:

Bumped Pad: Four corner pads (FCLK, VSS, Antenna B, Antenna A)

Bumping Material: 99.6% Gold

Bump Height: 25 μm ±3 μm

Bump Size: 103 μm x 103 μm (Covered all passivation opening of bond pad)

Other area except the four bumped pads: Covered by Polyamide

Thickness of Polyamide: 3 μm

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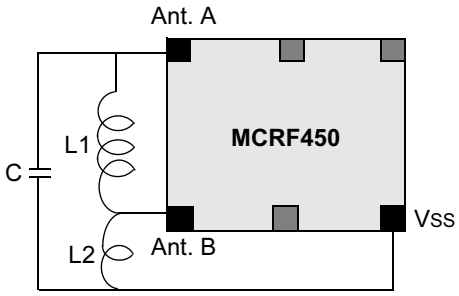
TABLE 2-7: PAD FUNCTION TABLE

Name	Function
Ant. Pad A	Connected to antenna coil L1.
Ant. Pad B	Connected to antenna coils L1 and L2 for MCRF450/451/455, NC for MCRF452.
VSS	Connected to antenna coil L2. Device ground during Test mode. (VSS = substrate)
FCLK	For device test only. Leave floating or connect to VSS in applications.
CLK	
VDD	For device test only. Leave floating in applications.

Note: NC = Not Connected.

FIGURE 2-2: EXTERNAL CIRCUIT CONFIGURATION FOR MCRF450

(a) Two inductors and one capacitor



L1 > L2 **Note:** Substrate = VSS

$$f_{tuned} = \frac{1}{2\pi\sqrt{L_T C}} \qquad f_{detuned} = \frac{1}{2\pi\sqrt{L_1 C}}$$

L_T = Total antenna inductance between Ant. A and VSS

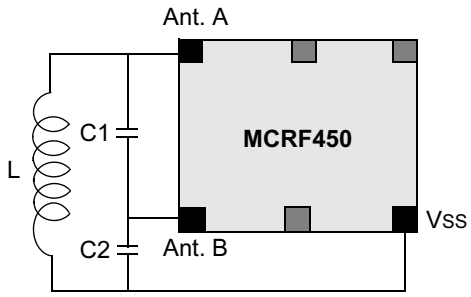
$$L_T = L_1 + L_2 + 2L_M$$

Where: L_M = mutual inductance of L1 and L2

$$L_M = K\sqrt{L_1 L_2}$$

K = coupling coefficient of two inductors ($0 \le K \le 1$)

(b) One inductor and two capacitors



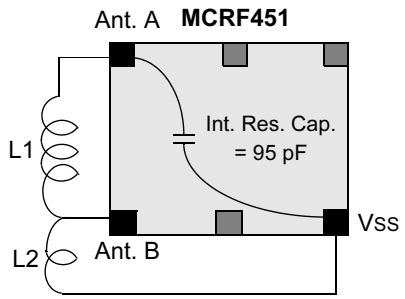
C1 ≥ C2 **Note:** Substrate = VSS

$$f_{tuned} = \frac{1}{2\pi\sqrt{L_T C_T}} \qquad f_{detuned} = \frac{1}{2\pi\sqrt{L C_1}}$$

$$C_T = \frac{C_1 C_2}{C_1 + C_2}$$

Note: Input parasitic capacitance between Antenna A and VSS pads = 3.5 pF. See application notes, AN710 and AN830 for antenna circuit design.

FIGURE 2-3: EXTERNAL CIRCUIT CONFIGURATION FOR MCRF451



L1 > L2 **Note:** Substrate = VSS

Internal Resonant Capacitor (Cres_100) = 95 pF

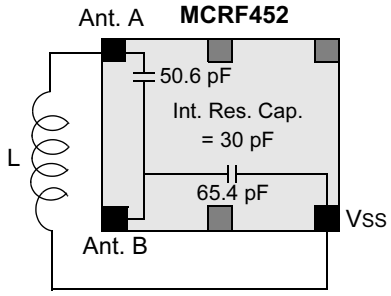
L1: External Antenna Coil A

L2: External Antenna Coil B

$$f_{tuned} = \frac{1}{2\pi\sqrt{(L_T)95\times10^{-12}}} \qquad f_{detuned} = \frac{1}{2\pi\sqrt{(L_1)95\times10^{-12}}}$$

L_T = Total antenna inductance between Ant. A and VSS

FIGURE 2-4: EXTERNAL CIRCUIT CONFIGURATION FOR MCRF452

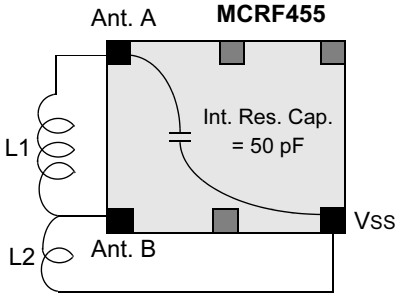


Note: Substrate = VSS

Internal Resonant Capacitor between Ant. A and VSS pads:
CRES_2_50 + parasitic capacitor = 30 pF

$$f_{tuned} = \frac{1}{2\pi\sqrt{(L)30\times10^{-12}}} \qquad f_{detuned} = \frac{1}{2\pi\sqrt{(L)50.6\times10^{-12}}}$$

FIGURE 2-5: EXTERNAL CIRCUIT CONFIGURATION FOR MCRF455



L1 > L2 **Note:** Substrate = VSS

L1: External Antenna Coil A

L2: External Antenna Coil B

Internal Resonant Capacitor (Cres_50) = 50 pF

$$f_{tuned} = \frac{1}{2\pi\sqrt{(L_T)50\times10^{-12}}} \qquad f_{detuned} = \frac{1}{2\pi\sqrt{(L_1)50\times10^{-12}}}$$

L_T = Total antenna inductance between Ant. A and VSS

Note: See application notes AN710 and AN830 for antenna circuit design of Figure 2-2 through Figure 2-5.

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TABLE 2-8: INTERNAL RESONANT CAPACITANCE AND ANTENNA INDUCTANCE REQUIREMENTS

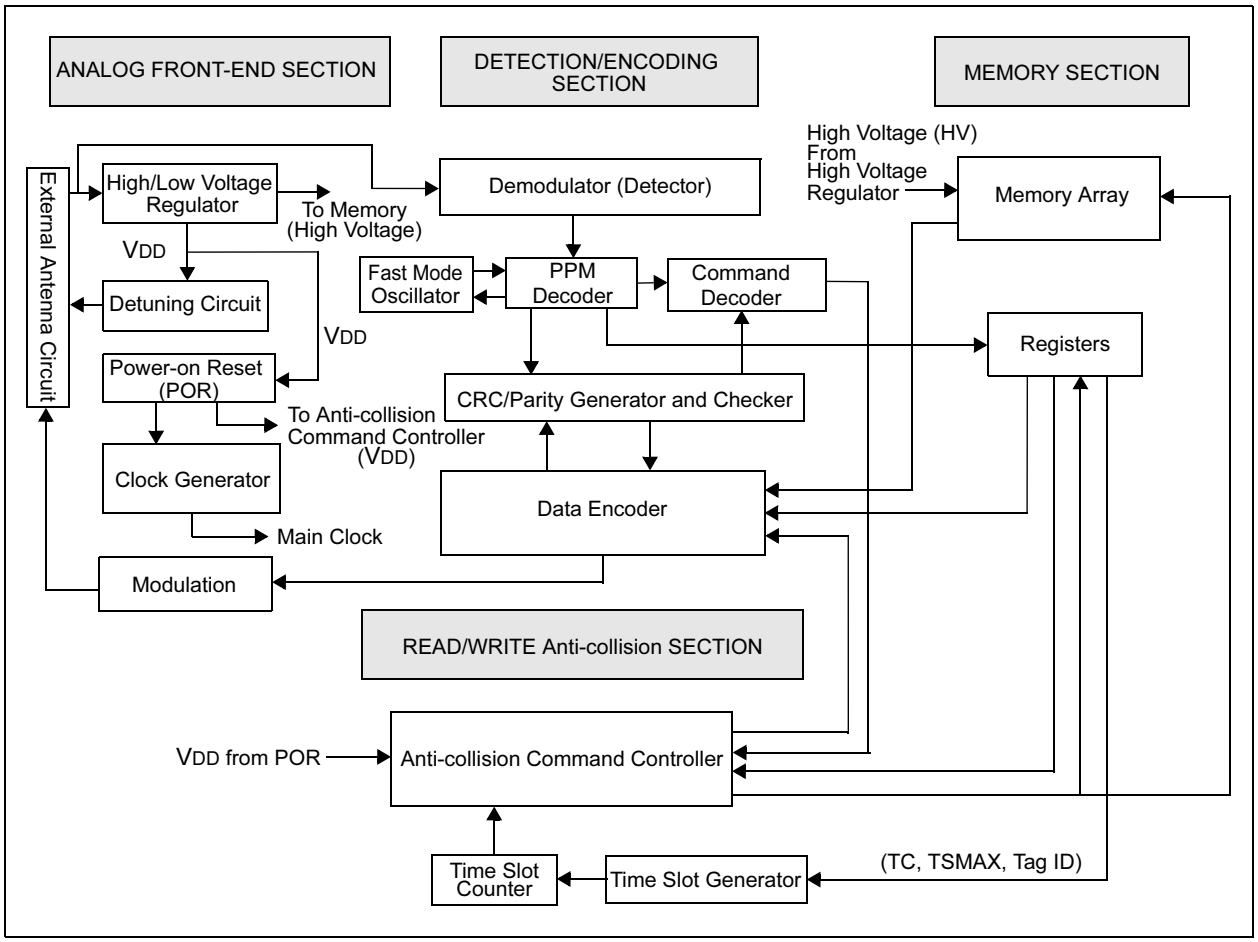
Device Name	Resonant Capacitance (Antenna A to Vss)	External Inductance Requirement between Antenna A and Vss for 13.56 MHz tag	Connection to External Antenna Circuit	Reference
MCRF451	95 pF ±10%	1.45 μH ±10%	Antenna A, B, and Vss pads	This device requires three connections to an external circuit. Good for direct die attachment onto antenna.
MCRF452	30 pF ±10%	4.591 μH ±10%	Antenna A and Vss pads	This device requires only two antenna connections. Good for both direct die attachment and COB.
MCRF455	50 pF ±10%	2.76 μH ±10%	Antenna A, B, and Vss pads	This device requires three connections to an external circuit. Good for direct die attachment onto antenna.

Note: The internal capacitance value for bumped die is about 1 pF higher than the unbumped die's capacitor.

3.0 BLOCK DIAGRAM

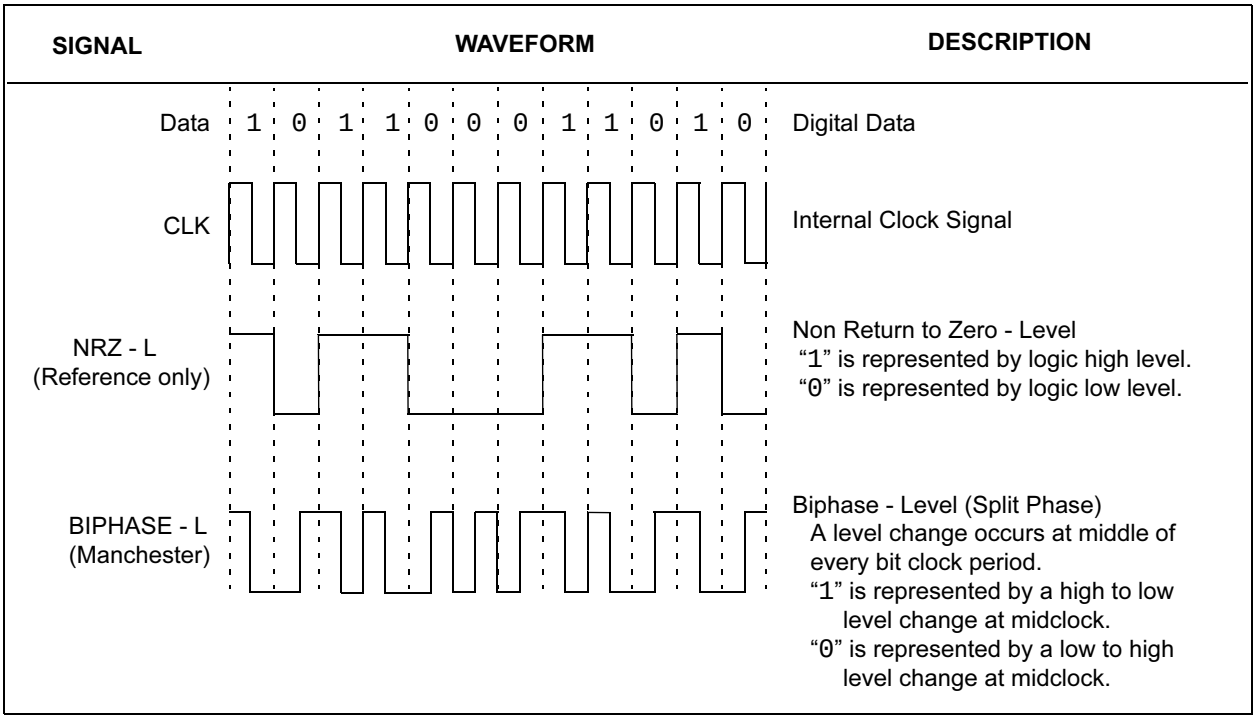
The device contains four major sections. They are: Analog Front-End, Detection/Encoding, Read/Write Anti-collision Logic and Memory sections. Figure 3-1 shows the block diagram of the device.

FIGURE 3-1: BLOCK DIAGRAM



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FIGURE 3-2: DATA WAVEFORM OF DEVICE



4.0 ANALOG FRONT-END

This section includes high and low voltage regulators, Power-on Reset, 70 kHz clock generator and modulation circuits.

4.1 High and Low Voltage Regulator

The high voltage circuit generates the programming voltage for the memory section. The low voltage circuit generates DC voltage (V_{DD}) to operate the device.

4.2 Power-On Reset (POR)

This circuit generates a Power-on Reset (POR) voltage. The POR releases when sufficient power has been developed by the voltage regulator to allow for correct operation.

4.3 Clock Generator

This circuit generates a clock (CLK). The main clock is generated by an on-board 70 kHz time base oscillator. This clock is used for all timing in the device, except for the Fast mode PPM decoding.

4.4 Data Modulation

The data modulation circuit consists of a modulation transistor and a LC resonant circuit. The resonant circuit must be tuned to the carrier frequency of the Interrogator (i.e., 13.56 MHz) for maximum performance.

The modulation transistor is placed between antenna B and V_{SS} pads. It is designed to result in the turn-on resistance of less than five ohms (R_M). This small turn-on resistance shorts the resonant circuit component between antenna B and V_{SS} pads as it turns on. This results in a change of the resonant frequency of the resonant circuit. Consequently, the resonant circuit becomes detuned with respect to the carrier frequency of the Interrogator. The voltage across the resonant circuit is minimized during this time. This condition is called “cloaking”.

The transistor, however, releases the resonant circuit as it turns off. Therefore, the resonant circuit tunes to the carrier frequency of the Interrogator again and develops maximum voltage. This condition is called “uncloaking”.

The device transmits data by cloaking and uncloaking, based on the on/off condition of the modulation transistor. Using the 70 kHz Manchester format, the data bit ‘0’ will be sent by cloaking and uncloaking the device for 7 μs each. Similarly, the data bit ‘1’ will be sent by uncloaking and cloaking the device for 7 μs each. See Figure 6-1 for the Manchester waveform.

4.5 Detuning Circuit

The purpose of this circuit is to prevent excessive RF voltage across the resonant circuit.

This circuit monitors V_{DD} and detunes the resonant circuit if the RF coil voltage exceeds the threshold limit (V_{DETUNE}), which is above the operating voltage of the device.

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5.0 DETECTION AND ENCODING

This section encodes data with the Manchester format and also detects commands from the Interrogator.

5.1 Demodulator (Detector)

This circuit demodulates the Interrogator commands and sends them to the PPM decoder.

5.2 Fast Mode Oscillator

This oscillator generates a clock frequency that is used for decoding Fast mode commands.

5.3 PPM Signal Decoder

This section decodes the PPM signals and sends the results to the command decoder and CRC/parity checker.

5.4 Command Decoder

This section decodes the Interrogator commands and sends the results to the Anti-collision/command controller.

5.5 CRC/Parity Generator and Checker

This section generates Cyclic Redundancy Code (CRC) and parity bits for transmitting and receiving data. The device utilizes a 16-bit CRC for error detection. Its polynomial and initial values are:

CRC Polynomial: $X^{16}+X^{12}+X^5+X^0$

Initial Value: $FFFF

This polynomial is also known as CRC CCITT (Consultative Committee for International Telegraph and Telephone). The Interrogator also uses the same CRC for data processing. The device uses the CRC in the following ways:

1. **CRC for blocks (except Blocks 0 and 2):** The Interrogator will send a Write command with CRC. When the device receives this command, it checks the CRC prior to any processing. If it is a correct CRC, the device programs the block data and also stores the CRC in the EEPROM. As soon as the data is written into memory, both the programmed data and Stored CRC (SCRC) are sent back to the Interrogator as verification. The device also sends the programmed data and SCRC when there is a response to the Read command.

   If the CRC is incorrect, the device ignores the incoming message (does not respond to the Interrogator) and waits for the next command with a correct CRC.

2. **CRC for Blocks 0 and 2:** When reading Block 0 or 2, a Calculated CRC (CCRC) is sent. This is because both the TF and FR bits in Block 0 are non write-protectable, while the rest of the bits in the block are write-protectable. This means the SCRC in the block no longer represents the CRC of the block data, if only the TF or the FR bit is reprogrammed. This is also true for Block 2, which is a write protection block. The write-protected bit cannot be reprogrammed once it has been written. Therefore, the SCRC in Blocks 0 and 2 are not used. Instead, the device calculates the current CRC of the block and sends it to the Interrogator.
3. **CRC for FRR response:** For the Fast Read (FR) response (this is the device response to an FRR command), the CCRC of the tag ID and FRF (Blocks 3-5) data is sent. The data length of the FRF is determined by DF bits (see Table 7-6).

5.6 Data Encoder

This section multiplexes serial data, encodes it into Manchester format and sends it to the modulation circuit. See Figure 3-2 for the Manchester waveform.

6.0 READ/WRITE ANTI-COLLISION LOGIC

This section includes the anti-collision algorithm of the device and consists of the Anti-collision/command controller, the time slot generator and the time slot counter.

6.1 Description of Algorithm

The read/write anti-collision algorithm is based on time division multiplexing of tag responses. Each device is allowed to communicate with the Interrogator in its time slot only. When not in its assigned time slot, the device remains in a nonmodulating condition. This enables the Interrogator to communicate with other devices in the same Interrogator field with fewer chances of data collision.

Figure 6-1 shows the anti-collision algorithm flowchart, which consists of four control loops. They are: Detection, Processing, Sleeping and Reactivation loops. All devices in the Interrogator's RF field are controlled by five different commands and internal control flags.

The Interrogator commands are:

1. **Fast Read Request (FRR):** If the TF bit (bit 30 or Block 0) is cleared, the device responds only to the FRR command. The FRR command consists of five specially timed gap pulses (refer to Figures 6-3 to 6-7). The position of the five gap pulses in the given time span (1.575 ms) determines the parameters of the command. The command has three parameters: TCMAX, TSMAX and Data transmission speed. The details of these parameters will be discussed in the following sections. If the device receives the FRR command, it sends the FR response and then listens for 1 ms (T_{LW}) for a matching code from the Interrogator.
2. **Fast Read Bypass (FRB):** This command is used in the Reactivation loop and is only applicable to a device with the FR bit (bit 31 in Block 0) cleared. The device responds with 64 bits of data, which includes Block 1 data (32-bit Tag ID), and then listens for 1 ms (T_{LW}) for a matching code from the Interrogator. The command structure is the same as the FRR command: five specially timed gap pulses (1.575 ms). The command parameter (Figure 6-8) determines the data rate (normal speed or fast speed) of subsequent Interrogator commands.
3. **Matching Code 1 (MC1):** This command consists of time calibration pulses (TCP) followed by 1-of-16 PPM signals. It is used when the device does not need any further processing. This MC1 command causes a device, which is in the detection loop, to enter the sleeping loop.
4. **Matching Code 2 (MC2)**: The command structure is the same as MC1: TCP followed by 1-of-16 PPM signals. The command is used when the device needs further processing (read/write). The device enters the processing loop if it receives this command in the detection loop.

   The MC1 and MC2 matching code command consists of 12 bits or 3 symbols. The first 8 bits, or the first two symbols, are selected from the 32-bit Tag ID. The next 4 bits, or the 3rd symbol, determine the matching code type (3 bits) and a parity bit (see **Section 6.2.3.6 "Calculation Of Matching Code"**). The command lasts for about 11.2 ms, including the TCP.
5. **End Process (EP):** This command consists of the time reference pulses followed by 1-of-16 PPM signals. The EP command causes a device to exit the processing loop and enter the sleeping loop.

6.1.1 DETECTION LOOP

If the FR bit (bit 31 of Block 0) is set, the device can enter this loop in two ways, depending on the condition of the TF bit (bit 30 of Block 0). They are:

1. When the TF bit is cleared, the device enters this loop and waits for a FRR command. This is called the "Interrogator-Talks-First" (ITF) mode.
2. When the TF bit is set, the device enters this loop by transmitting the FR response without waiting for an FRR command. This is called the "Tag-Talks-First" (TTF) mode.

For case 1 above, the parameters of the FRR are:

- Maximum number of time slots (TSMAX = 1, 16, or 64),
- Maximum transmission counter (TCMAX = 1, 2, or 4),
- Data transmission speed (Normal or Fast mode).

The purpose of the TSMAX and TCMAX parameters is to acknowledge the device in the detection loop as fast as possible. TSMAX represents the maximum number of time slots between the end of the FRR command and the beginning of the FR response. One time slot (T_{SLOT}) represents 2.5 ms. For example, TSMAX = 64 represents a maximum time delay of 160 ms before sending the FR response. See **Section 6.3 "Time Slot Generator"** for the calculation of actual time delay. TCMAX represents the maximum number of FR responses a device can send after an FRR command. For example, TCMAX = 4 means the device can send its FR response four times (after the FRR command) for acknowledgment (matching code).

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The TSMAX and TCMAX values are determined by the Interrogator's decision on how many tags are in the field. The Interrogator may assign TSMAX = 1 and TCMAX = 1, assuming there is only one tag in the field. The efficiency of the detection will increase in multiple tag environments by assigning a higher number to both the TSMAX and TCMAX. If the device receives the FRR, it clears the Position 1 flag, waits for its time slot, replies with the FR response and then listens for 1 ms. The FR response consists of a maximum of 160 Manchester data bits (default: 96 bits), which includes the 32-bit Tag ID and the FRF data (Blocks 3-5) (see Table 6-3 and Example 9-1).

To acknowledge the FR response, the Interrogator can start to send a matching code (MC) during the device's 1 ms listening window (T_{LW}). The MC is encoded with 1-of-16 PPM signal (see Figure 6-9). The MC1 is given to the device if the device does not need any further processing. If the device receives the MC1, it enters the sleeping loop and stays in the loop in a nonmodulating condition. The MC2 command is given to the device if further processing (read/write) is required. If the device receives the MC2 command, it enters the processing loop.

If the device misses the MC within the listening window, it sends the FR response again after its time slot when two conditions are met: (1) Position 1 flag is cleared and, (2) TCMAX has not elapsed. The device checks the condition (elapsed or not elapsed) of TCMAX using an internal transmission counter (TC). The TC consists of 3 bits. If the Position 1 flag is cleared, the device increments the TC by 1 each time it does not receive a MC during its listening window. See Figure 6-1 for a flow chart showing the conditional incrementing of the transmission counter. Table 6-1 shows an example of detecting the elapsed TCMAX using a rolling modulo-8 transmission counter.

For the TTF case, the device repeats its FR response (as long as it is energized) according to the TCMAX and TSMAX parameters, as specified in Table 7-5. Even though the device is operating in the TTF mode, it will respond to its correct MC during its listening window. If TCMAX = 1, 2 or 4, it will also respond to FRR commands, just as in the ITF case (see **Section 6.1.1.1 "Matching Code Queuing"**).

6.1.1.1 Matching Code Queuing

Once the device receives the FRR command, it sends the FR response and waits for a matching code (MC) during its listening window. If the device does not receive its correct MC code before its TCMAX has elapsed (see Table 6-1), it goes back to the beginning of the detection loop (position 1 in the loop) and waits for either a new FRR command or for the MC1 or MC2 matching code. This is called "matching code queuing". In this queuing, the device stays in the detection loop waiting for an Interrogator command (FRR or MC). This queuing takes place within the detection loop and is controlled by the conditions of "Set Position 1 Flag" and TCMAX.

This queuing allows the Interrogator to communicate with a device outside its listening window. The result is enhanced and accelerated processing of individual devices in a multiple tag environment.

TABLE 6-1: CONDITIONS FOR TCMAX = ELAPSED FOR ITF MODE

Rolling Modulo -8 TC			TCMAX = 1	TCMAX = 2	TCMAX = 4
0	0	1	elapsed	—	—
0	1	0	elapsed	elapsed	—
0	1	1	elapsed	—	—
1	0	0	elapsed	elapsed	elapsed
1	0	1	elapsed	—	—
1	1	0	elapsed	elapsed	—
1	1	1	elapsed	—	elapsed
0	0	0	elapsed	elapsed	—

6.1.2 PROCESSING LOOP

The reading and writing processes take place in this loop. Devices in this loop are waiting for commands for processing. In order to read from, or write to, the device, its "Processing Flag" (PF) must be set. Any device entering this loop with its PF cleared is called a "follow-along" tag. This follow-along tag in the loop is not processed for reading or writing.

If the device with the PF flag set receives the EP command, it exits this loop and enters the sleeping loop. However, the same EP command sends the follow-along tag back to the detection loop.

If the device receives the FRR or FRB command in this loop, it sees the command as invalid, resets itself and goes back to the initial power-up state.

6.1.3 SLEEPING LOOP

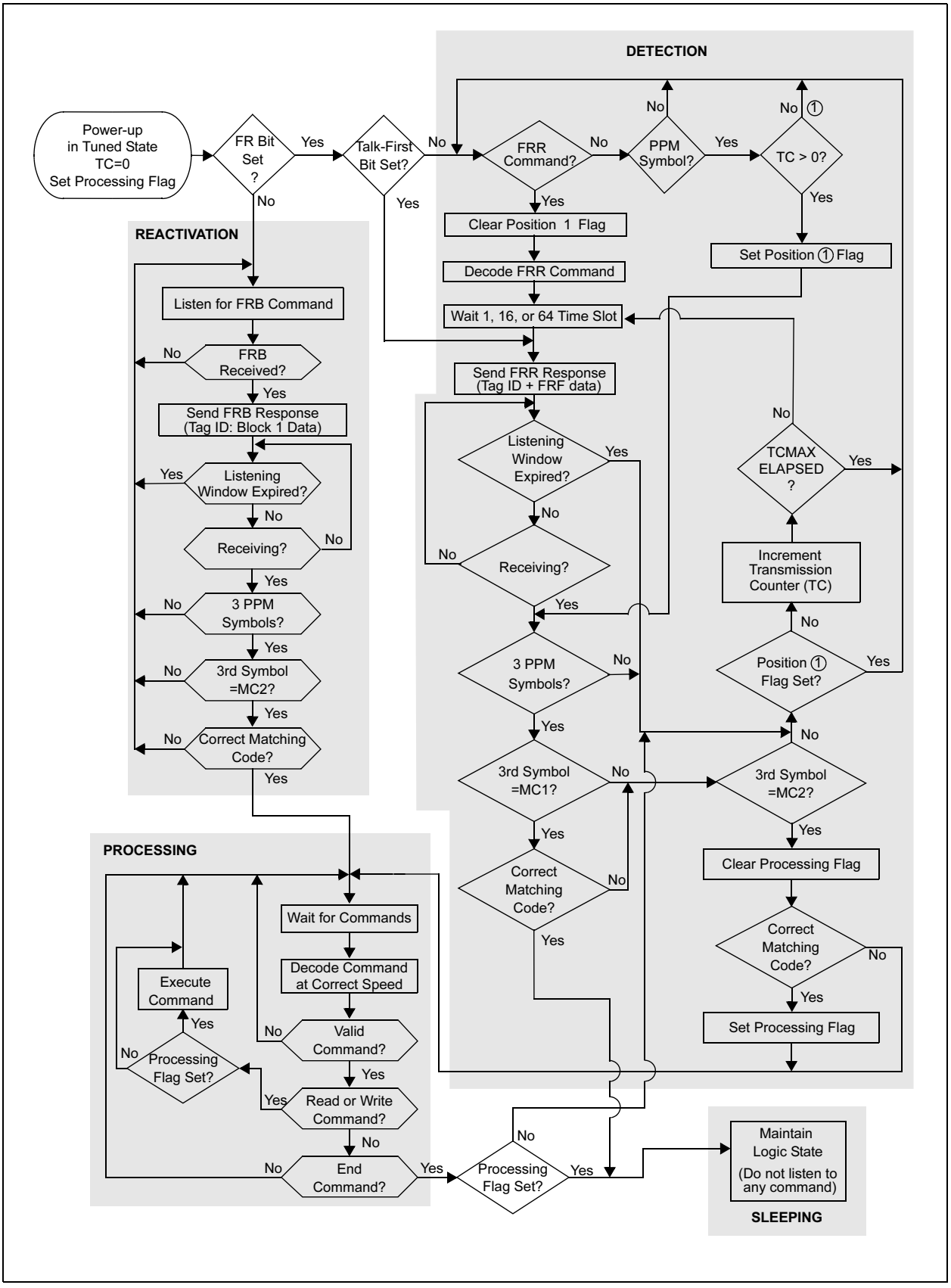
The sleeping loop is used to keep all processed devices in a "silent" condition. The devices stay in this loop in a nonmodulating condition as long as they remain in the field.

6.1.4 REACTIVATION LOOP

The reactivation loop is used to process a device with its FR bit cleared. A device in this loop waits for the FRB command. If a device receives the FRB command, it transmits the contents of Block 1 (Tag ID) to its memory and waits for a MC2 in its listening window. If the device receives the MC2, it leaves this loop and enters the processing loop. This reactivation loop has no anti-collision capability. It is designed for reactivation of single devices. This loop can be effectively used in retail store applications to process returning items from customers.

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FIGURE 6-1: ANTI-COLLISION FLOW CHART



6.2 Anti-collision Command Controller

This section discusses the anti-collision algorithm and describes the communications between the Interrogator and device.

6.2.1 STRUCTURE OF READ/ WRITE COMMAND SIGNALS

The Interrogator's Read/Write commands have the following structure:

Read/Write command = Command + Address + Data + Parity (or CRC)

The commands are summarized in the table below:

TABLE 6-2: READ/WRITE COMMANDS FROM INTERROGATOR TO DEVICE

Interrogator Command	Command Code	Address	Data	Parity or CRC	Symbol Length
Unused	0xx	xxxxx	—	—	—
Read 32-bit block	110	aaaaa	—	Parity	3 symbols
Unused	111	00xxx	—	—	—
Unused	111	0100x	—	—	—
End Process	111	01010	—	Parity	3 symbols
Unused	111	01011	—	—	—
Unused	111	011xx	—	—	—
Unused	111	1000x	—	—	—
Set Talk First Bit	111	10010	—	Parity	3 symbols
Set FR Bit	111	10011	—	Parity	3 symbols
Clear Talk First Bit	111	10100	—	Parity	3 symbols
Clear FR Bit	111	10101	—	Parity	3 symbols
Unused	111	1011x	—	—	—
Unused	111	11xxx	—	—	—
Unused	100	xxxxx	—	—	—
Write 32-bit block	101	aaaaa	32 bits	CRC-16	14 symbols

Legend: aaaaa = Block address
x = don't care

Note:

- Command and address are sent MSN (Most Significant nibble) first.
- Data and parity/CRC are sent LSN (Least Significant nibble) first.
- Calculation of Parity and CRC includes Command code, Address, and Data.
- See Microchip Application Note AN752 (DS00752) for the CRC-16 calculation algorithm.

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6.2.2 STRUCTURE OF DEVICE RESPONSE

When the device receives the Interrogator command, it responds with 70 kHz Manchester encoded data having the following structures:

Device Response to FRR Command: Preamble (8 bits) + TC (3 bits) + TP (4 bits) + '0' + 32 bits of Tag ID (Block 1 data) + FRF data (32 - 96 bits) + Calculated CRC (SCRC, 16 bits) of Tag ID and FRF data = 96 - 160 bits depending on FRF data length.

Note: The preamble + TC + TP + '0' are not included for the CRC calculation.

Device Response to FRB Command: Preamble (8 bits) + '00001' + '000' + 32 bits of Tag ID (Block 1 data) + Stored CRC (SCRC, 16 bits) of Block 1 = 64 bits.

Device Response of Interrogator's Read command for Blocks 0 and 2:

Preamble (8 bits) + Block Number (5 bits) + '000' + Block Data (32 bits) + Calculated 16 bit CRC (CCRC).

Note: The CCRC is calculated by using block number and block data only. Preamble and '000' are not included in the CRC calculation.

Device Response of Interrogator's Read Command for all other blocks:

Device Response = Preamble (8 bits) + Block Number (5 bits) + '000' + Block Data (32 bits) + Stored CRC (SCRC, 16 bits) in the same block.

TABLE 6-3: INTERROGATOR COMMANDS AND DEVICE RESPONSES

Interrogator Command	Delay	Device Response
Read Block 0 and Block 2 data	TDECODE	Preamble, block #, '000', block data, CCRC
Read block data except for Block 0 and Block 2	TDECODE	Preamble, block #, '000', block data, SCRC
Write block data	TWRITE	For Blocks 0 and 2: Preamble, block #, '000', block data, CCRC For all others: Preamble, block #, '000', block data, SCRC
Set Fast Read (FR) bit	TWRITE	Preamble, 1 byte '0's, Block 0 data, CCRC
Clear Fast Read (FR) bit	TWRITE	Preamble, 1 byte '0's, Block 0 data, CCRC
Set Talk First (TF) bit	TWRITE	Preamble, 1 byte '0's, Block 0 data, CCRC
Clear Talk First (TF) bit	TWRITE	Preamble, 1 byte '0's, Block 0 data, CCRC
End Process (EP)	TDECODE	Preamble
FRR	f(TSMAX, TCMAX, 8-bit Tag ID)	Preamble,TC, TP, '0', Tag ID, FRF, FRR_CCRC
FRB	TDECODE	Preamble, address of block #1 ('00001'), '000', Tag ID (32 bits), SCRC of Block 1

References used in this table are as follows:

Preamble = 11111110 (8 bits).'0' is transmitted last.

Block # = 5 bit addressed block, transmits Least Significant bit (LSb) first.

Block data = 32-bit data of the addressed block, transmits LSb first.

CCRC = Calculated CRC of the preceding block number and block data. Transmits LSb first.

SCRC = Stored CRC. This SCRC is the CRC of the Write command, address, and data from the Interrogator, LSb first. The device stores the received CRC for each block. See **Section 7.2 "Stored CRC (SCRC) Memory Section"** for details.

FRR_CRC = Calculated CRC of 32-bit Tag ID and fast read field (FRF) data.

TP = Tag parameters (4 bits: '0', DF0, DF1, parity). where DF0 and DF1 determine the FR field length (see Table 7-6).

TC = Transmission counter (3 bits), transmits LSb first.

Parity = Even parity bit of TC and TP.

Tag ID = 32 bits of unique identification code of the device, transmits LSb first. This Tag ID is preprogrammed in the factory prior to shipping.

8-bit Tag ID = 8 bits of Tag ID selected from the 32 bits of the unique tag identification code. Transmits LSb first (see **Section 6.2.3.6 "Calculation Of Matching Code"** for selecting the 8 bits from the Tag ID).

FRF = Fast Read Field (Blocks 3-5), transmits LSb first (see **Section 7.0 "Memory Section"**).

f(TSMAX, TCMAX, 8-bit Tag ID = Delay is a function of the TSMAX, TCMAX and 8-bit Tag ID.

TWRITE = Writing time for EEPROM (see Table 2-3).

TDECODE = Time requirement for command decoding (see Table 2-3).

Examples are given in **Section 9.0 "Examples"**.

6.2.3 DETECTION OF INTERROGATOR COMMANDS

The Interrogator sends commands to the device by amplitude modulating the carrier signal (gap pulse). The Interrogator uses two classes of encoding signals for modulation. They are (1) 1-of-16 PPM for data transmission, and (2) specially timed gap pulse sequence for the FRR and FRB commands. These commands consist of five gap pulses within nine possible gap pulse positions (1.575 ms). The combination of the possible gap positions determines the command type and parameters of the Fast Read command.

The Interrogator also sends TCP prior to the 1-of-16 PPM. The TCP is used to calibrate the time-base of the decoder in the device. The specifics of the two encoding methods and the TCP are described in the following sections.

6.2.3.1 Fast Read (FR) Commands

The FR commands are composed of five 175 μs wide gap pulses (see Figure 6-2) whose spacing within 1.575 ms determines the command type and its parameters. Table 6-4 shows the specification of the gap signal for the FR commands. Two commands are used for the fast read. They are: (1) Fast Read Request (FRR) in the Detection loop, and (2) Fast Read Bypass (FRB) in the Reactivation loop. See Tables 6-5 and 6-6 for the FRR gap pulse positions. See Figures 6-3 to 6-8 for the gap modulation patterns.

The parameters of FRR are: (1) number of time slots (TSMAX = 1,16, or 64), (2) maximum transmission counter (TCMAX) and (3) data transmission speed. The FRB has only a data transmission speed parameter (Normal or Fast Speed mode). The device extracts these parameters based on the positions of the five gap pulses within the 1.575 ms time span, as shown in Figures 6-3 to 6-8.

TSMAX = 1 is given if there is only one device in the field. This is called “Conveyor mode” or “single tag environment”. In this mode, the device responds with the FR response signal in every time slot until it receives a correct matching code, or until TCMAX is elapsed.

6.2.3.2 Data Transmission Speed

The Interrogator can send data with two different data rates: (1) Normal and (2) Fast Speed modes. The normal speed uses 2.8 ms/symbol, while the fast speed uses 160 μs/symbol. One symbol represents one 4-bit data packet (see **Section 6.2.3.4 “1-of-16 PPM”**). The data transmission speed is a parameter of the FRR and FRB commands. This parameter indicates the data speed of subsequent Interrogator commands. The data rate of the device output (70 kHz) is not affected by this parameter.

TABLE 6-4: SPECIFICATION OF GAP SIGNAL FOR FRR AND FRB COMMANDS

Number of gaps for one command	5
Total available number of gap positions within the command time span	9
Command time span	1.575 ms
Gap pulse width	175 μs

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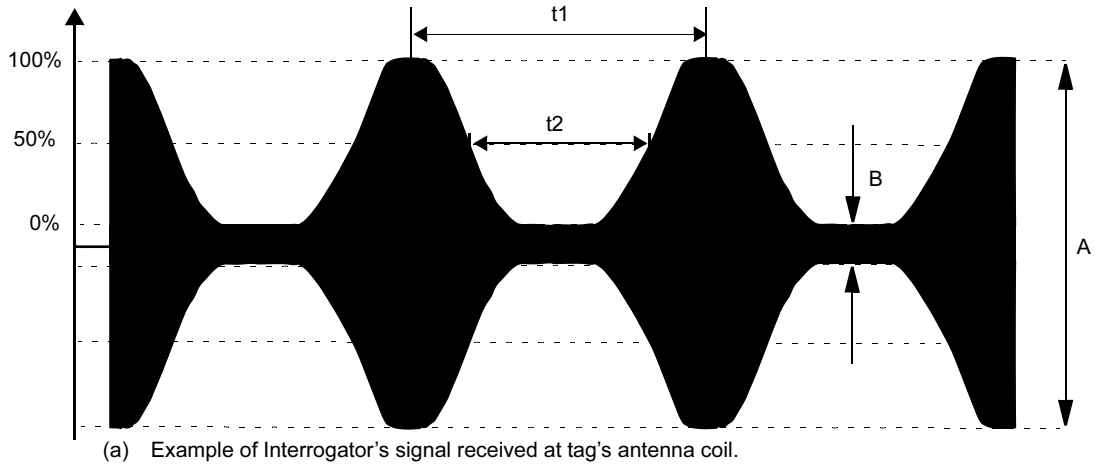
TABLE 6-5: SPECIFICATION OF MODULATION SEQUENCE FOR FRR COMMAND

Maximum Time Slot (TSMAX)	TCMAX	Gap Pulse Position	Data Transmission Mode
1	1	1, 2, 3, 4, 6	Normal Speed
		1, 3, 5, 6, 8	Fast Speed
	2	1, 2, 3, 4, 5	Normal Speed
		1, 3, 5, 6, 7	Fast Speed
	4	1, 2, 3, 5, 6	Normal Speed
		1, 3, 5, 7, 8	Fast Speed
16	1	1, 2, 4, 6, 8	Normal Speed
		1, 3, 4, 6, 8	Fast Speed
	2	1, 2, 4, 6, 7	Normal Speed
		1, 3, 4, 6, 7	Fast Speed
	4	1, 2, 4, 5, 6	Normal Speed
		1, 3, 4, 5, 6	Fast Speed
64	1	1, 2, 4, 5, 7	Normal Speed
		1, 3, 4, 5, 7	Fast Speed

TABLE 6-6: SPECIFICATION OF MODULATION SEQUENCE FOR FRB COMMAND

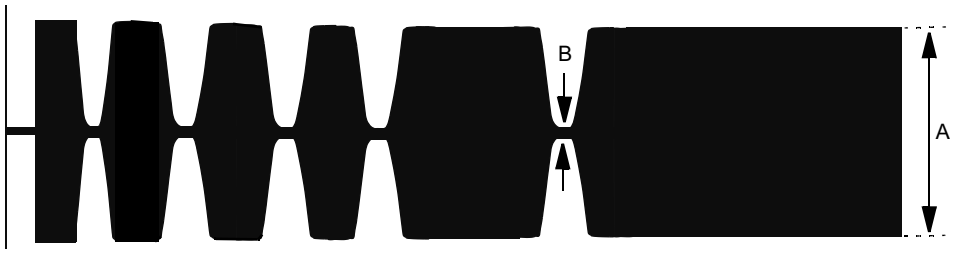
Symbol	Gap Pulse Position	Data Transmission Mode
FRB_N	1, 2, 3, 5, 7	Normal Speed
FRB_F	1, 3, 5, 7, 9	Fast Speed

FIGURE 6-2: PULSE WAVEFORM OF GAP AND 1-OF-16 PPM SIGNALS

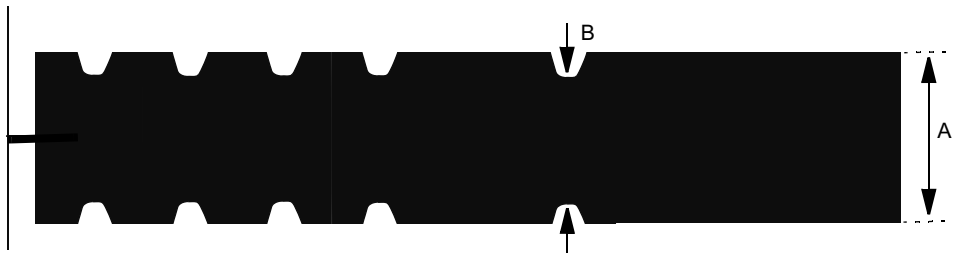


(a) Example of Interrogator's signal received at tag's antenna coil.
See Table 6-7 for the specifications of t1, t2, and modulation depth (modulation index).
The Modulation Index is defined as:

$$\text{Modulation Index} = \frac{A-B}{A+B} \times 100\%$$



(b) FRR command waveform for Figure 6-3 (A) with near 100% Modulation Index



(c) FRR command waveform for Figure 6-3 (A) with near 20% Modulation Index

TABLE 6-7: WAVEFORM CHARACTERISTICS OF GAP AND 1-0F-16 PPM SIGNALS

Signal	Symbol	Min	Typ	Max	Unit	Conditions
Gap signal and 1-of-16 PPM for Normal mode	t1	145	175	205	µs	PW$_{PPM_N}$
	t2	20	100	150	µs	Measured at 50%, See Figure 6-2 GAP$_{WIDTH_N}$
	MOD$_{INDEX_GAP}$	20	60	100	%	See Figure 6-2
1-of-16 PPM for Fast mode	t1	8.3	10	11.7	µs	PW$_{PPM_F}$
	t2	6.0	7.0	8.0	µs	Measured at 50%, See Figure 6-2 GAP$_{WIDTH_F}$
	MOD$_{INDEX_GAP}$	20	60	100	%	See Figure 6-2

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The following figures show the various modulation patterns of the Fast Read commands (FRR and FRB). Each command consists of a combination of five gap pulses within nine possible gap positions. The pulse width of each gap is 175 μs and the total time span of each command for the nine possible positions is 1.575 ms (175 μs x 9 = 1.575 ms).

In the figures, P*mn* represents *m*th gap pulse at *n*th gap position in the given data packet (symbol).

FIGURE 6-3: GAP MODULATION PATTERNS FOR FRR, NORMAL SPEED, TSMAX = 1

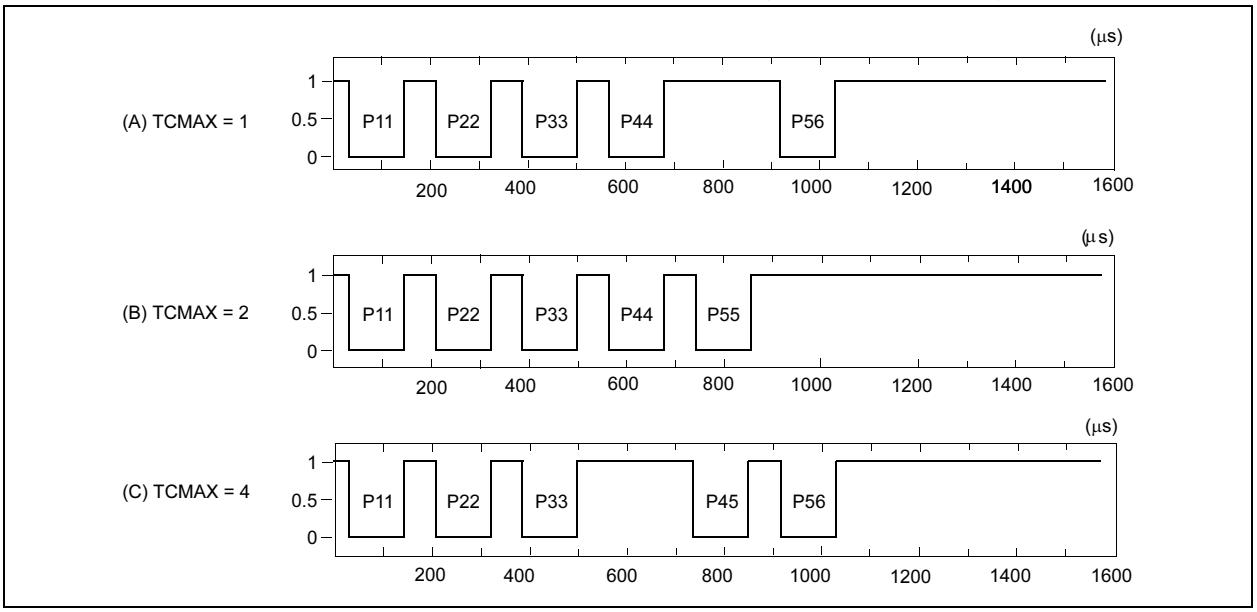


FIGURE 6-4: GAP MODULATION PATTERNS FOR FRR, FAST SPEED, TSMAX = 1

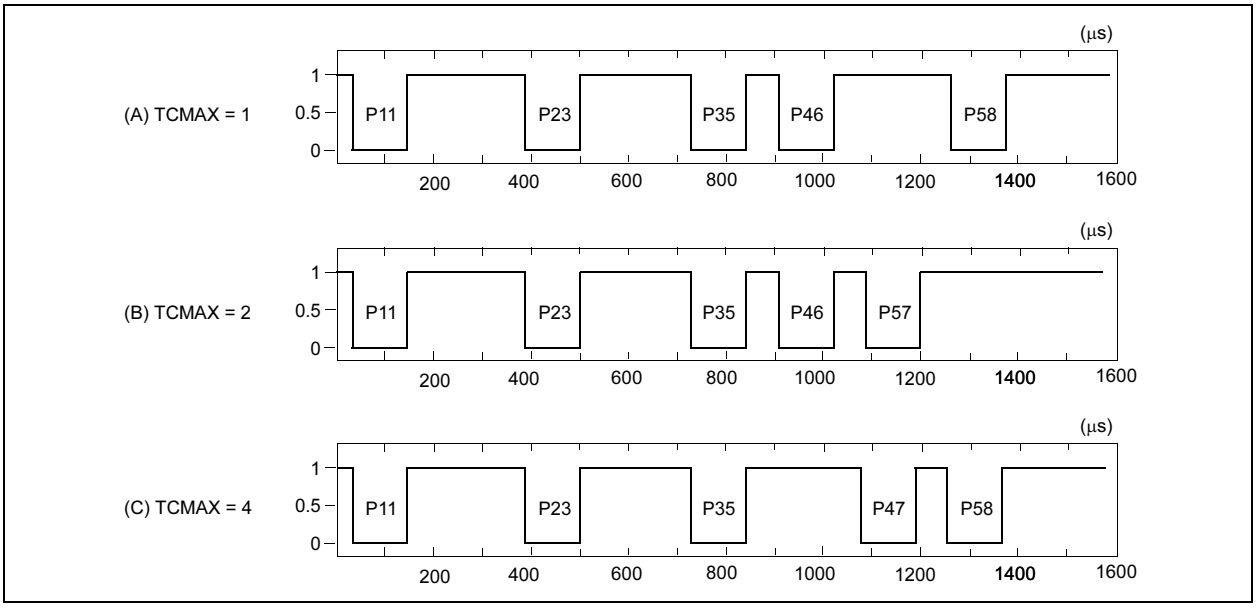


FIGURE 6-5: GAP MODULATION PATTERNS FOR FRR, NORMAL SPEED, TSMAX = 16

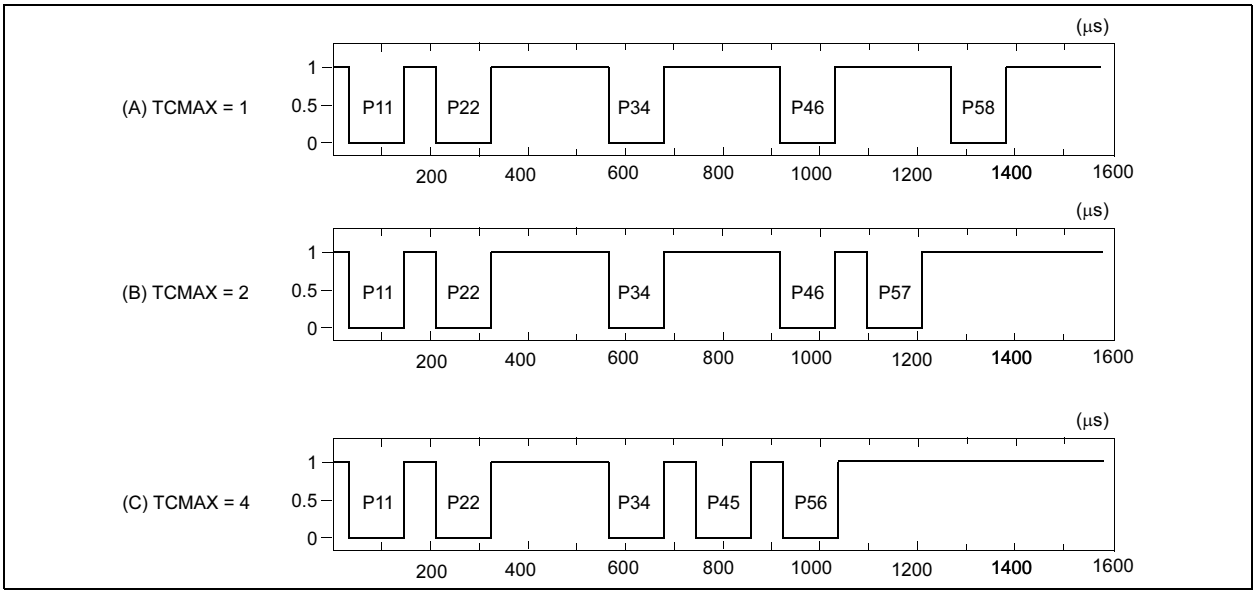


FIGURE 6-6: GAP MODULATION PATTERNS FOR FRR, FAST SPEED, TSMAX = 16

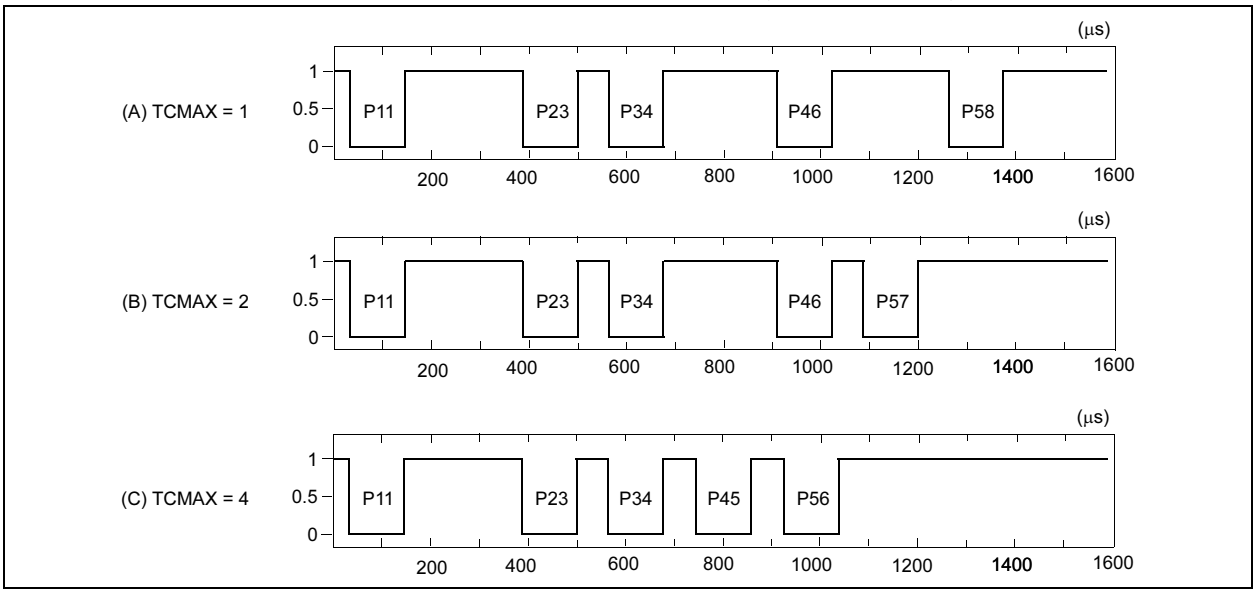
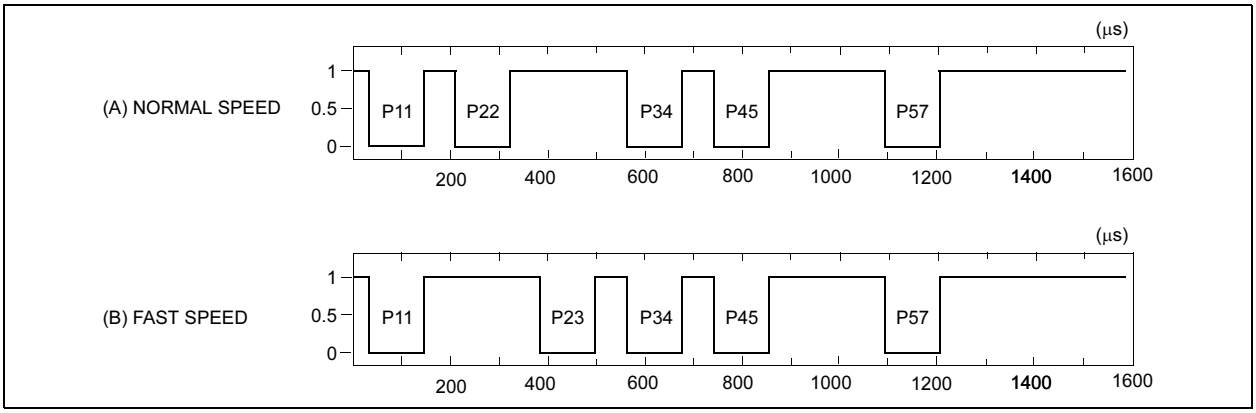
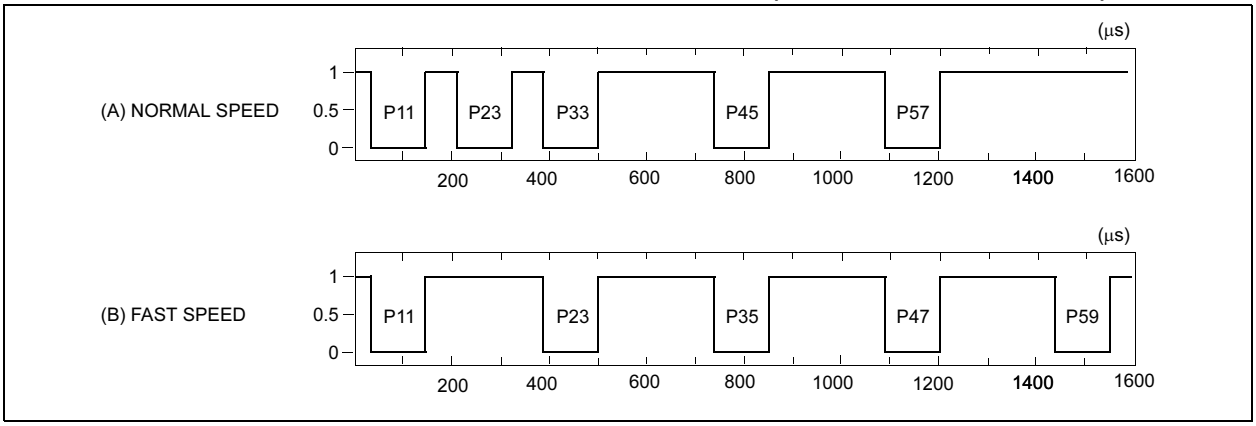


FIGURE 6-7: GAP MODULATION PATTERNS FOR FRR, TSMAX = 64, TCMAX = 1



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FIGURE 6-8: GAP MODULATION PATTERNS FOR FRB (FAST REQUEST BYPASS)



6.2.3.3 Usage Of TSMAX And TCMAX

The parameters of TSMAX and TCMAX are determined by an expected number of tags in the Detection Loop. The following table shows the recommended FRR command repeat times for each of the 7 possible combinations of TSMAX and TCMAX. The command repeat time in Table 6-8 is calculated by:

EQUATION 6-1: COMMAND REPEAT TIME

$$\text{Command Repeat Time} = TSMAX \times TCMAX \times 2.5ms \times 1.17$$

Where:

1.17 is related to the tolerance of the baud rate.

TABLE 6-8: FRR COMMAND REPEAT TIME VS. (TSMAX, TCMAX)

(TSMAX, TCMAX)	(1,1)	(1,2)	(1,4)	(16,1)	(16,2)	(16,4)	(64,1)
Command Repeat Time	2.925 ms	5.85 ms	11.7 ms	46.8 ms	93.6 ms	187.2 ms	187.2 ms

6.2.3.4 1-of-16 PPM

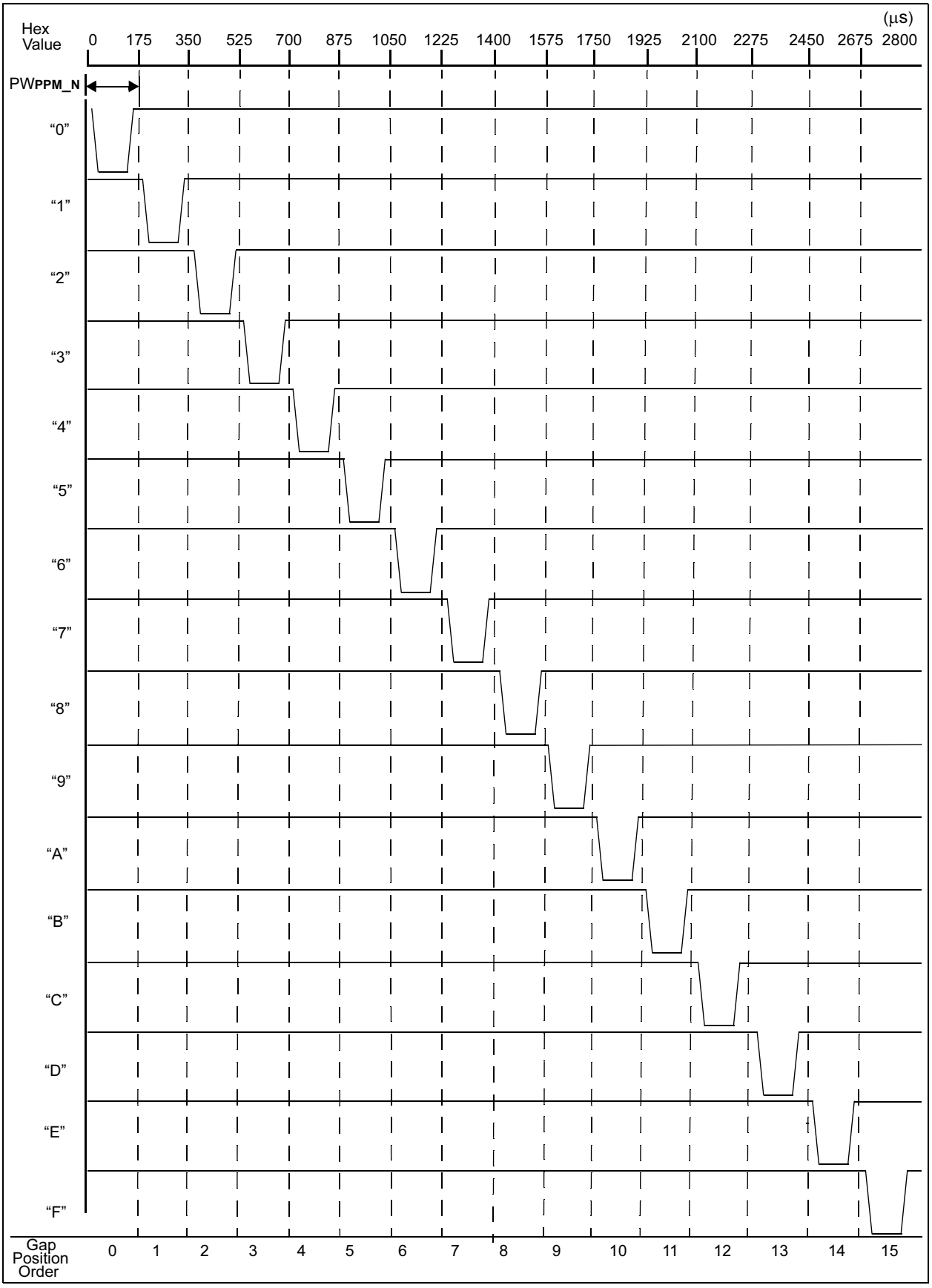
The Interrogator uses 1-of-16 Pulse Position Modulation (PPM) for MC1 and MC2 matching codes, End Process (EP) and also commands in Table 6-2. 1-of-16 PPM uses only one gap pulse in one of sixteen possible pulse positions for sending 4-bit symbols (2^4 = 16). This means one symbol (one data packet) represents 4 bits of binary data. One symbol lasts for 2.8 ms and 160 μs for Normal Speed and Fast Speed mode, respectively. All communications begin with time calibration pulses (TCP) composed of three pulses in positions, zero, six and fourteen of a 1-of-16 PPM symbol, as shown in Figure 6-10.

TABLE 6-9: 1-OF-16 PPM PULSE SPECIFICATIONS

	Normal Mode	Fast Mode
Modulation depth (MOD_{INDEX_GAP})	100% (max)	100% (max)
Pulse width	175 μs (typical)	10 μs (typical)
Gap width	100 μs (typical)	7 μs (typical)
Pulse positions per symbol	16	16
Symbol width	2.8 ms (typical)	160 μs (typical)
Calibration sequence	Pulses in positions 0, 6, 14	Pulses in positions 0, 6, 14

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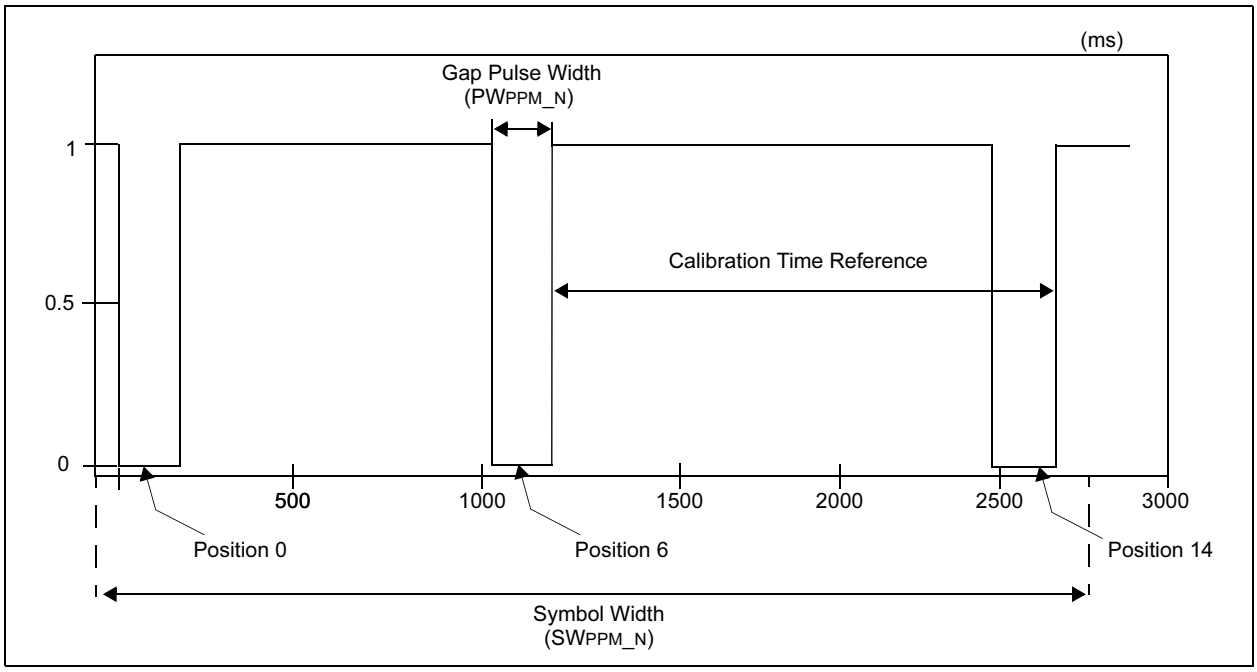
FIGURE 6-9: 1-OF-16 PPM REPRESENTATION FOR HEX VALUES FOR NORMAL SPEED MODE



6.2.3.5 Calibration Of Time Reference For Decoding

The device uses TCP to match its internal decoder timing to the Interrogator timing. The Interrogator transmits the timing pulses at the start of all commands and at least every 17 symbols. The TCP uses a code violation of the 1-of-16 PPM signal consisting of three gap pulses within one symbol. The first gap pulse is located at position 0, the second gap pulse at position 6 and the third at position 14 of the symbol. The time period between the last two gap pulses is used to calibrate the device's timing for decoding. Figure 6-10 shows the calibration pulses for Normal Speed mode. The waveform of the gap pulses is the same as the 1-of-16 PPM signal, as shown in Figure 6-2. For Fast Speed mode, the gap positions are the same. PW_{PPM_F} is the gap pulse width and SW_{PPM_F} is the symbol width of the Fast mode.

FIGURE 6-10: CALIBRATION PULSES FOR NORMAK SPEED MODE



6.2.3.6 Calculation Of Matching Code

When the Interrogator receives the FR response from a device, it sends an MC to select the device. The MC is sent during the device's listening window. There are two different types of matching codes: MC1 and MC2. Both MC1 and MC2 are used in the detection loop. MC2 is used in the reactivation loop, as detailed in Figure 6-1. The MC1 command is used to send the device to the sleeping loop, while MC2 is used to send the device to the processing loop.

The MC is an 8-bit "match" of tag ID followed by 4-bit matching code type and parity bit such that:

Matching code (12 bits) = "match (8 bits of tag ID)" + matching code type (3 bits)+ parity (1-bit)

The matching code type and parity bit is bit-wise structured as follows:

- MC1: `010P`
- MC2: `100P`

where P represents the parity bit of all match bits (8 bits) plus the MC type (3 bits).

The "match" part of the MC is 8 bits of the 32-bit Tag ID. The Interrogator selects the 8 bits from the 32-bit Tag ID by calculating the bit range of the Tag ID. Equation 6-2 shows the equation for selecting the bit range using the transmission counter (TC). Both the

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32-bit Tag ID and TC are included in the FR response. An example for the calculation of the matching code is given in Example 9-2.

EQUATION 6-2: BIT-WISE EQUATION FOR "MATCH"

"Match" = Tag ID bit range a: b
{4*TC} modulo 32: {4 (TC +1) + 3} modulo 32

where {} modulo 32 means the remainder of {} divided by 32. For example, {28} modulo 32 and {35} modulo 32 are 28 and 3, respectively.

6.3 Time Slot Generator

This block generates time slots for the device. The time slot represents the time delay between the end of the FRR command and the beginning of the FR response. The available time slots are 1, 16 or 64. One time slot represents 2.5 ms. The device calculates the actual time slot based on the TSMAX, TC and Tag ID. The maximum time slot (TSMAX) is assigned to the device by the FRR command (see Figures 6-3 to 6-7), or set to 16, if the TF bit is set.

Four or six bits out of the 32-bit Tag ID are used to calculate the time slot, with TC being the shift parameter to choose which portion of the 32-bit Tag ID is used, as shown in Equation 6-3.

EQUATION 6-3: TIME SLOT CALCULATION

TSMAX	Time Slot = Tag ID bit range a:b
64	{[4(TC+1)+1] modulo 32: [4 TC] modulo 32} XOR TC LSB
16	{[4(TC+1)-1] modulo 32: [4 TC] modulo 32} XOR TC LSB
1	0

Note: The exclusive-or (XOR) operation in Equation 6-3 is called "semi-inverting" in that it randomizes worst case tag IDs; for example: a Tag ID of '77777777' or '00000000'. Table 6-10 shows examples of the calculation.

TABLE 6-10: EXAMPLE: TAG ID = h´825FE1A0

TC	Relevant Tag ID		Selected Tag ID before XOR with LSB of TC		Calculated Time Slot (TS) (after XOR with LSB of TC)			
	Hexadecimal	Binary	TSMAX = 16	TSMAX = 64	TSMAX = 16		TSMAX = 64	
0	h´825FE1(A0)´	b'1010 0000'	h´0´	h´20´	h´0´	d´0´	h´20´	d´32´
1	h´825FE(1A)0´	b'0001 1010'	h´A´	h´1A´	h´5´	d´5´	h´25´	d´37´
2	h´825F(E1)A0´	b'1110 0001'	h´1´	h´21´	h´1´	d´1´	h´21´	d´33´
3	h´825(FE)1A0´	b'1111 1110'	h´E´	h´3E´	h´1´	d´1´	h´01´	d´1´
4	h´82(5F)E1A0´	b'0101 1111'	h´F´	h´1F´	h´F´	d´15´	h´1F´	d´31´
5	h´8(25)FE1A0´	b'0010 0101'	h´5´	h´25´	h´A´	d´10´	h´1A´	d´26´
6	h´(82)5FE1A0´	b'1000 0010'	h´2´	h´02´	h´2´	d´2´	h´02´	d´2´
7	h´(08)25FE1A´	b'0000 1000'	h´8´	h´08´	h´7´	d´7´	h´37´	d´55´

Legend: h´x..x´ represents hexadecimal number
d´x..x´ represents decimal number
b´x..x´ represents binary number

Table 6-10 shows the calculated time slot (TS): 5 for TC = 1 and TSMAX = 16 with Tag ID = h´825FE1A0´. This means the device waits for 12.5 ms (5 x 2.5 ms = 12.5 ms) in a nonmodulating condition between the end of FRR and the start of the FR response.

Also, the TS is 37 for TC = 1 and TSMAX = 64. This means the device waits for 92.5 ms (37 x 2.5 ms = 92.5 ms) between the end of FRR and the start of the FR response in a nonmodulating condition.

6.4 TIME SLOT COUNTER

This section generates the Sleep time (2.5 ms x TS) of the device. During the Sleep time, the device remains in a nonmodulating condition.

7.0 MEMORY SECTION

The memory section is organized into two groups: Main Memory Section and Stored CRC (SCRC) Memory Section.

7.1 Main Memory Section

The main section is organized into 32 blocks, as shown in Table 7-1, with each block having 32 bits. Each individual block can be read and written by the Interrogator's command. The first Blocks (0-2) are used for predefined parameters and device operation. The next three Blocks (3-5) are used as the FRF data.

The Blocks from 3 to 31 (29 blocks) are used for user data memory. Bits from 0 to 15 of Block 0 also can be used for user memory. The memory is read or written in 32-bit selectable units. The exceptions are the FR bit and the TF bit of Block 0, which are individually selectable.

Each block is accessed by the Interrogator's command based on block address. The reading of FRF blocks (Blocks 3-5) can be accomplished in two different ways: (1) by FRR command or (2) by Read Block command. The device sends the FRF data when it receives the FRR command. The length of the FRF data for the FRR command is determined by DF bits (see Table 7-6).

7.2 Stored CRC (SCRC) Memory Section

This memory section is used to store the CRC of the main memory section. It is organized into 32 blocks. Each block has 16 bits and contains the CRC of the corresponding memory block.

The Stored CRC (SCRC) is the CRC of the Interrogator's writing command (Write command + block address + data). The device stores the received Interrogator's CRC and sends back verification when it sends the block data. For the Block 0 and 2, the device sends CCRC instead of the SCRC. The device sends the CRC of each block as follows:

- Blocks 0 and 2: CCRC of block number and block data.
- Other blocks except Block 0 and 2: SCRC.
- CRC for FRR response: CCRC of Tag ID and FRF (Blocks 3-5) data. The data length of the FRF is determined by DF bits (B0: 26-27).

TABLE 7-1: MEMORY ORGANIZATION

Main Memory Section (32 blocks x 32 bits)	Stored CRC Section (32 blocks x 16 bits)	Comments
MSB … LSB	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
FR | TF | TFT | DF | MT | TM | Available to user (21 Bits)		Block 0 (Tag Parameters + User Memory)
Byte 3 | Byte 2 | Byte 1 | Byte 0		Block 1 (Tag ID = Serial Number)
31 30 29 28 27 26 25 24 | 23 22 21 20 19 18 17 16 | 15 14 13 12 11 10 9 8 | 7 6 5 4 3 2 1 0		Block 2 (Write Protection bits) (Clear bit 2 to write-protect Block 2)
Fast | Read | Field | (LS Block)		Block 3 (FR Field Least Significant Block)
Fast | Read | Field |		Block 4 (FR Field)
Fast | Read | Field | (MS Block)		Block 5 (FR Field Most Significant Block)
		Block 6 (User Data)
		Block 7 (User Data)
. . . . .		. . . . .
		Block 31 (User Data)

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7.3 Bit Layout

7.3.1 BLOCK 0

The bit layout in Block 0 is given in the following table.
FR and TF bits are not write-protectable.

TABLE 7-2: BIT LAYOUT OF BLOCK 0

B0:31	B0:30	B0:29	B0:28	B0:27	B0:26	B0:25	B0:24
FR	TF	TFT1	TFT0	DF1	DF0	MT1*	MT0*
B0:23	B0:22	B0:21	B0:20	B0:19	B0:18	B0:17	B0:16
TM2*	TM1*	TM0*	User Memory				
B0:15	B0:14	B0:13	B0:12	B0:11	B0:10	B0:9	B0:8
User Memory							
B0:7	B0:6	B0:5	B0:4	B0:3	B0:2	B0:1	B0:0
User Memory							

Note: * These are 'hardwired' bits, not EEPROM bits.

7.3.1.1 Description Of Bits

TABLE 7-3: FR BIT (B0:31)

FR	Reply to FRR (Fast Read Request) Command	Reply to FRB (Fast Read Bypass) Command	Application Example
0	No	Yes (see Example 9-1 for response)	"Item" has been purchased in retail EAS applications.
1	Yes (see Example 9-1 for response)	No	"Item" is unpaid in retail EAS applications.

Note: FR bit is not write-protectable.

TABLE 7-4: TF BIT (B0:30)

TF	Condition
0	Interrogator-Talks-First (ITF) mode: Wait for FRR command for FRR Response.
1	Tag-Talks-First (TFT) mode if FR bit is also set: Send Fast Read response without waiting for FRR command.

Note: TF bit is not write-protectable.

TABLE 7-5: TFT BITS (B0:29 - B0:28)

TFT1	TFT0	TCMAX [1] for Tag-Talks-First mode
0	0	1
0	1	2
1	0	4
1	1	Never Elapses (Default) [2]

Note 1: Only applicable in TTF mode. TSMAX parameter is set to 64 for TTF mode. For the ITF mode, the TCMAX is given in the FRR command.

2: The device continuously sends its FR response until it receives its correct matching code. On average, the device will send its FR response every 80 ms.

TABLE 7-6: DF BITS (B0:27 - B0:26)

DF1	DF0	FR Data Field Length
0	0	32 bits (Default)
0	1	48 bits
1	0	64 bits
1	1	96 bits

TABLE 7-7: MT BITS (B0:25 - B0:24)

MT1	MT0	Memory Type
0	0	Single level EEPROM (Default).
0	1	Reserved for future uses (e.g., multi level EEPROM).
1	0	Reserved for future uses.
1	1	Reserved for future uses.

Note: The MT bits are “hardwired”.

TABLE 7-8: TM BITS (B0:23 - B0:21)

TM2	TM1	TM0	Total Memory Size
0	0	0	512 bits
0	0	1	1 Kbit (Default)
0	1	0	TBD
0	1	1	TBD
1	0	0	TBD
1	0	1	TBD
1	1	0	TBD
1	1	1	TBD

Note: The TM bits are “hardwired”.

TABLE 7-9: B0: (20-0)

B0:(20-0)	Available for user

7.3.2 BLOCK 1: UNIQUE 32-BIT TAG ID

Block 1 contains 32 bits of unique Tag ID with SCRC. The ID is uniquely serialized by Microchip Technology Inc.

7.3.3 BLOCK 2: WRITE-PROTECT FOR THE FIRST KBITS

Each bit corresponds to a 32-bit block, (i.e., bit ‘0’ to Block 0, bit ‘1’ to Block 1, etc.). Program the corresponding bit to ‘0’ to write-protect the block. For example, program bit 10 to ‘0’ to write-protect the Block 10. The initial value (default) of Block 2 is ‘FFFFFFFD’. This means Block 1 (Tag ID) is write-protected before shipping to customer.

Write protection is a one way process, (i.e., once a block is write-protected, it cannot be modified). It should be noted that the write-protect block itself can be write-protected. TF and FR bits in Block 0 are not write-protectable, even if the write protection bit in the block is set.

TABLE 7-10: WRITE-PROTECT

Block X Write Status	Bit X of Write-Protect Block
Block X writable	1
Block X write-protected	0

7.3.4 BLOCKS 3 - 5: FAST READ FIELDS

These blocks contain data bits for the FR response. The state of the DF bits (see Table 7-6) in Block 0 determines the actual number of bits to be sent. This block can be used both as a customer ID and as additional tag ID numbers. These blocks are called Fast Read Field (FRF) because the device sends the FRF data immediately following the FRR command only (ITF mode), or as soon as energized (TTF mode), without an additional Block Read command. This means that the reading of this FRF data can be done by FRR command only. Reading of other block data requires the FRR and Block Read commands. Only the FRR device (FR bit = set) outputs the FRF data. The FRB device (FR bit = cleared) does not send the FRF data.

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8.0 DEVICE TESTING

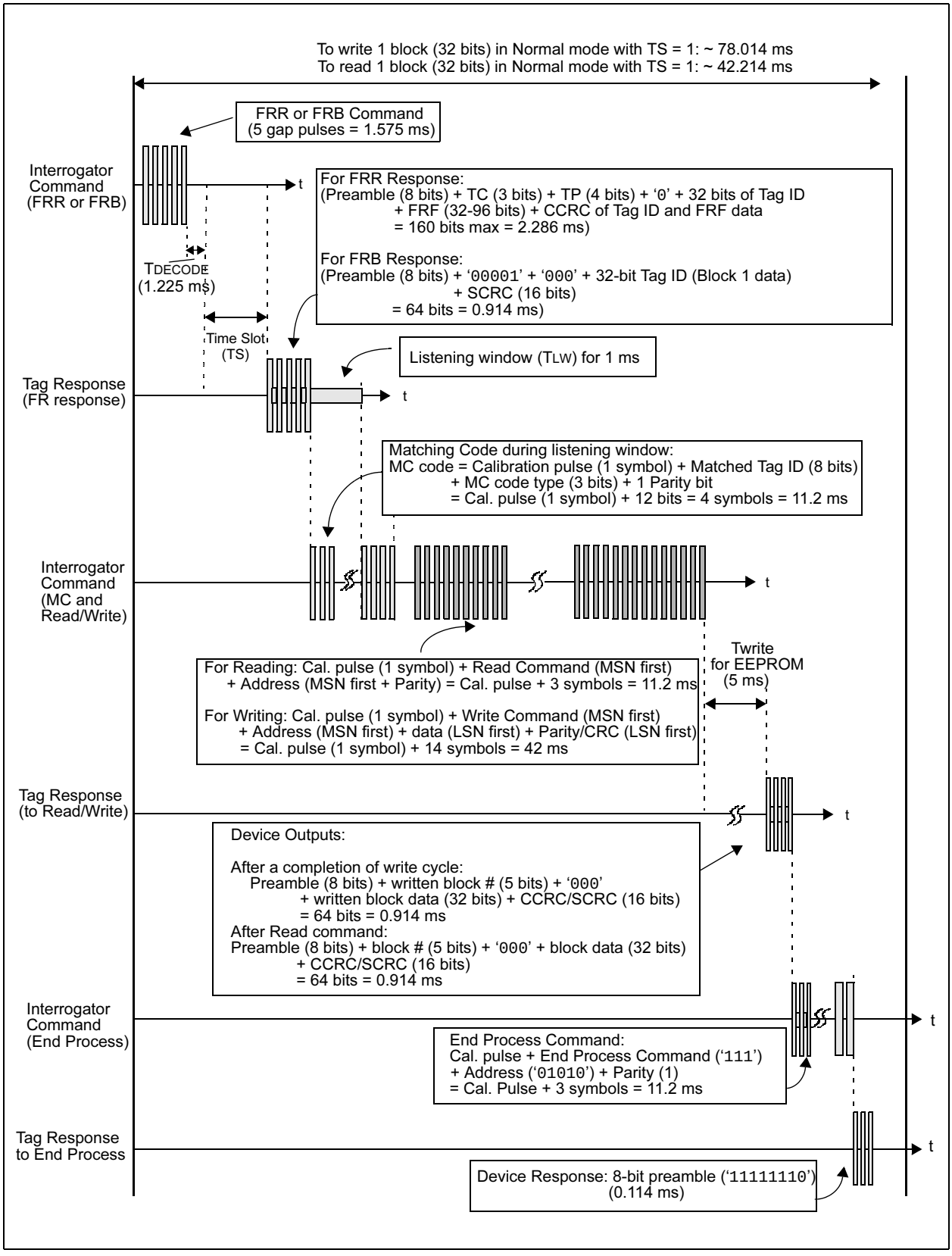
The device will be shipped to customers with the FR bit set, and with Block 1 write-protected.

The following bits are factory programmed prior to shipping:

1. DF0 (B0:26) and DF1(B0:27) are set to '0's.
2. TFT0 (B0:28) and TFT1(B0:29) bits are set to '1's.
3. All bits in the FR field (Blocks 3-5) are programmed to '1's.
4. Failed device in the Test mode: (1) Tag ID is programmed with "BADBADBA" and (2) inked with black color on the die (see **Section 10.0 "Failed Die Identification"**, for the failed die identification).

9.0 EXAMPLES

EXAMPLE 9-1: READ/WRITE PULSE SEQUENCE



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EXAMPLE 9-2: CALCULATION OF MATCHING CODE FOR TAG ID = 825FE1A0 (HEX, MSB FIRST)

The “match” part of the matching code is calculated by the Bit-Wise Equation in Equation 6-2:

“Match (8 bits)” = Tag ID bit range a:b = {4(TC)}modulo 32: {4(TC + 1) + 3} modulo 32

For TC = 2, the above equation gives a = 8, and b = 15.

The “Match (8 bits)” is chosen from (8th 9th 10th 11th) and (12th 13th 14th 15th) bits of the Tag ID.

Therefore, for the Tag ID = 825FE1A0 (hex) = b/1000 0010 0101 1111 1110 0001 1010 0000/,

“Match (8 bits)” = b/1110 0001/ = 1E (hex).

Using this “Match” part, a complete set of matching code is assembled as:

1E5 for MC1, and

1E9 for MC2

where:

5 in the MC1 was from b/0101/ (010 for MC1 and the last ‘1’ is a parity bit),

9 in the MC2 was from b/1001/ (100 for MC2 and the last ‘1’ is a parity bit).

Gap position in the 1-of-16 PPM signal for the calculated MC codes:

The gap position numbers in the 1-of-16 PPM for the calculated MC codes are (see Figure 6-9 for 1-of-16 PPM):

Positions 1, 14, and 5 for 1E5 for MC1 code

Positions 1, 14, and 9 for 1E9 for MC2 code.

The “Match” part of the matching code for various TCs are given in Table 9-1.

TABLE 9-1: CALCULATED “MATCH” FOR TAG ID = 825FE1A0 (HEX)

TC	“Match (8 bits) in hex”
0	0A
1	A1
2	1E
3	EF
4	F5
5	52
6	28
7	80

EXAMPLE 9-3: TO WRITE DATA INTO THE DEVICE

The Interrogator command structure for writing (see **Section 6.2.1 "Structure of Read/ Write Command Signals"**) is:

Calibration pulse + Writing Command (MSN first) + Address (MSN first) + Data (LSN first) + Parity/CRC (LSN first)

If the Interrogator wants to write data "0123cdef (hex, MSB to LSB)" to Block 5, the following message will be sent:

Calibration pulse + Write Command (MSN first) + Address (MSN first) + Data (LSN first) + Parity/CRC (LSN first)

= Cal. pulse + `101` (Write command) + `00101` (address) + f e d c 3 2 1 0 (data, hex) + CRC

= Calibration pulse + a 5 f e d c 3 2 1 0 6 0 2 e (hex string)

Note:	CRC = CRC for the Write command, address, and data. Calibration pulse is not included for the CRC calculation. See Application Note AN752 (DS00752) for the CRC calculation algorithm.

The hex string above is encoded with the 1-of-16 PPM signals. See Figure 6-10 for the 1-of-16 PPM representation of hex values.

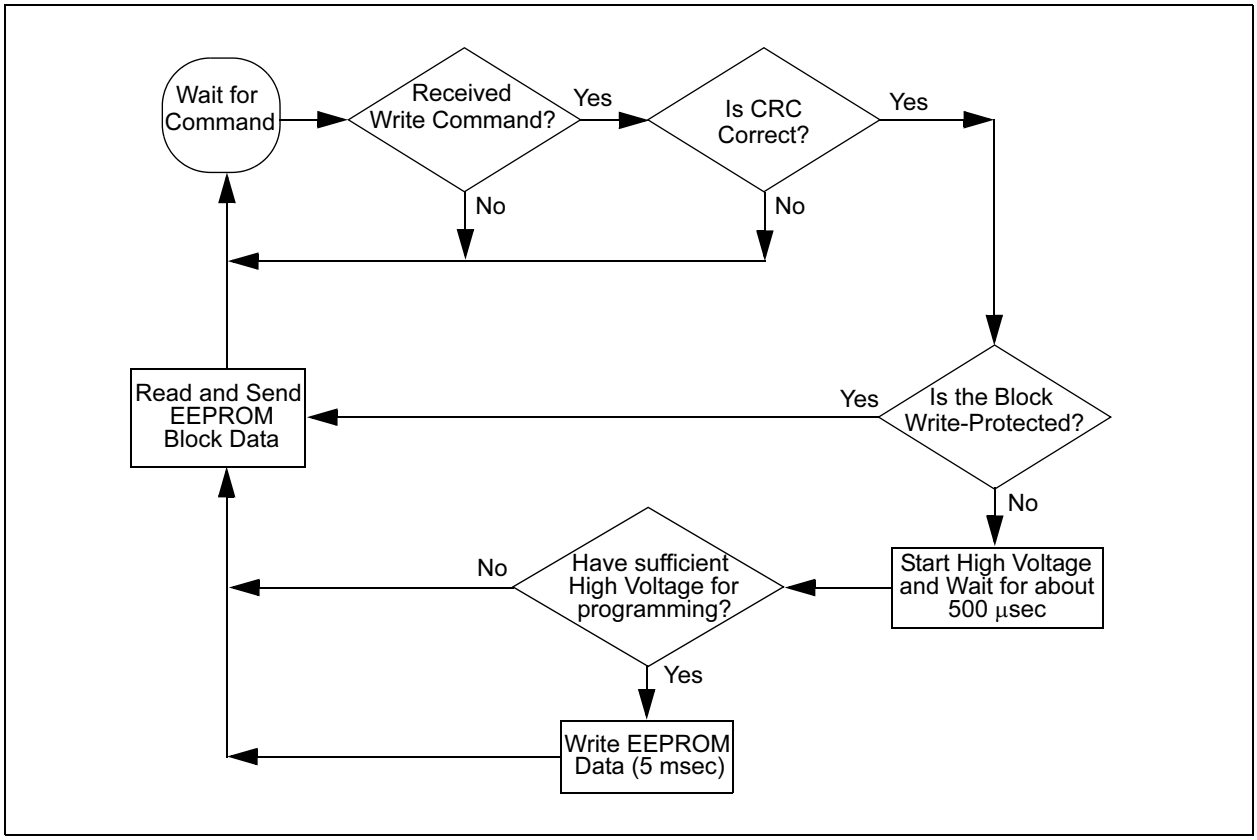
Referring to Figure 6-10, the gap positions in the 1-of-16 PPM for the above hex string are:

Positions 10 (a), 5 (5), 15 (f), 14 (e), 13 (d), 12 (c), 3 (3), 2 (2), 1 (1), 0 (0), 6 (6), 0 (0), 2 (2), e (14).

Device Response:

1. If writing is completed: The device sends the written data after 5 msec of EEPROM writing time.
2. If writing is failed due to insufficient programming voltage for unprotected block: The device sends the current block data after about 500 μsec of delay.
3. If writing is failed because the block is write-protected block: The device sends the current block data immediately after the command.
4. If writing is failed due to incorrect CRC: The device does not respond at all.

FIGURE 9-1: FLOW CHART FOR THE DEVICE RESPONSE TO THE WRITE COMMAND



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EXAMPLE 9-4: TO READ DATA FROM THE DEVICE

To read the content of Block 5 that has been programmed in the previous example, the Interrogator sends the following command:

Calibration pulse + Read Command (‘110’) + Address (‘00101’) + Parity (‘0’)

= Calibration pulse + C50 (hex)

The gap positions in the 1-of-16 PPM signal for the above hex string are:

12 (C), 5 (5), 0 (0).

Device Response:

When the device receives the above Interrogator command, the device outputs the following 70 kHz Manchester encoded data string (see **Section 6.2.2 “Structure of Device Response”**):

Preamble (8 bits) + Block number (5 bits, LSB first) + ‘000’ + Block Data (32 bits, LSB first) + SCRC (16 bits)

= 1-1-1-1-1-1-1-0 (f7) + 1-0-1-0-0-0-0-0 (5 0) + 1-1-1-1 0-1-1-1 1-0-1-1... 1-0-0-0

0-0-0-0 (f e d c 3 2 1 0) + 0-1-1-0 0-0-0-0 0-1-0-0 0-1-1-1 (602e).

EXAMPLE 9-5: TO SEND THE “END PROCESS” COMMAND

The Interrogator command structure (see **Section 6.2 “Anti-collision Command Controller”**) for the End Process is:

Calibration pulse + End Process Command (‘111’) + Address (‘01010’) + Parity (1) = Calibration pulse + EA1 (hex)

The gap positions in the 1-of-16 PPM signal for the above hex string are:

14 (E), 10 (A), 1 (1).

Device Response:

The device outputs the 8-bit preamble (‘11111110’) when it receives the End Process command, and enters the Sleeping Loop.

10.0 FAILED DIE IDENTIFICATION

Every die on the wafer is electrically tested according to the data sheet specifications and visually inspected to detect any mechanical damage, such as mechanical cracks and scratches.

Any failed die in the test or visual inspection is identified by black colored ink. Therefore, any die covered with black ink should not be used.

The ink dot specification:

- Ink dot size: 254 μm in circular diameter
- Position: central third of die
- Color: black

11.0 WAFER DELIVERY DOCUMENTATION

The wafer is shipped with the following information:

- Microchip Technology Inc. MP Code
- Lot Number
- Total number of wafers in the container
- Total number of good dice in the container
- Average die per wafer (DPW)
- Scribe number of wafers with number of good dice

12.0 NOTICE ON DIE AND WAFER HANDLING

The device is very susceptible to Electrostatic Discharge (ESD), which can cause a critical damage to the device. Special attention is needed during the handling process.

Any ultraviolet (UV) light can erase the memory cell contents of an unpackaged device. Fluorescent lights and sunlight can also erase the memory cell, although it takes more time than UV lamps. Therefore, keep any unpackaged device out of UV light and also avoid direct exposure of strong fluorescent lights and shining sunlight.

Certain IC manufacturing, COB, and tag assembly operations may use UV light. Operations such as back-grind de-tape, certain cleaning procedures, epoxy or glue cure should be done without exposing the die surface to UV light.

Using X-ray for die inspection will not harm the die, nor erase memory cell contents.

13.0 REFERENCES

It is recommended that the reader reference the following documents.

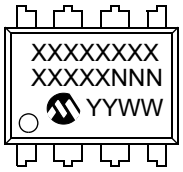
1. "*Antenna Circuit Design for RFID Applications*", AN710, DS00710.
2. "*RFID Tag and COB Development Guide with Microchip's RFID Devices*", AN830, DS00830.
3. "*CRC Algorithm for MCRF45X Read/Write Devices*", AN752, DS00752.
4. "*Interface Control Document for 13.56 MHz Anti-collision Interrogator*", AN759, DS00759.
5. "*13.56 MHz Reader Reference Design for the MCRF450/451/452/455 Read/Write Devices*", DS21654.

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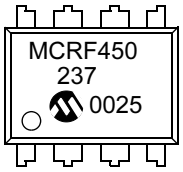
14.0 PACKAGING INFORMATION

14.1 Package Marking Information

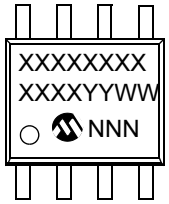
8-Lead PDIP (300 mil)



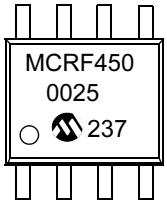
Example:



8-Lead SOIC (150 mil)



Example:



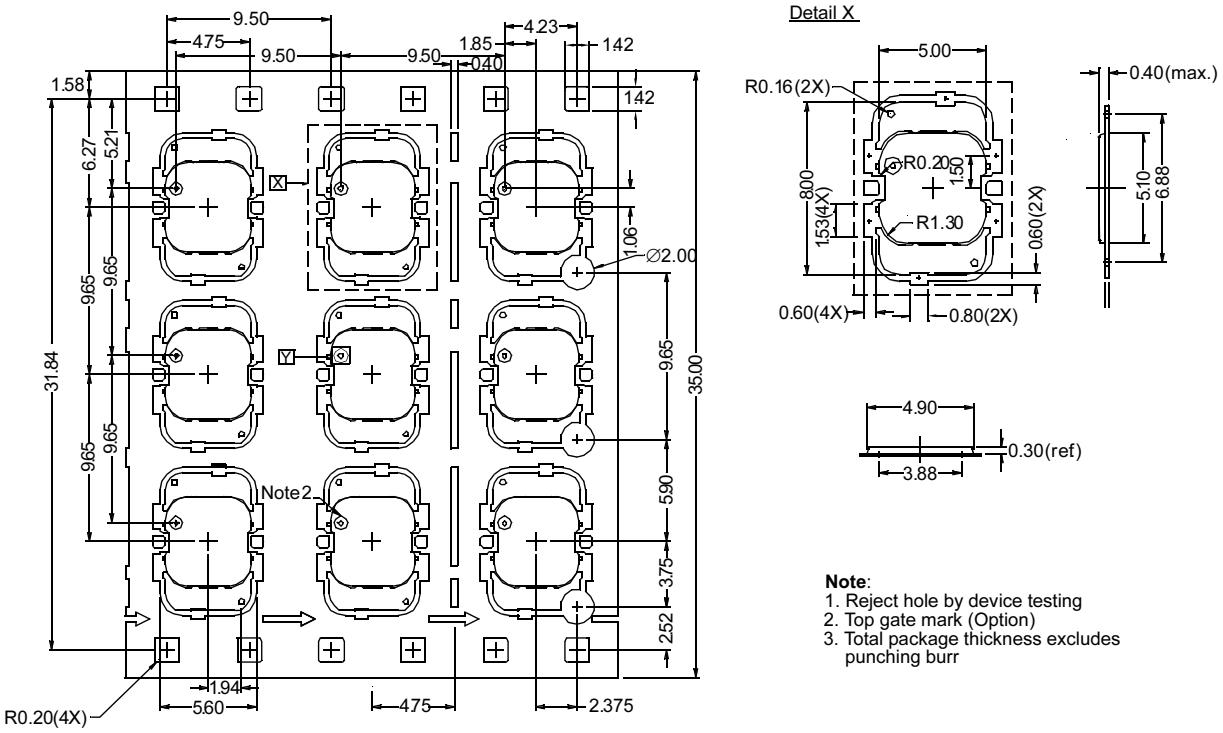
Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard device marking consists of Microchip part number, year code, week code, and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

Package Marking Information (Continued)

MCRF45X COB



Note:
1. Reject hole by device testing
2. Top gate mark (Option)
3. Total package thickness excludes punching burr

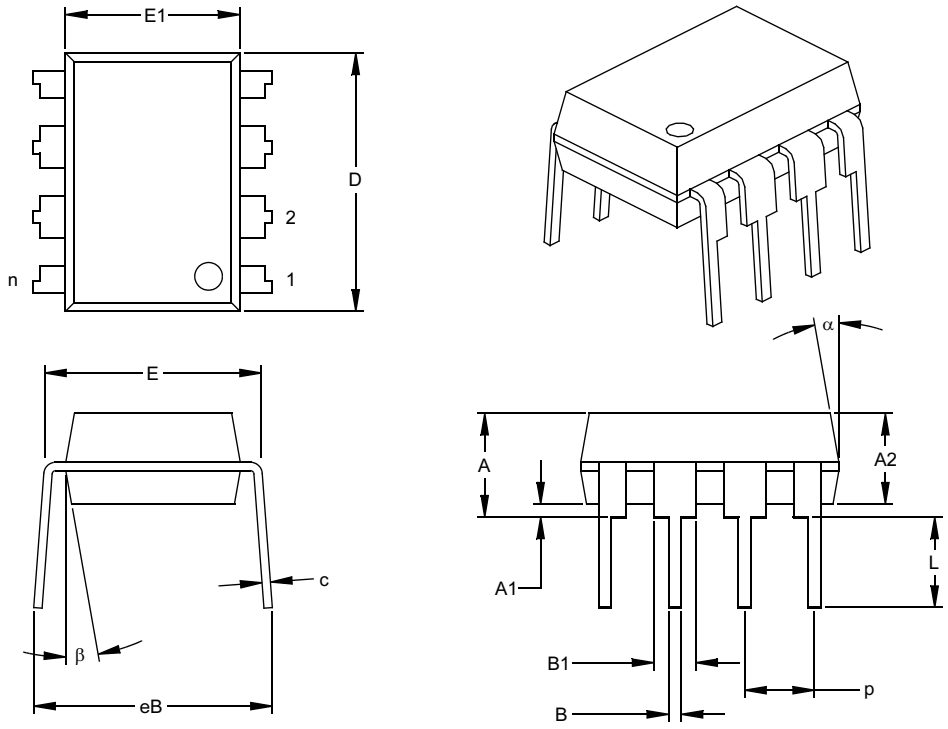
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	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

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8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

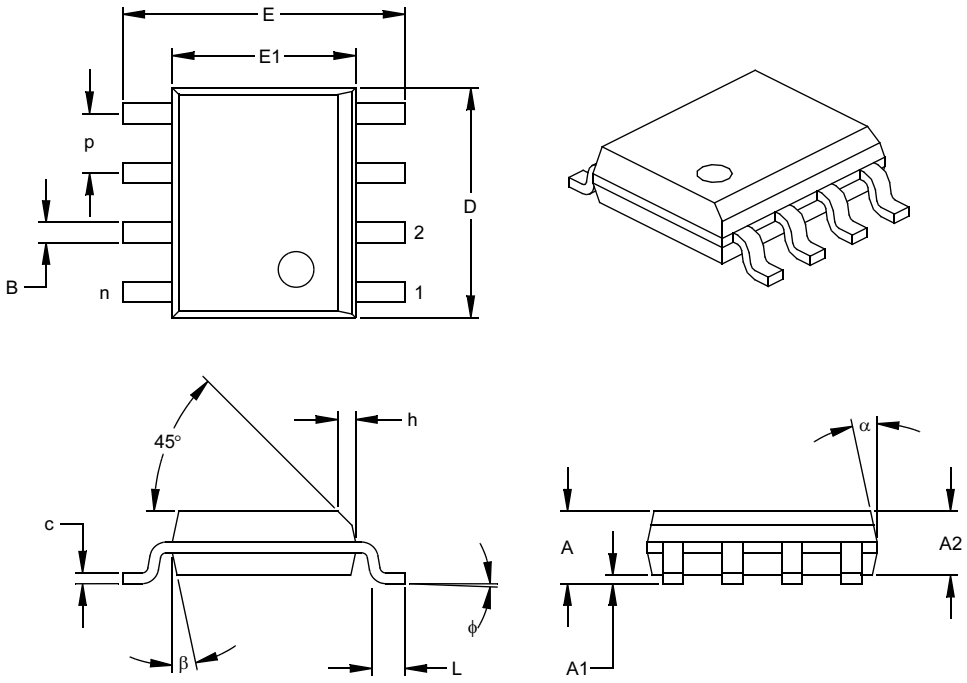


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

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Device: MCRF450/451/452/455 Literature Number: DS40232H

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCRF450:	13.56 MHz Anti-collision Read/Write MicroID device w/no internal resonant capacitor
	MCRF450/7M:	COB (Chip-On-Board) module with dual 68 pF capacitor
	MCRF451:	13.56 MHz Anti-collision Read/Write MicroID device w/100 pF internal resonant capacitor
	MCRF452:	13.56 MHz Anti-collision Read/Write MicroID device w/25 pF internal resonant capacitor
	MCRF455:	13.56 MHz Anti-collision Read/Write MicroID device w/50 pF internal resonant capacitor
Temperature Range:	=	-20°C to +70°C
Package:	WF	= Sawed 8" wafer on frame (8 mil backgrind)
	WFB	= Bumped, sawed 8" wafer on frame (8 mil backgrind
	W	= 8" wafer (11 mil backgrind)
	WB	= Bumped 8" wafer (8 mil backgrind)
	S	= Dice in waffle pack (8 mil backgrind)
	SB	= Bumped die in waffle pack (8 mil backgrind)
	X/SN	= SOIC (150 mil body), 8-lead (rotated pinout)
	P	= PDIP (300 mil body), 8-lead

Examples:

a) MCRF450/W: 13.56 MHz Anti-collision Read/Write MicroID device, 1 Kbit, no cap, 8" wafer, 11-mil backgrind.

b) MCRF450/7M: 13.56 MHz Anti-collision Read/Write MicroID COB (IST IOA2), 1 Kbit, 68 pF dual capacitor between antenna A and B, antenna B and Vss. Thickness = 0.4 mm.

c) MCRF451/WF: 13.56 MHz Anti-collision Read/Write MicroID device, 1 Kbit, 100 pF internal res cap, 8" wafer on frame, 8 mil backgrind.

d) MCRF451/S: 13.56 MHz Anti-collision Read/Write MicroID device in waffle pack, 1 Kbit, 100 pF internal res cap, 8-mil thickness.

e) MCRF452/WFB: 13.56 MHz Anti-collision Read/Write MicroID bumped device for flip-chip assembly, 1 Kbit, 50 pF dual (25 pF) internal res cap, Bumped 8" wafer, 8-mil backgrind wafer on frame.

f) MCRF455X/SN: 13.56 MHz Anti-collision Read/Write MicroID device in SOIC package, 1k bit, 50 pF internal res cap.

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2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
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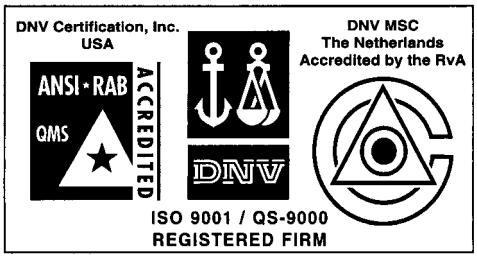
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