NOT RECOMMENDED FOR NEW DESIGNS
POSSIBLE SUBSTITUTE PRODUCT
ISL9208

X3100, X3101

4 Cell/3 Cell

Data Sheet | January 3, 2008 | FN8110.1

3 or 4 Cell Li-ion Battery Protection and Monitor IC

The X3100 is a protection and monitor IC for use in battery packs consisting of 4 series Lithium-Ion battery cells. The X3101 is designed to work in 3-cell applications. Both devices provide internal over-charge, over-discharge, and over-current protection circuitry, internal EEPROM memory, an internal voltage regulator, and internal drive circuitry for external FET devices that control cell charge, discharge, and cell voltage balancing.

Over-charge, over-discharge, and over-current thresholds reside in an internal EEPROM memory register and are selected independently via software using a 3MHz SPI serial interface. Detection and time-out delays can also be individually varied using external capacitors.

Using an internal analog multiplexer, the X3100 or X3101 allow battery parameters such as cell voltage and current (using a sense resistor) to be monitored externally by a separate microcontroller with A/D converter. Software on this microcontroller implements gas gauge and cell balancing functionality in software.

The X3100 and X3101 contain a current sense amplifier. Selectable gains of 10, 25, 80 and 160 allow an external 10-bit A/D converter to achieve better resolution than a more expensive 14-bit converter.

An internal 4k-bit EEPROM memory featuring IDLock™ allows the designer to partition and “lock in” written battery cell/pack data.

The X3100 and X3101 are each housed in a 28 Ld TSSOP package.

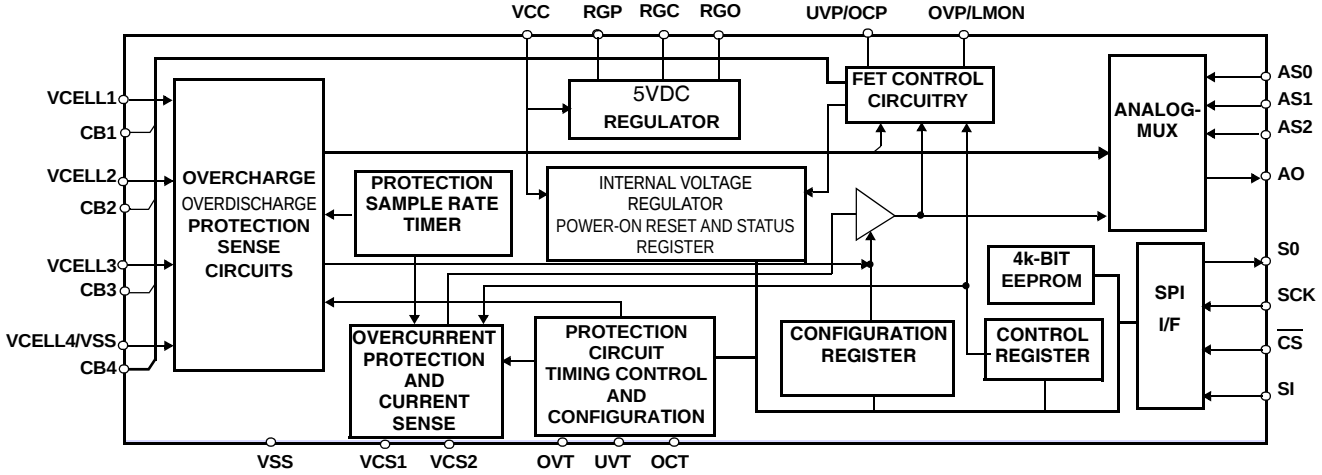
Features

- Software Selectable Protection Levels and Variable Protect Detection/Release Times
- Integrated FET Drive Circuitry
- Cell Voltage and Current Monitoring
- 0.5% Accurate Voltage Regulator
- Integrated 4k-bit EEPROM
- Flexible Power Management with 1µA Sleep Mode
- Cell Balancing Control
- Pb-Free Available (RoHS Compliant)

Benefit

- Optimize protection for chosen cells to allow maximum use of pack capacity
- Reduce component count and cost
- Simplify implementation of gas gauge
- Accurate voltage and current measurements
- Record battery history to optimize gas gauge, track pack failures and monitor system use
- Reduce power to extend battery life
- Increase battery capacity and improve cycle life battery life

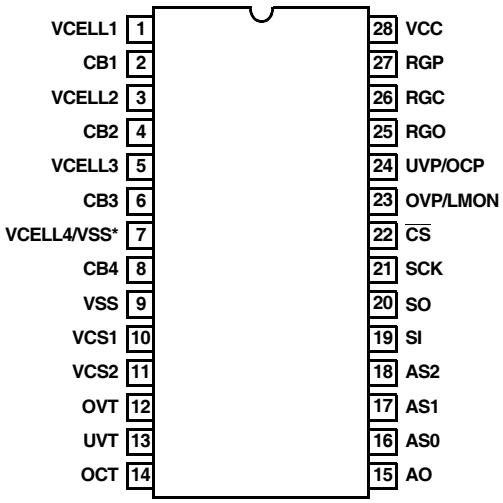
Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Pinout

X3100, X3101
(28 LD TSSOP)
TOP VIEW



*For X3101, Connect to GND

Ordering Information

PART NUMBER*	PART MARKING	V_{CC} LIMITS (V)	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
X3100V28*	X3100V	6 to 24	-20 to +70	28 Ld TSSOP	M28.173
X3100V28I	X3100V I	6 to 24	-20 to +70	28 Ld TSSOP	M28.173
X3100V28Z (Note)	X3100VZ	6 to 24	-20 to +70	28 Ld TSSOP (Pb-free)	M28.173
X3101V28*	X3101V	6 to 24	-20 to +70	28 Ld TSSOP	M28.173
X3101V28Z (Note)	X3101VZ	6 to 24	-20 to +70	28 Ld TSSOP (Pb-free)	M28.173

**Add “-T1” or “T2” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Descriptions

PIN NUMBER	PIN NAME	BRIEF DESCRIPTION
1	VCELL1	**Battery cell 1 voltage input.** This pin is used to monitor the voltage of this battery cell internally. The voltage of an individual cell can also be monitored externally at pin AO. The X3100 monitors 4 battery cells. The X3101 monitors 3 battery cells.
2	CB1	**Cell balancing FET control output 1.** This output is used to switch an external FET in order to perform cell voltage balancing control. This function can be used to adjust an individual cell voltage (e.g. during cell charging). CB1 can be driven high (Vcc) or low (Vss) to switch the external FET ON/OFF.
3	VCELL2	**Battery cell 2 voltage.** This pin is used to monitor the voltage of this battery cell internally. The voltage of an individual cell can also be monitored externally at pin AO. The X3100 monitors 4 battery cells. The X3101 monitors 3 battery cells.

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	BRIEF DESCRIPTION
4	CB2	**Cell balancing FET control output 2.** These outputs are used to switch an external FETs in order to perform cell voltage balancing control. This function can be used to adjust individual cell voltages (e.g. during cell charging). CB2 can be driven high (Vcc) or low (Vss) to switch the external FET ON/OFF.
5	VCELL3	**Battery cell 3 voltage.** This pin is used to monitor the voltage of each battery cell internally. The voltage of an individual cell can also be monitored externally at pin AO. The X3100 monitors 4 battery cells. The X3101 monitors 3 battery cells.
6	CB3	**Cell balancing FET control output 3.** This output is used to switch an external FET in order to perform cell voltage balancing control. This function can be used to adjust an individual cell voltage (e.g. during cell charging). CB3 can be driven high (Vcc) or low (Vss) to switch the external FET ON/OFF.
7	VCELL4/ VSS	**Battery cell 4 voltage (X3100) Ground (X3101).** This pin is used to monitor the voltage of this battery cell internally. The voltage of an individual cell can also be monitored externally at pin AO. The X3100 monitors 4 battery cells. The X3101 monitors 3 battery cells. For the X3101 device connect the VCELL4/VSS pin to ground.
8	CB4	**Cell balancing FET control output 4.** This output is used to switch an external FET in order to perform cell voltage balancing control. This function can be used to adjust individual cell voltages (e.g. during cell charging). CB4 can be driven high (Vcc) or low (Vss) to switch the external FET ON/OFF. When using the X3101, the CB4 pin can be left unconnected, or the FET control can be used for other purposes.
9	VSS	Ground.
10	VCS1	**Current sense voltage pin 1.** A sense resistor (R_{SENSE}) is connected between VCS1 and VCS2 (Figure 1). R_{SENSE} has a resistance in the order of 20mΩ to 100mΩ, and is used to monitor current flowing through the battery terminals, and protect against over-current conditions. The voltage at each end of R_{SENSE} can also be monitored at pin AO.
11	VCS2	**Current sense voltage pin 2.** A sense resistor (R_{SENSE}) is connected between VCS1 and VCS2 (Figure 1). R_{SENSE} has a resistance in the order of 20mΩ to 100mΩ, and is used to monitor current flowing through the battery terminals, and protect against over-current conditions. The voltage at each end of R_{SENSE} can also be monitored at pin AO.
12	OVT	**Over-charge detect/release time input.** This pin is used to control the delay time (T_{OV}) associated with the detection of an over-charge condition (see section “Over-charge Protection” on page 14).
13	UVT	**Over-discharge detect/release time input.** This pin is used to control the delay times associated with the detection (T_{UV}) and release (T_{UVR}) of an over-discharge (under-voltage) condition (see section “Over-discharge Protection” on page 16).
14	OCT	**Over-current detect/release time input.** This pin is used to control the delay times associated with the detection (T_{OC}) and release (T_{OCR}) of an over-current condition (see section “Over-Current Protection” on page 19).
15	AO	**Analog multiplexer output.** The analog output pin is used to externally monitor various battery parameter voltages. The voltages which can be monitored at AO (see section “Analog Multiplexer Selection” on page 21) are: – Individual cell voltages – Voltage across the current sense resistor (R_{SENSE}). This voltage is amplified with a gain set by the user in the control register (see section “Current Monitor Function” on page 21.) The analog select pins pins AS0 - AS2 select the desired voltage to be monitored on the AO pin.
16	AS0	**Analog output select pin 0.** These pins select which voltage is to be multiplexed to the output AO (see section “Sleep Control (SLP)” on page 11 and section “Current Monitor Function” on page 21)
17	AS1	**Analog output select pin 1.** These pins select which voltage is to be multiplexed to the output AO (see section “Sleep Control (SLP)” on page 11 and section “Current Monitor Function” on page 21)
18	AS2	**Analog output select pin 2.** These pins select which voltage is to be multiplexed to the output AO (see section “Sleep Control (SLP)” on page 11 and section “Current Monitor Function” on page 21)
19	SI	**Serial data input.** SI is the serial data input pin. All opcodes, byte addresses, and data to be written to the device are input on this pin.
20	SO	**Serial data output.** SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock. While $\overline{CS}$ is HIGH, SO will be in a High Impedance state. **Note:** SI and SO may be tied together to form one line (SI/SO). In this case, all serial data communication with the X3100 or X3101 is undertaken over one I/O line. This is permitted ONLY if no simultaneous read/write operations occur.
21	SCK	**Serial data clock input.** The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.
22	CS	**Chip select input pin.** When $\overline{CS}$ is HIGH, the device is deselected and the SO output pin is at high impedance. $\overline{CS}$ LOW enables the SPI serial bus.

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	BRIEF DESCRIPTION
23	OVP/ LMON	**Over-charge Voltage Protection output/Load Monitor output.** This one pin performs two functions depending upon the present mode of operation of the X3100 or X3101. Over-charge Voltage Protection (OVP) This pin controls the switching of the battery pack charge FET. This power FET is a P-channel device. As such, cell charge is possible when OVP/LMON=V_{SS}, and cell charge is prohibited when OVP/LMO = V_{CC}. In this configuration the X3100 and X3101 turn off the charge voltage when the cells reach the over-charge limit. This prevents damage to the battery cells due to the application of charging voltage for an extended period of time (see section “Over-charge Protection” on page 14). Load Monitor (LMON) In Over-current Protection mode, a small test current (7.5µA typ.) is passed out of this pin to sense the load resistance. The measured load resistance determines whether or not the X3100 or X3101 returns from an over-current protection mode (see section “Over-Current Protection” on page 19).
24	UVP/ OCP	**Over-discharge protection output/Over-current protection output.** Pin UVP/OCP controls the battery cell discharge via an external power FET. This P-channel FET allows cell discharge when UVP/OCP=Vss, and prevents cell discharge when UVP/OCP=Vcc. The X3100 and X3101 turn the external power FET off when the X3100 or X3101 detects either: Over-discharge Protection (UVP) In this case, pin 24 is referred to as “Over-discharge (Under-Voltage) protection (UVP)” (see section “Over-discharge Protection” on page 16). UVP/OCP turns off the FET to prevent damage to the battery cells by being discharged to excessively low voltages. Over-current protection (OCP) In this case, pin 24 is referred to as “Over-current protection (OCP)” (see section “Over-Current Protection” on page 19). UVP/OCP turns off the FET to prevent damage to the battery pack caused by excessive current drain (e.g. as in the case of a surge current resulting from a stalled disk drive).
25	RGO	**Voltage regulator output pin.** This pin is an input that connects to the collector of an external PNP transistor. The voltage at this pin is the regulated output voltage, but it also provides the feedback voltage for the regulator and the operating voltage for the device.
26	RGC	**Voltage regulator control pin.** This pin connects to the base of an external PNP transistor and controls the transistor turn on.
27	RGP	**Voltage regulator protection pin.** This pin is an input that connects to the emitter of an external PNP transistor and an external current limit resistor and provides a current limit voltage.
28	VCC	**Power supply.** This pin is provides the voltage for FET control, regulator operation, and wake-up circuits.

principles of operation

The X3100 and X3101 provide two distinct levels of functionality and battery cell protection:

First, in Normal mode, the device periodically checks each cell for an overcharge and overdischarge state, while continuously watching for a pack over-current condition. A protection mode violation results from an over-charge, over-discharge, or overcurrent state. The thresholds for these states are selected by the user through software. When one of these conditions occur, a Discharge FET or a Charge FET or both FETs are turned off to protect the battery pack. In an over-discharge condition, the X3100 and X3101 devices go into a low power sleep mode to conserve battery power. During sleep, the voltage regulator turns off, removing power from the microcontroller to further reduce pack current.

Second, in Monitor mode, a microcontroller with A/D converter measures battery cell voltage and pack current via pin AO and the X3100 or X3101 on-board MUX. The user can thus implement protection, charge/discharge, cell balancing or gas gauge software algorithms to suit the specific application and characteristics of the cells used. While monitoring these voltages, all protection circuits are on continuously.

In a typical application, the microcontroller is also programmed to provide an SMBus interface along with the Smart Battery System interface protocols. These additions allow an X3100 or X3101 based module to adhere to the latest industry battery pack standards.

Typical Application Circuit

The X3100 and X3101 have been designed to operate correctly when used as connected in the Typical Application Circuit (see Figure 1 on page 5).

The power MOSFET’s Q1 and Q2 are referred to as the “Discharge FET” and “Charge FET,” respectively. Since these FETs are p-channel devices, they will be ON when the gates are at V_{SS}, and OFF when the gates are at V_{CC}. As their names imply, the discharge FET is used to control cell discharge, while the charge FET is used to control cell charge. Diode D_1 allows the battery cells to receive charge even if the Discharge FET is OFF, while diode D_2 allows the cells to discharge even if the charge FET is OFF. D_1 and D_2 are integral to the Power FETs. It should be noted that the cells can neither charge nor discharge if both the charge FET and discharge FET are OFF.

Power to the X3100 or X3101 is applied to pin VCC via diodes D6 and D7. These diodes allow the device to be powered by the Li-Ion battery cells in normal operating conditions, and allow the device to be powered by an external source (such as a charger) via pin P+ when the battery cells are being charged. These diodes should have sufficient current and voltage ratings to handle both cases of battery cell charge and discharge.

The operation of the voltage regulator is described in section “Voltage Regulator” on page 22. This regulator provides a 5VDC±0.5% output. The capacitor (C1) connected from RGO to ground provides some noise filtering on the RGO output. The recommended value is 0.1µF or less. The value chosen must allow V_{RGO} to decay to 0.1V in 170ms or less when the X3100 or X3101 enter the sleep mode. If the decay is slower than this, a resistor (R1) can be placed in parallel with the capacitor.

During an initial turn-on period (T_{PUR} + T_{OC}), V_{RGO} has a stable, regulated output in the range of 5VDC ± 10% (see Figure). The selection of the microcontroller should take this into consideration. At the end of this turn on period, the X3100 and X3101 “self-tunes” the output of the voltage regulator to 5V+/-0.5%. As such, V_{RGO} can be used as a reference voltage for the A/D converter in the microcontroller. Repeated power-up operations, consistently re-apply the same “tuned” value for V_{RGO}.

Figure 1 shows a battery pack temperature sensor implemented as a simple resistive voltage divider, utilizing a thermistor (R_T) and resistor (R_T’). The voltage V_T can be fed to the A/D input of a microcontroller and used to measure and monitor the temperature of the battery cells. R_T’ should be chosen with consideration of the dynamic resistance range of R_T as well as the input voltage range of the microcontroller A/D input. An output of the microcontroller can be used to turn on the thermistor divider to allow periodic turn-on of the sensor. This reduces power consumption since the resistor string is not always drawing current.

Diode D3 is included to facilitate load monitoring in an Over-current protection mode (see section “Over-Current Protection” on page 19), while preventing the flow of current into pin OVP/LMON during normal operation. The N-Channel transistor turns off this function during the sleep mode.

Resistor R_{PU} is connected across the gate and drain of the charge FET (Q2). The discharge FET Q1 is turned off by the X3100 or X3101, and hence the voltage at pin OVP/LMON will be (at maximum) equal to the voltage of the battery terminal, minus one forward biased diode voltage drop (V_{P+} - V_{D7}). Since the drain of Q2 is connected to a higher potential (V_{P+}) a pull-up resistor (R_{PU}) in the order of 1MΩ should be used to ensure that the charge FET is completely turned OFF when OVP/LMON = V_{CC}.

The capacitors on the V_{CELL1} to V_{CELL4} inputs are used in a first order low pass filter configuration, at the battery cell voltage monitoring inputs (VCELL1 - VCELL4) of the X3100 or X3101. This filter is used to block any unwanted interference signals from being inadvertently injected into the monitor inputs. These interference signals may result from:

- Transients created at battery contacts when the battery pack is being connected/disconnected from the charger or the host.
- Electrostatic discharge (ESD) from something/someone touching the battery contacts.
- Unfiltered noise that exists in the host device.
- RF signals which are induced into the battery pack from the surrounding environment.

Such interference can cause the X3100 or X3101 to operate in an unpredictable manner, or in extreme cases, damage the device. As a guide, the capacitor should be in the order of 0.01µF and the resistor, should be in the order of 10kΩ. The capacitors should be of the ceramic type. In order to minimize interference, PCB tracks should be made as short and as wide as possible to reduce their impedance. The battery cells should also be placed as close to the X3100 or X3101 monitor inputs as possible.

Resistors R_{CB} and the associated n-channel MOSFET’s (Q_6 - Q_9) are used for battery cell voltage balancing. The X3100 and X3101 provide internal drive circuitry which allows the user to switch FETs Q_6 - Q_9 ON or OFF via the microcontroller and SPI port (see section “Cell Voltage Balance Control (CBC1-CBC4)” on page 12). When any of the these FETs are switched ON, a current, limited by resistor R_{CB}, flows across the particular battery cell. In doing so, the user can control the voltage across each individual battery cell. This is important when using Li-Ion battery cells since imbalances in cell voltages can, in time, greatly reduce the usable capacity of the battery pack. Cell voltage balancing may be implemented in various ways, but is usually performed towards the end of cell charging (“Top-of-charge method”). Values for R_{CB} will vary according to the specific application.

The internal 4kbit EEPROM memory can be used to store the cell characteristics for implementing such functions as gas gauging, battery pack history, charge/discharge cycles, and minimum/maximum conditions. Battery pack manufacturing data as well as serial number information can also be stored in the EEPROM array. An SPI serial bus provides the communication link to the EEPROM.

A current sense resistor (R_{SENSE}) is used to measure and monitor the current flowing into/out of the battery terminals, and is used to protect the pack from over-current conditions (see section “Over-Current Protection” on page 19). R_{SENSE} is also used to externally monitor current via a

microcontroller (see section “Current Monitor Function” on page 21).

FETs Q4 and Q5 may be required on general purpose I/Os of the microcontroller that connect outside of the package. In some cases, without FETs, pull-up resistors external to the pack force a voltage on the V_{CC} pin of the microcontroller during a pack sleep condition. This voltage can affect the proper tuned voltage of the X3100/X3101 regulator. These FETs should be turned-on by the microcontroller. (See Figure 1.)

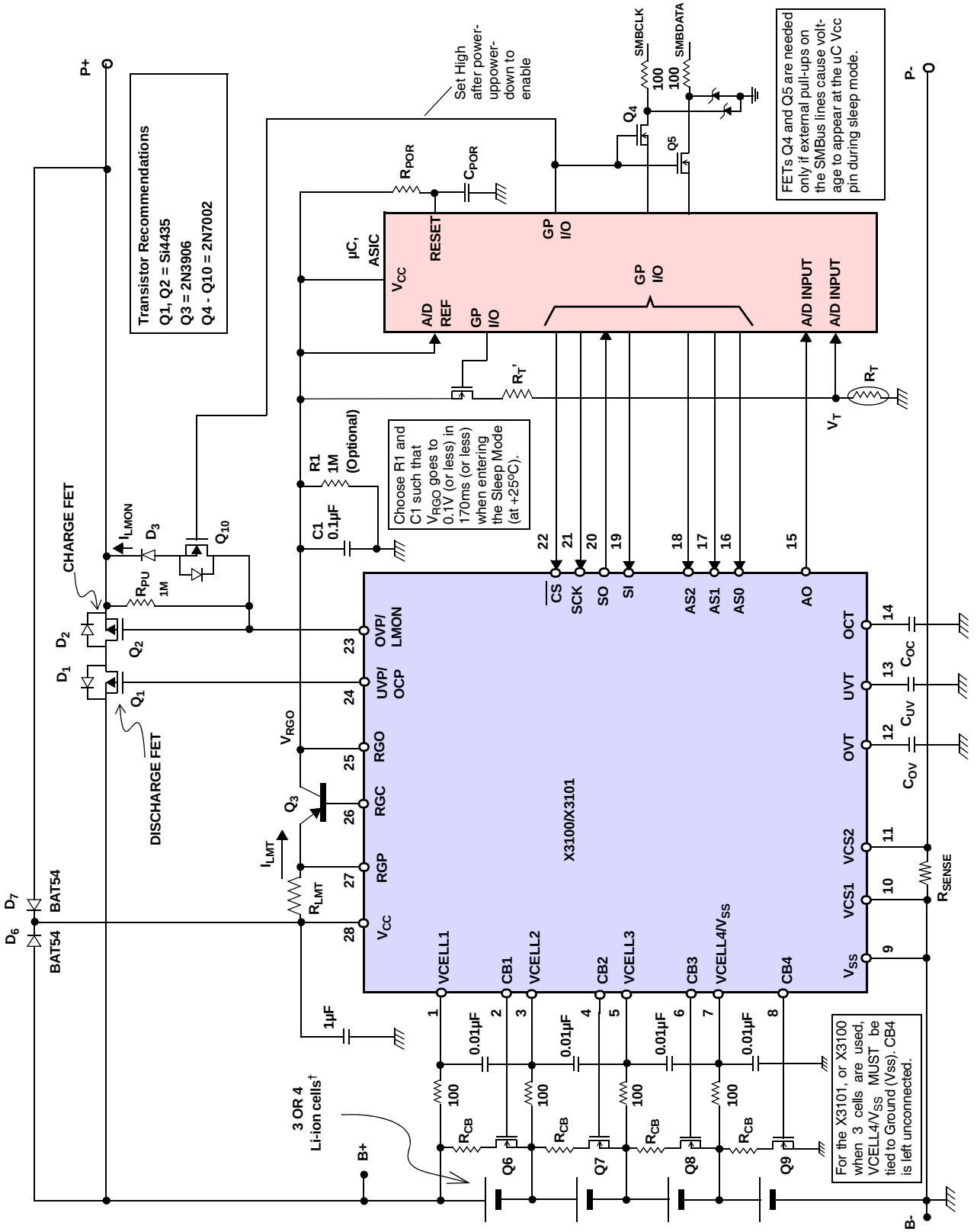
Power-on Sequence

Initial connection of the Li-Ion cells in the battery pack will not normally power-up the battery pack. Instead, the X3100 or X3101 enters and remains in the SLEEP mode. To exit the SLEEP mode, after the initial power-up sequence, or following any other SLEEP MODE, a minimum of 16V (X3100 V_{SLR}) or 12V (X3101 V_{SLR}) is applied to the VCC pin, as would be the case during a battery charge condition. (See Figure .)

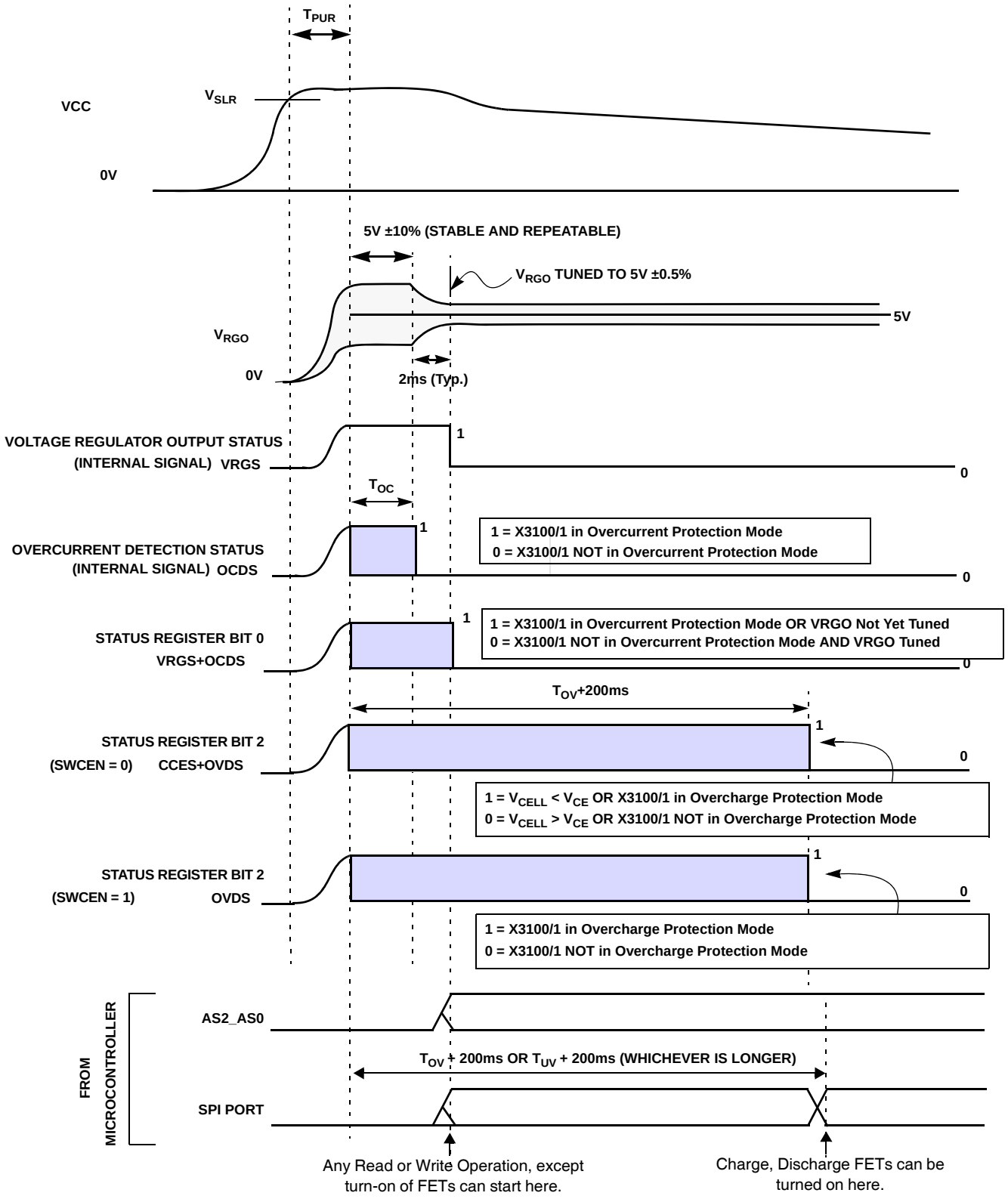
When V_{SLR} is applied to VCC, the analog select pins (AS2 - AS0) and the SPI communication pins ($\overline{CS}$, CLK, SI, SO) must be low, so the X3100 and X3101 power-up correctly into the normal operating mode. This can be done by using a power-on reset circuit.

When entering the normal operating mode, either from initial power-up or following the SLEEP MODE, all bits in the control register are zero. With UVPC and OVPC bits at zero, the charge and discharge FETs are off. The microcontroller must turn these on to activate the pack. The microcontroller would typically check the voltage and current levels prior to turning on the FETs via the SPI port. The software should prevent turning on the FETs throughout an initial measurement/calibration period. The duration of this period is T_{OV} + 200ms or T_{UV} + 200ms, whichever is longer.

Typical Application Circuit



Power-up Timing (Initial Power-up or after Sleep Mode)



Configuration Register

The X3100 and X3101 can be configured for specific user requirements using the Configuration Register.

TABLE 1. CONFIGURATION REGISTER FUNCTIONALITY

BIT(s)	NAME	FUNCTION
0 to 5	–	(don't care)
6	SWCEN	Switch Cell Charge Enable threshold function ON/OFF
7	CELLN	Set the number of Li-ion battery cells used (3 or 4)
8 to 9	VCE1-VCE0	Select Cell Charge Enable threshold
10 to11	VOC1-VOC0	Select overcurrent threshold
12 to 13	VUV1-VUV0	Select overdischarge (under voltage) threshold
14 to 15	VOV1-VOV0	Select overcharge voltage threshold

TABLE 2. CONFIGURATION REGISTER—UPPER BYTE

15	14	13	12	11	10	9	8
VOV1	VOV0	VUV1	VUV0	VOC1	VOC0	VCE1	VCE0

X3100 Default = 33H; X3101 Default = 03H.

TABLE 3. CONFIGURATION REGISTER—LOWER BYTE

7	6	5	4	3	2	1	0
CELLN	SWCEN	x	x	x	x	x	x

X3100 Default = C0H; X3101 Default = 40H.

Overcharge Voltage Settings

VOV1 and VOV0 control the cell over-charge level. See section "Over-charge Protection" on page 14.

TABLE 4. OVERCHARGE VOLTAGE THRESHOLD SELECTION

CONFIGURATION REGISTER BITS		
VOV1	VOV0	OPERATION (V)
0	0	V_{OV} = 4.20 (Default)
0	1	V_{OV} = 4.25
1	0	V_{OV} = 4.30
1	1	V_{OV} = 4.35

Overdischarge Settings

VUV1 and VUV0 control the cell over-discharge (under voltage threshold) level. See section "Over-discharge Protection" on page 16.

TABLE 5. OVERDISCHARGE THRESHOLD SELECTION.

CONFIGURATION REGISTER BITS		OPERATION	
VUV1	VUV0	X3100	X3101
0	0	V_{UV} = 1.95V	V_{UV} = 2.25V (X3101 default)
0	1	V_{UV} = 2.05V	V_{UV} = 2.35V
1	0	V_{UV} = 2.15V	V_{UV} = 2.45V
1	1	V_{UV} = 2.25V (X3100 default)	V_{UV} = 2.55V

Overcurrent Settings

VOC1 and VOC0 control the pack over-current level. See section "Over-Current Protection" on page 19.

TABLE 6. OVERCURRENT THRESHOLD VOLTAGE SELECTION

CONFIGURATION REGISTER BITS		
VOC1	VOC0	OPERATION
0	0	V_{OC} = 0.075V (Default)
0	1	V_{OC} = 0.100V
1	0	V_{OC} = 0.125V
1	1	V_{OC} = 0.150V

Cell Charge Enable Settings

VCE1, VCE0 and SWCEN control the pack charge enable function. SWCEN enables or disables a circuit that prevents charging if the cells are at too low a voltage. VCE1 and VCE0 select the voltage that is recognized as too low. See section "Sleep Mode" on page 16.

TABLE 7. CELL CHARGE ENABLE FUNCTION

CONFIGURATION REGISTER BITS	
SWCEN	OPERATION
0	Charge enable function: ON
1	Charge enable function: OFF

TABLE 8. CELL CHARGING THRESHOLD VOLTAGE SELECTION

CONFIGURATION REGISTER BITS		
VCE1	VCE0	OPERATION
0	0	V_{CE} = 0.5V
0	1	V_{CE} = 0.80V
1	0	V_{CE} = 1.10V
1	1	V_{CE} = 1.40V (Default)

Cell Number Selection

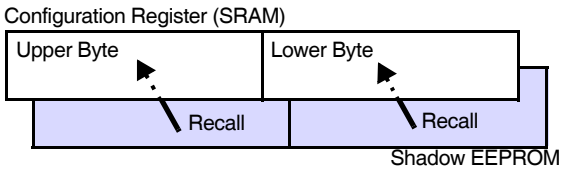
The X3100 is designed to operate with four (4) Li-Ion battery cells. The X3101 is designed to operate with three (3) Li-ion battery cells. The CELLN bit of the configuration register (Table 9) sets the number of cells recognized. For the X3101, the value for CELLN should always be zero.

Table 9. Selection of Number of Battery Cells[1]

Configuration Register Bit	
CELLN	**Operation**
1	4 Li-Ion battery cells (X3100 default)
0	3 Li-Ion battery cells (X3100 or X3101)

The configuration register consists of 16 bits of NOVRAM memory (Table 2, Table 3). This memory features a high-speed static RAM (SRAM) overlaid bit-for-bit with non-volatile “Shadow” EEPROM. An automatic array recall operation reloads the contents of the shadow EEPROM into the SRAM configuration register upon power-up (Figure 1).

Figure 1. Power-up of Configuration Register



The configuration register is designed for unlimited write operations to SRAM, and a minimum of 1,000,000 store operations to the EEPROM. Data retention is specified to be greater than 100 years.

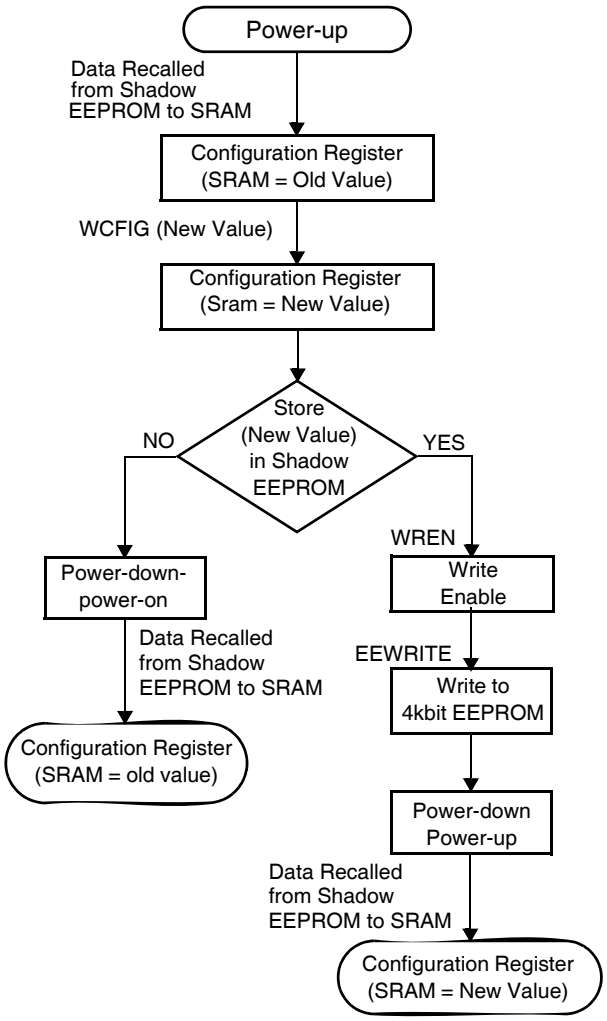
It should be noted that the bits of the shadow EEPROM are for the dedicated use of the configuration register, and are NOT part of the general purpose 4kbit EEPROM array.

The WCFIG command writes to the configuration register, see Table 30 and section “X3100/X3101 SPI Serial Communication” on page 23.

After writing to this register using a WCFIG instruction, data will be stored only in the SRAM of the configuration register. In order to store data in shadow EEPROM, a WREN instruction, followed by a EEWRITE to any address of the 4kbit EEPROM memory array must occur, see Figure 2. This sequence initiates an internal nonvolatile write cycle which permits data to be stored in the shadow EEPROM cells. It must be noted that even though a EEWRITE is made to the general purpose 4kbit EEPROM array, the value and address to which it is written, is unimportant. If this procedure is not followed, the configuration register will power-up to the last previously stored values following a power-down sequence.

1. In the case that the X3100 or X3101 is configured for use with only three Li-Ion battery cells (i.e. CELLN = 0), then VCELL4 (pin 7) MUST be tied to Vss (pin 9) to ensure correct operation.

Figure 2. Writing to Configuration Register



CONTROL REGISTER

The Control Register is realized as two bytes of volatile RAM (Table 10, Table 11). This register is written using the WCNTR instruction, see Table 30 and section "X3100/X3101 SPI Serial Communication" on page 23.

Table 10. Control Register—Upper Byte

15	14	13	12	11	10	9	8
CBC4	CBC3	CBC2	CBC1	UVPC	OVPC	CSG1	CSG0

Table 11. Control Register—Lower Byte

7	6	5	4	3	2	1	0
SLP	0	0	x	x	x	x	x

Since the control register is volatile, data will be lost following a power-down and power-up sequence. The default value of the control register on initial power-up or when exiting the SLEEP MODE is 00h (for both upper and lower bytes respectively). The functions that can be manipulated by the Control Register are shown in Table 12.

Table 12. Control Register Functionality

Bit(s)	Name	Function
0-4	–	(don't care)
5,6	0, 0	Reserved—write 0 to these locations.
7	SLP	Select sleep mode.
8,9	CSG1, CSG0	Select current sense voltage gain
10	OVPC	OVP control: switch pin OVP = V_{CC}/V_{SS}
11	UVPC	UVP control: switch pin UVP = V_{CC}/V_{SS}
12	CBC1	CB1 control: switch pin CB1 = V_{CC}/V_{SS}
13	CBC2	CB2 control: switch pin CB2 = V_{CC}/V_{SS}
14	CBC3	CB3 control: switch pin CB3 = V_{CC}/V_{SS}
15	CBC4	CB4 control: switch pin CB4 = V_{CC}/V_{SS}

Sleep Control (SLP)

Setting the SLP bit to '1' forces the X3100 or X3101 into the sleep mode, if $V_{CC} < V_{SLP}$. See section "Sleep Mode" on page 16.

Table 13. Sleep Mode Selection

Control Register Bits	
SLP	Operation
0	Normal operation mode
1	Device enters Sleep mode

Current Sense Gain (CSG1, CSG0)

These bits set the gain of the current sense amplifier. These are x10, x25, x80 and x160. For more detail, see section “Current Monitor Function” on page 21.

Table 14. Current Sense Gain Control

Control Register Bits		Operation
CSG1	CSG0	
0	0	Set current sense gain = x10
0	1	Set current sense gain = x25
1	0	Set current sense gain = x80
1	1	Set current sense gain = x160

Charge/Discharge Control (OVPC, UVPC)

The OVPC and UVPC bits allow control of cell charge and discharge externally, via the SPI port. These bits control the OVP/LMON and UVP/OCP pins, which in turn control the external power FETs.

Using P-channel power FETs ensures that the FET is on when the pin voltage is low (Vss), and off when the pin voltage is high (Vcc).

OVP/LMON and UVP/OCP can be controlled by using the WCNTR Instruction to set bits OVPC and UVPC in the Control register (See page 11).

Table 15. UVP/OVP Control

Control Register Bits		Operation
OVPC	UVPC	
1	x	Pin OVP = V_{SS} (FET ON)
0	x	Pin OVP = V_{CC} (FET OFF)
x	1	Pin UVP = V_{SS} (FET ON)
x	0	Pin UVP = V_{CC} (FET OFF)

It is possible to set/change the values of OVPC and UVPC during a protection mode. A change in the state of the pins OVP/LMON and UVP/OCP, however, will not take place until the device has returned from the protection mode.

Cell Voltage Balance Control (CBC1-CBC4)

This function can be used to adjust individual battery cell voltage during charging. Pins CB1 - CB4 are used to control external power switching devices. Cell voltage balancing is achieved via the SPI port.

Table 16. CB1—CB4 Control

Control Register Bits				Operation
CBC4	CBC3	CBC2	CBC1	
x	x	x	1	Set CB1 = V_{CC} (ON)
x	x	x	0	Set CB1=V_{SS} (OFF)
x	x	1	x	Set CB2 = V_{CC} (ON)
x	x	0	x	Set CB2 = V_{SS} (OFF)
x	1	x	x	Set CB3 = V_{CC} (ON)
x	0	x	x	Set CB3 = V_{SS} (OFF)
1	x	x	x	Set CB4 = V_{CC} (ON)
0	x	x	x	Set CB4 = V_{SS} (OFF)

CB1 - CB4 can be controlled by using the WCNTR Instruction to set bits CBC1 - CBC4 in the control register (Table 16).

STATUS REGISTER

The status of the X3100 or X3101 can be verified by using the RDSTAT command to read the contents of the Status Register (Table 17).

Table 17. Status Register.

7	6	5	4	3	2	1	0
0	0	0	0	0	CCES+ OVDS	UVDS	VRGS+ OCDS

The function of each bit in the status register is shown in Table 18.

Bit 0 of the status register (VRGS+OCDS) actually indicates the status of two conditions of the X3100 or X3101. Voltage Regulator Status (VRGS) is an internally generated signal which indicates that the output of the Voltage Regulator (VRGO) has reached an output of 5VDC ± 0.5%. In this case, the voltage regulator is said to be “tuned”. Before the signal VRGS goes low (i.e. before the voltage regulator is tuned), the voltage at the output of the regulator is nominally 5VDC ± 10% (See section “Voltage Regulator” on page 22.) Over-current Detection Status (OCDS) is another internally generated signal which indicates whether or not the X3100 or X3101 is in over-current protection mode.

Signals VRGS and OCDS are logically OR’ed together (VRGS + OCDS) and written to bit 0 of the status register (See Table 18, Table 17 and Figure).

Bit 1 of the status register simply indicates whether or not the X3100 or X3101 is in over-discharge protection mode.

Bit 2 of the status register (CCES+OVDS) indicates the status of two conditions of the X3100 or X3101. Cell Charge Enable Status (CCES) is an internally generated signal which indicates the status of any cell voltage (V_{CELL}) with respect to the Cell Charge Enable Voltage (V_{CE}). Over-charge Voltage Detection Status (OVDS) is an internally generated signal which indicates whether or not the X3100 or X3101 is in over-charge protection mode.

When the cell charge enable function is switched ON (configuration bit SWCEN=0), the signals CCES and OVDS are logically OR'ed (CCES+OVDS) and written to bit 2 of the status register. If the cell charge enable function is switched OFF (configuration bit SWCEN=1), then bit 2 of the status register effectively only represents information about the over-charge status (OVDS) of the X3100 or X3101 (See Table 18, Table 17 and Figure).

Table 18. Status Register Functionality.

Bit(s)	Name	Description	Case	Status	Interpretation
0	VRGS+OCDS	Voltage regulator status + Over-current detection status	-	1	V_{RGO} not yet tuned (V_{RGO} = 5V ± 10%) **OR** X3100/X3101 in over-current protection mode.
				0	V_{RGO} tuned (V_{RGO} = 5V ± 0.5%) **AND** X3100/X3101 NOT in over-current protection mode.
1	UVDS	Over-discharge detection status	-	1	X3100/X3101 in over-discharge protection mode
				0	X3100/X3101 NOT in over-discharge protection mode
2	CCES+OVDS	Cell charge enable status + Over-charge detection status	SWCEN =0†	1	$V_{CELL} < V_{CE}$ **OR** X3100/X3101 in over-charge protection mode
				0	$V_{CELL} > V_{CE}$ **AND** X3100/X3101 NOT in over-charge protection mode
			SWCEN =1†	1	X3100/X3101 in over-charge protection mode
				0	X3100/X3101 NOT in over-charge protection mode
3 - 7	-		-	0	Not used (always return zero)

Notes: † This bit is set in the configuration register.

X3100/X3101 INTERNAL PROTECTION FUNCTIONS

The X3100 and the X3101 provide periodic monitoring (see section "Periodic Protection Monitoring" on page 13) for over-charge and over-discharge states and continuous monitoring for an over-current state. It has automatic shutdown when a protection mode is encountered, as well as automatic return after the device is released from a protection mode. When sampling voltages through the analog port (Monitor Mode), over-charge and over-discharge protection monitoring is also performed on a continuous basis.

Voltage thresholds for each of these protection modes (V_{OV}, V_{UV}, and V_{OC} respectively) can be individually selected via software and stored in an internal non-volatile register. This feature allows the user to avoid the restrictions of mask programmed voltage thresholds, and is especially useful during prototype/evaluation design stages or when cells with slightly different characteristics are used in an existing design.

Delay times for the detection of, and release from protection modes (T_{OV}, T_{UV}/T_{UVR}, and T_{OC}/T_{OCR} respectively) can be individually varied by setting the values of external capacitors connected to pins OVT, UVT, OCT.

Periodic Protection Monitoring

In normal operation, the analog select pins are set such that AS2 = L, AS1 = L, AS0 = L. In this mode the X3100 and X3101 conserve power by sampling the cells for over or over-discharge conditions.

In this state over-charge and over-discharge protection circuitry are usually off, but are periodically switched on by the internal Protection Sample Rate Timer (PSRT). The over-charge and over-discharge protection circuitry is on for approximately 2ms in each 125ms period. Over-current monitoring is continuous. In monitor mode (see page 21) over-charge and over-discharge monitoring is also continuous.

Over-charge Protection

The X3100 and X3101 monitor the voltage on each battery cell (V_{CELL}). If for any cell, $V_{CELL} > V_{OV}$ for a time exceeding T_{OV}, then the Charge FET will be switched OFF (OVP/LMON = V_{CC}). The device has now entered Over-charge protection mode (Figure 3). The status of the discharge FET (via pin UVP) will remain unaffected.

While in over-charge protection mode, it is possible to change the state of the OVPC bit in the control register such that OVP/LMON = Vss (Charge FET = ON). Although the OVPC bit in the control register can be changed, the change will not be seen at pin OVP until the X3100 or X3101 returns from over-charge protection mode.

The over-charge detection delay T_{OV}, is varied using a capacitor (C_{OV}) connected between pin OVT and GND. A typical delay time is shown in Table 10. The delay T_{OV} that results from a particular capacitance C_{OV}, can be approximated by the following linear equation:

$$T_{OV}\ (s) \approx 10 \times C_{OV}\ (\mu F).$$

Table 19. Typical over-charge detection time

Symbol	C_{OV}	Delay
T_{OV}	0.1µF	1.0s (Typ)

The device further continues to monitor the battery cell voltages, and is released from over-charge protection mode when $V_{CELL} < V_{OVR}$, for all cells. When the X3100 or X3101 is released from over-charge protection mode, the charge FET is automatically switched ON (OVP/LMON = V_{SS}). When the device returns from over-charge protection mode, the status of the discharge FET (pin UVP/OCP) remains unaffected.

The value of V_{OV} can be selected from the values shown in Table 4 by setting bits VOV1, VOV0. These bits are set by using the WCFIG instruction to write to the configuration register.

Figure 3. Over-charge Protection Mode—Event Diagram

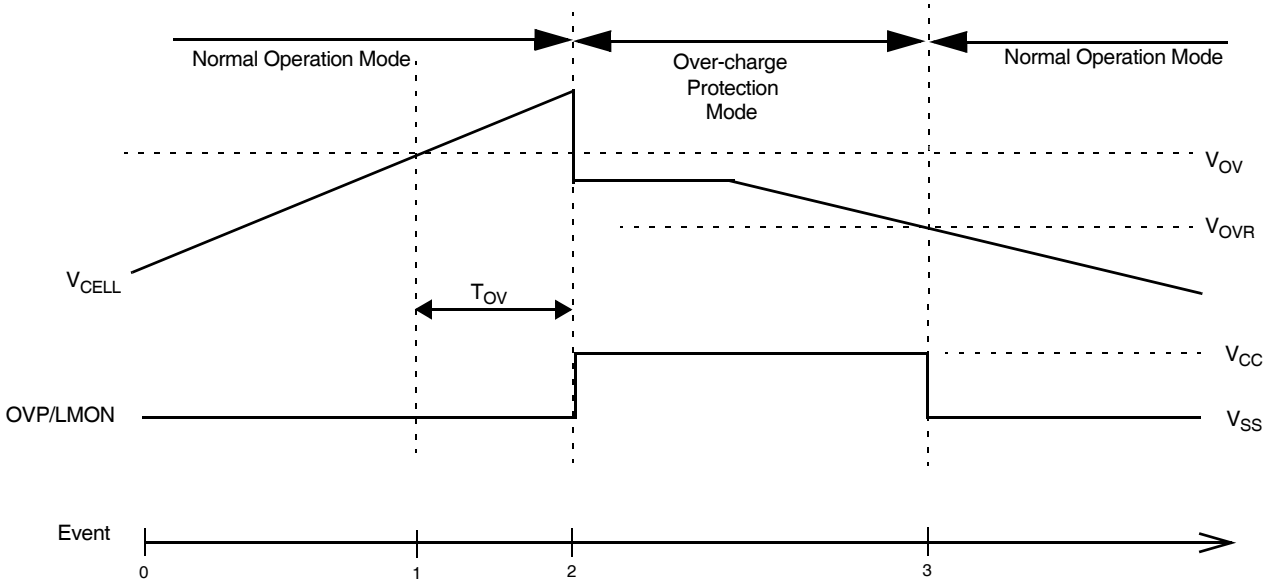


Table 20. Over-charge Protection Mode—Event Diagram Description

Event	Event Description
[0,1)	— Discharge FET is ON (UVP/OCP = V_{SS}). — Charge FET is ON (OVP/LMON = V_{SS}), and hence battery cells are permitted to receive charge. — All cell voltages (V_{CELL} - V_{CELL4}) are below the over-charge voltage threshold (V_{OV}). — The device is in normal operation mode (i.e. not in a protection mode).
[1]	— The voltage of one or more of the battery cells (V_{CELL}), exceeds V_{OV}. — The internal over-charge detection delay timer begins counting down. — The device is still in normal operation mode
(1,2)	The internal over-charge detection delay timer continues counting for T_{OV} seconds.
[2]	The internal over-charge detection delay timer times out **AND** V_{CELL} still exceeds V_{OV}. — Therefore, the internal over-charge sense circuitry switches the charge FET OFF (OVP/LMON=Vcc). — The device has now entered over-charge protection mode.
(2,3)	While in over-charge protection mode: — The battery cells are permitted to discharge via the discharge FET, and diode D_2 across the charge FET — The X3100 or X3101 monitors the voltages V_{CELL1} - V_{CELL4} to determine whether or not they have all fallen below the “Return from over-charge threshold” (V_{OVR}). — (It is possible to change the status of UVP/OCP or OVP/LMON using the control register)
[3]	— All cell voltages fall below V_{OVR}—The device is now in normal operation mode. — The X3100/X3101 automatically switches charge FET = ON (OVP/LMON = Vss) — The status of the discharge FET remains unaffected. — Charging of the battery cells can now resume.

Over-discharge Protection

If $V_{CELL} < V_{UV}$, for a time exceeding T_{UV}, the cells are said to be in a over-discharge state (Figure 4). In this instance, the X3100 and X3101 automatically switch the discharge FET OFF (UVP/OCP = Vcc), and then enter sleep mode.

The over-discharge (under-voltage) value, V_{UV}, can be selected from the values shown in Table 5 by setting bits VUV1, VUV0 in the configuration register. These bits are set using the WCFIG command. Once in the sleep mode, the following steps must occur before the X3100 or X3101 allows the battery cells to discharge:

– The X3100 and X3101 must wake from sleep mode (see section “Voltage Regulator” on page 22).

– The charge FET must be switched ON by the microcontroller (OVP/LMON=V_{SS}), via the control register (see section “Control Register Functionality” on page 11).

– All battery cells must satisfy the condition: $V_{CELL} > V_{UVR}$ for a time exceeding T_{UVR}.

– The discharge FET must be switched ON by the microcontroller (UVP/OCP=V_{SS}), via the control register (see section “Control Register Functionality” on page 11)

The times T_{UV}/T_{UVR} are varied using a capacitor (C_{UV}) connected between pin UVT and GND (Table 13). The delay T_{UV} that results from a particular capacitance C_{UV}, can be approximated by the following linear equation:

$$T_{UV}\ (s) \approx 10 \times C_{UV}\ (\mu F)$$

$$T_{UVR}\ (ms) \approx 70 \times C_{UV}\ (\mu F)$$

Table 21. Typical Over-discharge Delay Times

Symbol	Description	C_{UV}	Delay
T_{UV}	Over-discharge detection delay	0.1µF	1.0s (Typ)
T_{UVR}	Over-discharge release time	0.1µF	7ms (Typ)

Sleep Mode

The X3100 or X3101 can enter sleep mode in two ways:

i) The device enters the over-discharge protection mode.

ii) The user sends the device into sleep mode using the control register.

A sleep mode can be induced by the user, by setting the SLP bit in the control register (Table 13) using the WCNTR Instruction.

In sleep mode, power to all internal circuitry is switched off, minimizing the current drawn by the device to 1µA (max). In this state, the discharge FET and the charge FET are switched OFF (OVP/LMON=V_{CC} and UVP/OCP=V_{CC}), and the 5VDC regulated output (V_{RGO}) is 0V. Control of UVP/OCP and OVP/LMON via bits UVPC and OVPC in the control register is also prohibited.

The device returns from sleep mode when $V_{CC} \geq V_{SLR}$. (e.g. when the battery terminals are connected to a battery charger). In this case, the X3100 or the X3101 restores the 5VDC regulated output (section “Voltage Regulator” on page 22), and communication via the SPI port resumes.

If the Cell Charge Enable function is enabled when V_{CC} rises above V_{SLR}, the X3100 and X3101 internally verifies that the individual battery cell voltages (V_{CELL}) are larger than the cell charge enable voltage (V_{CE}) before allowing the FETs to be turned on. The value of V_{CE} is selected by using the WCFIG command to set bits VCE1–VCE0 in the configuration register.

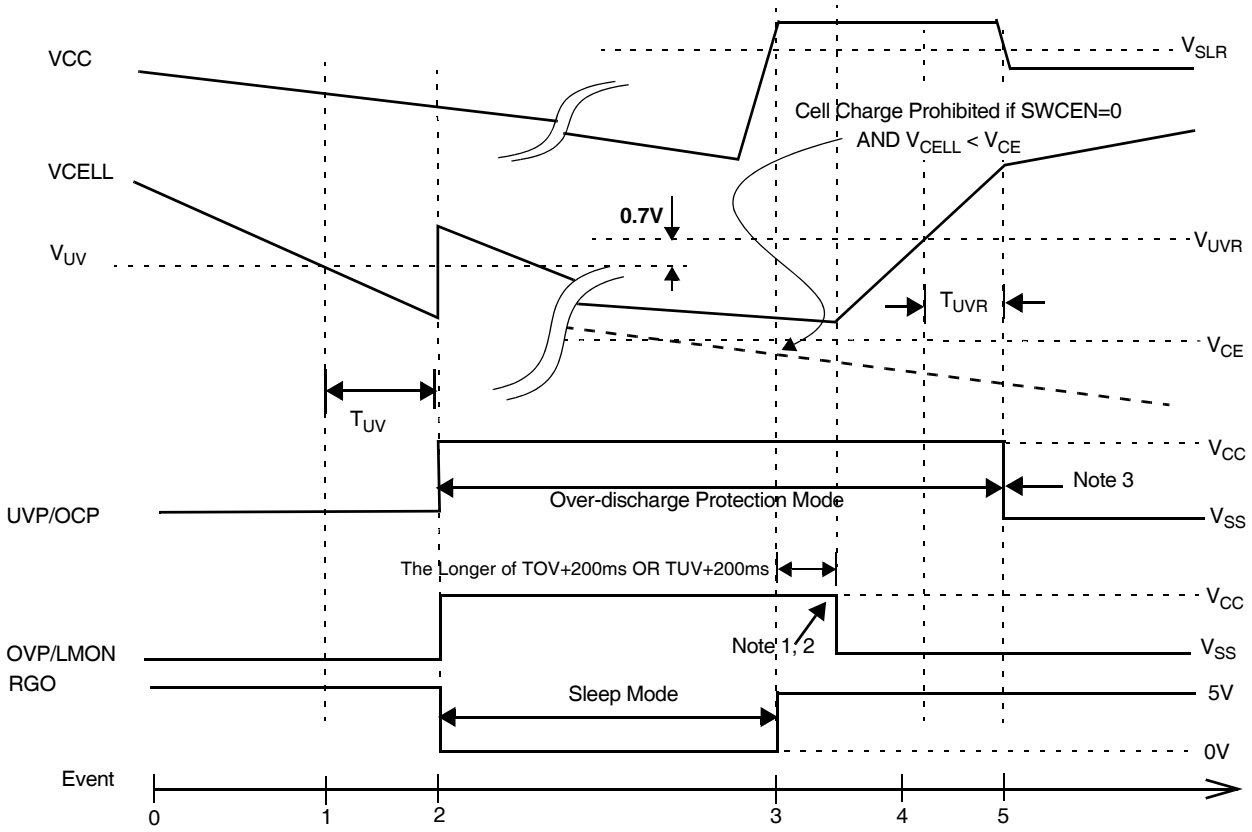
Only if the condition “$V_{CELL} > V_{CE}$” is satisfied can the state of charge and discharge FETs be changed via the control register. Otherwise, if $V_{CELL} < V_{CE}$ for any battery cell then both the Charge FET and the discharge FET are OFF (OVP/LMON=Vcc and UVP/OCP=V_{CC}). Thus both charge and discharge of the battery cells via terminals P+ / P- is prohibited[1].

The cell charging threshold function can be switched ON or OFF by the user, by setting bit SWCEN in the configuration register (Table 7) using the WCFIG command. In the case that this cell charge enable function is switched OFF, then V_{CE} is effectively set to 0V.

Neither the X3100 nor the X3101 enter sleep mode (automatically or manually, by setting the SLP bit) if $V_{CC} \geq V_{SLR}$. This is to ensure that the device does not go into a sleep mode while the battery cells are at a high voltage (e.g. during cell charging).

1. In this case, charging of the battery may resume ONLY if the cell charge enable function is switched OFF by setting bit SWCEN = 1 in the configuration register (See Above, “CONFIGURATION REGISTER FUNCTIONALITY” on page 9).

Figure 4. Over-discharge Protection Mode—Event Diagram



Note 1: If SWEN = 0 and $V_{CELL} < V_{CE}$, then OVP/LMON stays high and charging is prohibited.

Note 2: OVP/LMON stays high until the microcontroller writes a "1" to the OVPC bit in the control register. This sets the signal low, which turns on the charge FET. It cannot be turned on prior to this time.

Note 3: UVP/OCP stays high until the microcontroller writes a "1" to the UVPC bit in the control register. This sets the signal low, which turns on the discharge FET. The FET cannot be turned on prior to this time.

Table 22. Over-discharge Protection Mode—Event Diagram Description

Event	Event Description
[0,1)	—Charge FET is ON (OVP/LMON = V_{SS}) —Discharge FET is ON (UVP/OCP = V_{SS}), and hence battery cells are permitted to discharge. —All cell voltages ($VCELL_1$ - $VCELL_4$) are above the Over-discharge threshold voltage (V_{UV}). —The device is in normal operation mode (i.e. not in a protection mode).
[1]	—The voltage of one or more of the battery cells (V_{CELL}), falls below V_{UV}. —The internal over-discharge detection delay timer begins counting down. —The device is still in normal operation mode
(1,2)	The internal over-discharge detection delay timer continues counting for T_{UV} seconds.
[2]	—The internal over-discharge detection delay timer times out, AND V_{CELL} is still below V_{UV}. —The internal over-discharge sense circuitry switches the discharge FET OFF (UVP/OCP = Vcc). —The charge FET is switched OFF (OVP/LMON = V_{CC}). —The device has now entered over-discharge protection mode. —At the same time, the device enters sleep mode (See section "Voltage Regulator" on page 22).
(2,3)	While device is in sleep (in over-discharge protection) mode: —The power to ALL internal circuits is switched OFF limiting power consumption to less than 1µA. —The output of the 5VDC voltage regulator (RGO) is 0V. —Access to the X3100/X3101 via the SPI port is NOT possible.

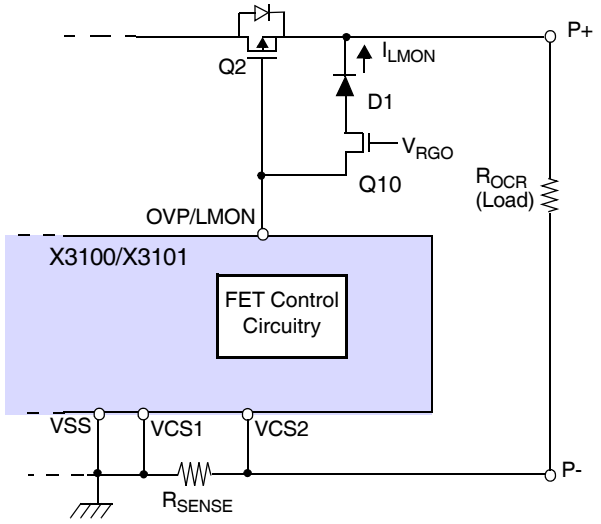
Table 22. Over-discharge Protection Mode—Event Diagram Description (Continued)

Event	Event Description	
[3]	Return from sleep mode (but still in over-discharge protection mode): — Vcc rises above the “Return from Sleep mode threshold Voltage” (V_{SLR})—This would normally occur in the case that the battery pack was connected to a charger. The X3100/X3101 is now powered via P+/P-, and not the battery pack cells. — Power is returned to ALL internal circuitry — 5VDC output is returned to the regulator output (RGO). — Access is enabled to the X3100/X3101 via the SPI port. — The status of the discharge FET remains OFF (It is possible to change the status of UVPC in the control register, although it will have no effect at this time).	
(3,4)	If the cell charge enable function is switched ON AND $V_{CELL} > V_{CE}$ OR Charge enable function is switched OFF	— The X3100/X3101 initiates a reset operation that takes the longer of T_{OV+} 200ms or T_{UV} + 200ms to complete. Do not write to the FET control bits during this time. — The charge FET is switched On (OVP/LMON = Vss) by the microcontroller by writing a “1” to the OVPC bit in the control register. — The battery cells now receive charge via the charge FET and diode D1 across the discharge FET (which is OFF). — The X3100/X3101 monitors the V_{CELL} voltage to determine whether or not it has risen above V_{UVR}.
	If the cell charge enable function is switched ON **AND** $V_{CELL} < V_{CE}$	— Charge/discharge of the battery cells via P+ is no longer permitted (Charge FET and discharge FET are held OFF). — (Charging may re-commence only when the Cell Charge Enable function is switched OFF - See Sections: “Configuration Register” page 4, and “Sleep mode” page 17.)
[4]	— The voltage of all of the battery cells (V_{CELL}), have risen above V_{UVR}. — The internal Over-discharge release timer begins counting down. — The X3100/X3101 is still in over-discharge protection mode.	
(4,5)	— The internal over-discharge release timer continues counting for t_{UVR} seconds. — The X3100/X3101 should be in monitor mode (AS2:AS0 not all low) for recovery time based on t_{UVR}. Otherwise recovery is based on two successive samples about 120ms apart.	
[5]	— The internal over-discharge release timer times out, AND V_{CELL} is still above $V_{UVR.}$ — The device returns from over-discharge protection mode, and is now in normal operation mode. — The Charger voltage can now drop below VSLR and the X3100/X3101 will not go back to sleep. — The discharge FET is can now be switched ON (UVP/OCP = V_{SS}) by the microcontroller by writing a “1” to the UVPC bit of the control register. — The status of the charge FET remains unaffected (ON) — The battery cells continue to receive charge via the charge FET and discharge FET (both ON).	

Over-Current Protection

In addition to monitoring the battery cell voltages, the X3100 and X3101 continually monitor the voltage VCS_{21} (VCS_2 - VCS_1) across the current sense resistor (R_{SENSE}). If VCS_{21} > V_{OC} for a time exceeding T_{OC}, then the device enters over-current protection mode (Figure 7). In this mode, the X3100 and X3101 automatically switch the discharge FET OFF (UVP/OCP = Vcc) and hence prevent current from flowing through the terminals P+ and P-.

Figure 5. Over-Current Protection



The 5VDC voltage regulator output (V_{RGO}) is always active during an over-current protection mode.

Once the device enters over-current protection mode, the X3100 and X3101 begin a load monitor state. In the load monitor state, a small current (I_{LMON} = 7.5µA typ.) is passed out of pin OVP/LMON in order to determine the load resistance. The load resistance is the impedance seen looking out of pin OVP/LMON, between terminal P+ and pin VSS (See Figure 5.)

If the load resistance > R_{OCR} (I_{LMON} = 0µA) for a time exceeding T_{OCR}, then the X3100 or X3101 is released from over-current protection mode. The discharge FET is then automatically switched ON (UVP/OCP = Vss) by the X3100 or X3101, unless the status of UVP/OCP has been changed in control register (by manipulating bit UVPC) during the over-current protection mode.

T_{OC}/T_{OCR} are varied using a capacitor (C_{OC}) connected between pin OCT and VSS. A list of typical delay times is shown in Table 23. Note that the value C_{OC} should be larger than 1nF.

The delay T_{OC} and T_{OCR} that results from a particular capacitance C_{OC} can be approximated by the following equations:

$$T_{OC}\ (ms) \approx 10{,}000 \times C_{OC}\ (\mu F)$$

$$T_{OCR}\ (ms) \approx 10{,}000 \times C_{OC}\ (\mu F)$$

Table 23. Typical Over-Current Delay Times

Symbol	Description	C_{OC}	Delay
T_{OC}	Over-current detection delay	0.001µF	10ms (Typ)
T_{OCR}	Over-current release time	0.001µF	10ms (Typ)

The value of V_{OC} can be selected from the values shown in Table 6, by setting bits VOC1, VOC0 in the configuration register using the WCFIG command.

Note: If the Charge FET is turned off, due to an overcharge condition or by direct command from the microcontroller, the cells are not in an undervoltage condition and the pack has a load, then excessive current may flow through Q10 and diode D1. To eliminate this effect, the gate of Q10 can be turned off by the microcontroller through an unused X3101 cell balance output, or directly from a microcontroller port instead of connecting to V_{RGO}.

Figure 6. Over-Current Protection Mode—Event Diagram

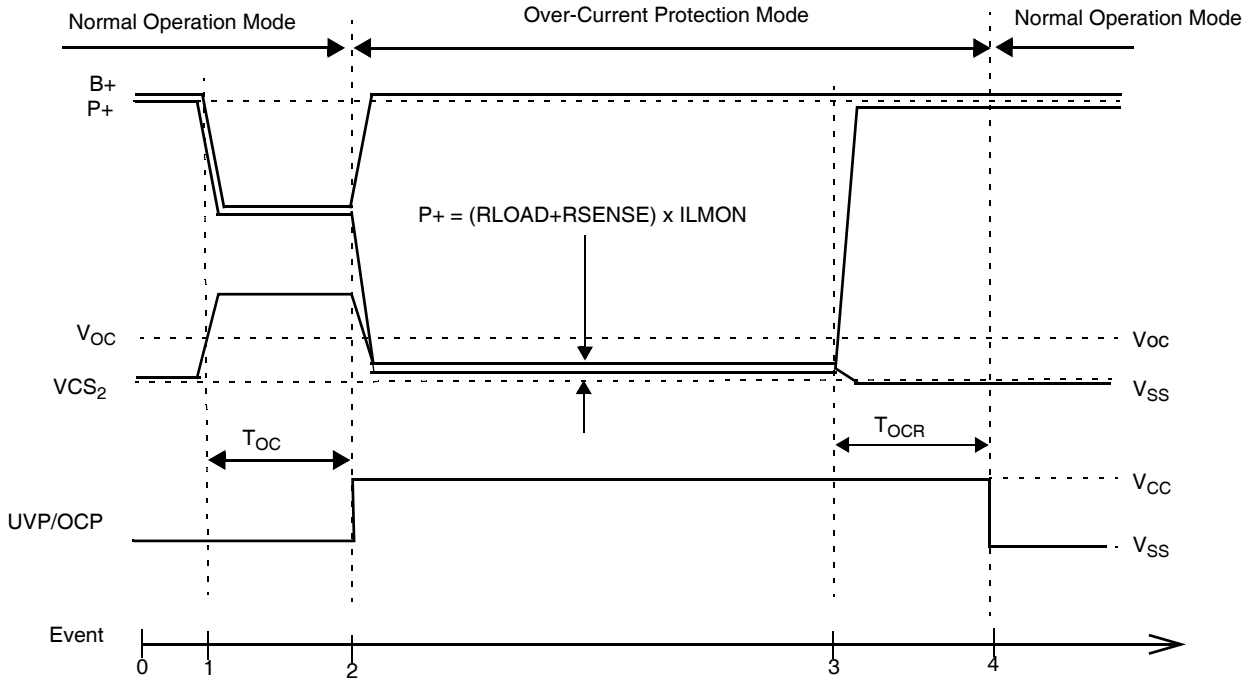


Table 24. Over-Current Protection Mode—Event Diagram Description

Event	Event Description
[0,1)	—Discharge FET is ON (OCP = Vss). Battery cells are permitted to discharge. —VCS_{21} (VCS_2 - VCS_1) is less than the over-current threshold voltage (V_{OC}). —The device is in normal operation mode (i.e. not in a protection mode).
[1]	—Excessive current flows through the battery terminals P+, dropping the voltage. (See Figure 6.). —The positive battery terminal voltage (P+) falls, and VCS_{21} exceeds V_{OC}. —The internal over-current detection delay timer begins counting down. —The device is still in Normal Operation Mode
(1,2)	The internal Over-current detection delay timer continues counting for T_{OC} seconds.
[2]	—The internal over-current detection delay timer times out, AND VCS_{21} is still above $V_{OC.}$ —The internal over-current sense circuitry switches the discharge FET OFF (UVP/OCP = Vcc). —The device now begins a load monitor state by passing a small test current (I_{LMON} = 7.5µA) out of pin OVP/LMON. This senses if an over-current condition (i.e. if the load resistance < R_{OCR}) still exists across P+/P-. —The device has now entered over-current protection mode. —It is possible to change the status of UVPC and OVPC in the control register, although the status of pins UVP/OCP and OVP/LMON will not change until the device has returned from over-current protection mode.
(2,3)	—The X3100/X3101 now continuously monitors the load resistance to detect whether or not an over-current condition is still present across the battery terminals P+/P-.

Table 24. Over-Current Protection Mode—Event Diagram Description (Continued)

Event	Event Description
[3]	—The device detects the load resistance has risen above R_{OCR}. —Voltages P+ and VCS_{21} return to their normal levels. —The test current from pin OVP/LMON is stopped (I_{LMON} = 0µA) —The device has now returned from the load monitor state —The internal over-current release time timer begins counting down. —Device is still in over-current protection mode.
(3,4)	The internal over-current release timer continues counting for T_{OCR} seconds.
[4]	—The internal over-current release timer times out, and VCS_{21} is still below $V_{OC.}$ —The device returns from over-current protection mode, and is now in normal operation mode. —The discharge FET is automatically switched ON (UVP/OCP = Vss)—unless the status of UVPC has been changed in the control register during the over-current protection mode. —The status of the charge FET remains unaffected. —Discharge of the battery cells is once again possible.

MONITOR MODE

Analog Multiplexer Selection

The X3100 and X3101 can be used to externally monitor individual battery cell voltages, and battery current. Each quantity can be monitored at the analog output pin (AO), and is selected using the analog select (AS0 - AS2) pins (Table 25). Also, see Figure 7.

Table 25. AO Selection Map

AS2	AS1	AS0	AO output
L	L	L	V_{SS}(1)
L	L	H	$VCELL_1$ - $VCELL_2$ ($VCELL_{12}$)
L	H	L	$VCELL_2$ - $VCELL_3$ ($VCELL_{23}$)
L	H	H	$VCELL_3$ - $VCELL_4$ ($VCELL_{34}$)
H	L	L	$VCELL_4$ - Vss ($VCELL_4$)
H	L	H	VCS_1 - VCS_2 (VCS_{12})(2)
H	H	L	VCS2 - VCS_1 (VCS_{21})(2)
H	H	H	V_{SS}

Notes: (1) This is the normal state of the X3100 or X3101. While in this state Over-charge and Over-discharge Protection conditions are periodically monitored (See "Periodic Protection Monitoring" on page 13.)

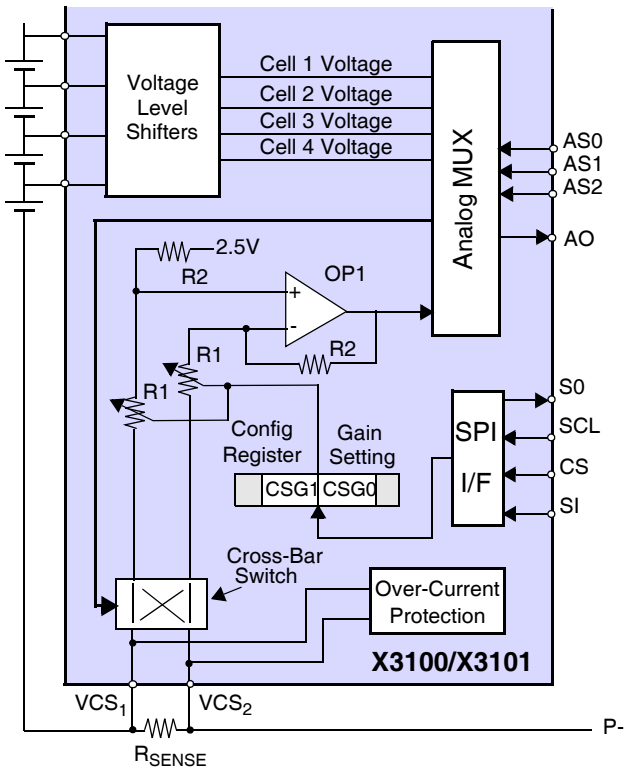
(2) VCS_1, VCS_2 are read at AO with respect to a DC bias voltage of 2.5V (See section "Current Monitor Function" on page 21).

Current Monitor Function

The voltages monitored at pins VCS_1 and VCS_2 can be used to calculate current flowing through the battery terminals, using an off-board microcontroller with an A/D.

Since the value of the sense resistor (R_{SENSE}) is small (typically in the order of tens of mΩ), and since the resolution of various A/D converters may vary, the voltage across R_{SENSE} (VCS_1 and VCS_2) is amplified internally with a gain of between 10 and 160, and output to pin AO (Figure 7).

Figure 7. X3100/X3101 Monitor Circuit



The internal gain of the X3100 or X3101 current sense voltage amplifier can be selected by using the WCNTR Instruction to set bits CSG1 and CSG0 in the control register (Table 14). The CSG1 and CSG0 bits select one of four input resistors to Op Amp OP1. The feedback resistors remain constant. This ratio of input to feedback resistors determines the gain. Putting external resistors in series with the inputs reduces the gain of the amplifier.

VCS1 and VCS2 are read at AO with respect to a DC bias voltage of 2.5V. Therefore, the voltage range of VCS_{12} and VCS_{21} changes depending upon the direction of current flow (i.e. battery cells are in Charge or Discharge—Table 21).

Table 26. AO Voltage Range for VCS_{12} and VCS_{21}

AO	Cell State	AO Voltage Range
VCS_{12}	Charge	$2.5V \leq AO \leq 5.0V$
VCS_{12}	Discharge	$0V \leq AO \leq 2.5V$
VCS_{21}	Charge	$0V \leq AO \leq 2.5V$
VCS_{21}	Discharge	$2.5V \leq AO \leq 5.0V$

By calculating the difference of VCS_{12} and VCS_{21} the offset voltage of the internal op-amp circuitry is cancelled. This allows for the accurate calculation of current flow into and out of the battery cells.

Pack current is calculated using the following formula:

$$\text{Pack Current} = \frac{(VCS_{12} - VCS_{21})}{(2)(\text{gain setting})(\text{current sense resistor})}$$

VOLTAGE REGULATOR

The X3100 and X3101 are able to supply peripheral devices with a regulated 5VDC±0.5% output at pin RGO. The voltage regulator should be configured externally as shown in Figure 8.

The non-inverting input of OP1 is fed with a high precision 5VDC supply. The voltage at the output of the voltage regulator (V_{RGO}) is compared to this 5V reference via the inverting input of OP1. The output of OP1 in turn drives the regulator pnp transistor (Q1). The negative feedback at the regulator output maintains the voltage at 5VDC±0.5% (including ripple) despite changes in load, and differences in regulator transistors.

When power is applied to pin VCC of the X3100 or X3101, V_{RGO} is regulated to 5VDC±10% for a nominal time of T_{OC}+2ms. During this time period, V_{RGO} is "tuned" to attain a final value of 5VDC±0.5% (Figure).

The maximum current that can flow from the voltage regulator (I_{LMT}) is controlled by the current limiting resistor (R_{LMT}) connected between RGP and VCC. When the voltage across VCC and RGP reaches a nominal 2.5V (i.e. the threshold voltage for the FET), Q2 switches ON, shorting VCC to the base of Q1. Since the base voltage of Q1 is now higher than the emitter voltage, Q1 switches OFF, and hence the supply current goes to zero.

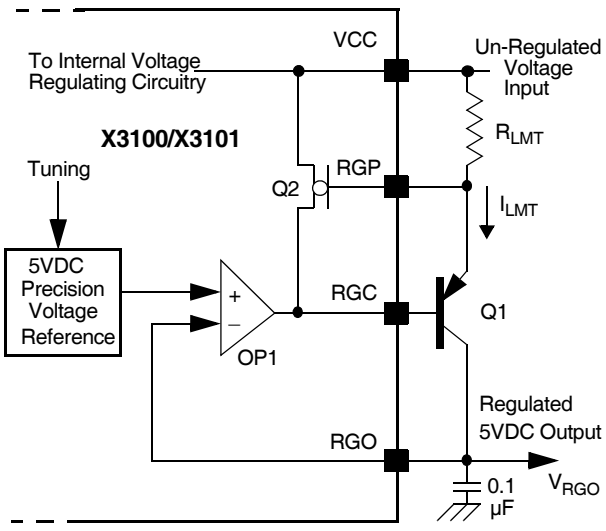
Typical values for R_{LMT} and I_{LMT} are shown in Table 27. In order to protect the voltage regulator circuitry from damage in case of a short-circuit, $R_{LMT} \geq 10\Omega$ should always be used.

Table 27. Typical Values for R_{LMT} and I_{LMT}

R_{LMT}	Voltage Regulator Current Limit (I_{LMT})
10Ω	250mA ± 50% (Typical)
25Ω	100mA ± 50% (Typical)
50Ω	50mA ± 50% (Typical)

When choosing the value of R_{LMT}, the drive limitations of the PNP transistor used should also be taken into consideration. The transistor should have a gain of at least 100 to support an output current of 250mA.

Figure 8. Voltage Regulator Operation



4KBIT EEPROM MEMORY

The X3100 and X3101 contain a CMOS 4k-bit serial EEPROM, internally organized as 512 x 8 bits. This memory is accessible via the SPI port, and features the IDLock function.

The 4kbit EEPROM array can be accessed by the SPI port at any time, even during a protection mode, except during sleep mode. After power is applied to VCC of the X3100 or X3101, EEREAD and EEWRITE Instructions can be executed only after times t_{PUR} (power-up to read time) and t_{PUW} (power-up to write time) respectively.

IDLock is a programmable locking mechanism which allows the user to lock data in different portions of the EEPROM memory space, ranging from as little as one page to as much as 1/2 of the total array. This is useful for storing information such as battery pack serial number, manufacturing codes, battery cell chemistry data, or cell characteristics.

EEPROM Write Enable Latch

The X3100 and X3101 contain an EEPROM "Write Enable" latch. This latch must be SET before a write to EEPROM operation is initiated. The WREN instruction will set the latch and the WRDI instruction will reset the latch (Figure 9). This latch is automatically reset upon a power-up condition and after the completion of a byte or page write cycle.

IDLock Memory

Intersil's IDLock memory provides a flexible mechanism to store and lock battery cell/pack information. There are seven distinct IDLock memory areas within the array which vary in size from one page to as much as half of the entire array.

Prior to any attempt to perform an IDLock operation, the WREN instruction must first be issued. This instruction sets the "Write Enable" latch and allows the part to respond to an IDLock sequence. The EEPROM memory may then be IDLocked by writing the SET IDL instruction (Table 30 and Figure 17), followed by the IDLock protection byte.

Table 28. IDLock Partition Byte Definition

IDLock Protection Bytes	EEPROM Memory Address IDLocked
0000 0000	None
0000 0001	000h - 07Fh
0000 0010	080h - 0FFh
0000 0011	100h - 17Fh
0000 0100	180h - 1FFh
0000 0101	000h - 0FFh
0000 0110	000h - 00Fh
0000 0111	1F0h - 1FFh

The IDLock protection byte contains the IDLock bits IDL2-IDL0, which defines the particular partition to be locked (Table 28). The rest of the bits [7:3] are unused and must be written as zeroes. Bringing $\overline{CS}$ HIGH after the two byte IDLock instruction initiates a nonvolatile write to the status register. Writing more than one byte to the status register will overwrite the previously written IDLock byte.

Once an IDLock instruction has been completed, that IDLock setup is held in a nonvolatile IDLock Register (Table 29) until the next IDLock instruction is issued. The sections of the memory array that are IDLocked can be read but not written until IDLock is removed or changed.

Table 29. IDLock Register

7	6	5	4	3	2	1	0
0	0	0	0	0	IDL2	IDL1	IDL0

Note: Bits [7:3] specified to be "0's"

X3100/X3101 SPI SERIAL COMMUNICATION

The X3100 and X3101 are designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of many popular microcontroller families. This interface uses four signals, $\overline{CS}$, SCK, SI and SO. The signal $\overline{CS}$ when low, enables communications with the device. The SI pin carries the input signal and SO provides the output signal. SCK clocks data in or out. The X3100 and X3101 operate in SPI mode 0 which requires SCK to be normally low when not transferring data. It also specifies that the rising edge of SCK clocks data into the device, while the falling edge of SCK clocks data out.

This SPI port is used to set the various internal registers, write to the EEPROM array, and select various device functions.

The X3100 and X3101 contain an 8-bit instruction register. It is accessed by clocking data into the SI input. $\overline{CS}$ must be LOW during the entire operation. Table 30 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock, and then start it again to resume operations where left off.

Table 30. X3100/X3101 Instruction Set

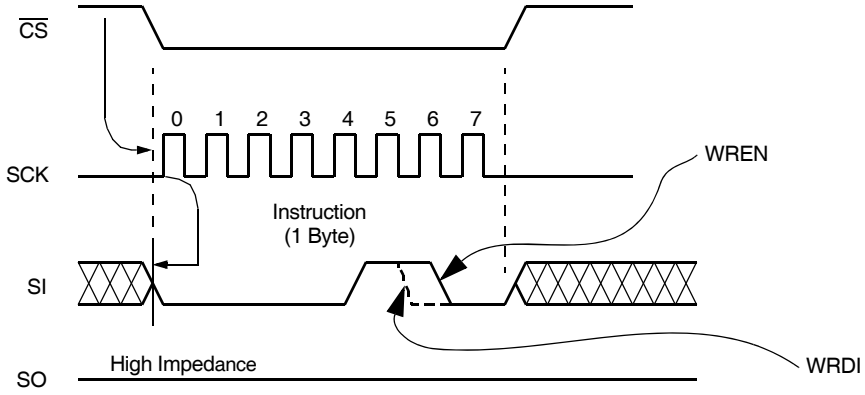
Instruction Name	Instruction Format*	Description
WREN	0000 0110	Set the write enable latch (write enable operation)—Figure 9
WRDI	0000 0100	Reset the write enable latch (write disable operation)—Figure 9
EEWRITE	0000 0010	Write command followed by address/data (4kbit EEPROM)—Figure 10, Figure 11
EEREAD STAT	0000 0101	Reads IDLock settings & status of EEPROM EEWRITE instruction—Figure 12
EEREAD	0000 0011	Read operation followed by address (for 4kbit EEPROM)—Figure 13
WCFIG	0000 1001	Write to configuration register followed by two bytes of data—Figure 2, Figure 14. Data stored in SRAM only and will power-up to previous settings—Figure 1
WCNTR	0000 1010	Write to control register, followed by two bytes of data—Figure 15
RDSTAT	0000 1011	Read contents of status register—Figure 16
SET IDL	0000 0001	Set EEPROM ID lock partition followed by partition byte—Figure 17

*Instructions have the MSB in leftmost position and are transferred MSB first.

Write Enable/Write Disable (WREN/WRDI)

Any write to a nonvolatile array or register, requires the WREN command be sent prior to the write command. This command sets an internal latch allowing the write operation to proceed. The WRDI command resets the internal latch if the system decides to abort a write operation. See Figure 9.

Figure 9. EEPROM Write Enable Latch (WREN/WRDI) Operation Sequence



EEPROM Write Sequence (EEWRITE)

Prior to any attempt to write data into the EEPROM of the X3100 or X3101, the “Write Enable” latch must first be set by issuing the WREN instruction (See Table 30 and Figure 9). $\overline{CS}$ is first taken LOW. Then the WREN instruction is clocked into the X3100 or X3101. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the write operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the write operation will be ignored.

To write data to the EEPROM memory array, the user issues the EEWRITE instruction, followed by the 16 bit address and the data to be written. Only the last 9 bits of the address are used and bits [15:9] are specified to be zeroes. This is minimally a thirty-two clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The host may continue to write up to 16 bytes of data to the X3100 or X3101. The only restriction is the 16 bytes must reside on the same page. If the address counter reaches the end of the page and the clock continues, the counter will “roll over” to the first address of the page and overwrite any data that may have been previously written.

For a byte or page write operation to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of the last data byte to be written is clocked in. If it is brought HIGH at any other time, the write operation will not be completed. Refer to Figure 10 and Figure 11 for detailed illustration of the write sequences and time frames in which $\overline{CS}$ going HIGH are valid.

EEPROM Read Status Operation (EEREAD STAT)

If there is not a nonvolatile write in progress, the EEREAD STAT instruction returns the IDLock byte from the IDLock register which contains the IDLock bits IDL2-IDL0 (Table 29). The IDLock bits define the IDLock condition (Table 28). The other bits are reserved and will return ‘0’ when read.

If a nonvolatile write to the EEPROM (i.e. EEWRITE instruction) is in progress, the EEREAD STAT returns a HIGH on SO. When the nonvolatile write cycle in the EEPROM is completed, the status register data is read out.

Clocking SCK is valid during a nonvolatile write in progress, but is not necessary. If the SCK line is clocked, the pointer to the status register is also clocked, even though the SO pin shows the status of the nonvolatile write operation (See Figure 12).

Figure 10. EEPROM Byte Write (EEWRITE) Operation Sequence

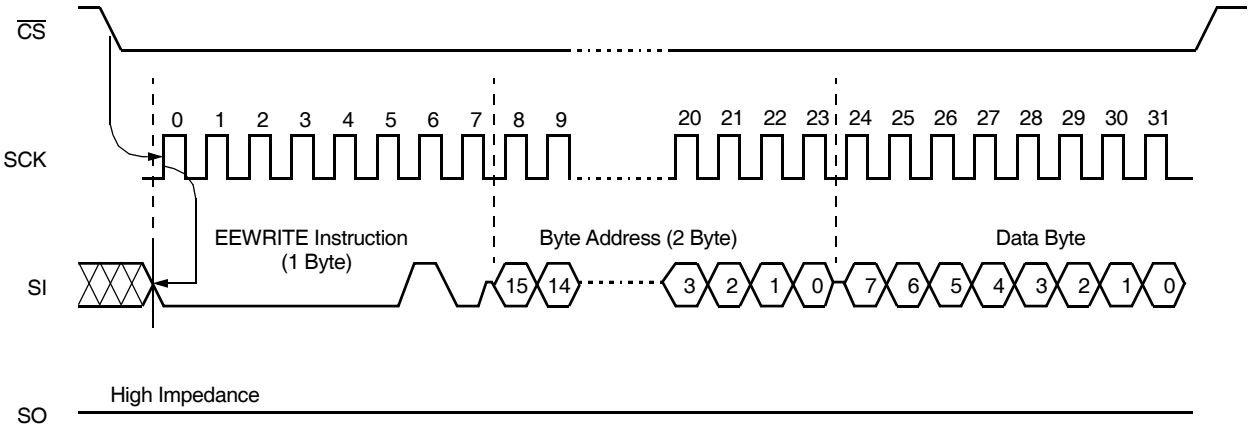


Figure 11. EEPROM Page Write (EEWRITE) Operation Sequence

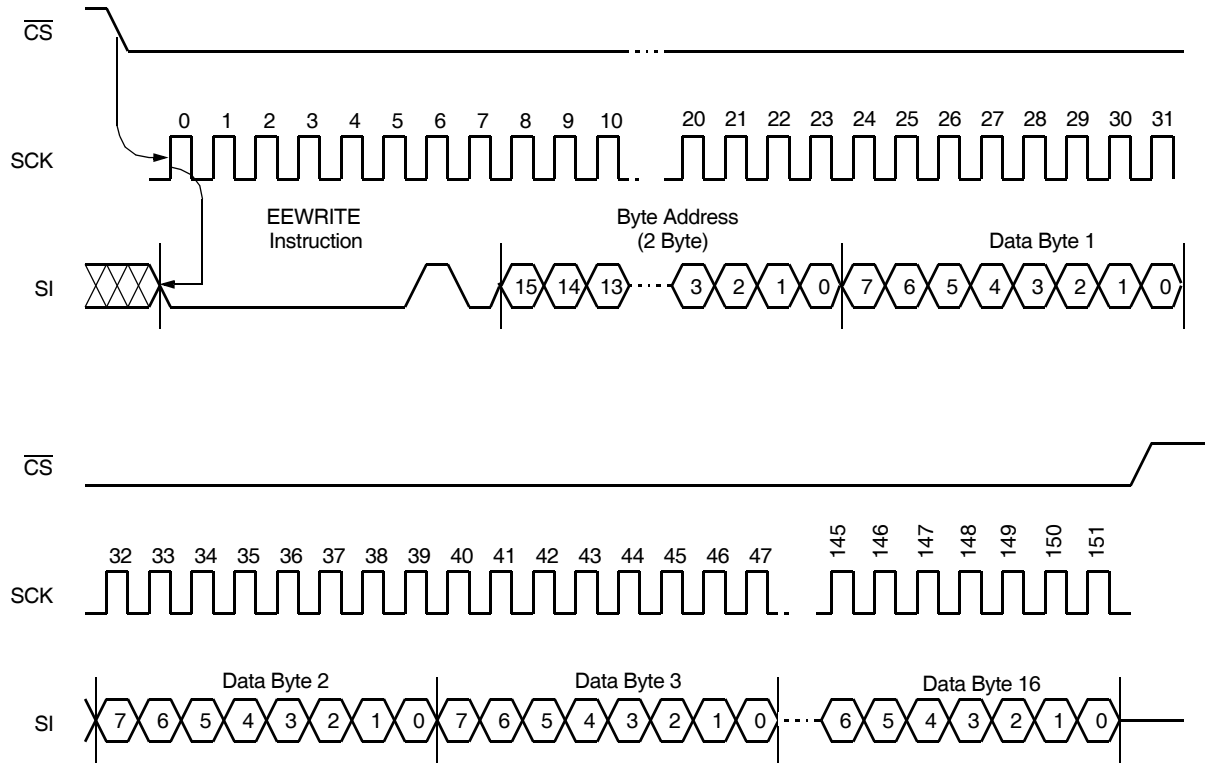
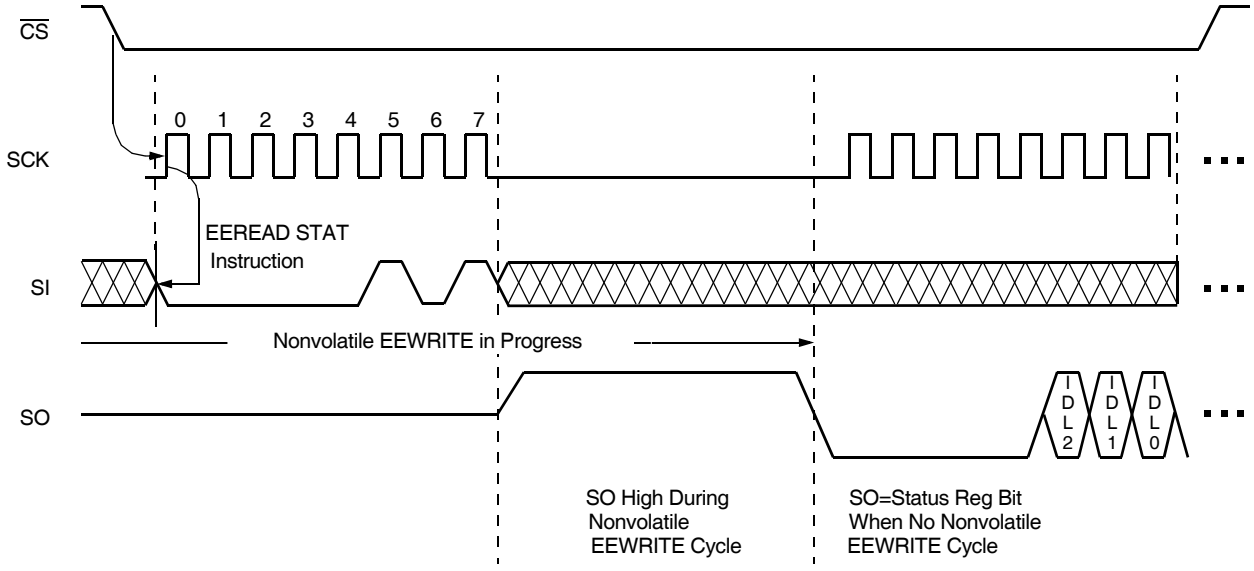


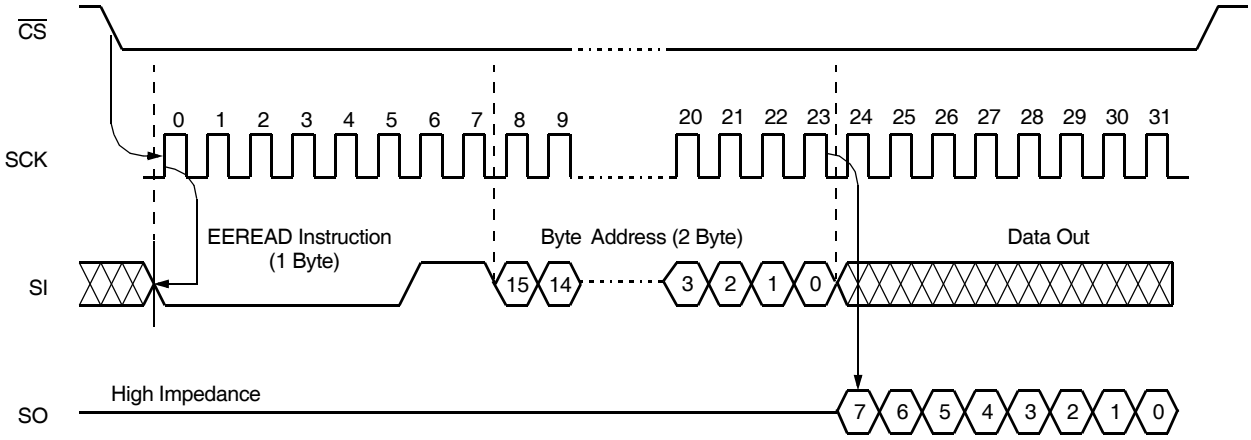
Figure 12. EEPROM Read Status (EEREAD STAT) Operation Sequence



EEPROM Read Sequence (EEREAD)

When reading from the X3100 or X3101 EEPROM memory, $\overline{CS}$ is first pulled LOW to select the device. The 8-bit EEREAD instruction is transmitted to the X3100 or X3101, followed by the 16-bit address, of which the last 9 bits are used (bits [15:9] specified to be zeroes). After the EEREAD opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (01FFh), the address counter rolls over to address 0000h, allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH. Refer to the EEPROM Read (EEREAD) operation sequence illustrated in Figure 13.

Figure 13. EEPROM (EEREAD) Read Operation Sequence



Write Configuration Register (WCFIG)

The Write Configuration Register (WCFIG) instruction updates the static part of the Configuration Register. These new values take effect immediately, for example writing a new Over-discharge voltage limit. However, to make these changes permanent, so they remain if the cell voltages are removed, an EEWRITE operation to the EEPROM array is required following the WCFIG command. This command is shown in Figure 14.

Write Control Register (WCNTRL)

The Write Control Register (WCNTRL) instruction updates the contents of the volatile Control Register. This command sets the status of the FET control pins, the cell balancing outputs, the current sense gain and external entry to the sleep mode. Since this instruction controls a volatile register, no other commands are required and there is no delay time needed after the instruction, before subsequent commands. The operation of the WCNTRL command is shown in Figure 15.

Figure 14. Write Configuration Register (WCFIG) Operation Sequence

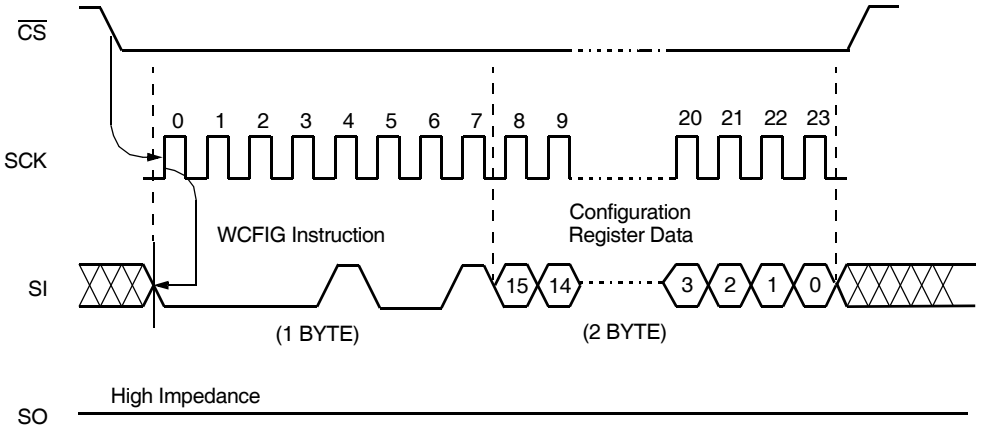
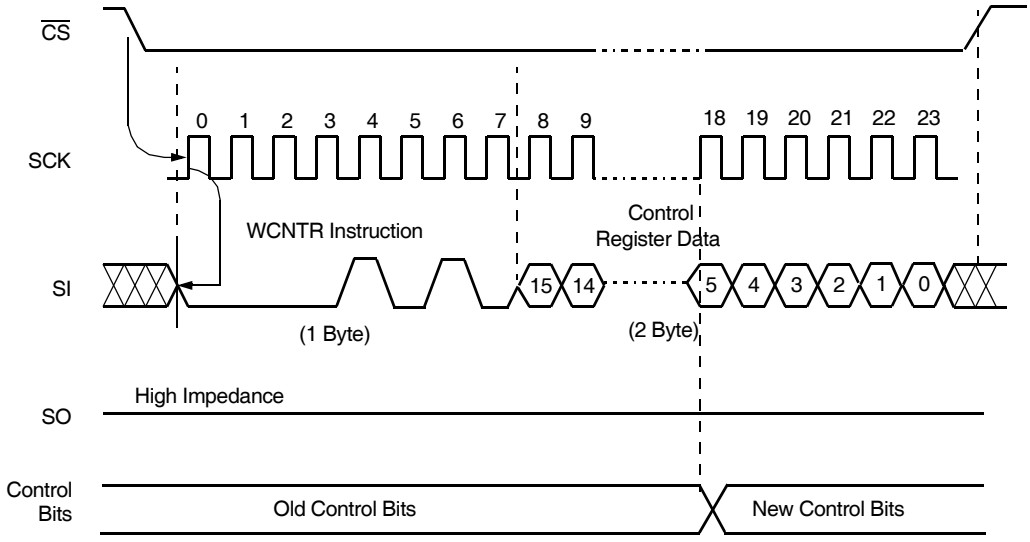


Figure 15. Write Control Register (WCNTR) Operation Sequence



Read Status Register (RDSTAT)

The Read Status Register (RDSTAT) command returns the status of the X3100 or X3101. The Status Register contains three bits that indicate whether the voltage regulator is stabilized, and if there are any protection failure conditions. The operation of the RDSTAT instruction is shown in Figure 16.

Set ID Lock (SET IDL)

The contents of the EEPROM memory array in the X3100 or X3101 can be locked in one of eight configurations using the SET ID lock command. When a section of the EEPROM array is locked, the contents cannot be changed, even when a valid write operation attempts a write to that area. The SET IDL command operation is shown in Figure 17.

Figure 16. Read Status Register (RDSTAT) Operation Sequence

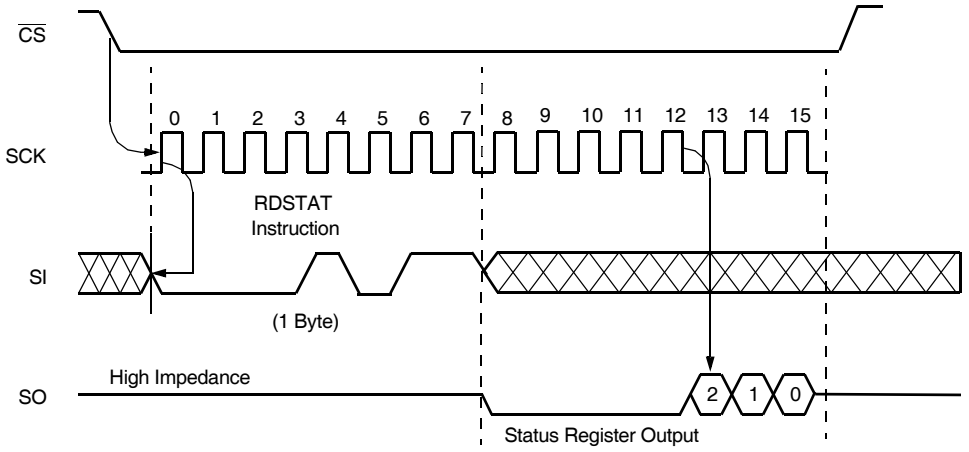
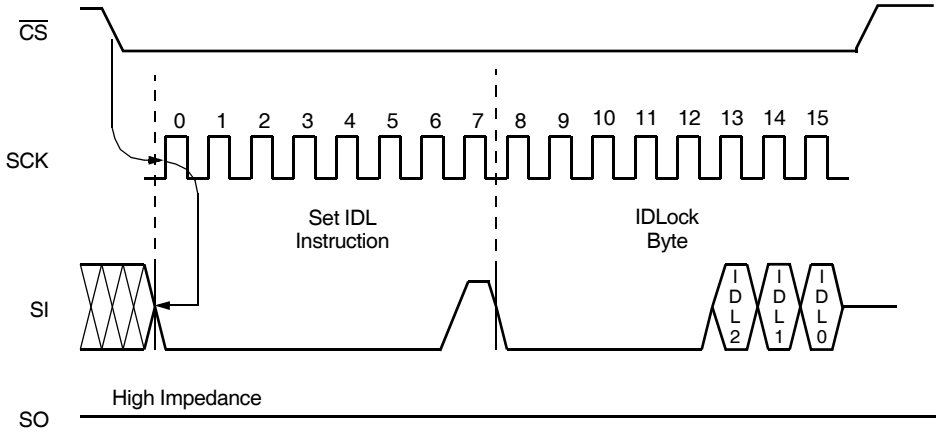


Figure 17. EEPROM IDLock (SET IDL) Operation Sequence



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
	Storage temperature	-55	125	°C
	Operating temperature	-40	85	°C
	DC output current		5	mA
	Lead temperature (soldering 10 seconds)		300	°C
VCC	Power supply voltage	V_{SS}-0.5	V_{SS}+27.0	V
VCELL	Cell voltage	-0.5	6.75	V
V_{TERM1}	Terminal voltage (Pins: SCK, SI, SO, CS, AS0, AS1, AS2, VCS1, VCS2, OVT, UVT, OCT, AO)	V_{SS}-0.5	V_{RGO} + 0.5	V
V_{TERM2}	Terminal voltage (VCELL1)	V_{SS}-0.5	V_{CC} + 1.0	V
V_{TERM3}	Terminal voltage (all other pins)	V_{SS}-0.5	V_{CC} + 0.5	V

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those indicated in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	-20°C	+70°C

Supply Voltage	Limits
X3100/X3101	6V to 24V

D.C. OPERATING CHARACTERISTICS

(Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{LI}	Input leakage current (SCK, SI, $\overline{CS}$, ASO, AS1, AS2)		±10	µA	
I_{LO}	Output leakage current (SO)		±10	µA	
V_{IL}(1)	Input LOW voltage (SCK, SI, $\overline{CS}$, AS0, AS1, AS2)	- 0.3	V_{RGO} x 0.3	V	
V_{IH}(1)	Input HIGH voltage (SCK, SI, $\overline{CS}$, AS0, AS1, AS2)	V_{RGO} x 0.7	V_{RGO} + 0.3	V	
VOL1	Output LOW voltage (SO)		0.4	V	I_{OL} = 1.0mA
VOH1	Output HIGH voltage (SO)	V_{RGO} - 0.8		V	I_{OH} = -0.4mA
VOL2	Output LOW voltage (UVP/OCP, OVP/LMON, CB1-CB4)		0.4	V	I_{OL} = 100uA
VOH2	Output HIGH voltage (UVP/OCP, OVP/LMON, CB1-CB4)	V_{CC}-0.4		V	I_{OH} = -20uA
VOL3	Output LOW voltage (RGC)		0.4	V	I_{OL} = 2mA, RGP = V_{CC}, RGO = 5V
VOH3	Output HIGH voltage (RGC)	V_{CC}-4.0		V	I_{OH} = -20µA, RGP = V_{CC} - 4V, RGO = 5V

Note: (1) V_{IL} min. and V_{IH} max. are for reference only and are not 100% tested.

OPERATING CHARACTERISTICS X3100

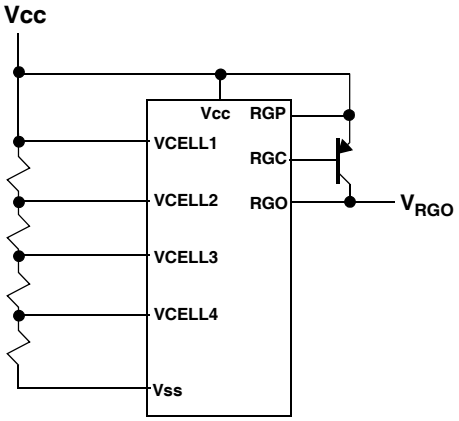
(Over the recommended operating conditions unless otherwise specified)

Description	Sym	Condition	Min	Typ(2)	Max	Unit
5V regulated voltage	V_{RGO}	On power-up or at wake-up	4.5		5.5	V
		After self-tuning (@10mA V_{RGO} current; 25ºC)	4.98	4.99	5.00	
		After self-tuning (@10mA V_{RGO} current; 0 - 50ºC)(5)	4.95		5.02	
		After self-tuning (@50mA V_{RGO} current)(5)	4.90		5.00	V
5VDC voltage regulator current limit	I_{LMT}(3)	R_{LMT} = 10Ω		250		mA
V_{CC} supply current (1)	Icc1	Normal operation		85	250	µA
V_{CC} supply current (2)	Icc2	during nonvolatile EEPROM write		1.3	2.5	mA
V_{CC} supply current (3)	Icc3	During EEPROM read SCK=3.3MHz		0.9	1.2	mA
V_{CC} supply current (4)	Icc4	Sleep mode			1	µA
V_{CC} supply current (5)	Icc5	Monitor mode AN2, AN1, AN0 not equal to 0.		365	600	µA
Cell over-charge protection mode voltage threshold (Default in Boldface)	V_{OV}(4)	**V_{OV} = 4.20V (VOV1, VOV0 = 0,0)** 0ºC to 50ºC	**4.10** **4.15**		**4.275** **4.25**	**V**
		V_{OV} = 4.25V (VOV1, VOV0 = 0,1) 0ºC to 50ºC	4.15 4.20		4.325 4.30	V
		V_{OV} = 4.30V (VOV1, VOV0 = 1,0) 0ºC to 50ºC	4.2 4.25		4.375 4.35	V
		V_{OV} = 4.35V (VOV1, VOV0 = 1,1) 0ºC to 50ºC	4.25 4.30		4.425 4.40	V
Cell over-charge protection mode release voltage threshold	V_{OVR}			V_{OV} - 0.20		V
Cell over-charge detection time	T_{OV}	C_{OV} = 0.1uF		1		s
Cell over-discharge protection mode (SLEEP) threshold. (Default in Boldface)	V_{UV}(4)	V_{UV} = 1.95V (VUV1, VUV0 = 0,0)	1.85		2.05	V
		V_{UV} = 2.05V (VUV1, VUV0 = 0,1)	1.95		2.15	V
		V_{UV} = 2.15V (VUV1, VUV0 = 1,0)	2.05		2.25	V
		V_{UV} = 2.25V (VUV1, VUV0 = 1,1)	**2.15**		**2.35**	**V**
Cell over-discharge protection mode release threshold	V_{UVR}			V_{UV} + 0.7		V
Cell over-discharge detection time	T_{UV}	C_{UV} = 0.1µF C_{UV} = 200pF		1 2		s ms
Cell over-discharge release time	T_{UVR}	C_{UV} = 0.1µF C_{UV} = 200pF		7 100		ms µs

Description	Sym	Condition	Min	Typ(2)	Max	Unit
Over-current mode detection voltage (Default in Boldface)	V_{OC}(4)	**V_{OC} = 0.075V (VOC1, VOC0 = 0,0)**	**0.050**		**0.100**	**V**
		0°C to 50°C	**0.060**		**0.090**	
		V_{OC} = 0.100V (VOC1, VOC0 = 0,1)	0.075		0.125	V
		0°C to 50°C	0.085		0.115	
		V_{OC} = 0.125V (VOC1, VOC0 = 1,0)	0.100		0.150	V
		0°C to 50°C	0.110		0.140	
		V_{OC} = 0.150V (VOC1, VOC0 = 1,1)	0.125		0.175	V
		0°C to 50°C	0.135		0.165	
Over-current mode detection time	T_{OC}	C_{OC} = 0.001µF		10		ms
		C_{OC} = 200pF		2		
Over-current mode release time	T_{OCR}	C_{OC} = 0.001µF		10		ms
		C_{OC} = 200pF		2		
Load resistance over-current mode release condition	R_{OCR}	Releases when OVP/LMON pin > 2.5V		250		kΩ
Cell charge threshold voltage	V_{CE}(4)	V_{CE} = 0.5V (Vce1, Vce0 = 0,0)	0.4	0.5	0.6	V
		V_{CE} = 0.8V (Vce1, Vce0 = 0,1)	0.7	0.8	0.9	V
		V_{CE} = 1.1V (Vce1, Vce0 = 1,0)	1	1.1	1.2	V
		V_{CE} = 1.4V (Vce1, Vce0 = 1,1)	1.3	1.4	1.5	V
X3100 wake-up voltage (For Vcc above this voltage, the device wakes up)	V_{SLR}	See Wake-up test circuit	12.5		15.5	V
X3100 sleep voltage (For Vcc above this voltage, the device cannot go to sleep)	V_{SLP}	See Sleep test circuit	11.5		14.5	V

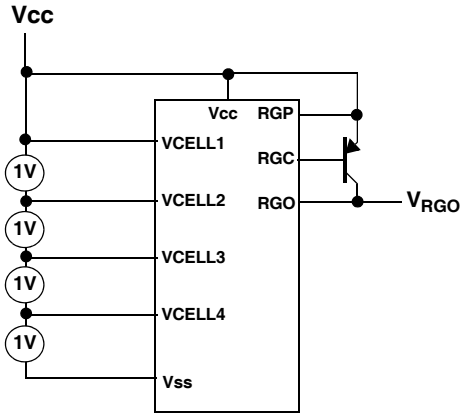
Notes: (2) Typical at 25°C.
(3) See Figure 10 on page 22.
(4) The default setting is set at the time of shipping, but may be changed by the user via changes in the configuration register.
(5) For reference only, this parameter is not 100% tested.

Wake-up test circuit (X3100)



Increase Vcc until V_{RGO} turns on

Sleep test circuit (X3100)



Decrease Vcc until V_{RGO} turns off

OPERATING CHARACTERISTICS X3101

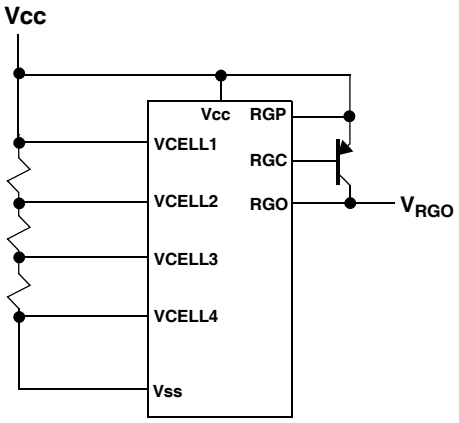
(Over the recommended operating conditions unless otherwise specified)

Description	Sym	Condition	Min	Typ(2)	Max	Unit
5V regulated voltage	V_{RGO}	On power-up or at wake-up	4.5		5.5	V
		After self-tuning (@10mA V_{RGO} current; 25ºC)	4.98	4.99	5.00	
		After self-tuning (@10mA V_{RGO} current; 0 - 50ºC)(5)	4.95		5.02	
		After self-tuning (@50mA V_{RGO} current)(5)	4.90		5.00	V
5VDC voltage regulator current limit	I_{LMT}(3)	R_{LMT} = 10Ω		250		mA
V_{CC} supply current (1)	Icc1	Normal operation		85	250	µA
V_{CC} supply current (2)	Icc2	during nonvolatile EEPROM write		1.3	2.5	mA
V_{CC} supply current (3)	Icc3	During EEPROM read SCK = 3.3MHz		0.9	1.2	mA
V_{CC} supply current (4)	Icc4	Sleep mode			1	µA
V_{CC} supply current (5)	Icc5	Monitor mode AN2, AN1, AN0 not equal to 0.		365	600	µA
Cell over-charge protection mode voltage threshold (Default in Boldface)	V_{OV}(4)	**V_{OV} = 4.20V (VOV1, VOV0 = 0,0)** **0ºC to 50ºC**	**4.10** **4.15**		**4.275** **4.25**	**V**
		V_{OV} = 4.25V (VOV1, VOV0 = 0,1) 0ºC to 50ºC	4.15 4.20		4.325 4.30	V
		V_{OV} = 4.30V (VOV1, VOV0 = 1,0) 0ºC to 50ºC	4.2 4.25		4.375 4.35	V
		V_{OV} = 4.35V (VOV1, VOV0 = 1,1) 0ºC to 50ºC	4.25 4.30		4.425 4.40	V
Cell over-charge protection mode release voltage threshold	V_{OVR}			V_{OV} - 0.20		V
Cell over-charge detection time	T_{OV}	C_{OV} = 0.1uF		1		s
Cell over-discharge protection mode (SLEEP) threshold. (Default in Boldface)	V_{UV}(4)	**V_{UV} = 2.25V (VUV1, VUV0 = 0,0)**	**2.15**		**2.35**	**V**
		V_{UV} = 2.35V (VUV1, VUV0 = 0,1)	2.25		2.45	V
		V_{UV} = 2.45V (VUV1, VUV0 = 1,0)	2.35		2.55	V
		V_{UV} = 2.55V (VUV1, VUV0 = 1,1)	2.45		2.65	V
Cell over-discharge protection mode release threshold	V_{UVR}			V_{UV} + 0.7		V
Cell over-discharge detection time	T_{UV}	C_{UV} = 0.1µF C_{UV} = 200pF		1 2		s ms
Cell over-discharge release time	T_{UVR}	C_{UV} = 0.1µF C_{UV} = 200pF		7 100		ms µs

Description	Sym	Condition	Min	Typ(2)	Max	Unit
Over-current mode detection voltage (Default in Boldface)	V_{OC}(4)	**V_{OC} = 0.075V (VOC1, VOC0 = 0,0)**	**0.050**		**0.100**	**V**
		0°C to 50°C	**0.060**		**0.090**	
		V_{OC} = 0.100V (VOC1, VOC0 = 0,1)	0.075		0.125	V
		0°C to 50°C	0.085		0.115	
		V_{OC} = 0.125V (VOC1, VOC0 = 1,0)	0.100		0.150	V
		0°C to 50°C	0.110		0.140	
		V_{OC} = 0.150V (VOC1, VOC0 = 1,1)	0.125		0.175	V
		0°C to 50°C	0.135		0.165	
Over-current mode detection time	T_{OC}	C_{OC} = 0.001µF		10		ms
		C_{OC} = 200pF		2		
Over-current mode release time	T_{OCR}	C_{OC} = 0.001µF		10		ms
		C_{OC} = 200pF		2		
Load resistance over-current mode release condition	R_{OCR}	Releases when OVP/LMON pin > 2.5V		250		kΩ
Cell charge threshold voltage	V_{CE}	V_{CE} = 0.5V (Vce1, Vce0 = 0,0)	0.4	0.5	0.6	V
		V_{CE} = 0.8V (Vce1, Vce0 = 0,1)	0.7	0.8	0.9	V
		V_{CE} = 1.1V (Vce1, Vce0 = 1,0)	1	1.1	1.2	V
		V_{CE} = 1.4V (Vce1, Vce0 = 1,1)	1.3	1.4	1.5	V
X3101 wake-up voltage (For Vcc above this voltage, the device wakes up)	V_{SLR}	See Wake-up test circuit	10.5		12.5	V
X3101 sleep voltage (For Vcc above this voltage, the device cannot go to sleep)	V_{SLP}	See Sleep test circuit	9.5		11.5	V

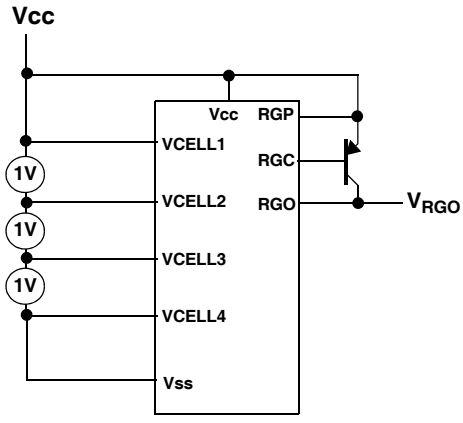
Notes: (2) Typical at 25°C.
(3) See Figure 10 on page 22.
(4) The default setting is set at the time of shipping, but may be changed by the user via changes in the configuration register.
(5) For reference only, this parameter is not 100% tested.

Wake-up test circuit (X3101)



Increase Vcc until V_{RGO} turns on

Sleep test circuit (X3101)



Decrease Vcc until V_{RGO} turns off

POWER-UP TIMING

Symbol	Parameter	Min.	Max.
t_{PUR}(6)	Power-up to SPI read operation (RDSTAT, EEREAD STAT)		T_{OC} + 2ms
t_{PUW1}(6)	Power-up to SPI write operation (WREN, WRDI, EEWRITE, WCFIG, SET IDL, WCNTR)		T_{OC} + 2ms
t_{PUW2}(6)	Power-up to SPI write operation (WCNTR - bits 10 and 11)		T_{OV} + 200ms or T_{UV} + 200ms(7)

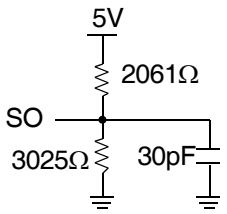
Notes: (6) t_{PUR}, t_{PUW1} and t_{PUW2} are the delays required from the time V_{CC} is stable until a read or write can be initiated. These parameters are not 100% tested.
(7) Whichever is longer.

CAPACITANCE T_A = +25°C, f = 1 MHz, V_{RGO} = 5V

Symbol	Parameter	Max.	Units	Conditions
C_{OUT}(8)	Output capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(8)	Input capacitance (SCK, SI, $\overline{CS}$)	6	pF	V_{IN} = 0V

Notes: (8) This parameter is not 100% tested.

Equivalent A.C. Load Circuit



A.C. TEST CONDITIONS

Input pulse levels	0.5 - 4.5V
Input rise and fall times	10ns
Input and output timing level	2.5V

A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

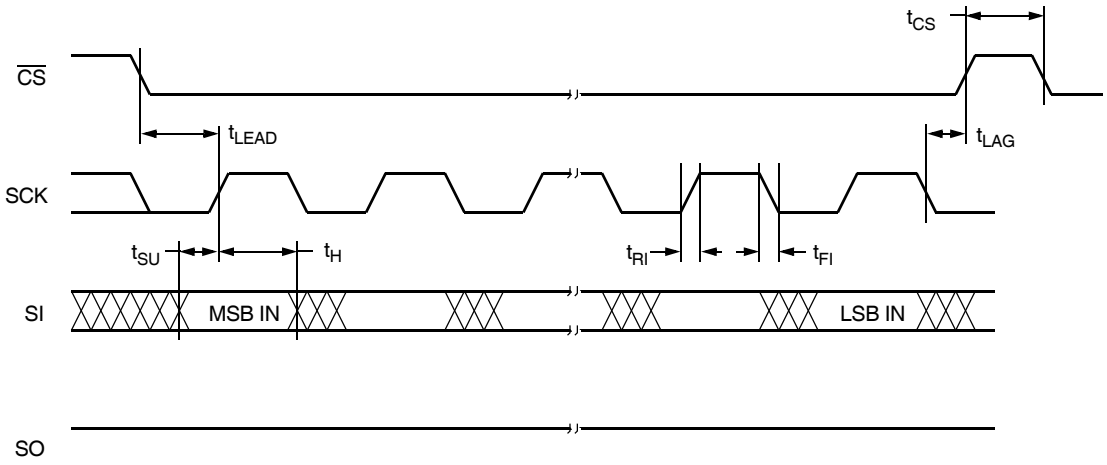
SERIAL INPUT TIMING

Symbol	Parameter	Voltage	Min.	Max.	Units
f_{SCK}	Clock frequency		0	3.3	MHz
t_{CYC}	Cycle time		300		ns
t_{LEAD}	$\overline{CS}$ lead time		150		ns
t_{LAG}	$\overline{CS}$ lag time		150		ns
t_{WH}	Clock HIGH time		130		ns
t_{WL}	Clock LOW time		130		ns
t_{SU}	Data setup time		20		ns
t_H	Data hold time		20		ns
t_{RI}(9)	Data in rise time			2	µs
t_{FI}(9)	Data in fall time			2	µs
t_{CS}	$\overline{CS}$ deselect time		100		ns
t_{WC}(10)	Write cycle time			5	ms

Notes: (9) This parameter is not 100% tested

(10) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

Serial Input Timing

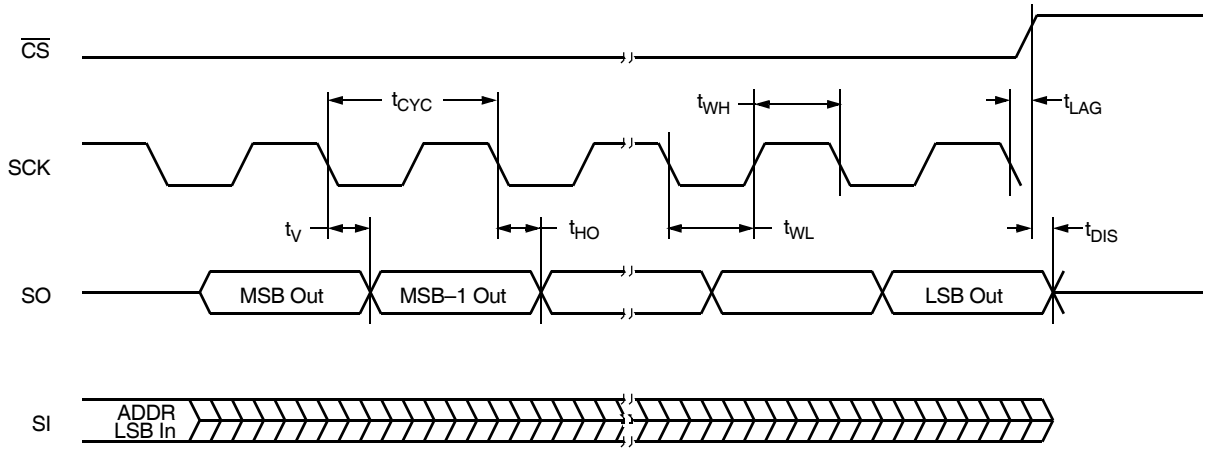


Serial Output Timing

Symbol	Parameter	Voltage	Min.	Max.	Units
f_{SCK}	Clock Frequency		0	3.3	MHz
t_{DIS}	Output Disable Time			150	ns
t_V	Output Valid from Clock LOW			130	ns
t_{HO}	Output Hold Time		0		ns
t_{RO}(11)	Output Rise Time			50	ns
t_{FO}(11)	Output Fall Time			50	ns

Notes: (11)This parameter is not 100% tested.

Serial Output Timing



SYMBOL TABLE

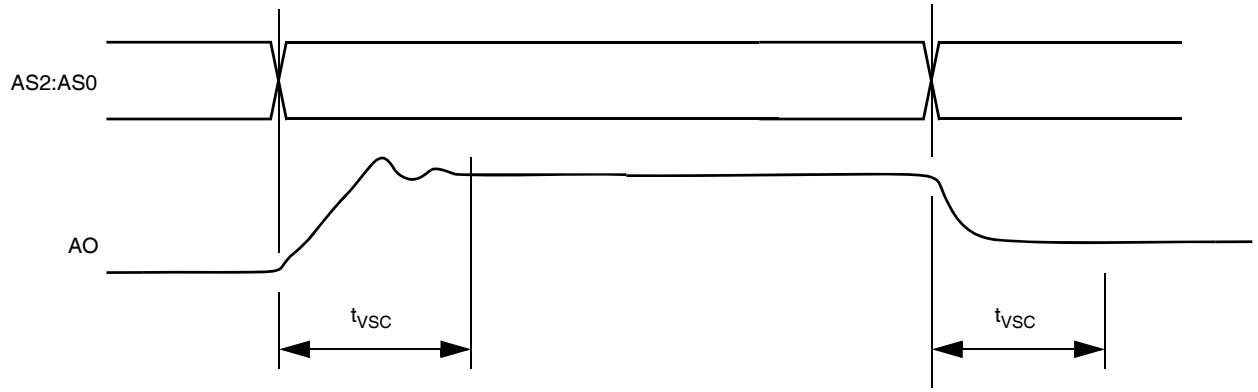
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Analog Output Response Time

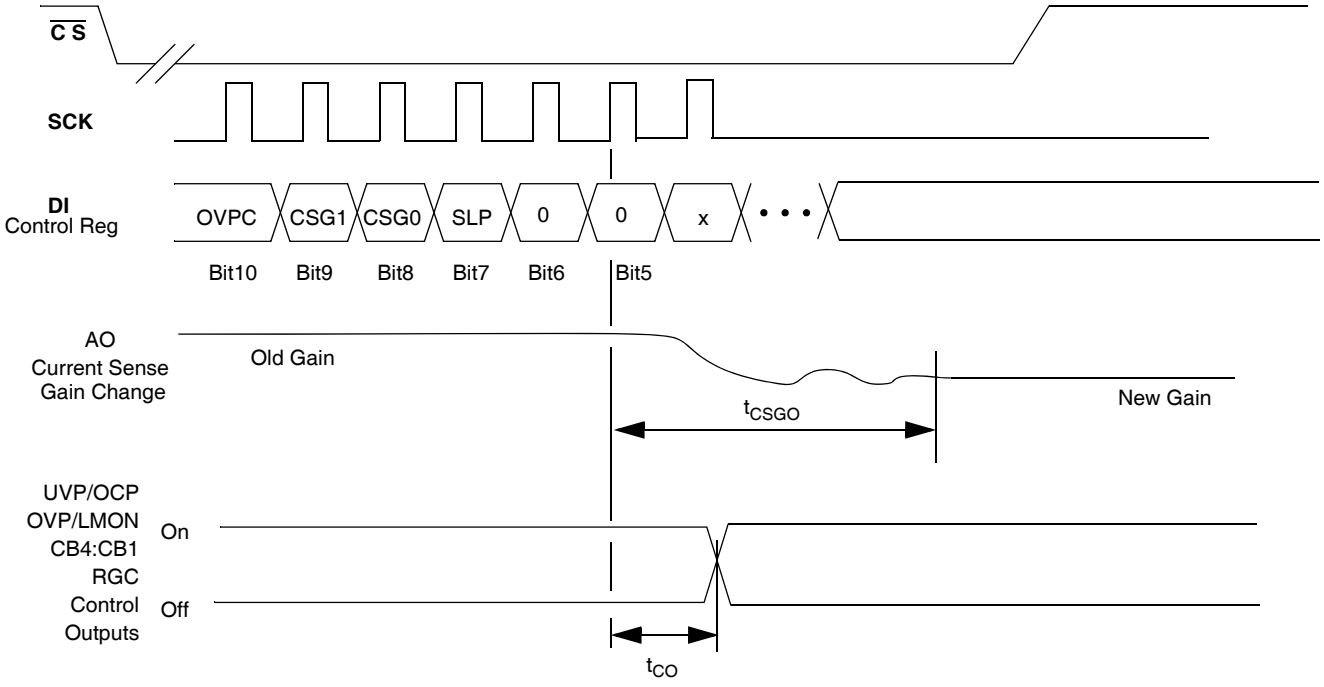
Symbol	Parameter	Min.	Typ.	Max.	Units
t_{VSC}	AO Output Stabilization Time (Voltage Source Change)			1.0	ms
t_{CSGO}	AO Output Stabilization Time (Current Sense Gain Change)			1.0	ms
t_{CO}	Control Outputs Response Time (UVP/OCP, OVP/MON, CB4, CB3, CB2, CB1, RGC)			1.0	µs

ANALOG OUTPUT RESPONSE TIME

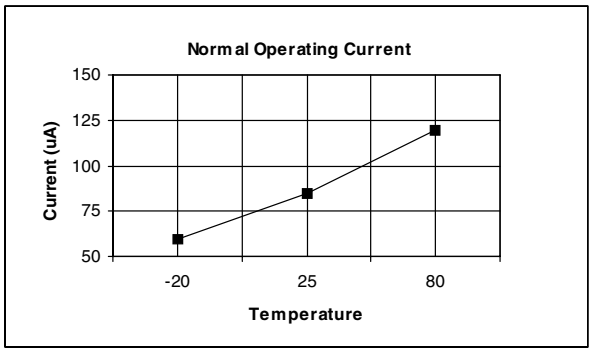
Change in Voltage Source

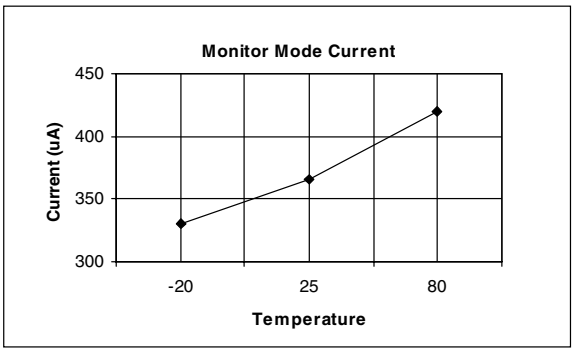


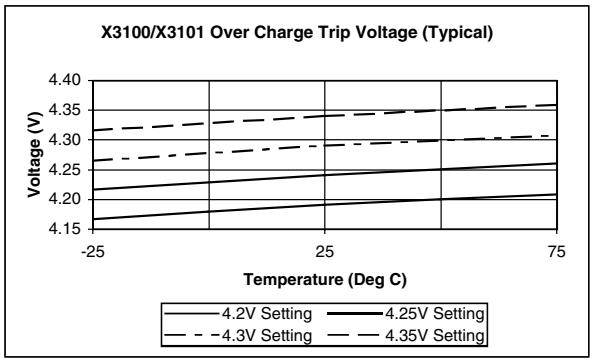
Change in Current Sense Gain Amplification and Control Bits

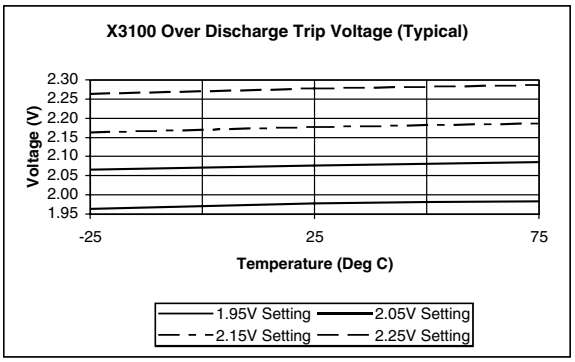


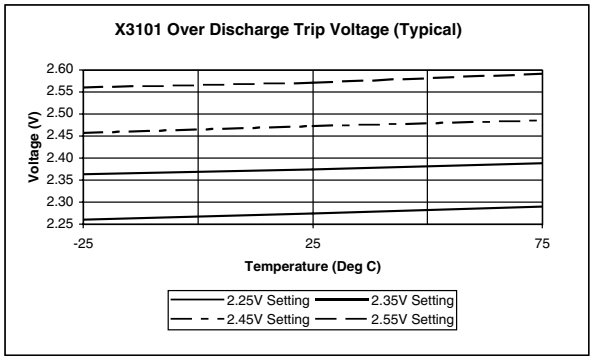
TYPICAL OPERATING CHARACTERISTICS

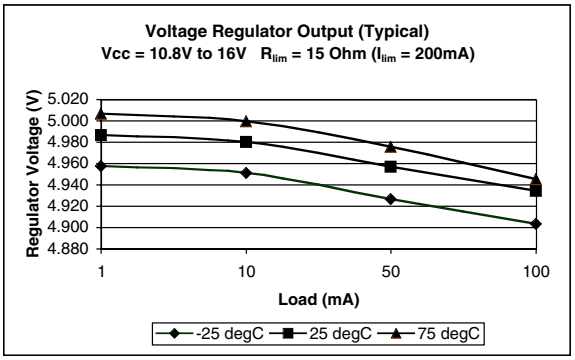


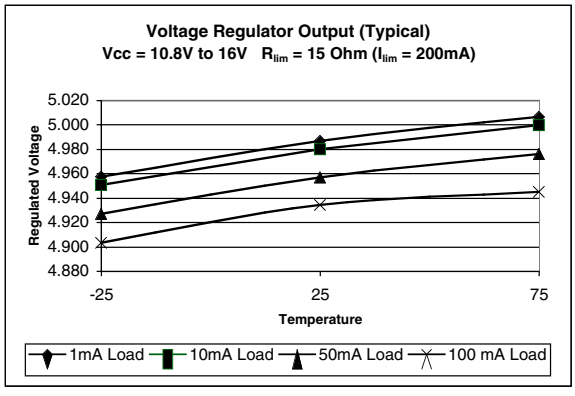






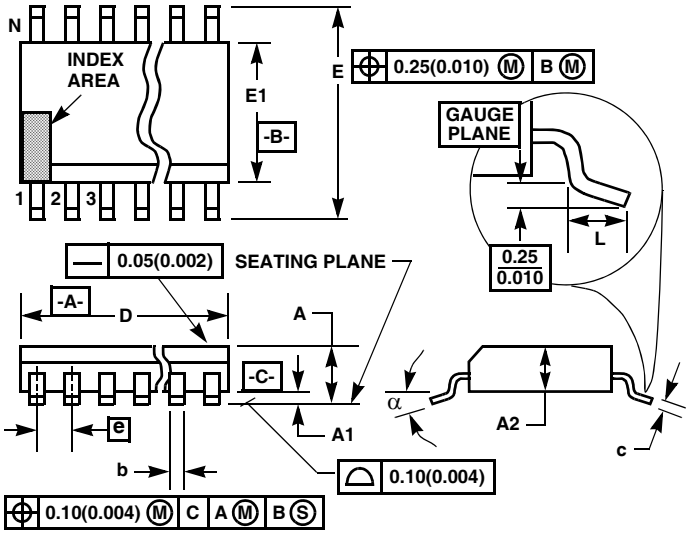






For typical performance of current and voltage monitoring circuits, please refer to Application Note AN142 and AN143

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AE, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M28.173

28 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.378	0.386	9.60	9.80	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 0 6/98

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