Digital pulse compression module

CI F06 Expander and Compressor

To make an enquiry please email: info@rakon.fr

Product description



CI F06 unit includes a digital pulse expander and the matched digital pulse compressor housed in a single unit.

The pulse expander generates a frequency coded pulse, also called a chirp. Pulse output is IF analog.

The pulse compressor performs matched filtering of the expanded chirp. Compressor pulse input and output are IF analog.

CI F06 may be customized to generate and match linear or non linear chirps.

CI F06 may be used as a replacement of existing SAW based pulse expander and/or compressor to overcome device obsolescence or enhance RADAR performances.

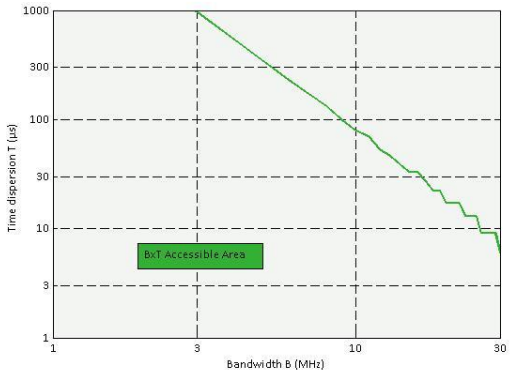
CI F06 behavior and performances are reproducible from one unit to the other. No matching is needed. CI F06 may be used with CI F04/05 to get multiple compressor channels, also without matching required from one unit to the other.

Rakon will customize pulse expander chirp and pulse compression filter according to the characteristics requested by the customer (Chirp duration, bandwidth, compressed pulse width, chirp slope …).

The unit is provided with FPGA firmware loaded, including pulse expander waveforms and pulse compression filter.

Features

- Single channel pulse expander unit
- Single channel pulse compressor unit
- IF analog I/Os
- 2 selectable waveforms for expander and compressor
- High precision clock
- BITE function
- High BxT compression gain



Applications

- SAW based pulse compression RADARS upgrade

Technical description

CI F06 functional block diagram is featured on Fig. 1.

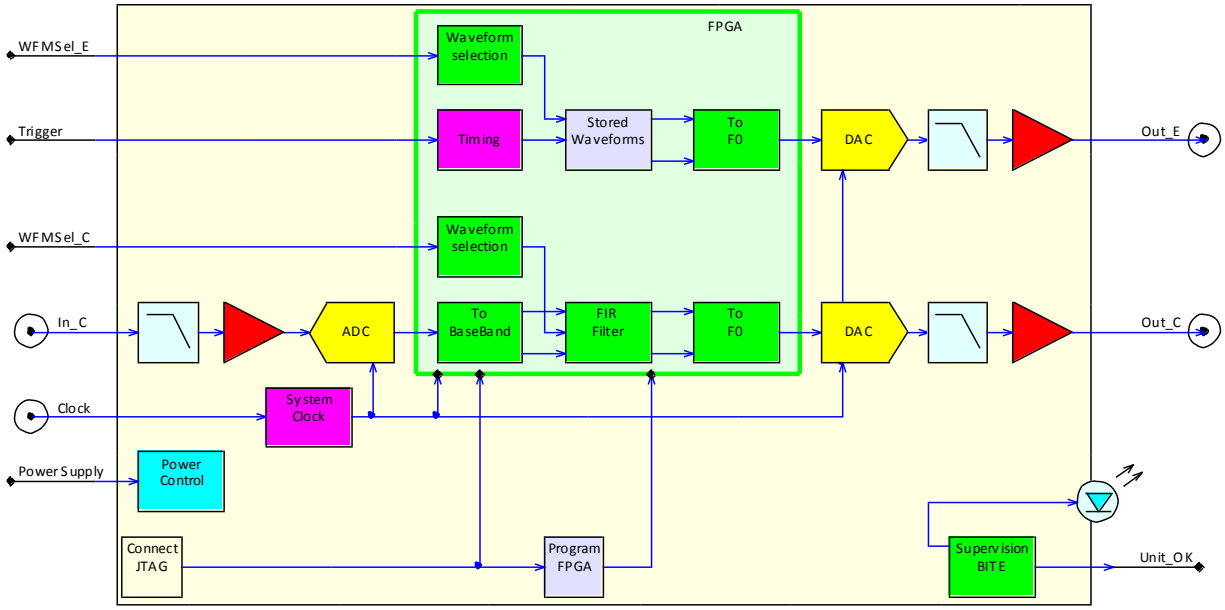


Fig. 1 : CI F06 functional block diagram

Unit description.

The internal low noise system clock is locked on an external clock (derived from the RADAR system clock). For proper operation, the clock should be a good quality clock, with a low phase noise close to the carrier.

CI F06 unit is provided with FPGA firmware loaded. Functions, and channels specifications (time dispersion, compressed pulse width, side lobes level…) should be provided by customer; Rakon will customize the FPGA program to fulfill customer requirements.

CI F06 unit continuously monitors internal power supply and FPGA program integrity. If voltage exceeds nominal levels, or if FPGA program is corrupted, Unit_OK output is deasserted, and LED is turned off. The Unit_OK output indicates the GO-NOGO state of the compressor.

Pulse expander channel description.

After each Trigger pulse, a chirp defined by the samples set selected by WFMSel_E is generated, and presented to the DAC input to be translated into an analog signal. Trigger input have to be synchronized with Clock input.

For better compatibility with old SAW based subsystems, an adjustable additional delay may be inserted.

Expander waveform is selected among 2 possible waveforms, using WFMSel_E input, as presented in Table 1. Each time WFMSel_E signal changes, the new set of waveform coefficients will be active for the next trigger pulse.

Table 1 : Expander waveform selection

WFMSel_E	Expander waveform
0	Waveform E0 (TBD)
1	Waveform E1 (TBD)

Pulse compressor channel description.

Input chirps are filtered (anti-aliasing filter), sampled and down-converted to baseband. I and Q baseband data are processed by FIR filters whose coefficients are matched with the expander chirp characteristics. Digital baseband I/Q compressed pulse is then up-converted to carrier frequency and converted into analog signal.

As inputs and outputs are IF analog signals, CI F06 is well suited to upgrade SAW based pulse compression Radars. For better compatibility with old SAW based subsystems, an adjustable additional delay may be inserted.

Fig. 2 gives the maximum chirp duration value vs. bandwidth achievable for the compressor channel.

Compressor waveform is selected among 2 possible waveforms, using WFMSel_C input, as presented in Table 2. Each time WFMSel_C signal changes, the new set of waveform coefficients will be active 50 µs later.

Table 2 : Compressor waveform selection

WFMSel_C	Compressor waveform
0	Waveform C0 (TBD)
1	Waveform C1 (TBD)

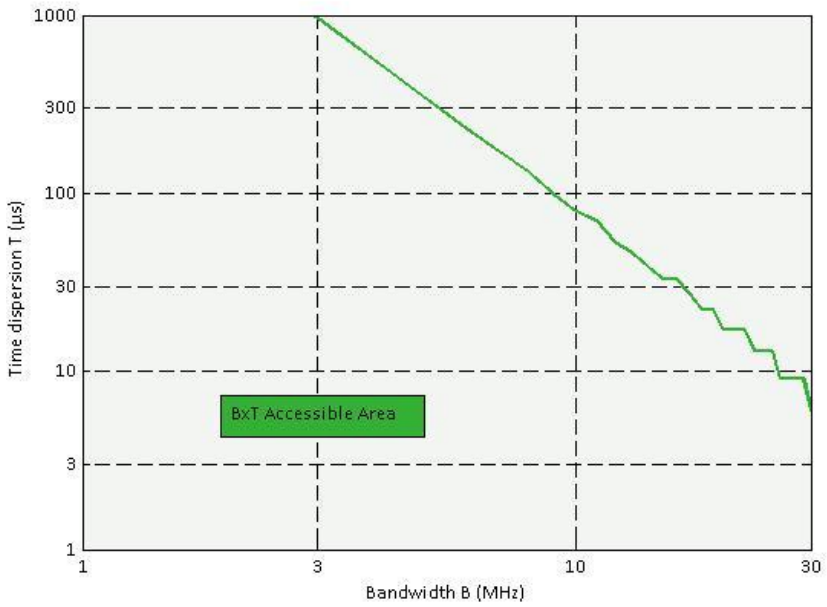


Fig. 2 : Accessible B x T area

Specifications

1 Environmental conditions

Line	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Procedures and conditions refer to MIL-STD-810G					
1.1	Temperature operating		-25		+60	°C
1.2	Temperature storage		-40		+85	°C
1.3	Humidity operating	@ 30 °C, (non condensing)			95	% RH
1.4	Shock	11 ms, 3 axes, 2 dir, half sine pulse			30	g
1.5	Random Vibration	20 to 500 Hz, 3 axes			0.1	g^2/Hz
1.6	EMI - EMC	In accordance with MIL-STD 461 E				

2 Electrical Interface

Line	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Power supply					
2.1	Voltage		11		26	V
2.2	Current	@ Power supply = 15 V		600 [1]		mA
	Clock Input					
	Refers to Clock					
2.3	Input level		-10	0	10	dBm
2.4	Frequency		0		250	MHz
2.5	Phase noise @ 1 kHz	For a 20 MHz clock input			-130	dBc/Hz
2.6	VSWR				1.5:1	
	RF Input signal					
	Refers to In_C					
2.7	Maximum input level			10		dBm
2.8	Input noise floor	Inside chirp bandwidth		-130		dBm/Hz
2.9	VSWR				1.3:1	

[1] Current highly depends on waveform characteristics (B, T, …)

2 Electrical Interface

Line	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	RF expander output signal					
	Refers to Out_E					
2.10	Maximum output level			10		dBm
2.11	Output level variation with temperature				± 1	dB
2.12	Maximum time domain amplitude ripple			± 0.1		dB
2.13	Rise / Fall time	From 10 % to 90 % max level			50	ns
2.14	Spurious harmonic level				-70	dBc
2.15	Output noise floor	Inside chirp bandwidth		-140		dBm/Hz
2.16	Maximum phase error within the chirp			± 2		Deg.
2.17	VSWR				1.3:1	
	RF compressor output signal					
	Refers to Out_C					
2.18	Maximum output level			0		dBm
2.19	Output noise floor	Inside chirp bandwidth		-150		dBm/Hz
2.20	VSWR				1.3:1	
	RS-422 control inputs					
	Refers to Trigger, WFMSel_E, WFMSel_C inputs					
2.21	Impedance			120		Ω
2.22	Setup time	To clock rising edge	50			ns
2.23	Hold time	From clock rising edge	50			ns

3 CI F06 expander operation Performances

Line	Parameter	Test Condition	Min.	Typ.	Max.	Unit
3.1	Center frequency (F0)				75 – B/2	MHz
3.2	Maximum bandwidth (B)			45		MHz
3.3	Maximum time dispersion (T)			1000		µs
3.4	Minimal expander delay (TE)	Measured from first Clock rising edge after Trigger low to high transition, to the center of the output chirp.		T/2 + 0.3		µs
3.5	Maximal additional expander delay (TE)	Measured from first Clock rising edge after Trigger low to high transition, to the center of the output chirp.		1		ms
3.6	Modulation slope		Up-chirp / Down-chirp			
3.7	Modulation type		Linear / Non linear			

4 CI F06 compressor operation Performances

Line	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Note: Values given bellow are typical values given as a rough guide. Depending on the required parameters (B, T,…) other limitations may rise, e.g. side lobe levels highly depends on bandwidth (B) and time dispersion (T), τ_{-3dB} highly depends on bandwidth (B), …					
4.1	Center frequency (F0)				75 – B/2	MHz
4.2	Maximum bandwidth (B)			45		MHz
	Maximum time dispersion (T)					
4.3	B < 3 MHz			950		µs
4.4	B < 7 MHz			170		µs
4.5	B < 20 MHz			17		µs
4.6	Minimum compressed pulse width @ -3 dB (τ_{-3dB})			35		ns
4.7	Side lobe level (SLL)			35 to 45		dB
4.8	Minimal compressor delay (TC)	Measured from the center of the input chirp, to the center of the compressed pulse output		T/2 + 2.5		µs
4.9	Maximal additional Compressor delay (TC)	Measured from the center of the input chirp, to the center of the compressed pulse output		1		ms
4.10	CW Insertion loss @ F0			25		dB
4.11	Modulation slope		Up-chirp / Down-chirp			
4.12	Modulation type		Linear / Non linear			

Mechanical features

5 Mechanical features

Line	Parameter	Test Condition	Min.	Typ.	Max.	Unit
5.1	Unit outline without connectors			175 x 152 x 27.1		mm^3
5.2	Unit weight			< 0.6		kg
5.3	Material			AG4.5MC		
5.4	Treatment			Ni15 / Zn1		
5.5	Screws			A4-70 stainless steel		

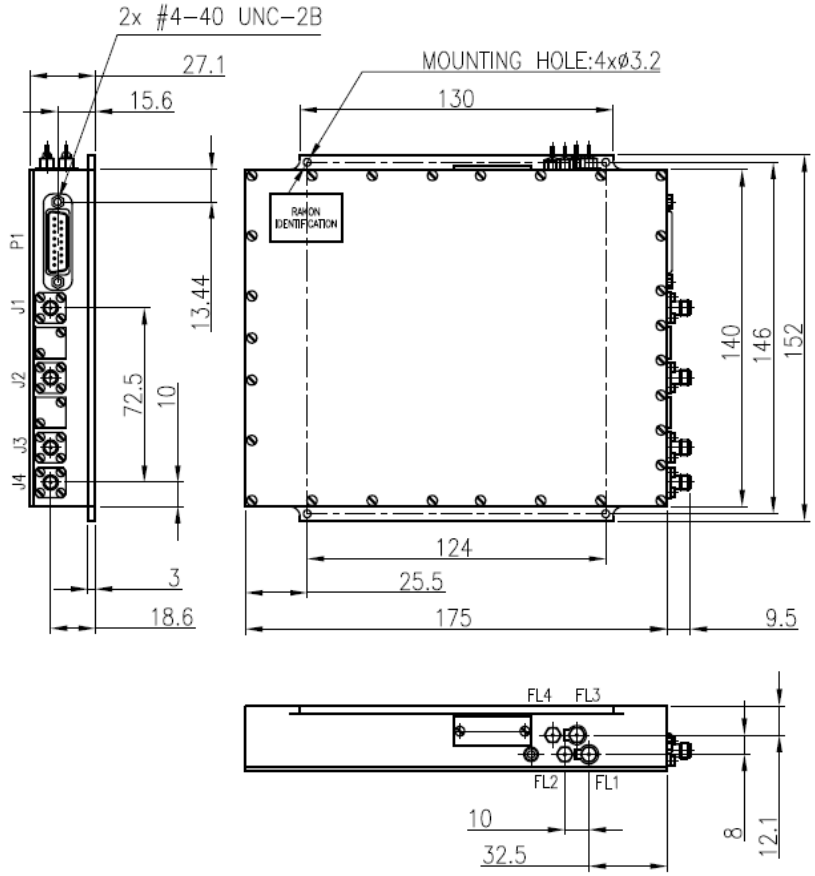


Fig. 3 : Mechanical drawing

Reliability

6 Reliability information

Line	Parameter	Test Condition	Value	Unit
6.1	Estimated mean time between failure	FIDES 2004, 30°C ambient	> 250 000	H

7 Interfaces description

Line	Pin number	Name	Description
	J1 to J4 : SMA – Jack		
7.1	J1	Clock	Reference clock input AC, 50 Ω
7.2	J2	In_C	Compressor RF chirp input AC, 50 Ω
7.3	J3	Out_E	Expander RF chirp output AC, 50 Ω
7.4	J4	Out_C	Compressor RF compressed pulse output AC, 50 Ω
	FL01 to FL04 : By-pass filter		
7.5	FL01	Power supply return	Power supply return
7.6	FL02	Power supply	Power supply
7.7	FL03	Pi filter	Not used
7.8	FL04	Pi filter	Not used
	P1 : MIL-C-24308 15-pin SubD Connector		
7.9	P1 – 3 / P1 – 11	WFMSel_E +/-	Expander Waveform selection input RS-422 compatible input, 120 Ω differential impedance
7.10	P1 – 4 / P1 – 12	WFMSel_C +/-	Compressor Waveform selection input RS-422 compatible input, 120 Ω differential impedance
7.11	P1 – 2 / P1 – 10	Trigger +/-	Trigger input Time reference = First clock rising edge following Trigger low to high transition. RS-422 compatible input, 120 Ω differential impedance
7.12	P1 – 5 / P1 – 13	Unit_OK +/-	BITE output RS-422 level, Logic 1 = Unit OK Indicates the GO-NOGO state of the unit
7.13	P1 – 8	GND	Ground
7.14	P1 – 15	OC Unit OK	Open Collector BITE Input-Output TTL Level with 300 Ω internal pull-up, Logic 1 = Unit OK Indicates the GO-NOGO state of the unit May be tied to other OC Unit OK to generate a global System OK when 2 or more CI F06 units are used
	P3 : MOLEX type 87833-1420		
7.15	P3	JTAG	JTAG interface for program download