User-Programmable Dual High-Performance Clock Generator

Description

The ICS2572 is a dual-PLL (phase-locked loop) clock generator with differential video outputs specifically designed for high-resolution, high-refresh rate, video applications. The video PLL generates any of 16 pre-programmed frequencies through selection of the address lines FS0-FS3. Similarly, the auxiliary PLL can generate any one of four pre-programmed frequencies via the MS0 & MS1 lines.

A unique feature of the ICS2572 is the ability to redefine frequency selections after power-up. This permits complete set-up of the frequency table upon system initialization.

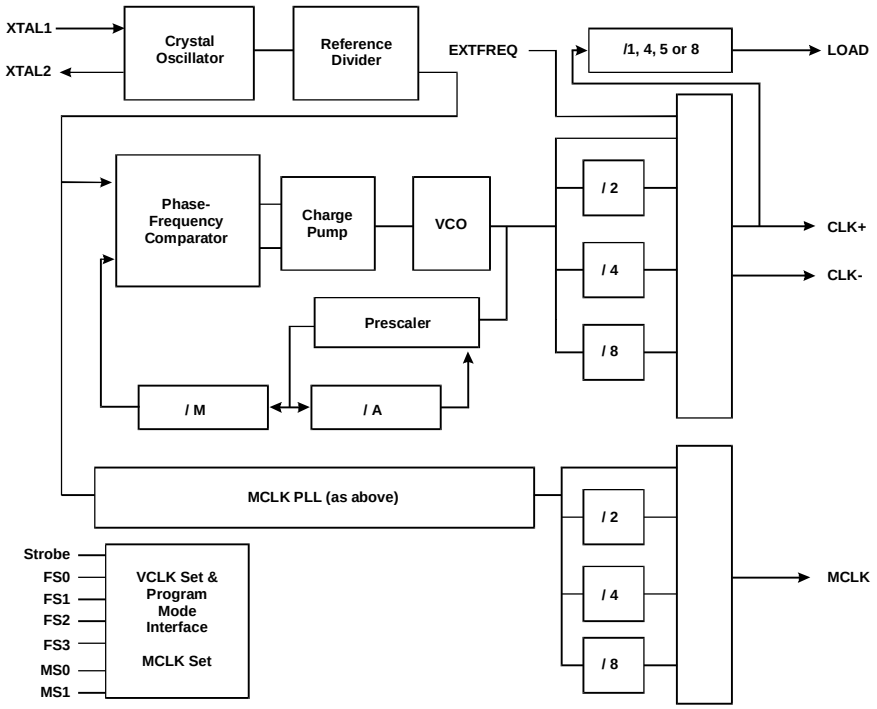
Features

- Advanced ICS monolithic phase-locked loop technology
- Supports high-resolution graphics - differential CLK output to 185 MHz
- Divided dotclock output (LOAD) available
- Simplified device programming
- Sixteen selectable VCLK frequencies (all user re-programmable)
- Four selectable MCLK frequencies (all user re-programmable)
- Windows NT compatible

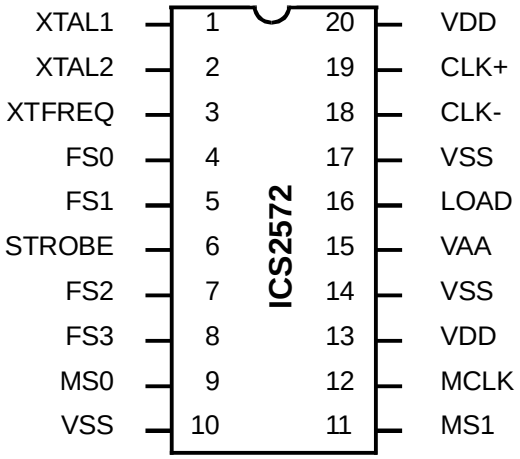
Applications

- High end PC/low end workstation graphics designs requiring differential output
- X Terminal graphics

Block Diagram



Pin Configuration



20-Pin DIP or SOIC
J-4, J-7

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	XTAL1	A	Quartz crystal connection 1/Reference Frequency Input.
2	XTAL2	A	Quartz crystal connection 2.
3	EXTFREQ	I	External Frequency Input
4	FS0	I	VCLK PLL Frequency Select LSB.
5	FS1	I	VCLK PLL Frequency Select Bit.
7	FS2	I	VCLK PLL Frequency Select Bit.
8	FS3	I	VCLK PLL Frequency Select MSB.
6	STROBE	I	Control for Latch of VCLK Select Bits (FS0-FS3).
9	MS0	I	MCLK PLL Frequency Select LSB.
11	MS1	I	MCLK PLL Frequency Select MSB.
19	CLK+	O	Pixel Clock Output (not inverted)
18	CLK-	O	Pixel Clock Output (inverted)
16	LOAD	O	Divided Dotclock (/4, 5, or 8)
12	MCLK	O	MCLK Frequency Output
17	RESERVED	-	Must Be Connected to VSS.
10, 14	VSS	P	Device Ground. All pins must be connected.
13, 20	VDD	P	Output Stage Vdd. All pins must be connected.
15	VAA	P	Synthesizer Vdd.

Digital Inputs

The FS0-FS3 pins and the STROBE pin are used to select the desired operating frequency of the VCLK output from the 16 pre-programmed/user-programmed selections in the ICS2572. These pins are also used to load new frequency data into the registers.

Available configurations for the STROBE input include: positive-edge triggered, negative-edge triggered, high-level transparent, and low-level transparent (see Ordering Information).

VCLK Output Frequency Selection

To change the VCLK output frequency, simply write the appropriate data to the ICS2572 FS inputs. Do not perform any further writes to the device for 50 milliseconds (assumes a 14.318 MHz reference). The synthesizer will output the new frequency programmed into that location after a brief delay (see timeout specifications).

MCLK Output Frequency Selection

The MS0-MS1 pins are used to directly select the desired operating frequency of the MCLK output from the four pre-programmed/user-programmed selections in the ICS2572. These inputs are not latched, nor are they involved with memory programming operations.

Programming Mode Selection

A programming sequence is defined as a period of at least 50 milliseconds of no data writes to the ICS2572 (to clear the shift register) followed by a series of data writes (as shown here):

FS0	FS1	FS2	FS3
X	X	**START** bit (must be "0")	0
X	X	"	1
X	X	**R/W*** control	0
X	X	"	1
X	X	**L0** (location LSB)	0
X	X	"	1
X	X	**L1**	0
X	X	"	1
X	X	**L2**	0
X	X	"	1
X	X	**L3**	0
X	X	"	1
X	X	**L4** (location MSB)	0
X	X	"	1
X	X	**N0** (feedback LSB)	0
X	X	"	1
X	X	**N1**	0
X	X	"	1
X	X	**N2**	0
X	X	"	1
X	X	**N3**	0
X	X	"	1
X	X	**N4**	0
X	X	"	1
X	X	**N5**	0
X	X	"	1
X	X	**N6**	0
X	X	"	1
X	X	**N7** (feedback MSB)	0
X	X	"	1
X	X	**EXTFREQ** bit (selected if "1")	0
X	X	"	1
X	X	**D0** (post-divider LSB)	0
X	X	"	1
X	X	**D1** (post-divider MSB)	0
X	X	"	1
X	X	**STOP1** bit (must be "1"	0
X	X	"	1
X	X	**STOP2** bit (must be "1")	0
X	X	"	1

Observe that the internal shift register is "clocked" by a transition of FS3 data from "0" to "1." If an extended sequence of register loading is to be performed (such as a power-on initialization sequence), note that it is not necessary to implement the 50 millisecond delay between them. Simply repeat the sequence above as many times as desired. Writes to the FS port will not be treated as frequency select data until up to 50 milliseconds have transpired since the last write. Note that FS0 and FS1 inputs are "don't care."

Data Description

Location Bits (L0-L4)

The first five bits after the start bit control the frequency location to be re-programmed according to this table. The rightmost bit (the LSB) of the five shown in each selection of the table is the first one sent.

Table 1 - Location Bit Programming

L[4-0]	LOCATION
01100	VCLK Address 12
01101	VCLK Address 13
01110	VCLK Address 14
01111	VCLK Address 15
10010	MCLK Address 2
10011	MCLK Address 3

Feedback Set Bits (N0-N7)

These bits control the feedback divider setting for the location specified. The modulus of the feedback divider will be equal to the value of these bits + 257. The least significant bit (N0) is sent first.

Post-Divider Set Bits (D0-D1)

These bits control the post-divider setting for the location specified according to this table. The least significant bit (D0) is sent first.

Table 2 - Post-Divider Programming

D[1-0]	POST-DIVIDER
00	9
01	4
10	2
11	1

Read/Write* Control Bit

When set to a "0," the ICS2572 shift register will transfer its contents to the selected memory register at the completion of the programming sequence outlined above.

When this bit is a "1," the selected memory location will be transferred to the shift register to permit a subsequent readback of data. No modification of device memory will be performed.

To readback any location of memory, perform a "dummy" write of data (complete with start and stop bits) to that location but set the R/W* control bit (make it "1"). At the end of the sequence (i.e., after the stop bits have been "clocked"), "clocking" of the FS3 input 11 more times will output the data bits only in the same sequence as above on the FS0 pin.

EXTFREQ Input

The EXTFREQ input allows an externally generated frequency to be routed to the VCLK output pin under device programming control. If the EXTFREQ bit is set (logic "1") at the selected address location (*VCLK addresses only*), the frequency applied to the EXTFREQ input will be routed to the VCLK output.

Frequency Synthesizer Description

Refer to Figure 1 for a block diagram of the ICS2572.

The ICS2572 generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed-loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL. The phase-frequency detector shown in the block diagram drives the VCO to a frequency that will cause the two inputs to the phase-frequency detector to be matched in frequency and phase. This occurs when:

$$F_{VCO}=F_{XTAL1}* \quad \frac{N}{2}$$

where N is the effective modulus of the feedback divider chain and R is the modulus of the reference divider chain.

The feedback divider on the ICS2572 may be set to any integer value from 257 to 512. This is done by the setting of the N0-N7 bits. The standard reference divider on the ICS2572 is fixed to a value of 43 (this may be set to a different value via ROM programming; contact factory). The ICS2572 is equipped with a post-divider and multiplexer that allows the output frequency range to be scaled down from that of the VCO by a factor of 2, 4, or 8.

Therefore, the *VCO* frequency range will be from 5.976 to 11.906 (257/43 to 512/43) of the reference frequency. The *output* frequency range will be from 0.747 to 11.906 times the reference frequency. Worst case accuracy for any desired frequency within that range will be 0.2%.

If a 14.31818 MHz reference is used, the output frequency range would be from 10.697 MHz to 170.486 MHz.

Programming Example

Suppose that we want differential CLK output to be 45.723 MHz. We will assume the reference frequency to be 14.31818 MHz.

The VCO frequency range will be 85.565 MHz to 170.486 MHz (5.976 * 14.31818 to 11.906 * 14.31818). We will need to set the post-divider to two to get an output of 45.723 MHz.

The VCO will then need to be programmed to two times 45.723 MHz, or 91.446 MHz. To calculate the required feedback divider modulus we divide the VCO frequency by the reference frequency and multiply by the reference divider:

$$\frac{91.446}{14.31818} *43=274.62$$

which we round off to 275. The exact output frequency will be:

$$\frac{275}{43} *14.31818* \frac{1}{2} =45.784 \text{ MHz}$$

The value of the N programming bits may be calculated by subtracting 257 from the desired feedback divider modulus. Thus, the N value will be set to 18 (275-257) or 00010010_2. The D bit programming is 10_2 (from Table 2).

LOAD Frequency Selection

The LOAD (or divided dotclock) output frequency will be the CLK+/CLK- frequency divided by 1, 4, 5, or 8. The choice of modulus is a factory option, and is specified along with the ROM frequencies in the VCLK and MCLK tables by way of the two-digit suffix of the part number.

Reference Oscillator & Crystal Selection

The ICS2572 has on-board circuitry to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in parallel-resonant (also called anti-resonant mode. See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

Crystals characterized for their series-resonant frequency may also be used with the ICS2572. Be aware that the oscillation frequency in circuit will be slightly higher than the frequency that is stamped on the can (typically 0.025-0.05%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the ICS2572 outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

External Reference Sources

An external frequency source may be used as the reference for the VCLK and MCLK PLLs. To implement this, simply connect the reference frequency source to the XTAL1 pin of the ICS2572. For best results, insure that the clock edges are as clean and fast as possible and that the input voltage thresholds are not violated.

Power Supply

The ICS2572 has two VSS pins to reduce the effects of package inductance. Both pins are connected to the same potential on the die (the ground bus). BOTH of these pins should connect to the ground plane of the video board as close to the package as is possible.

The ICS2572 has a VDD pin which is the supply of +5 volt power to all output stages. This pin should be connected to the power plane (or bus) using standard high-frequency decoupling practice. That is, use low-capacitors should have low series inductance and be mounted close to the ICS2572.

The VAA pin is the power supply for the synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to “track” through power supply fluctuations without visible effects.

Absolute Maximum Ratings

Supply voltage . . . . . -.5V to +7V
Logic inputs . . . . . .-.5V to V_{DD} +.5V
Ambient operating temp . . . . . 0 to 70°C
Storage temperature . . . . . -85 to + 150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

DC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TTL-Compatible Inputs			-	-	-	
(FS0-3, MS0-1, STROBE):			-	-	-	
Input High Voltage	V_{ih}		2.0	-	VDD+0.5	V
Input Low Voltage	V_{il}		VSS-0.5	-	0.8	V
Input High Current	I_{ih}		-	-	10	uA
Input Low Current	I_{il}		-	-	200	uA
Input Capacitance	C_{in}		-	-	8	pF
XTAL1:			-	-	-	
Input High Voltage	Vxh		VDD*0.75	-	VDD+0.5	V
Input Low Voltage	Vxl		VSS-0.5	-	VDD*0.25	V
CLK+/CLK- Output Sink Current	Isink		-	-	-	mA
High Voltage (Other Outputs)	Voh		4	-	-	V
@Ioh=0.4mA			-	-	-	
Low Voltage (Other Outputs)	Vol		-	-	0.4	V
@Iol=8.0mA			-	-	-	

AC Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Phase-Locked Loop:			-	-	-	
VCLK, MCLK VCO Frequency	Fvco		100	-	235	MHz
PLL Acquire Time	Tlock		-	500	-	uSec
Crystal Oscillator			-	-	-	
Crystal Frequency Range	Fxtal		5	-	25	MHz
Parallel Loading Capacitance			-	20	-	pF
XTAL1 Minimum High Time	Txhi		8	-	-	ns
XTAL1 Minimum Low Time	Txlo		8	-	-	ns
Power Supplies:			-	-	-	-
VDD Supply Current	idd		-	-	35	mA
VAA Supply Current	Iaa		-	-	10	mA
Digital Outputs:			-	-	-	
CLK+/CLK- Recommended Termination			50	-	2	ohms
Other Outputs Rise Time @ Cload=20pF	Tf		-	-	2	ns
Other Outputs Fall Time @ Cload=20pF	Tf		-	-	-	ns

PATTERN	ICS2572-01			
Reference Divider	43			
VCLK ADDR	FbkDiv/PostDiv - F_{VCLK}(MHz)			
0	300/1- 99.89			
1	378/1 - 125.87			
2	277/1 - 92.24			
3	432/4 - 35.96			
4	302/2 - 50.28			
5	340/2 - 56.61			
6	EXTFREQ-			
7	270/2 - 44.95			
8	405/1 - 134.86			
9	384/4 - 31.97			
A	330/1 - 109.88			
B	481/2 - 80.08			
C	479/4 - 39.87			
D	270/2 - 44.95			
E	450/2 - 74.92			
F	390/2 - 64.93			
MCLK ADDR	FbkDiv/PostDiv - F_{MCLK}			
0	481/4 - 40.04			
1	270/2 - 44.95			
2	396/4 - 32.97			
3	300/2 - 49.95			

Ordering Information

ICS2572N-SXX or ICS2572M-SXX (0.300" DIP or SOIC Package)

Example:

ICS XXXX N-SXX

- **S=Strobe Option/XX=Default Frequencies**
- **Package Type**
  - N=DIP (Plastic)
  - M=SOIC
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  - ICS, AV=Standard Device; GSP=Genlock Device

Where:

"s" denotes strobe option:	A - positive level transparent (i.e., 2494 interface compatible)
"xx" denotes default frequencies:	B - negative level transparent
	C - positive edge triggered
	D - negative edge triggered

NOTES