

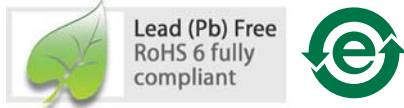
# HSMP-381x, 481x

## Surface Mount RF PIN

### Low Distortion Attenuator Diodes



## Data Sheet



### Description/Applications

The HSMP-381x series is specifically designed for low distortion attenuator applications. The HSMP-481x products feature ultra low parasitic inductance in the SOT-23 and SOT-323 packages. They are specifically designed for use at frequencies which are much higher than the upper limit for conventional diodes.

A SPICE model is not available for PIN diodes as SPICE does not provide for a key PIN diode characteristic, carrier lifetime.

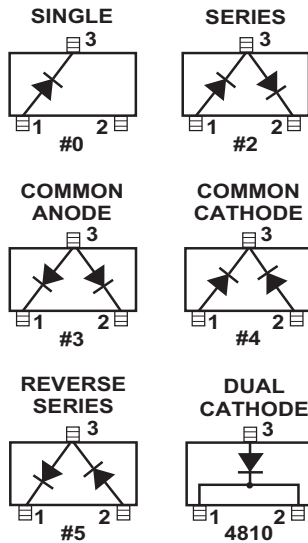
### Features

- Diodes Optimized for:
  - Low Distortion Attenuating
  - Microwave Frequency Operation
- Surface Mount Packages
  - Single and Dual Versions
  - Tape and Reel Options Available
- Low Failure in Time (FIT) Rate<sup>[1]</sup>
- Lead free

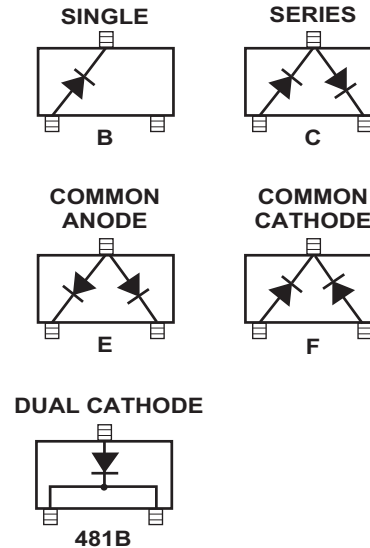
#### Note:

1. For more information see the Surface Mount PIN Reliability Data Sheet.

### Package Lead Code Identification, SOT-23 (Top View)



### Package Lead Code Identification, SOT-323 (Top View)



## Absolute Maximum Ratings<sup>[1]</sup> $T_c = +25^\circ\text{C}$

Symbol	Parameter	Unit	SOT-23	SOT-323
$I_f$	Forward Current (1 $\mu\text{s}$ Pulse)	Amp	1	1
$P_{IV}$	Peak Inverse Voltage	V	Same as $V_{BR}$	Same as $V_{BR}$
$T_j$	Junction Temperature	$^\circ\text{C}$	150	150
$T_{stg}$	Storage Temperature	$^\circ\text{C}$	-65 to 150	-65 to 150
$\theta_{jc}$	Thermal Resistance <sup>[2]</sup>	$^\circ\text{C}/\text{W}$	500	150

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2.  $T_c = +25^\circ\text{C}$ , where  $T_c$  is defined to be the temperature at the package pins where contact is made to the circuit board.

## Electrical Specifications $T_c = +25^\circ\text{C}$ (Each Diode)

### Conventional Diodes

Part Number HSMP-	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage $V_{BR}$ (V)	Maximum Total Capacitance $C_T$ (pF)	Minimum Resistance at $I_F = 0.01\text{mA}$ , $R_H$ ( $\Omega$ )	Maximum Resistance at $I_F = 20\text{mA}$ , $R_L$ ( $\Omega$ )	Maximum Resistance at $I_F = 100\text{mA}$ , $R_T$ ( $\Omega$ )	Resistance at $I_F = 1\text{mA}$ , $R_M$ ( $\Omega$ )
3810	E0	0	Single	100	0.35	1500	10	3.0	48 to 70
3812	E2	2	Series						
3813	E3	3	Common Anode						
3814	E4	4	Common Cathode						
3815	E5	5	Reverse Series						
381B	E0	B	Single						
381C	E2	C	Series						
381E	E3	E	Common Anode						
381F	E4	F	Common Cathode						
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10\mu\text{A}$	$V_R = 50\text{V}$ $f = 1\text{MHz}$	$I_F = 0.01\text{mA}$ $f = 100\text{MHz}$	$I_F = 20\text{mA}$ $f = 100\text{MHz}$	$I_F = 100\text{mA}$ $f = 100\text{MHz}$	$I_F = 1\text{mA}$ $f = 100\text{MHz}$

### High Frequency (Low Inductance, 500 MHz – 3 GHz) PIN Diodes

Part Number HSMP-	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage $V_{BR}$ (V)	Maximum Series Resistance $R_S$ ( $\Omega$ )	Series Resistance $I_F = 1\text{mA}$ , $R_M$ ( $\Omega$ )	Typical Total Capacitance $C_T$ (pF)	Maximum Total Capacitance $C_T$ (pF)	Typical Total Inductance $L_T$ (nH)
4810	EB	B	Dual Cathode	100	3	48 - 70	0.35	0.4	1
481B	EB	B	Dual Cathode						
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10\mu\text{A}$	$I_F = 100\text{mA}$ $f = 100\text{MHz}$	$I_F = 1\text{mA}$ $f = 100\text{MHz}$	$V_R = 50\text{V}$ $f = 1\text{MHz}$	$V_R = 50\text{V}$ $f = 1\text{MHz}$	$f = 500\text{MHz}$ - 3GHz

### Typical Parameters at $T_c = 25^\circ\text{C}$

Part Number	Series Resistance	Carrier Lifetime	Reverse Recovery Time	Total Capacitance
HSMP-	$R_s$ ( $\Omega$ )	$\tau$ (ns)	$T_{rr}$ (ns)	$C_t$ (pF)
381x	53	1500	300	0.27 @ 50 V
Test Conditions	$I_F = 1$ mA $f = 100$ MHz	$I_F = 50$ mA $I_R = 250$ mA	$V_R = 10$ V $I_F = 20$ mA 90% Recovery	$f = 1$ MHz

### Typical Parameters at $T_c = 25^\circ\text{C}$ (unless otherwise noted), Single Diode

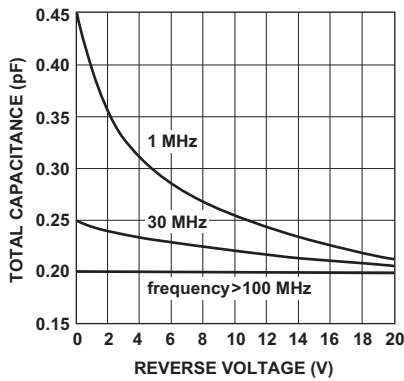


Figure 1. RF Capacitance vs. Reverse Bias.

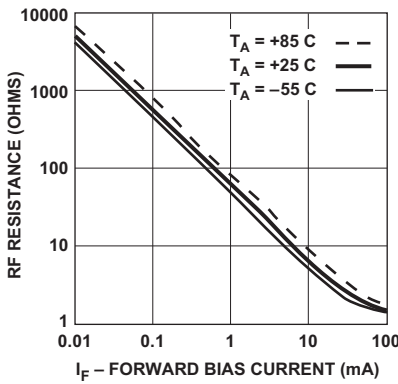


Figure 2. RF Resistance vs. Forward Bias Current,  $f = 100\text{MHz}$

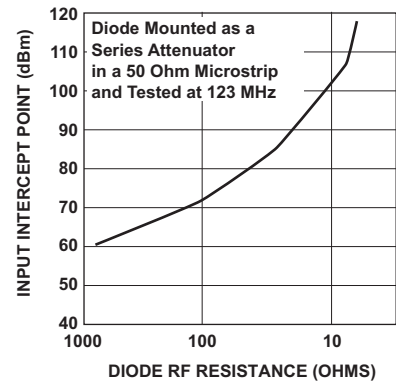


Figure 3. 2nd Harmonic Input Intercept Point vs. Diode RF Resistance.

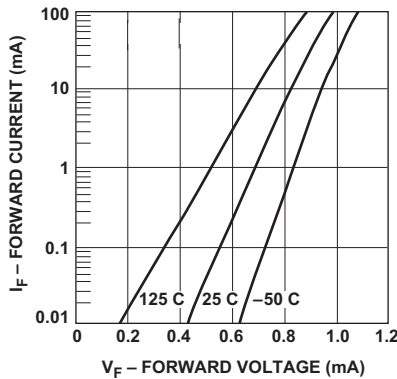


Figure 4. Forward Current vs. Forward Voltage.

### Typical Applications for Multiple Diode Products

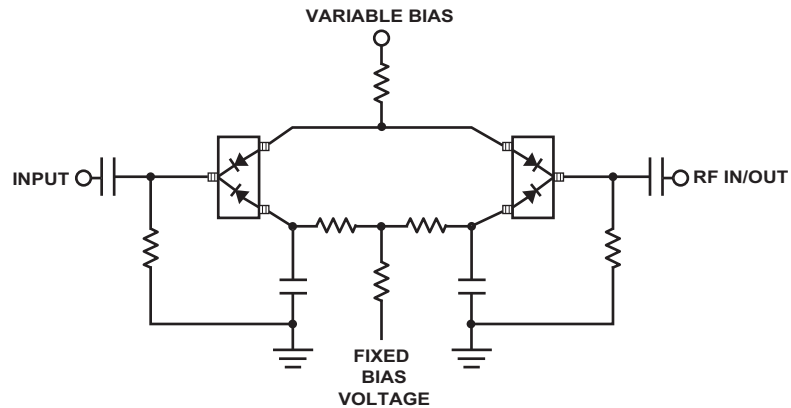


Figure 5. Four Diode  $\pi$  Attenuator. See Application Note 1048 for Details.

Notes:

3. Typical values were derived using limited samples during initial product characterization and may not be representative of the overall distribution.

## Typical Applications for HSMP-481x Low Inductance Series

### Microstrip Series Connection for HSMP-481x Series

In order to take full advantage of the low inductance of the HSMP-481x series when using them in series applications, both lead 1 and lead 2 should be connected together, as shown in Figure 7.

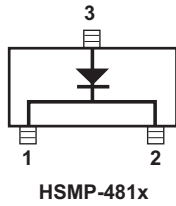


Figure 6. Internal Connections.

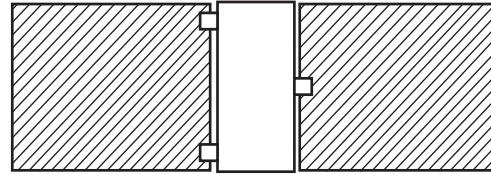


Figure 7. Circuit Layout.

### Microstrip Shunt Connections for HSMP-481x Series

In Figure 8, the center conductor of the microstrip line is interrupted and leads 1 and 2 of the HSMP-481x series diode are placed across the resulting gap. This forces the 1.5 nH lead inductance of leads 1 and 2 to appear as part of a low pass filter, reducing the shunt parasitic inductance and increasing the maximum available attenuation. The 0.3 nH of shunt inductance external to the diode is created by the via holes, and is a good estimate for 0.032" thick material.

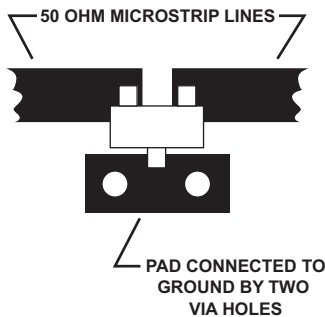


Figure 8. Circuit Layout.

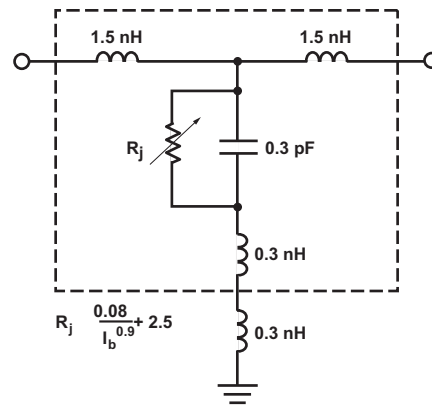


Figure 9. Equivalent Circuit.

## Typical Applications for HSMP-481x Low Inductance Series (continued)

### Co-Planar Waveguide Shunt Connection for HSMP-481x Series

Co-Planar waveguide, with ground on the top side of the printed circuit board, is shown in Figure 10. Since it eliminates the need for via holes to ground, it offers lower shunt parasitic inductance and higher maximum attenuation when compared to microstrip circuit.

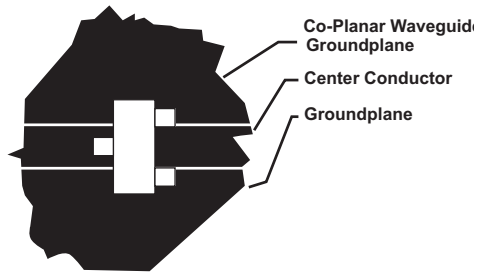


Figure 10. Circuit Layout.

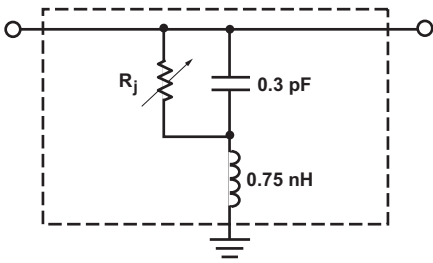
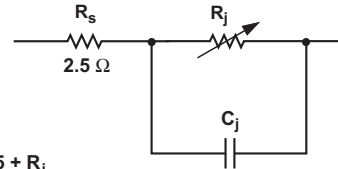


Figure 11. Equivalent Circuit.

### Equivalent Circuit Model HSMP-381x Chip\*



$$R_T = 2.5 + R_j$$

$$C_T = C_P + C_j$$

$$R_j = \frac{80}{I^{0.9}} \Omega$$

I = Forward Bias Current in mA

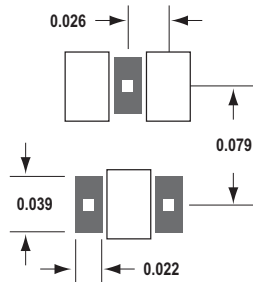
\*See AN1124 for package models.

0.18 pF\*  
\* Measured at -20 V

## Assembly Information

### SOT-323 PCB Footprint

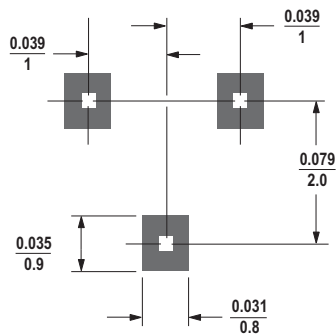
A recommended PCB pad layout for the miniature SOT-323 (SC-70) package is shown in Figure 12 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the performance.



Dimensions in inches

**Figure 12. Recommended PCB Pad Layout for Avago's SC70 3L/SOT-323 Products.**

### SOT-23 PCB Footprint



Dimensions in  $\frac{\text{inches}}{\text{mm}}$

**Figure 13. Recommended PCB Pad Layout for Avago's SOT-23 Products.**

## SMT Assembly

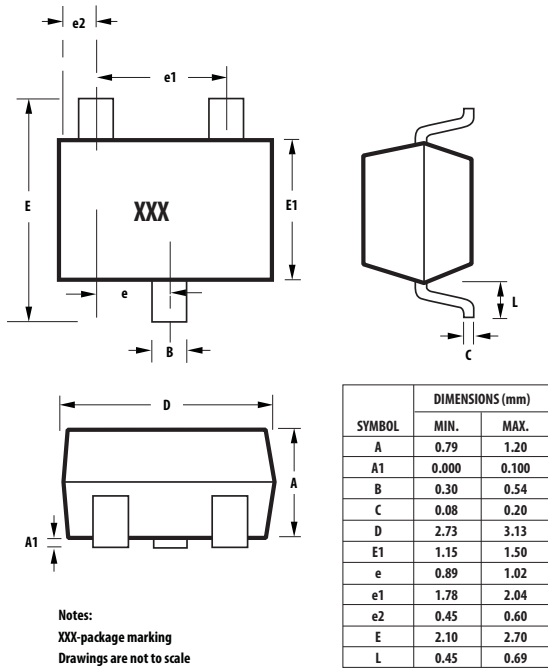
Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT-323/-23 package, will reach solder reflow temperatures faster than those with a greater mass.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

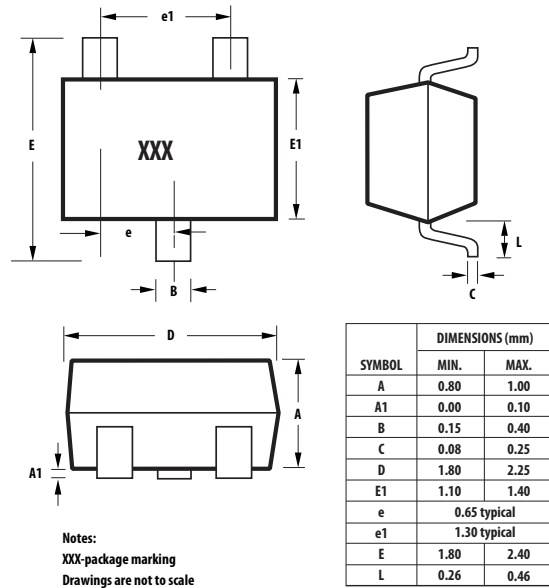
The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone ( $T_{MAX}$ ) should not exceed 260°C.

These parameters are typical for a surface mount assembly process for Avago diodes. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

## Package Dimensions Outline 23 (SOT-23)



## Outline SOT-323 (SC-70)

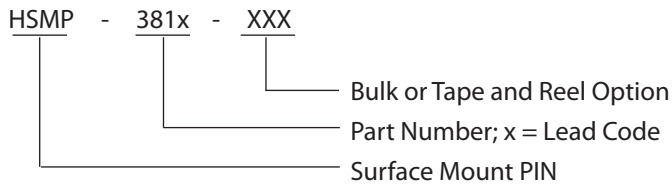


## Package Characteristics

Lead Material ..... Copper (SOT-323); Alloy 42 (SOT-23)  
 Lead Finish ..... Tin 100% (Lead-free option)  
 Maximum Soldering Temperature ..... 260°C for 5 seconds  
 Minimum Lead Strength..... 2 pounds pull  
 Typical Package Inductance ..... 2 nH  
 Typical Package Capacitance ..... 0.08 pF (opposite leads)

## Ordering Information

Specify part number followed by option. For example:

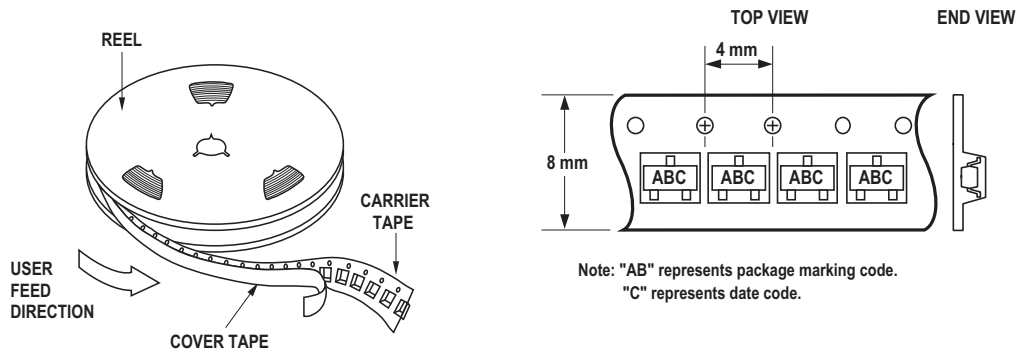


## Option Descriptions

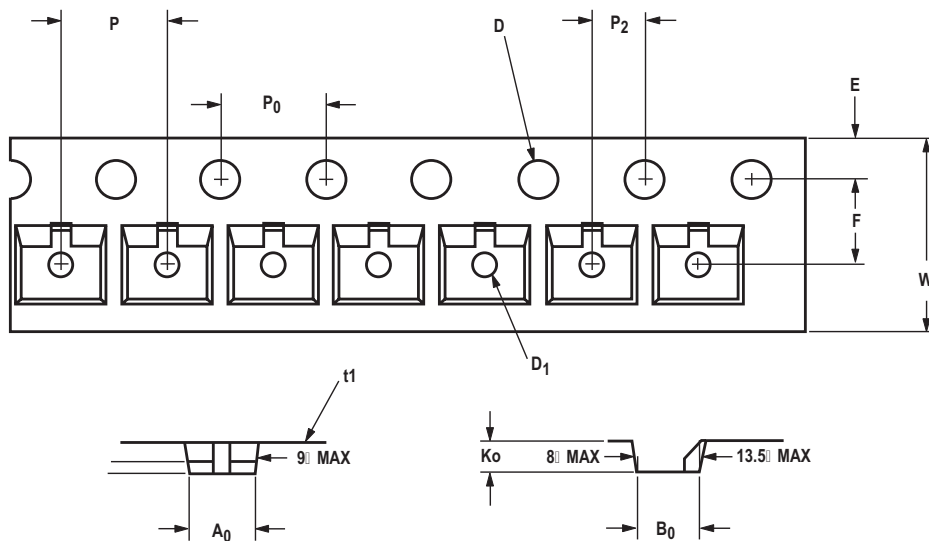
- BLKG = Bulk, 100 pcs. per antistatic bag
- TR1G = Tape and Reel, 3000 devices per 7" reel
- TR2G = Tape and Reel, 10,000 devices per 13" reel

Tape and Reeling conforms to Electronic Industries RS-481, "Taping of Surface Mounted Components for Automated Placement."

## Device Orientation For Outlines SOT-23/323



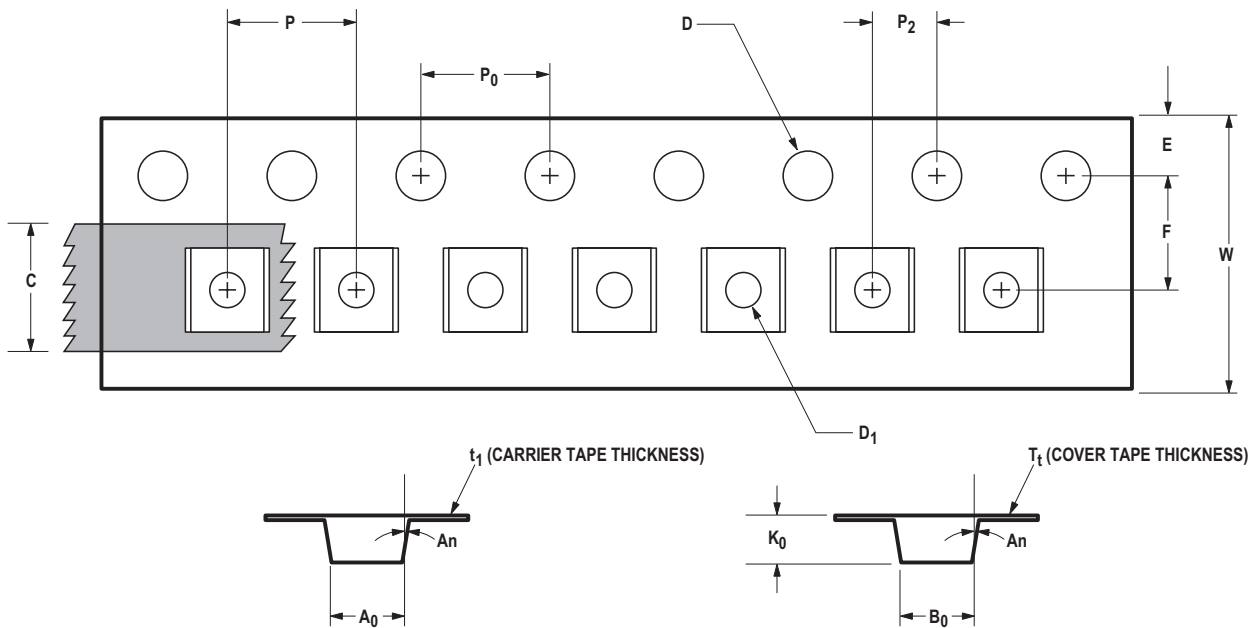
## Tape Dimensions and Product Orientation For Outline SOT-23



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	$A_0$	$3.15 \pm 0.10$	$0.124 \pm 0.004$
	WIDTH	$B_0$	$2.77 \pm 0.10$	$0.109 \pm 0.004$
	DEPTH	$K_0$	$1.22 \pm 0.10$	$0.048 \pm 0.004$
	PITCH	$P$	$4.00 \pm 0.10$	$0.157 \pm 0.004$
	BOTTOM HOLE DIAMETER	$D_1$	$1.00 \pm 0.05$	$0.039 \pm 0.002$
PERFORATION	DIAMETER	$D$	$1.50 \pm 0.10$	$0.059 \pm 0.004$
	PITCH	$P_0$	$4.00 \pm 0.10$	$0.157 \pm 0.004$
	POSITION	$E$	$1.75 \pm 0.10$	$0.069 \pm 0.004$
CARRIER TAPE	WIDTH	$W$	$8.00 \pm 0.30 - 0.10$	$0.315 \pm 0.012 - 0.004$
	THICKNESS	$t_1$	$0.229 \pm 0.013$	$0.009 \pm 0.0005$
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	$F$	$3.50 \pm 0.05$	$0.138 \pm 0.002$
	CAVITY TO PERFORATION (LENGTH DIRECTION)	$P_2$	$2.00 \pm 0.05$	$0.079 \pm 0.002$



## Tape Dimensions and Product Orientation For Outline SOT-323



	DESCRIPTION	SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	$A_0$	$2.40 \pm 0.10$	$0.094 \pm 0.004$
	WIDTH	$B_0$	$2.40 \pm 0.10$	$0.094 \pm 0.004$
	DEPTH	$K_0$	$1.20 \pm 0.10$	$0.047 \pm 0.004$
	PITCH	$P$	$4.00 \pm 0.10$	$0.157 \pm 0.004$
	BOTTOM HOLE DIAMETER	$D_1$	$1.00 + 0.25$	$0.039 + 0.010$
PERFORATION	DIAMETER	$D$	$1.55 \pm 0.05$	$0.061 \pm 0.002$
	PITCH	$P_0$	$4.00 \pm 0.10$	$0.157 \pm 0.004$
	POSITION	$E$	$1.75 \pm 0.10$	$0.069 \pm 0.004$
CARRIER TAPE	WIDTH	$W$	$8.00 \pm 0.30$	$0.315 \pm 0.012$
	THICKNESS	$t_1$	$0.254 \pm 0.02$	$0.0100 \pm 0.0008$
COVER TAPE	WIDTH	$C$	$5.4 \pm 0.10$	$0.205 \pm 0.004$
	TAPE THICKNESS	$T_t$	$0.062 \pm 0.001$	$0.0025 \pm 0.00004$
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	$F$	$3.50 \pm 0.05$	$0.138 \pm 0.002$
	CAVITY TO PERFORATION (LENGTH DIRECTION)	$P_2$	$2.00 \pm 0.05$	$0.079 \pm 0.002$
ANGLE	FOR SOT-323 (SC70-3 LEAD) FOR SOT-363 (SC70-6 LEAD)	$A_n$	8: C MAX 10: C MAX	

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AV02-0402EN - December 22, 2009

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