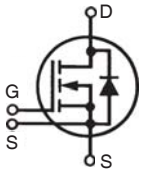
IXYS

Advance Technical Information

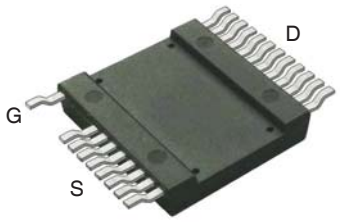
TrenchT4™ Power MOSFET

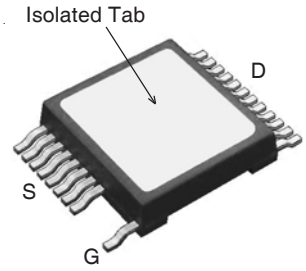
MMIX1T660N04T4

V_{DSS} = 40V
I_{D25} = 660A
$R_{DS(on)}$ ≤ 0.85mΩ



N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode





G = Gate D = Drain
S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 175°C	40	V
V_{DGR}	T_J = 25°C to 175°C, R_{GS} = 1MΩ	40	V
V_{GSM}	Transient	±15	V
I_{D25}	T_C = 25°C (Chip Capability)	660	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	2600	A
I_A	T_C = 25°C	330	A
E_{AS}	T_C = 25°C	5	J
P_D	T_C = 25°C	830	W
T_J		-55 ... +175	°C
T_{JM}		175	°C
T_{stg}		-55 ... +175	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	Plastic Body for 10s	260	°C
V_{ISOL}	50/60 Hz, 1 Minute	2500	V~
F_C	Mounting Force	50..200 / 11..45	N/lb.
Weight		8	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 250μA	40			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250μA	2.0		4.0	V
I_{GSS}	V_{GS} = ±15V, V_{DS} = 0V			±200	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0V			10	μA
	T_J = 150°C			1.5	mA
$R_{DS(on)}$	V_{GS} = 10V, I_D = 100A, Note 1			0.85	mΩ

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Substrate
  - Excellent Thermal Transfer
  - Increased Temperature and Power Cycling Capability
  - High Isolation Voltage (2500V~)
- 175°C Operating Temperature
- High Current Handling Capability
- Fast Intrinsic Diode
- Avalanche Rated
- Low $R_{DS(on)}$

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- DC-DC Converters and Offi-Line UPS
- Primary-Side Switch
- High Speed Power Switching Applications

© 2016 IXYS CORPORATION, All Rights Reserved

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.
g_{fs}	V_{DS} = 10V, I_D = 60A, Note 1	110	180	S
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		44.0	nF
C_{oss}			6.5	nF
C_{rss}			3.5	nF
R_{Gi}	Gate Input Resistance		2.5	Ω
$t_{d(on)}$	**Resistive Switching Times** V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{DSS} R_G = 1Ω (External)		40	ns
t_r			430	ns
$t_{d(off)}$			386	ns
t_f			260	ns
$Q_{g(on)}$	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{DSS}		860	nC
Q_{gs}			240	nC
Q_{gd}			290	nC
R_{thJC}				0.18 °C/W
R_{thCS}			0.05	°C/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
I_S	V_{GS} = 0V			660	A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			2640	A
V_{SD}	I_F = 100A, V_{GS} = 0V, Note 1			1.4	V
t_{rr}	I_F = 150A, V_{GS} = 0V -di/dt = 100A/μs V_R = 30V		60		ns
I_{RM}			2.1		A
Q_{RM}			63		nC

Note 1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,860,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405 B2 6,710,463 6,727,585 6,759,692 6,771,478 B2 7,005,734 B2 7,063,975 B2 7,071,537 7,157,338B2

Fig. 1. Output Characteristics @ T_J = 25ºC

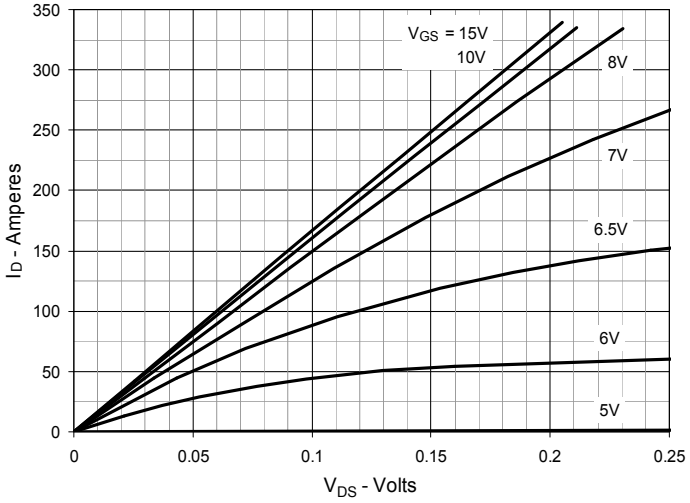


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

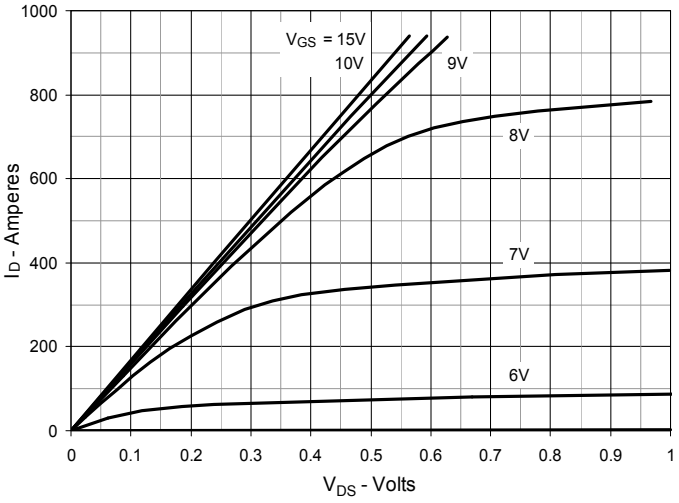


Fig. 3. Output Characteristics @ T_J = 150ºC

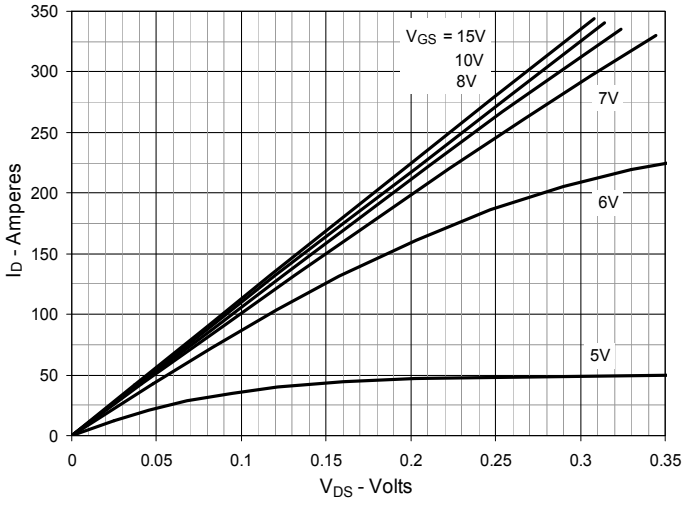


Fig. 4. Normalized $R_{DS(on)}$ vs. Junction Temperature

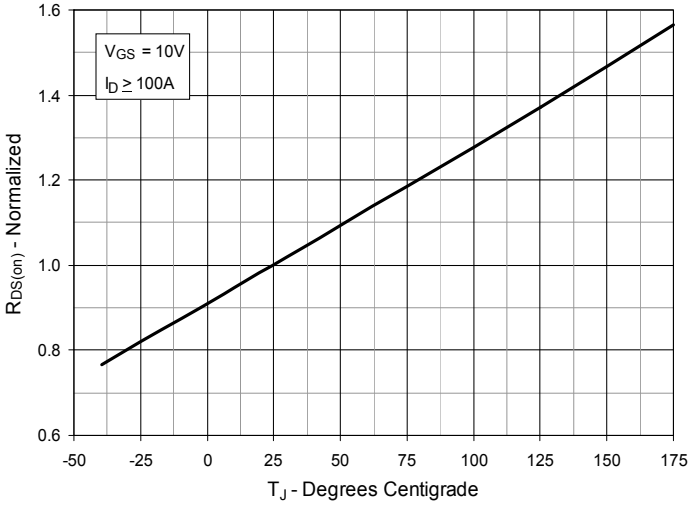


Fig. 5. Normalized $R_{DS(on)}$ to I_D = 100A vs. Drain Current

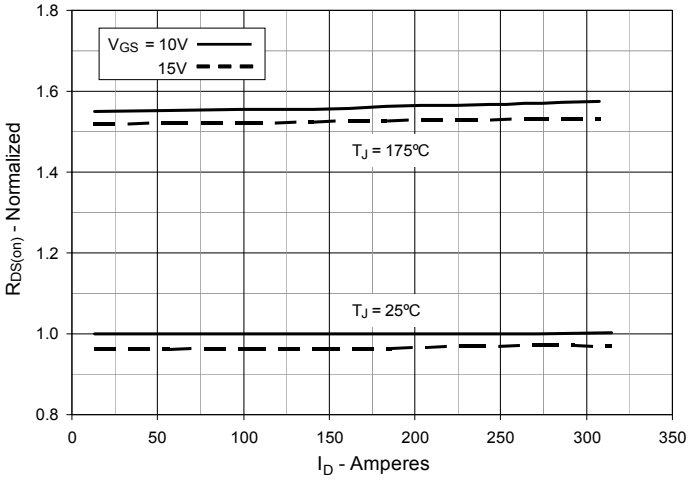
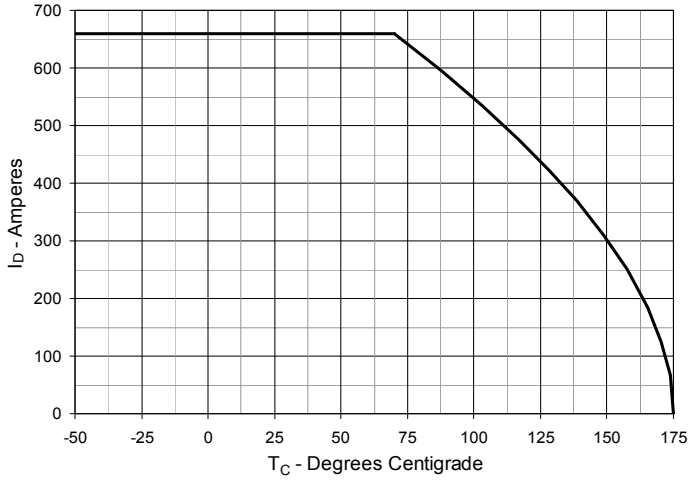


Fig. 6. Drain Current vs. Case Temperature



© 2016 IXYS CORPORATION, All Rights Reserved

Fig. 7. Input Admittance

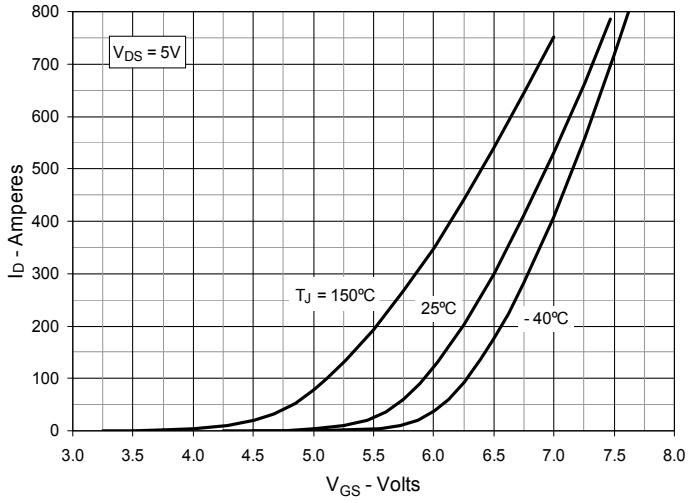


Fig. 8. Transconductance

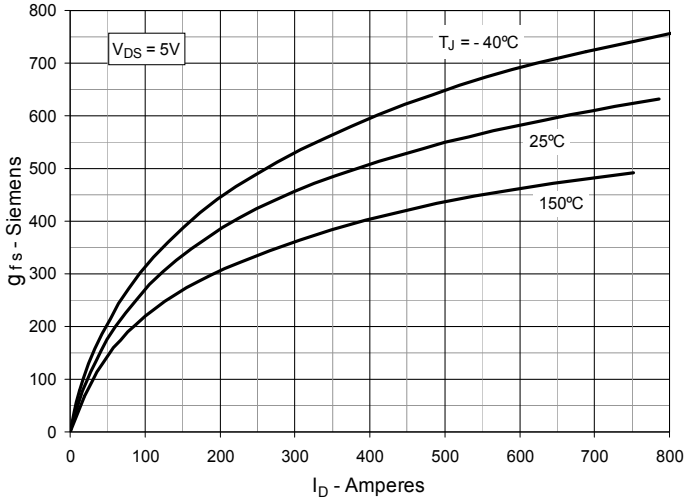


Fig. 9. Forward Voltage Drop of Intrinsic Diode

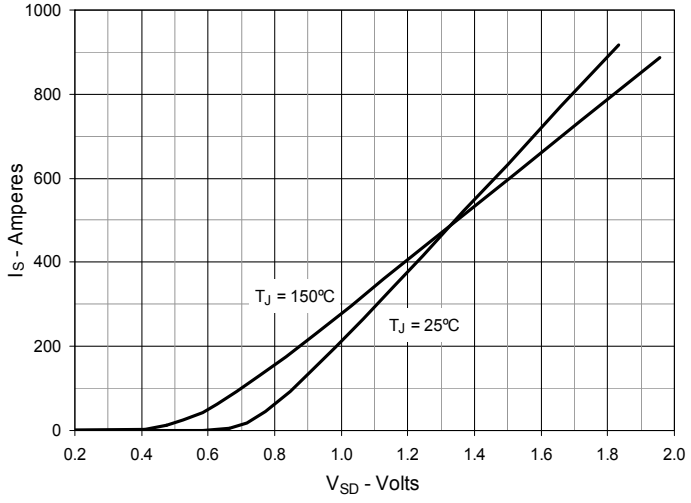


Fig. 10. Gate Charge

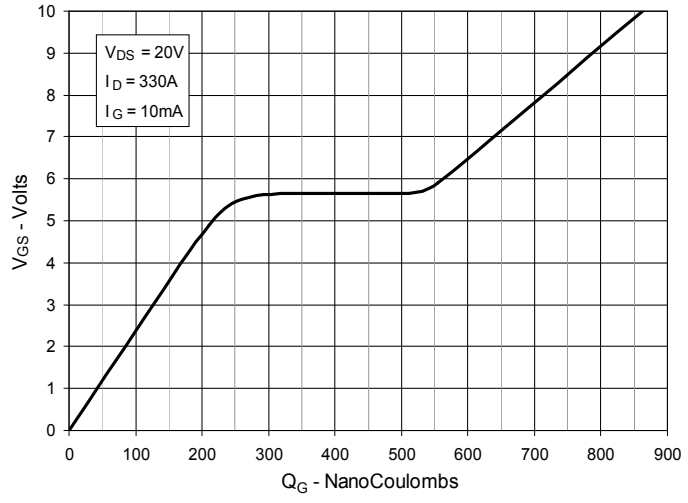


Fig. 11. Capacitance

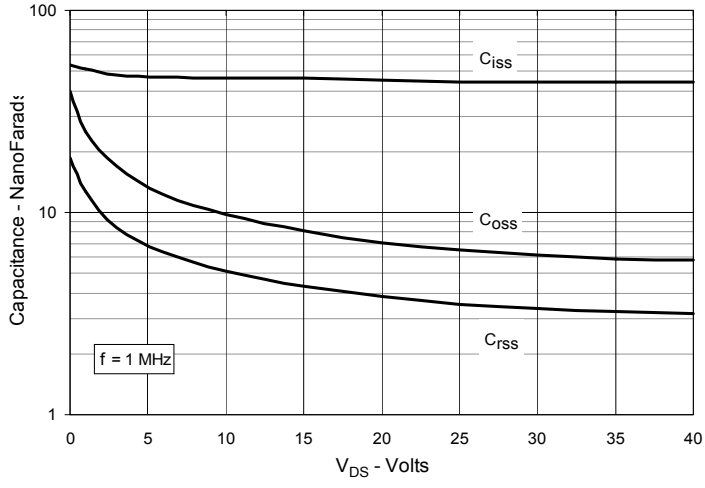
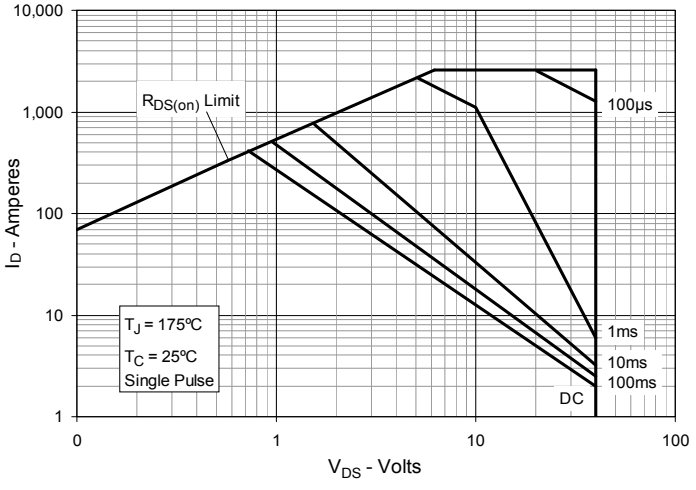


Fig. 12. Forward-Bias Safe Operating Area



IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

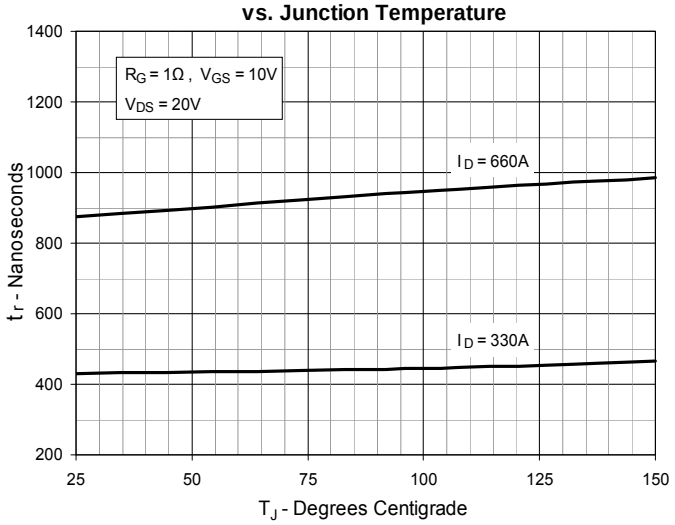


Fig. 14. Resistive Turn-on Rise Time vs. Drain Current

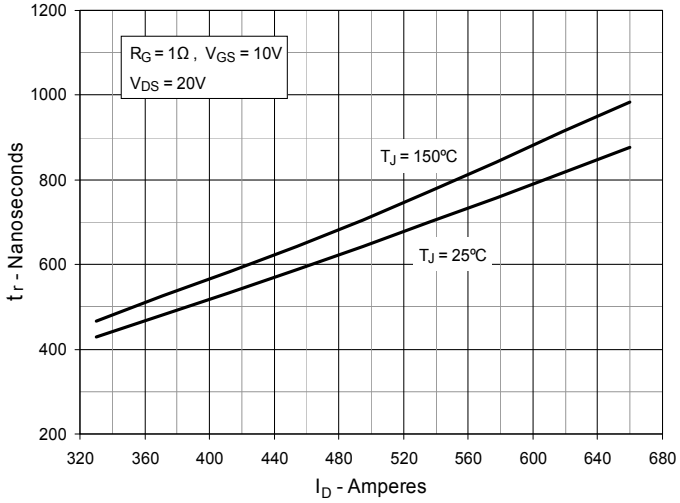


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

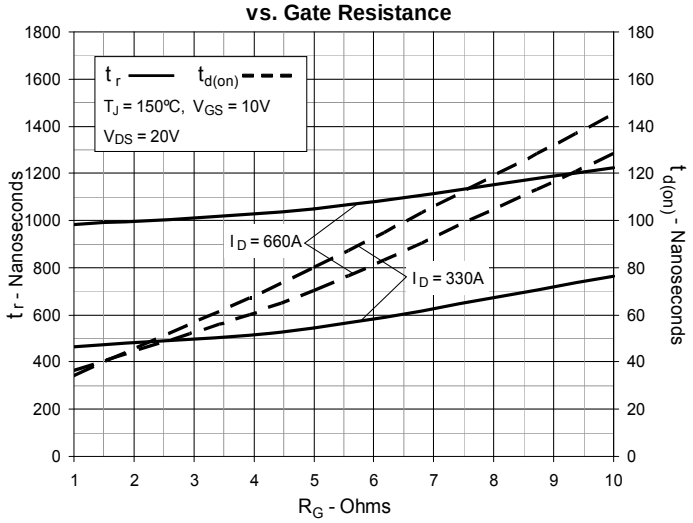


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

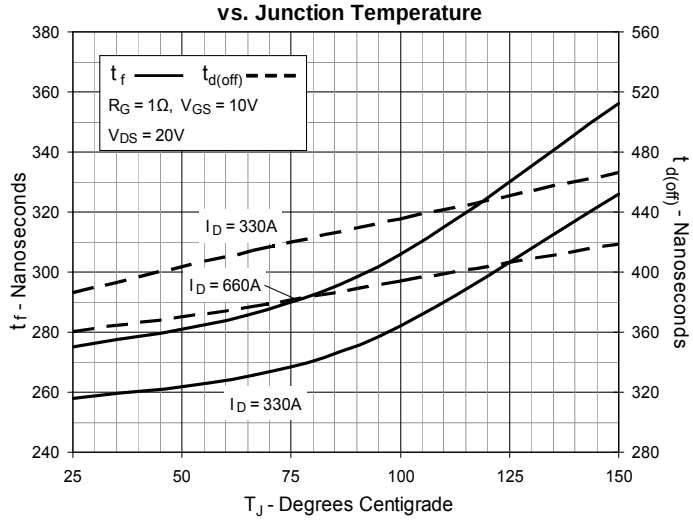


Fig. 17. Resistive Turn-off Switching Times vs. Drain Current

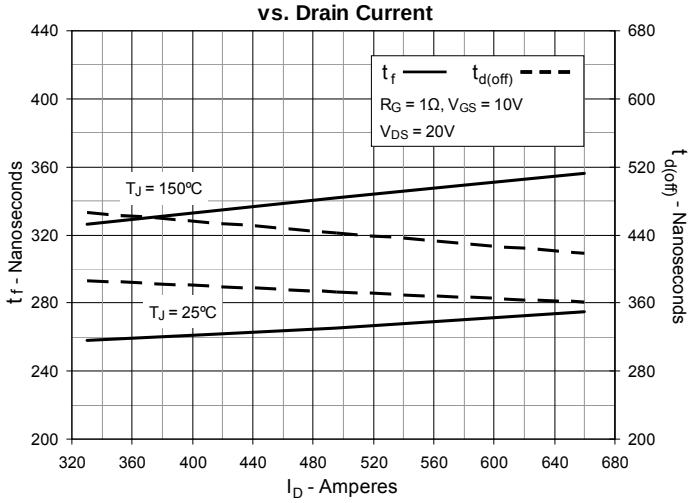
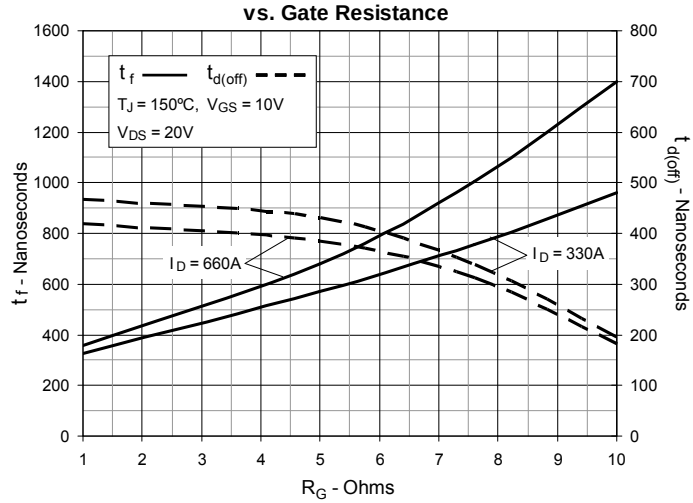
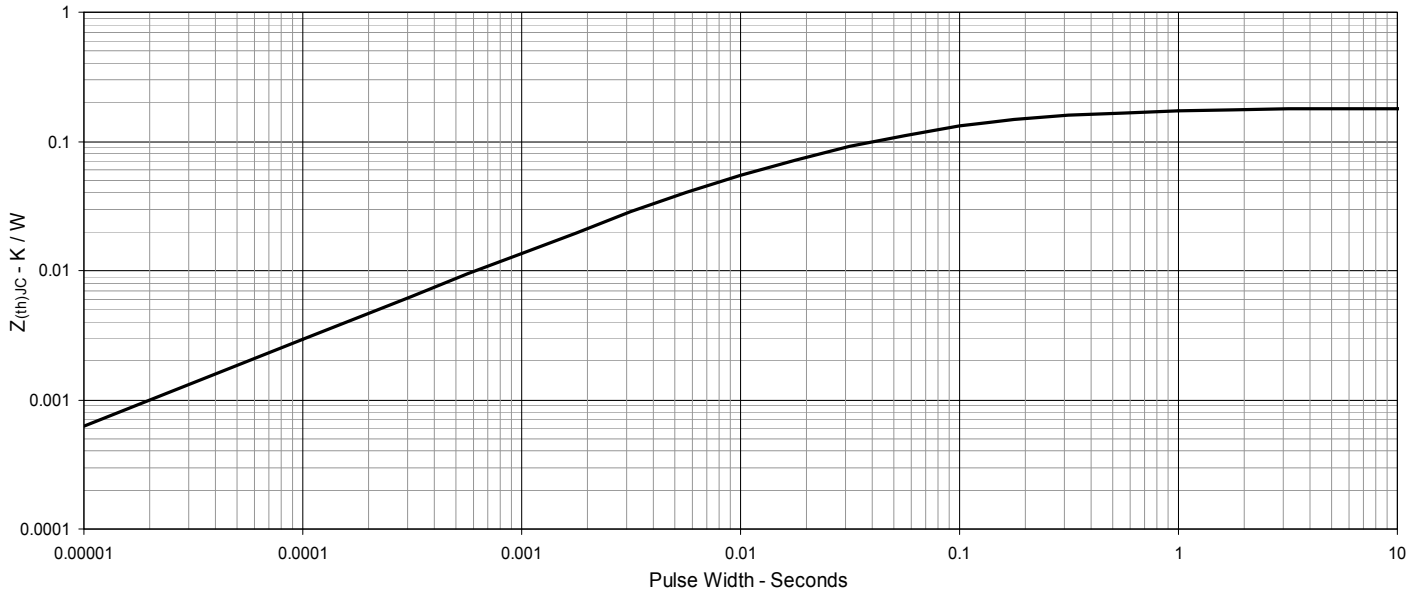


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance

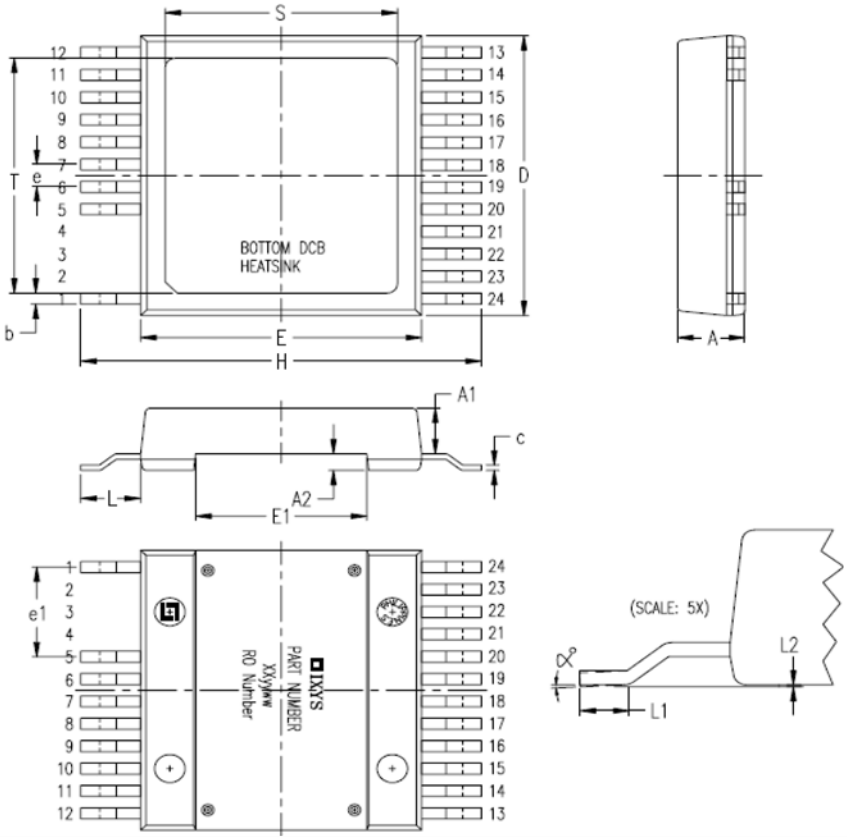


© 2016 IXYS CORPORATION, All Rights Reserved

Fig. 19. Maximum Transient Thermal Impedance



Package Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.209	.224	5.30	5.70
A1	.154	.161	3.90	4.10
A2	.055	.063	1.40	1.60
b	.035	.045	0.90	1.15
c	.018	.026	0.45	0.65
D	.976	.994	24.80	25.25
E	.898	.915	22.80	23.25
E1	.543	.559	13.80	14.20
e	.079 BSC		2.00 BSC	
e1	.315 BSC		8.00 BSC	
H	1.272	1.311	32.30	33.30
L	.181	.209	4.60	5.30
L1	.051	.067	1.30	1.70
L2	.000	.006	0.00	0.15
S	.736	.760	18.70	19.30
T	.815	.839	20.70	21.30
∝	0	4°	0	4°

PIN: 1 = Gate
5-12 = Source
13-24 = Drain

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.