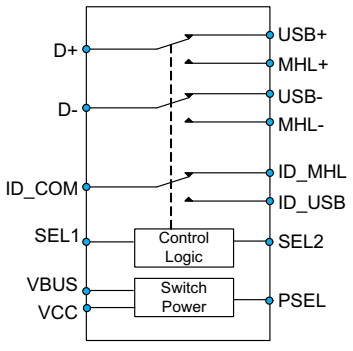
TS3USB3200 SPDT USB 2.0 High-Speed (480 Mbps) and Mobile High-Definition Link (MHL) or Mobility Display Port (MyDP) Switch With additional SPDT ID Select Switch and Flexible Power Control

1 Features

- V_{CC} Range: 2.7 V to 4.3 V
- Mobile High-Definition Link (MHL) or Mobility Display Port (MyDP) Switch
  - Bandwidth (–3 dB): 5.5 GHz
  - Ron (Typical): 5.7 Ω
  - Con (Typical): 2.5 pF
- USB Switch
  - Bandwidth (–3 dB): 5.5 GHz
  - Ron (Typical): 4.6 Ω
  - Con (Typical): 2.5 pF
- Current Consumption: 40 µA Typical
- Special Features
  - Flexible Power Control: Device Can be Powered by V_{BUS} Without V_{CC} or by V_{CC} Alone
  - I_{OFF} Protection Prevents Current Leakage in Powered-Down State (V_{CC} and V_{BUS}= 0 V)
  - 1.8-V Compatible Control Inputs (SEL1, SEL2, and PSEL)
  - Overvoltage Tolerance (OVT) on All I/O Pins up to 5.5 V Without External Components
- ESD Performance:
  - 3.5-kV Human-Body Model (A114B, Class II)
  - 1-kV Charged Device Model (C101)
- Package:
  - 16-Pin UQFN Package (2.6 × 1.8 mm, 0.4-mm Pitch)

Switch Diagram



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2 Applications

- USB 2.0 Applications
- Mobile High-Definition Link (MHL) Applications
- Mobility Display Port (MyDP) Applications
- Mobile Phones

3 Description

The TS3USB3200 is a differential single-pole, double throw (SPDT) multiplexer that includes a high-speed Mobile High-Definition Link (MHL) or Mobility Display Port (MyDP) switch and a USB 2.0 High-Speed (480 Mbps) switch in the same package. Additionally included is a single-pole, double throw (SPDT) USB/MHL or MyDP ID switch for easy information control. These configurations allow the system designer to use a common USB or Mico-USB connector for both MHL/MyDP video signals and USB data.

The TS3USB3200 has a V_{CC} range of 2.7 V to 4.3 V and also has the option to be powered by V_{BUS} without V_{CC}. The device supports a overvoltage tolerance (OVT) feature which allows the I/O pins to withstand overvoltage conditions (up to 5.5 V). The power-off protection feature forces all I/O pins to be in high impedance mode when power is not present. This allows full isolation of the signals lines without excessive leakage current. The select pins of TS3USB3200 are compatible with 1.8-V control voltage, allowing them to be directly interfaced with the General Purpose I/O (GPIO) from a mobile processor.

The TS3USB3200 comes with a small 16-pin UQFN package (2.6 mm × 1.8 mm in size), which makes it a perfect candidate for mobile applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3USB3200	UQFN (16)	2.60 mm × 1.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2013) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Removed *Ordering Information* table, see POA at the end of the data sheet ... 1
- Changed *Thermal Information* table ... 4

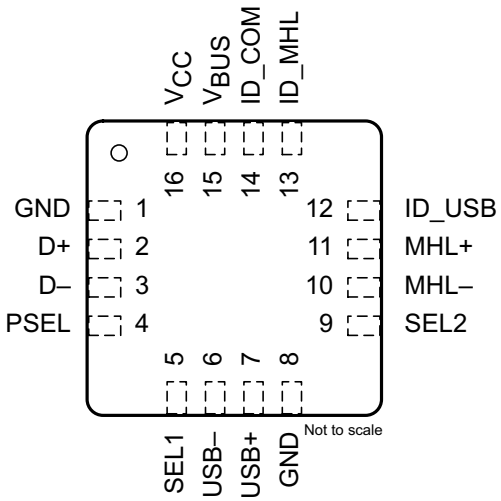
Changes from Original (June 2012) to Revision A **Page**

- Added Mobility Display Port (MyDP) option functionality. ... 1
- Changed $V_{I/O}$ MIN value from –0.3 to –0.5. ... 4
- Updated Typical Application diagrams. ... 11

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5 Pin Configuration and Functions

RSV Package
16-Pin UQFN
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	GND	Ground	Ground
2	D+	I/O	Data Signal Path (Differential +)
3	D–	I/O	Data Signal Path (Differential –)
4	PSEL	Input	Power Source Select Line
5	SEL1	Input	Control Input Select Line 1
6	USB–	I/O	USB Data Signal Path (Differential –)
7	USB+	I/O	USB Data Signal Path (Differential +)
8	GND	Ground	Ground
9	SEL2	Input	Control Input Select Line 2
10	MHL–	I/O	MHL Data Signal Path (Differential–)
11	MHL+	I/O	MHL Data Signal Path (Differential +)
12	ID_USB	I/O	ID Signal Path for USB
13	ID_MHL	I/O	ID Signal Path for MHL
14	ID_COM	I/O	ID Common Signal Path
15	V_{BUS}	Power	Alternative Device Power
16	V_{CC}	Power	Power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
V_{CC} ,V_{BUS}	Supply voltage(3)		–0.3	5.5	V
$V_{I/O}$	Input/Output DC voltage(3)		–0.5	5.5	V
I_K	Input/Output port diode current	$V_{I/O}$ < 0	–50		mA
V_I	Digital input voltage range (SEL1, SEL2, PSEL)		–0.3	5.5	V
I_{IK}	Digital logic input clamp current(3)	V_I < 0	–50		mA
I_{CC}	Continuous current through V_{CC}			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	4.3	V
V_{BUS}	V_{BUS} Supply voltage	4.3	5.5	V
$V_{I/O\ (USB)}$ $V_{I/O\ (ID)}$	Analog voltage for USB and ID signal path	0	3.6	V
$V_{I/O\ (MHL)}$	Analog voltage for MHL signal path	1.6	3.4	V
V_I	Digital input voltage (SEL1, SEL2, PSEL)	0	V_{CC}	V
$T_{RAMP\ (VCC)}$	Power supply ramp time requirement (V_{CC})	100	1000	µs/V
$T_{RAMP\ (VBUS)}$	Power supply ramp time requirement (V_{BUS})	100	1000	µs/V
T_A	Operating free-air temperature	–40	85	ºC

6.4 Thermal Information

THERMAL METRIC(1)		TS3USB3200 RSV (UQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	109.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

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6.5 Electrical Characteristics

T_A = –40°C to 85°C, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
MHL SWITCH							
R_{ON}	ON-state resistance	V_{CC} = 2.7 V	$V_{I/O}$ = 1.6 V, I_{ON} = –8 mA		5.7		Ω
ΔR_{ON}	ON-state resistance match between + and – paths	V_{CC} = 2.7 V	$V_{I/O}$ = 1.6 V, I_{ON} = –8 mA		0.4		Ω
$R_{ON\ (FLAT)}$	ON-state resistance flatness	V_{CC} = 2.7 V	$V_{I/O}$ = 1.6 V to 3.4 V, I_{ON} = –8 mA		1		Ω
I_{OZ}	OFF leakage current	V_{CC} = 4.3 V	Switch OFF, $V_{MHL+/MHL-}$ = 1.6 V to 3.4 V, $V_{D+/D-}$ = 0 V	–2		2	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0 V	Switch ON or OFF, $V_{MHL+/MHL-}$ = 1.6 V to 3.4 V, $V_{D+/D-}$ = NC	–10		10	µA
I_{ON}	ON leakage current	V_{CC} = 4.3 V	Switch ON, $V_{MHL+/MHL-}$ = 1.6 V to 3.4 V, $V_{D+/D-}$ = NC	–2		2	µA
USB SWITCH							
R_{ON}	ON-state resistance	V_{CC} = 2.7 V	$V_{I/O}$ = 0.4 V, I_{ON} = –8 mA		4.6		Ω
ΔR_{ON}	ON-state resistance match between + and – paths	V_{CC} = 2.7 V	$V_{I/O}$ = 0.4 V, I_{ON} = –8 mA		0.4		Ω
$R_{ON\ (FLAT)}$	ON-state resistance flatness	V_{CC} = 2.7 V	$V_{I/O}$ = 0 V to 0.4 V, I_{ON} = –8 mA		1		Ω
I_{OZ}	OFF leakage current	V_{CC} = 4.3 V	Switch OFF, $V_{USB+/USB-}$ = 0 V to 4.3 V, $V_{D+/D-}$ = 0 V	–2		2	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0 V	Switch ON or OFF, $V_{USB+/USB-}$ = 0 V to 4.3 V, $V_{D+/D-}$ = NC	–10		10	µA
I_{ON}	ON leakage current	V_{CC} = 4.3 V	Switch ON, $V_{USB+/USB-}$ = 0 V to 4.3 V, $V_{D+/D-}$ = NC	–2		2	µA
ID SWITCH							
R_{ON}	ON-state resistance	V_{CC} = 2.7 V	$V_{I/O}$ = 3.3 V, I_{ON} = –8 mA		6.5		Ω
ΔR_{ON}	ON-state resistance match between + and – paths	V_{CC} = 2.7 V	$V_{I/O}$ = 3.3 V, I_{ON} = –8 mA		0.4		Ω
I_{OZ}	OFF leakage current	V_{CC} = 4.3 V	Switch OFF, V_{ID_MHL/ID_USB} = 0 V to 4.3 V, V_{ID_COM} = 0 V	–1		1	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0 V	Switch ON or OFF, V_{ID_MHL/ID_USB} = 0 V to 4.3 V, V_{ID_COM} = NC	–10		10	µA
I_{ON}	ON leakage current	V_{CC} = 4.3 V	Switch ON, V_{ID_MHL/ID_USB} = 0 V to 4.3 V, V_{ID_COM} = 0 V	–1		1	µA
DIGITAL CONTROL INPUTS (SEL1, SEL2, PSEL)							
V_{IH}	Input logic high	V_{CC} = 2.7 V to 4.3 V		1.3			V
V_{IL}	Input logic low	V_{CC} = 2.7 V to 4.3 V				0.6	V
I_{IN}	Input leakage current	V_{CC} = 4.3 V, $V_{I/O}$ = 0 V to 4.3 V, V_{IN} = 0 V to 2 V		–10		10	µA

6.6 Dynamic Characteristics

T_A = –40°C to 85°C, Typical values are at V_{CC} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
MHL(1)/USB/ ID SWITCH							
t_{pd}	Propagation Delay	R_L = 50 Ω, C_L = 5 pF	V_{CC} = 2.7 V to 4.3 V		0.1		ns
t_{ON}	Turnon time	R_L = 50 Ω, C_L = 5 pF	V_{CC} = 2.7 V to 4.3 V			400	ns
t_{OFF}	Turnoff time	R_L = 50 Ω, C_L = 5 pF	V_{CC} = 2.7 V to 4.3 V			400	ns
$t_{SK(P)}$	Skew of opposite transitions of same output	V_{CC} = 2.7 V or 3.3V	V_{CC} = 2.7 V to 4.3 V		0.1	0.2	ns
$C_{ON(MHL)}$	MHL path ON capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 or 3.3 V, f = 240 MHz	Switch ON		1.6		pF
$C_{ON(USB)}$	USB path ON capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 or 3.3 V, f = 240 MHz	Switch ON		1.4		pF
$C_{OFF(MHL)}$	MHL path OFF capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 or 3.3 V, f = 240 MHz	Switch OFF		1.4		pF
$C_{OFF(USB)}$	USB path OFF capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 or 3.3 V, f = 240 MHz	Switch OFF		1.6		pF
C_I	Digital input capacitance	V_{CC} = 3.3 V, V_I = 0 or 2V			2.2		pF

(1) Specified by Design

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Dynamic Characteristics (continued)

T_A = –40°C to 85°C, Typical values are at V_{CC} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
O_{ISO}	OFF Isolation	V_{CC} = 2.7 V to 4.3 V, R_L = 50 Ω, f = 240 MHz	Switch OFF		–37		dB
X_{TALK}	Crosstalk	V_{CC} = 2.7 V to 4.3 V, R_L = 50 Ω, f = 240 MHz	Switch ON		–37		dB
$BW_{(MHL)}$	MHL path –3-dB bandwidth	V_{CC} = 2.7 V to 4.3 V, R_L = 50 Ω	Switch ON		5.5		GHz
$BW_{(USB)}$	USB path –3-dB bandwidth	V_{CC} = 2.7 V to 4.3 V, R_L = 50 Ω	Switch ON		5.5		GHz
$BW_{(ID)}$	ID path –3-dB bandwidth	V_{CC} = 2.7 V to 4.3 V, R_L = 50 Ω	Switch ON		4		GHz
SUPPLY							
V_{BUS}	V_{BUS} Power supply voltage			4.3		5.5	V
V_{CC}	Power supply voltage			2.7		4.3	V
I_{CC}	Positive supply current	V_{CC} = 4.3 V, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 0 V	Switch ON or OFF		40	70	µA
$I_{CC, VBUS}$	Positive supply current (V_{BUS} mode)	V_{CC} = 0 V, V_{BUS} = 5.5 V, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 0 V	Switch ON or OFF			50	µA

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6.7 Typical Characteristics

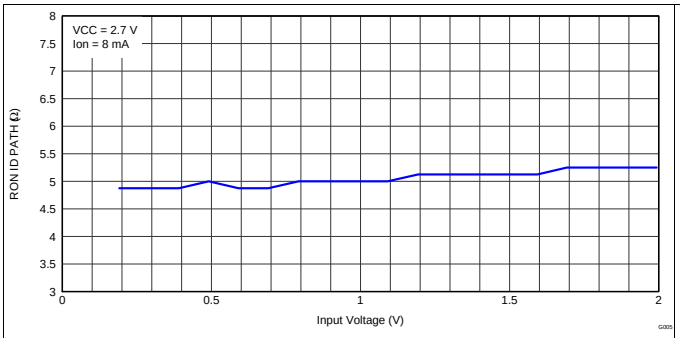


Figure 1. ON-Resistance vs VI for MHL Switch

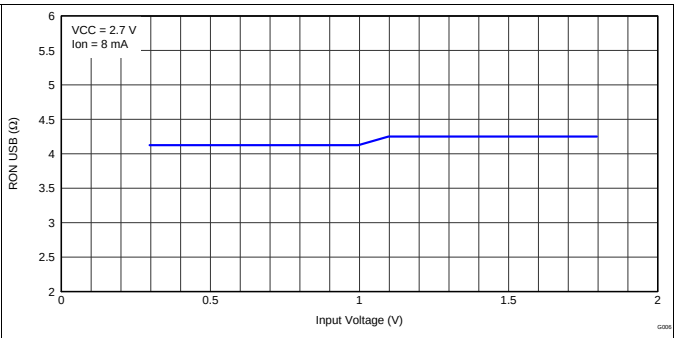


Figure 2. ON-Resistance vs VI for USB Switch

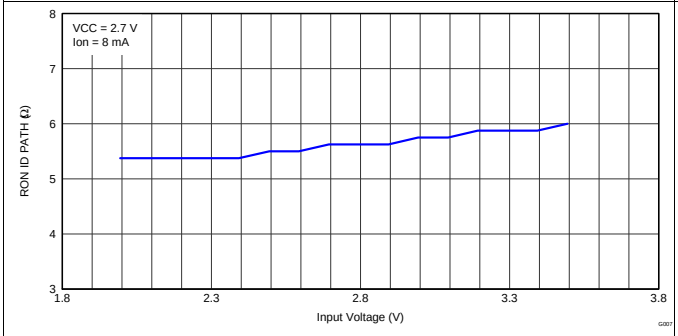


Figure 3. ON-Resistance vs VI for ID Switch

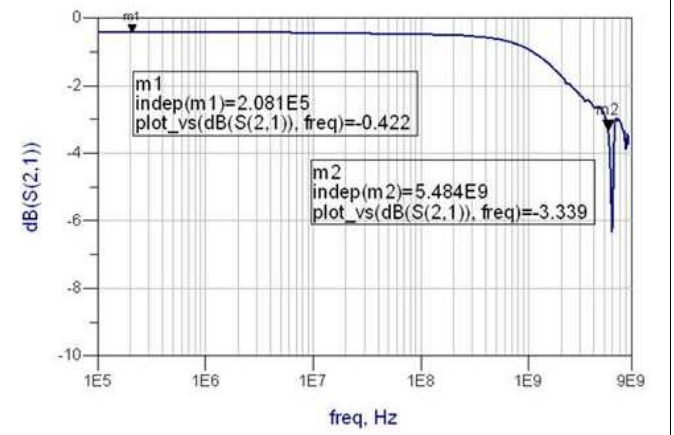


Figure 4. Gain vs Frequency for MHL Switch

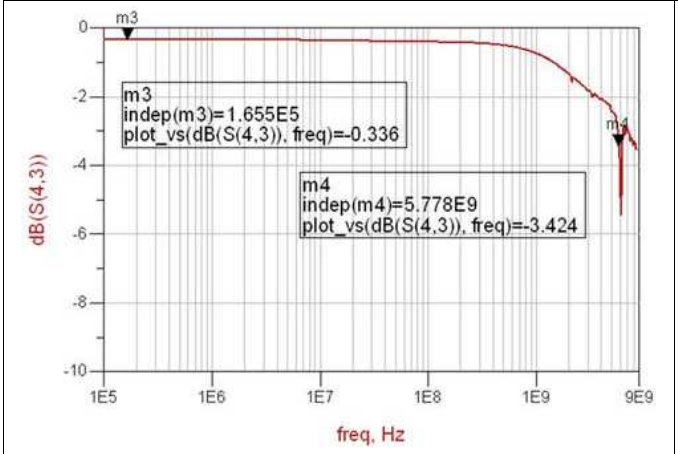


Figure 5. Gain vs Frequency for USB Switch

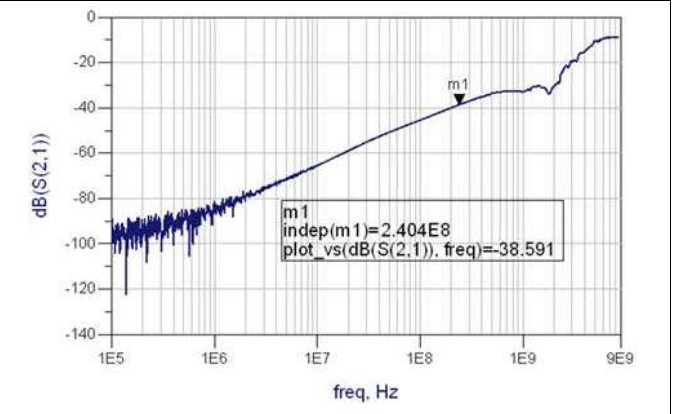


Figure 6. Off Isolation vs Frequency for MHL Path

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Typical Characteristics (continued)

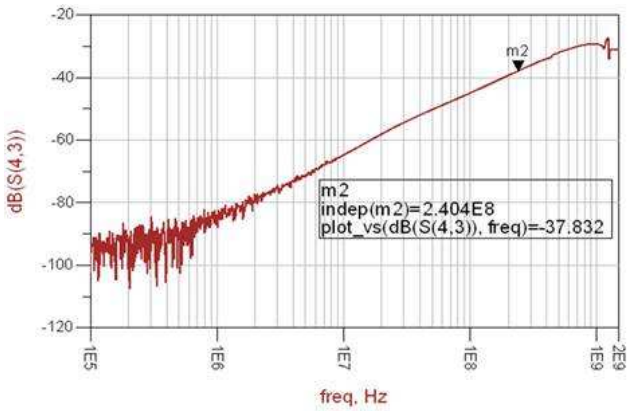


Figure 7. Off Isolation vs Frequency for USB Path

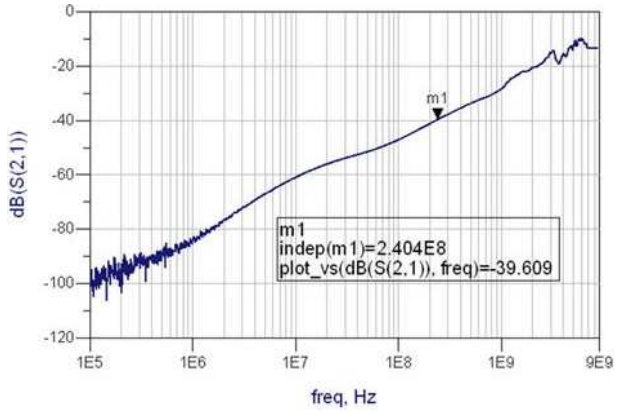


Figure 8. Crosstalk vs Frequency for MHL Path

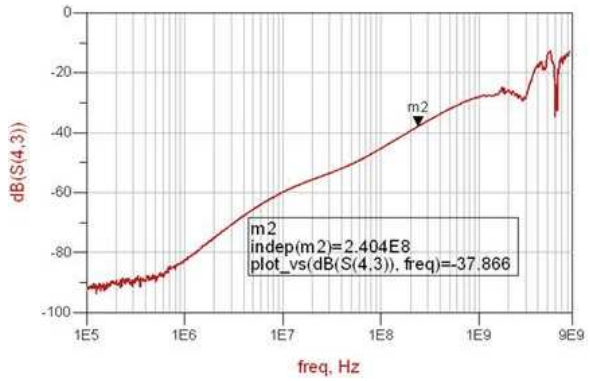


Figure 9. Crosstalk vs Frequency for USB Path

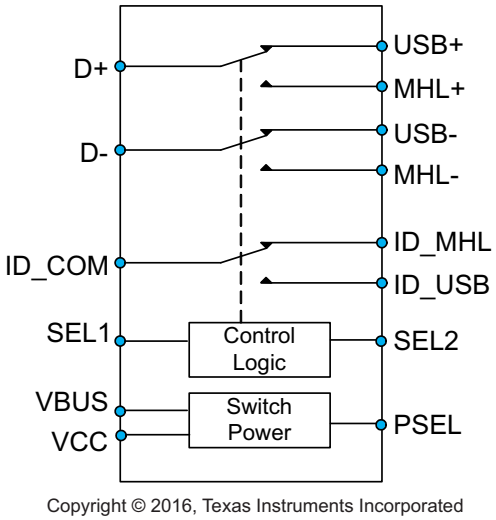
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7 Detailed Description

7.1 Overview

The TS3USB3200 supports high-speed Mobile High-Definition Link (MHL) or Mobility Display Port (MyDP) switching, as well as USB 2.0 High-Speed (480 Mbps) switching in the same package. An additional integrated ID switch is also included to support USB/MHL or MyDP ID for easy information control. These configurations allow the system designer to use a common USB or Mico-USB connector to support both MHL/MyDP video signals and USB data.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Flexible Power Control

Device can be powered by V_{BUS} or by V_{CC}. This allows the device to run off a 4.3-V battery voltage or 5 V from an external USB device. If both a battery and external USB device are supplying voltage on the V_{CC} and V_{BUS} pins the PSEL can be used to select which power supply is used to save battery power.

7.3.2 I_{OFF} Protection Prevents Current Leakage in Powered Down State (V_{CC} and V_{BUS}= 0 V)

When there is no power supplied to the IC, all of the I/O signal paths are placed in a high impedance state, which isolates the data paths when they are not being used.

7.3.3 1.8-V Compatible Control Inputs (SEL1, SEL2, and PSEL)

The TS3USB3200 logic control input pins can operate with 1.8-V logic since the V_{IH} minimum for the SEL1, SEL2, and PSEL is 1.3 V.

7.4 Device Functional Modes

The TS3USB32000 device can select which power supply pin V_{CC} or V_{BUS} will power the device when voltages are present on both pins.

Table 1. Function Table (Power Source)

V_{CC}	V_{BUS}	PSEL (1)	POWER SOURCE
L	L	X	No Power. All I/O in High-Z
L	H	X	V_{BUS}
H	L	X	V_{CC}
H	H	L	V_{CC}
H	H	H	V_{BUS}

(1) The PSEL pin has 6-MΩ weak pulldown resistor to GND to make its default value to be LOW.

Table 2. Function Table (Signal and ID Select)

SEL1 (1)	SEL2 (1)	CONNECTION	High-Z
L	L	D+/D– to USB+/USB–, ID_COM to ID_USB	MHL+/MHL–, ID_MHL
L	H	D+/D– to USB+/USB–, ID_COM to ID_MHL	MHL+/MHL–, ID_USB
H	L	D+/D– to MHL+/MHL–, ID_COM to ID_USB	USB+/USB–, ID_MHL
H	H	D+/D– to MHL+/MHL–, ID_COM to ID_MHL	USB+/USB–, ID_USB

(1) The SEL1 and SEL2 pins have 6-MΩ weak pulldown resistor to GND to make their default value to be LOW.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

For Mobility Display Port Applications (MyDP) the signal voltage must be biased to ensure that the signal never exceeds the *Recommended Operating Conditions* for the TS3USB3200. Namely the $V_{I/O}$ must never operate outside the range of 0 V to 3.6 V.

The control pins (SEL1 and SEL2) have built-in 6-MΩ pulldown resistors to ensure the USB paths are enabled for TS3USB3200 and allow connectivity to the TSU5611 USB accessory switch.

8.2 Typical Applications

8.2.1 TS3USB3200 Configured to be Powered by VBUS Through the MicroUSB Connector

During manufacturing test when battery power is not available, the TS3USB3200 can be configured, as shown in Figure 10, to be powered by VBUS through the microUSB connector.

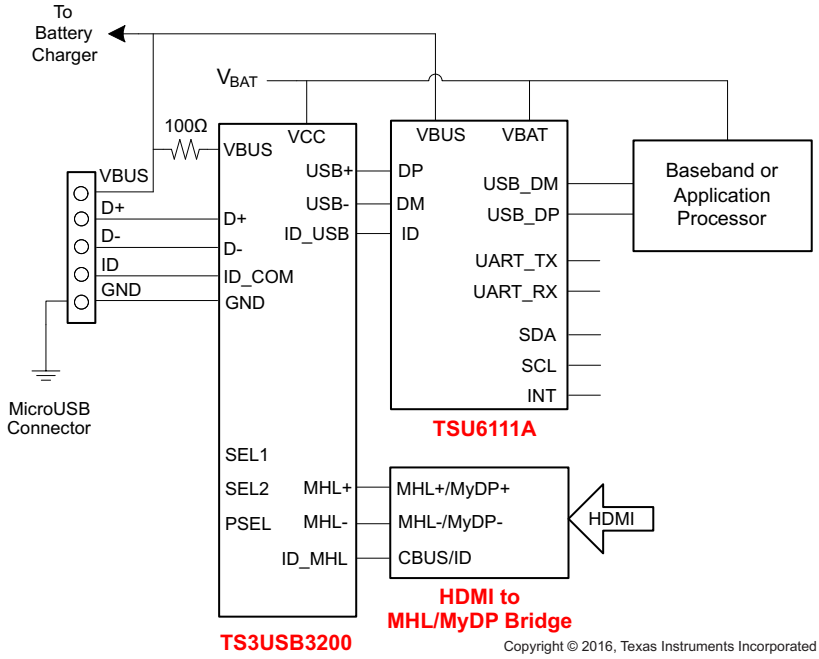


Figure 10. Typical Application Schematic Powered by VBUS

8.2.1.1 Design Requirements

Design requirements of the MHL and USB 1.0,1.1, and 2.0 standards must be followed. The TS3USB3200 has internal 6-MΩ pulldown resistors on SEL and $\overline{OE}$, so no external resistors are required on the logic pins. The internal pulldown resistor on SEL ensures the USB channel is selected by default. The internal pulldown resistor on $\overline{OE}$ enables the switch when power is applied to VCC.

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

The TS3USB3200 can be properly operated without any external components. However, TI recommends that unused pins must be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device.

8.2.1.3 Application Curves

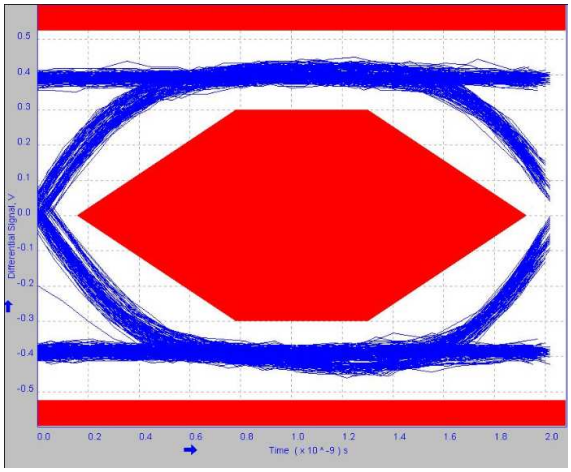


Figure 11. 480-Mbps USB 2.0 Eye Pattern With No Device

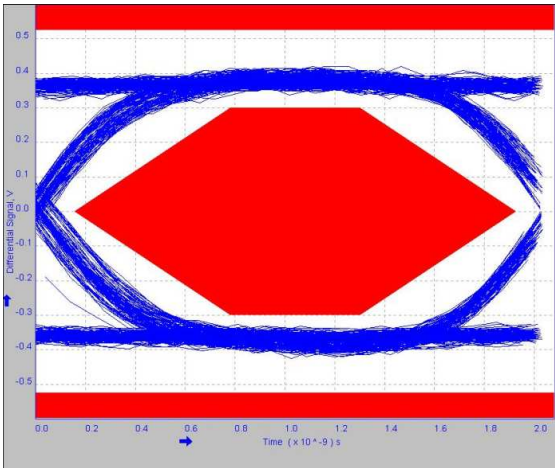


Figure 12. 480-Mbps USB 2.0 Eye Pattern for USB Switch

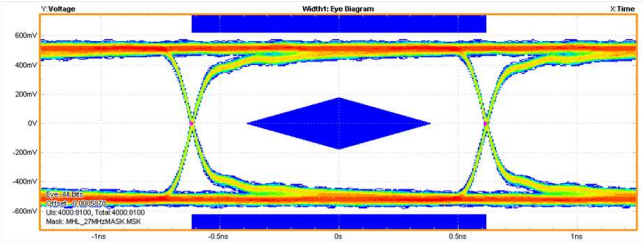


Figure 13. Eye Pattern: 0.7-Gbps MHL Eye Pattern for With No Device

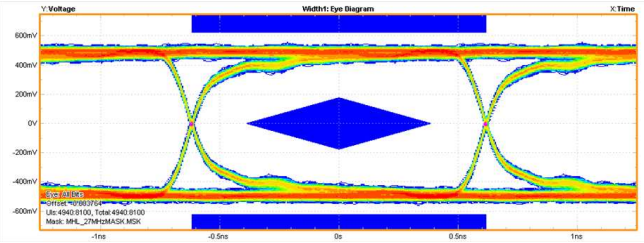


Figure 14. Eye Pattern: 0.7-Gbps MHL Eye Pattern for MHL Switch

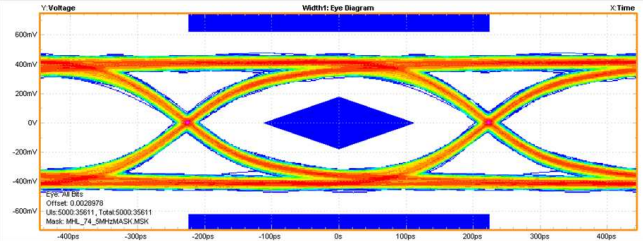


Figure 15. Eye Pattern: 2.2-Gbps MHL Eye Pattern for With No Device

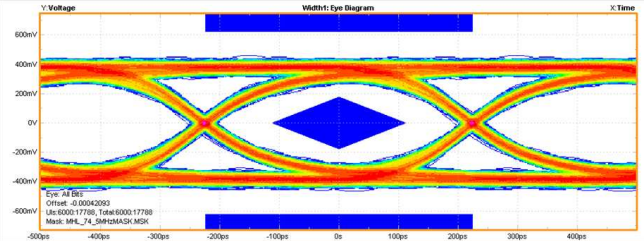


Figure 16. Eye Pattern: 2.2-Gbps MHL Eye Pattern for MHL Switch

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Typical Applications (continued)

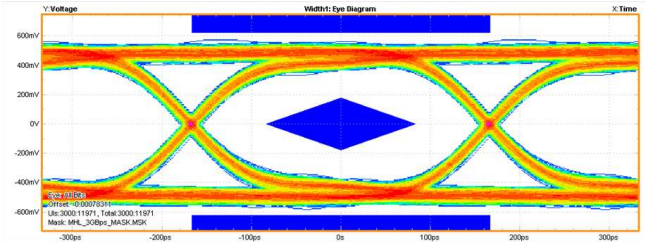


Figure 17. Eye Pattern: 3-Gbps MHL Eye Pattern for With No Device

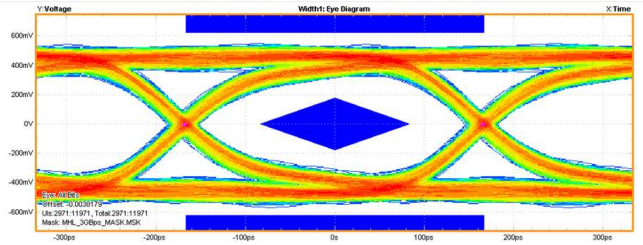


Figure 18. Eye Pattern: 3-Gbps MHL Eye Pattern for MHL Switch

8.2.2 TS3USB3200 Powered by Mobile Device's Standalone Battery

The TS3USB3200 can also be powered by the mobile device's standalone battery. Figure 19 shows a typical implementation. The VBUS pin of the TS3USB3200 can simply be grounded under such conditions.

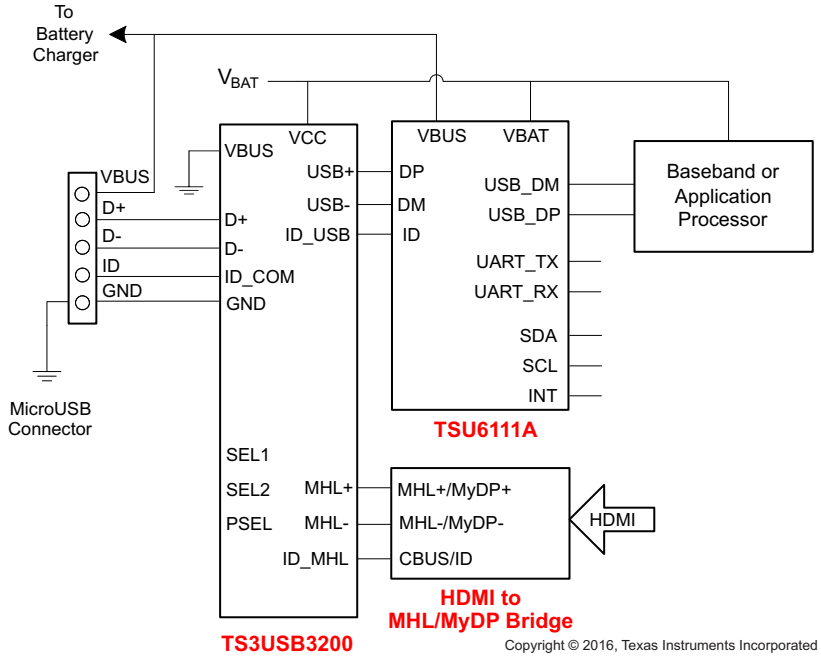


Figure 19. Typical Application Schematic Powered by Mobile Devices

8.2.2.1 Design Requirements

The TS3USB3200 can be properly operated without any external components. However, TI recommends that unused pins must be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device.

8.2.2.2 Detailed Design Procedure

The VBUS pin of the TS3USB3200 can simply be grounded under such conditions.

9 Power Supply Recommendations

Power to the device is supplied through the VCC pin and must follow the USB 1.0, 1.1, and 2.0 standards. TI recommends placing a bypass capacitor as close to the supply pin VCC as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

10 Layout

10.1 Layout Guidelines

Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass capacitors near the D+/D– traces.

The high-speed D+/D- must match and be no more than 4 inches long; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D– traces must match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or ICs that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub must be less than 200 mm.

Route all high-speed USB signal traces over continuous GND planes, with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed-circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 20.

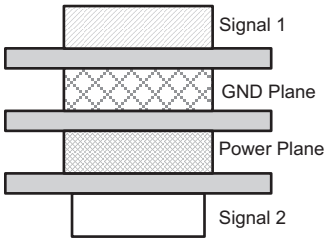


Figure 20. Four-Layer Board Stack-Up

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

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10.2 Layout Example

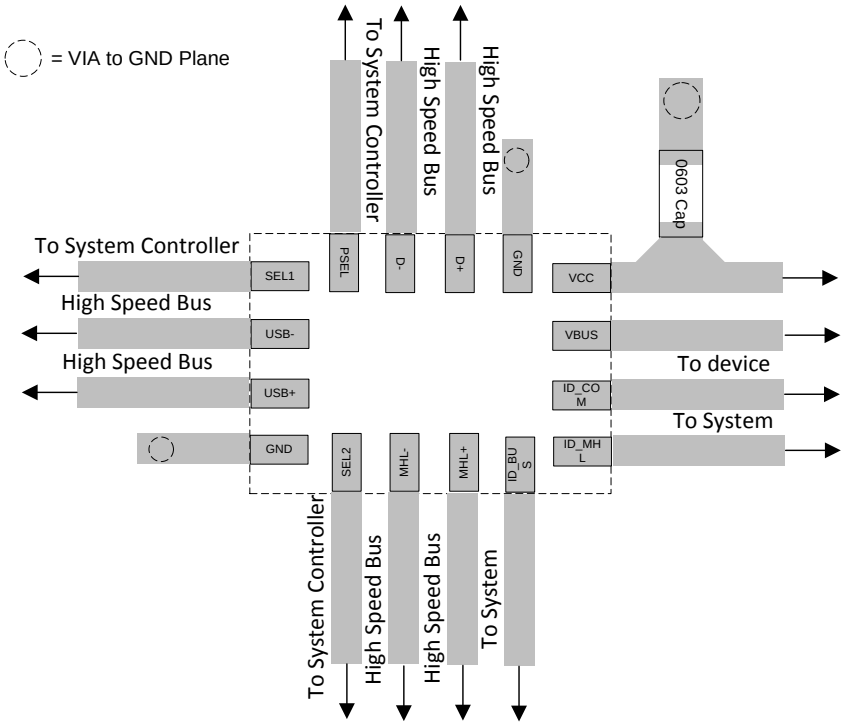


Figure 21. TS3USB3200 Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3USB32008RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTV	Samples
TS3USB3200RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTO	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

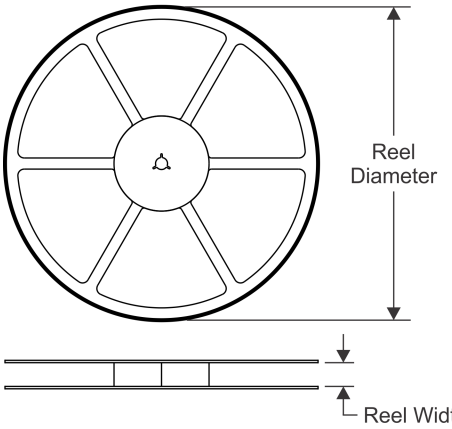
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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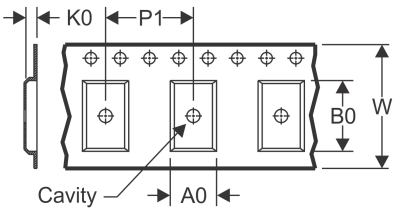
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

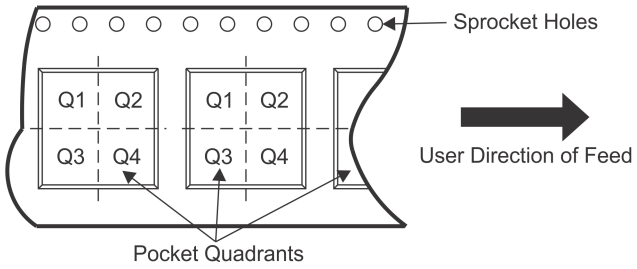


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

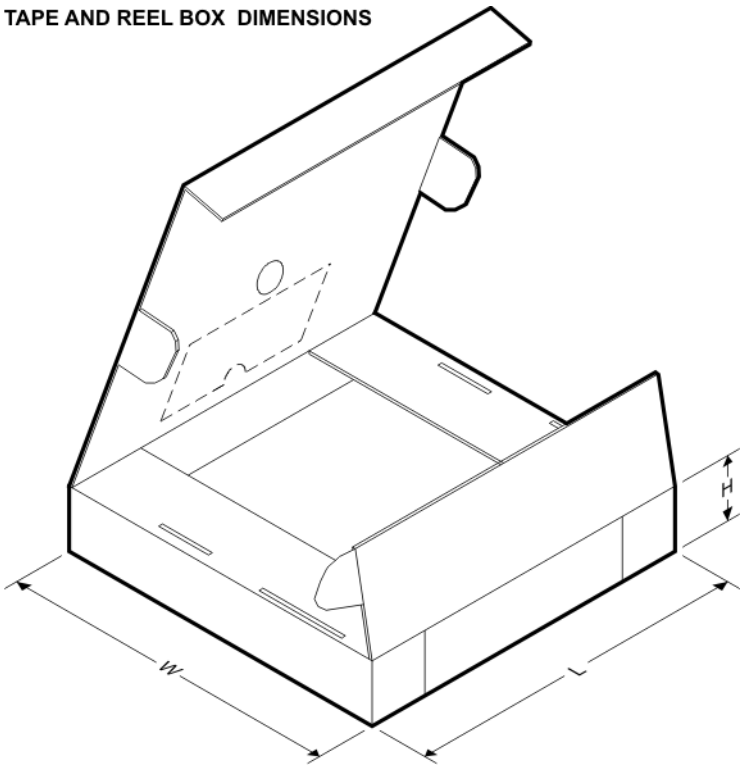
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USB3200RSVR	UQFN	RSV	16	3000	180.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1

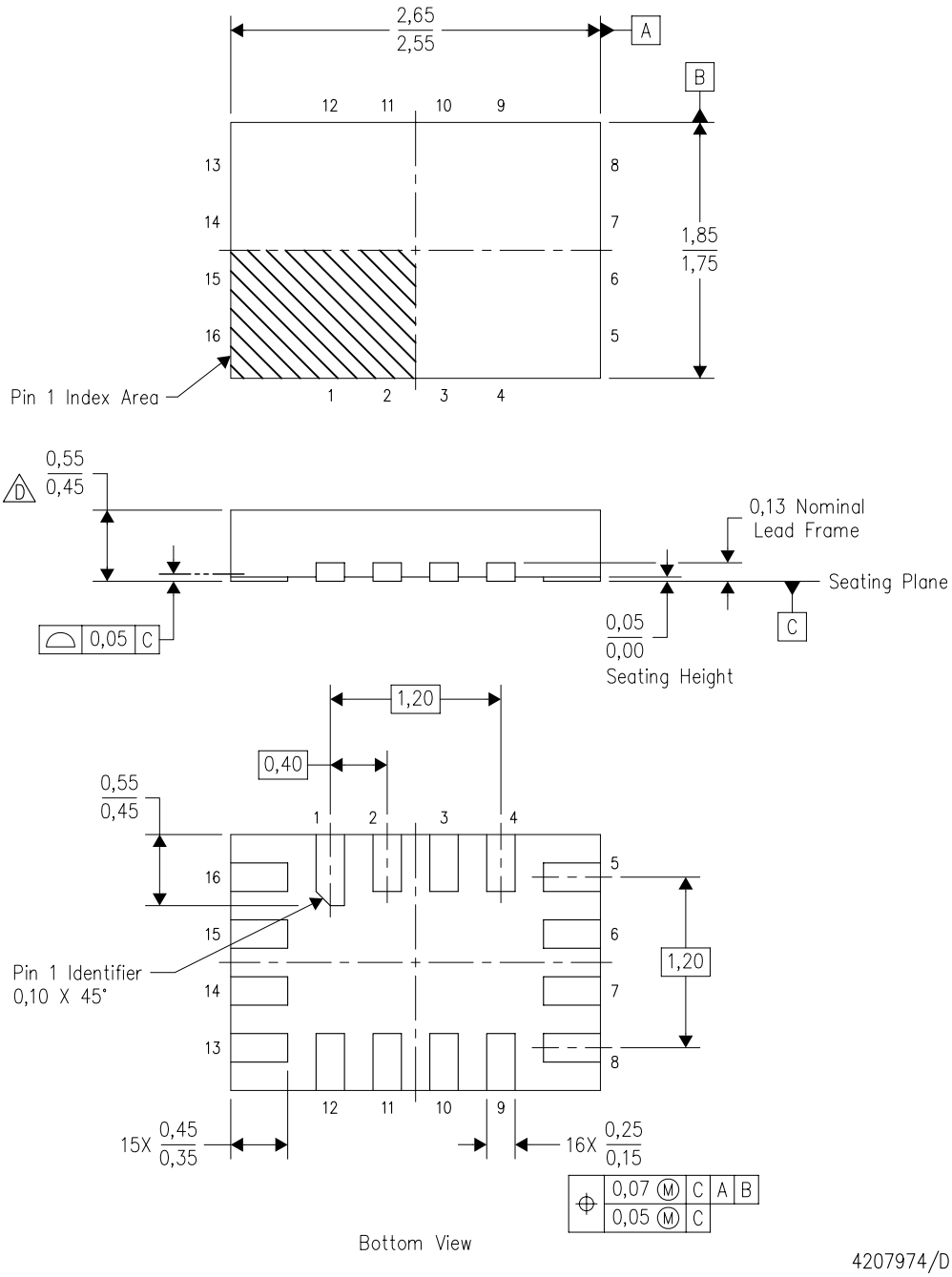
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

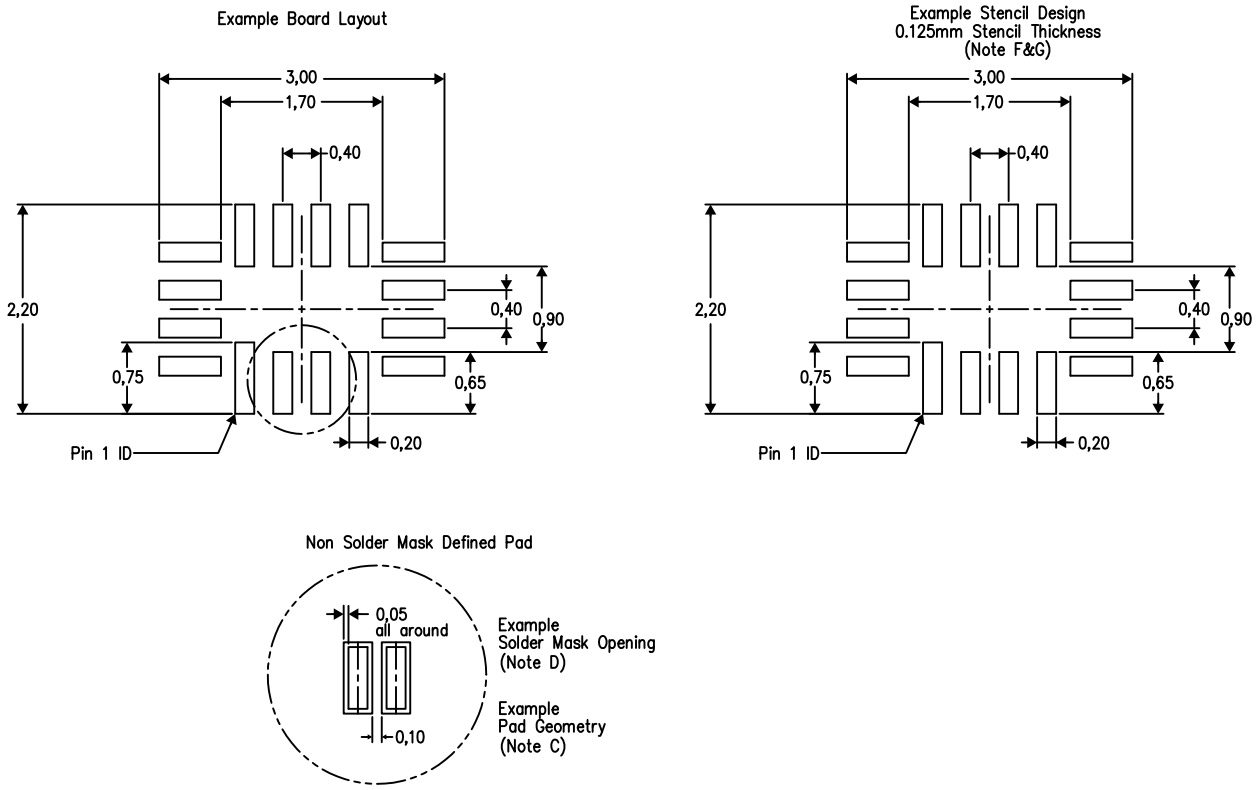
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USB3200RSVR	UQFN	RSV	16	3000	203.0	203.0	35.0

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UFHE, except minimum package thickness.

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



4208244/C 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
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OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
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