SRDA05-4 and SRDA12-4

RailClamp®
Low Capacitance TVS Array

PROTECTION PRODUCTS

Description

RailClamp® TVS arrays are low capacitance ESD protection devices designed to protect sensitive components from overvoltage caused by electrostatic discharge (ESD), electrical fast transients (EFT), and lightning surge. It offers desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

The unique design incorporates surge rated, low capacitance steering diodes and a TVS diode in a single package. During transient conditions, the steering diodes direct the transient current to ground via the internal low voltage TVS. The TVS clamps the transient voltage to a safe level. The low capacitance array configuration allows the user to protect up to four data lines. The SRDA05-4 may be used to protect lines operating up to 5 volts while the SRDA12-4 may be used on lines operating up to 12 volts.

These devices are in an 8-pin SOIC package. It measures 3.9 x 4.9mm. The high surge capability means it can be used in high threat environments in applications such as CO/CPE equipment, telecommunication lines, and video lines.

Features

- Transient protection for high-speed data lines to
  - IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  - IEC 61000-4-4 (EFT) 40A (5/50ns)
  - IEC 61000-4-5 (Lightning) 20-25A (8/20µs)
- Array of surge rated diodes with internal TVS diode
- Protects four I/O lines
- Low capacitance (<15pF)
- Low operating voltage: 5V or 12V
- Low clamping voltage
- Solid-state technology

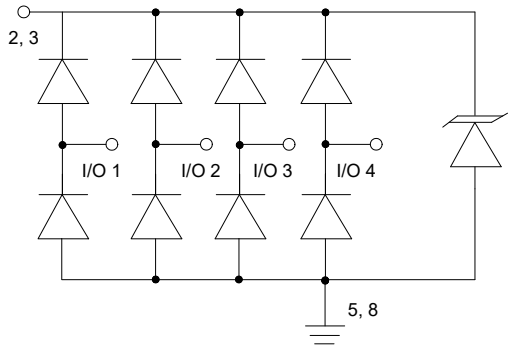
Mechanical Characteristics

- JEDEC SOIC-8 Package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Lead Finish: Matte Sn
- Marking : Marking Code
- Packaging : Tape and Reel

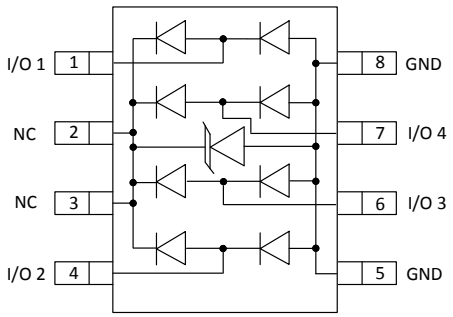
Applications

- T1/E1 secondary IC Side Protection
- T3/E3 secondary IC Side Protection
- Analog Video Protection
- Microcontroller Input Protection
- Base stations
- I^2C Bus Protection

Circuit Diagram



Schematic and Pin Configuration



SO-8 (Top View)

Absolute Maximum Ratings

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{PK}	500	W
Peak Forward Voltage (I_F = 1A, tp = 8/20µs)	V_{PP}	1.5	V
Lead Soldering Temperature	T_L	260 (10 sec.)	^oC
Operating Temperature	T_{OP}	-40 to +85	^oC
Storage Temperature	T_{STG}	-55 to +150	^oC

Electrical Characteristics (T=25^{o}C unless otherwise specified)

SRDA05-4

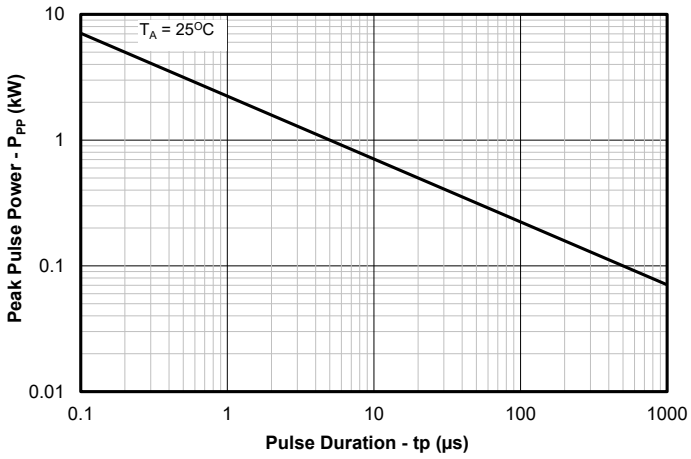
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}					5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1 mA		6			V
Reverse Leakage Current	I_R	V_{RWM} = 5V				10	µA
Clamping Voltage	V_C	t_p = 8/20µs	I_{PP} = 1A			9.8	V
			I_{PP} = 10A			12	
			I_{PP} = 25A			20	
Peak Pulse Current	I_{PP}	t_p = 8/20µs				25	A
Junction Capacitance	C_J	V_R = 0V, f = 1MHz	I/O to GND		8	15	pF
			I/O to I/O		4		

SRDA12-4

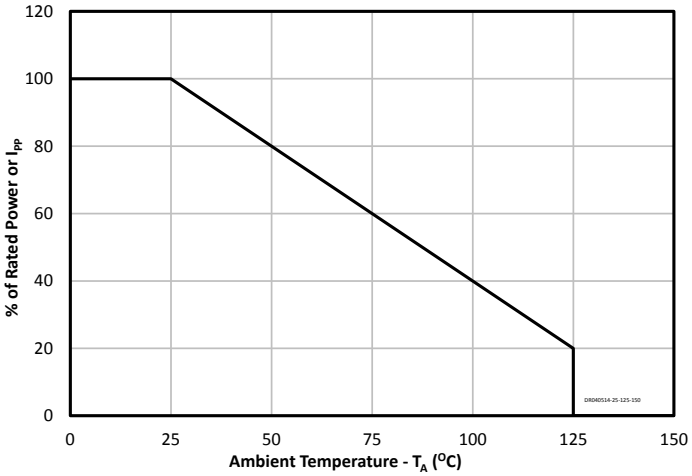
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}					12	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1 mA		13.3			V
Reverse Leakage Current	I_R	V_{RWM} = 12V				1	µA
Clamping Voltage	V_C	t_p = 8/20µs	I_{PP} = 1A			17	V
			I_{PP} = 10A			20	
			I_{PP} = 20A			25	
Peak Pulse Current	I_{PP}	t_p = 8/20µs				20	A
Junction Capacitance	C_J	V_R = 0V, f = 1MHz	I/O to GND		8	15	pF
			I/O to I/O		4		

Typical Characteristics

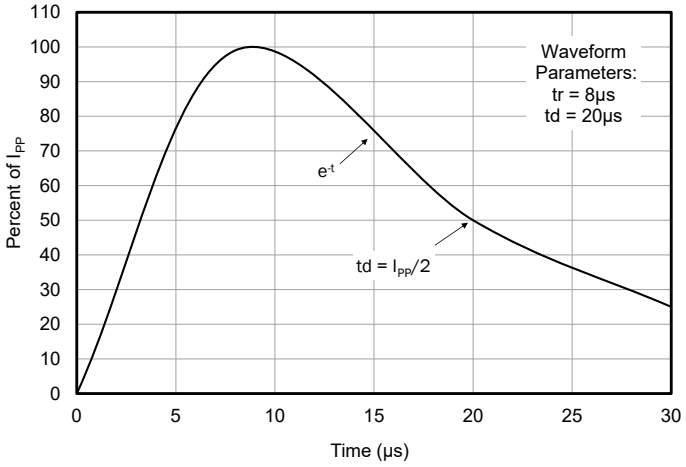
Non-Repetitive Peak Pulse Power vs. Pulse Time



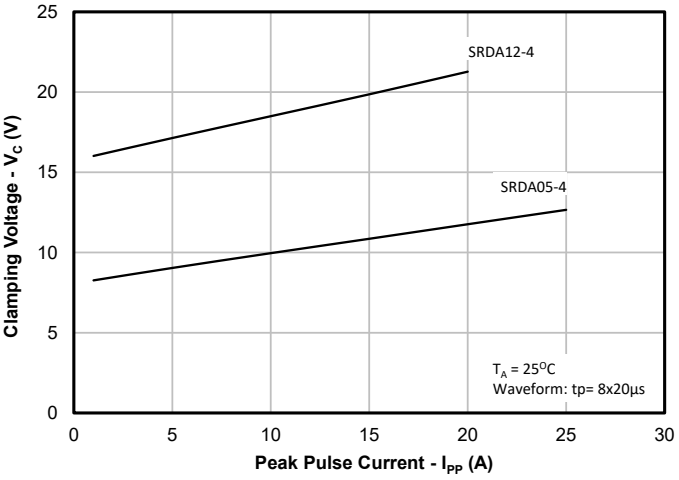
Power Derating Curve



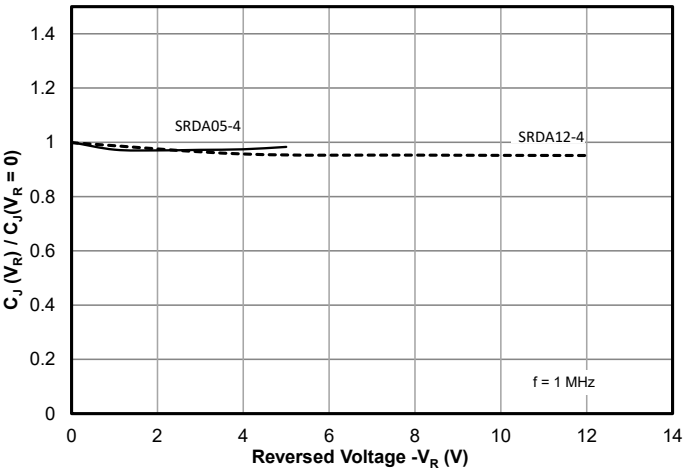
Pulse Waveform



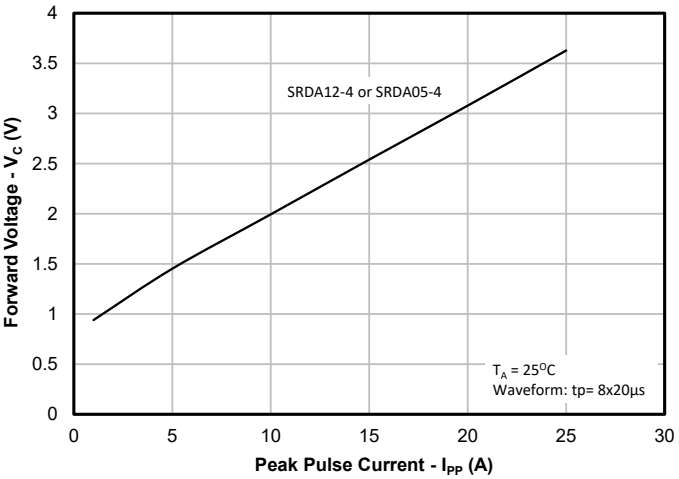
Clamping Voltage vs. Peak Pulse Current



Variation of Capacitance vs. Reverse Voltage



Forward Voltage vs. Forward Current



Application Information

Device Connection Options for Protection of Four High-Speed Lines

The SRDA TVS is designed to protect four data lines from transient over voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus V_F) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at Pins 1, 4, 6 and 7. The negative reference is connected at Pins 5 and 8. These pins should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance.

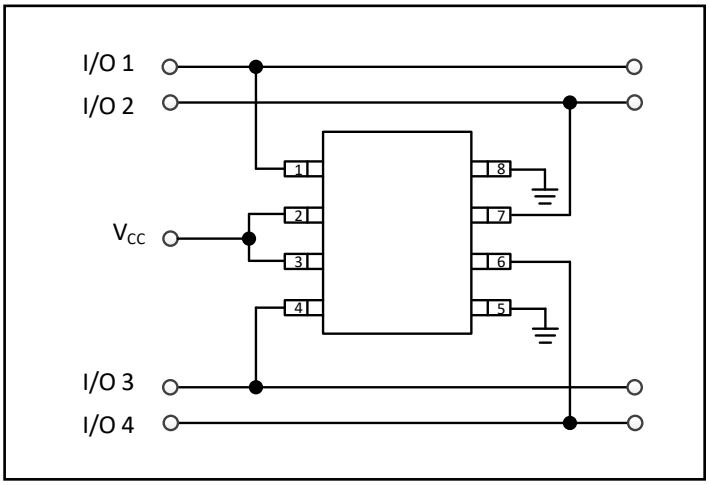
The positive reference is connected at pins 2 and 3. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pins 2 & 3 directly to the positive supply rail (V_{CC}). In this configuration the data lines are referenced to the supply voltage. The internal TVS prevents over-voltage on the supply rail.
2. The SRDA can be isolated from the power supply by adding a series resistor between Pins 2 and 3 and V_{CC}. A value of 10kΩ is recommended. The internal TVS and steering diodes remain biased, providing the advantage of lower capacitance.
3. In applications where no positive supply reference is available, or complete supply isolation is desired, the internal TVS may be used as the reference. In this case, pins 2 and 3 are not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one V_F drop).

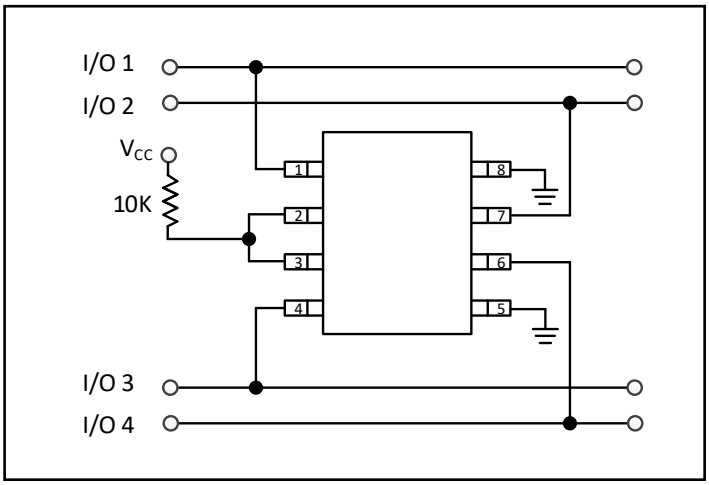
ESD Protection With RailClamps

RailClamps are optimized for ESD protection using the rail-to-rail topology. Along with good board layout, these devices virtually eliminate the disadvantages of using discrete components to implement this topology. Consider the situation shown in Figure 1 where discrete diodes or diode arrays are configured for rail-to rail protection on a high speed line. During positive duration ESD events, the top diode will be forward biased when the voltage on the protected line exceeds the reference voltage plus the V_F drop of the diode. For negative events, the bottom diode will be biased.

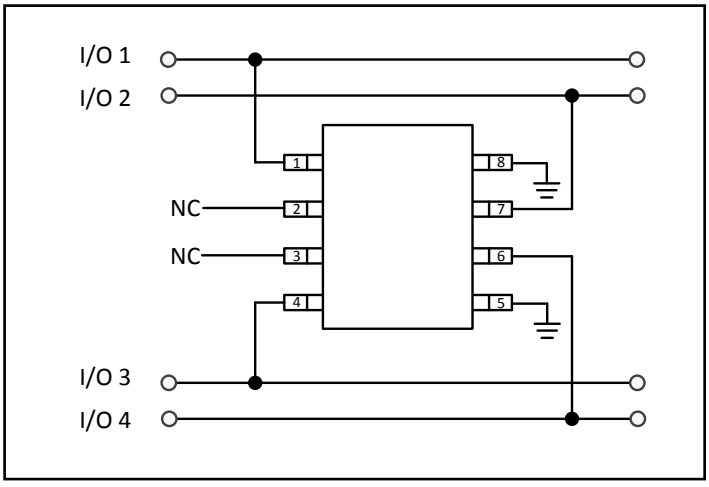
Data Line and Power Supply Protection Using VCC as Reference



Data Line Protection with Bias and Power Supply Isolation Resistor



Data Line Protection Using Internal TVS as Reference



Application Information

When the voltage exceeds the V_F, at first approximation, the clamping voltage due to the characteristics of the protection diodes is given by:

$V_C = V_{CC} + V_F$ (for positive duration pulses)
$V_C = -V_F$ (for negative duration pulses)

However, for fast rise time transient events, the effects of parasitic inductance must also be considered as shown in Figure 2. Therefore, the actual clamping voltage seen by the protected circuit will be:

$V_C = V_{CC} + V_F + L_P di_{ESD}/dt$ (for positive duration pulses)
$V_C = -V_F - L_G di_{ESD}/dt$ (for negative duration pulses)

ESD current reaches a peak amplitude of 30A in 1ns for a level 4 ESD contact discharge per IEC 61000-4-2. Therefore, the voltage overshoot due to 1nH of series inductance is:

$V = L_P di_{ESD}/dt = 1X10^{-9} (30 / 1X10^{-9}) = 30V$

Example:
Consider a V_{CC} = 5V, a typical V_F of 30V (at 30A) for the steering diode and a series trace inductance of 10nH. The clamping voltage seen by the protected IC for a positive 8kV (30A) ESD pulse will be:

$V_C = 5V + 30V + (10nH \times 30V/nH) = 335V$

This does not take into account that the ESD current is directed into the supply rail, potentially damaging any components that are attached to that rail. Also note the high V_F of the discrete diode. It is not uncommon for the V_F of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. It is also possible that the power dissipation capability of the discrete diode will be exceeded, thus destroying the device. The RailClamp is designed to overcome the inherent disadvantages of using discrete signal diodes for ESD suppression. The RailClamp's integrated TVS helps to mitigate the effects of parasitic inductance in the power supply connection. During an ESD event, the current will be directed through the integrated TVS to ground.

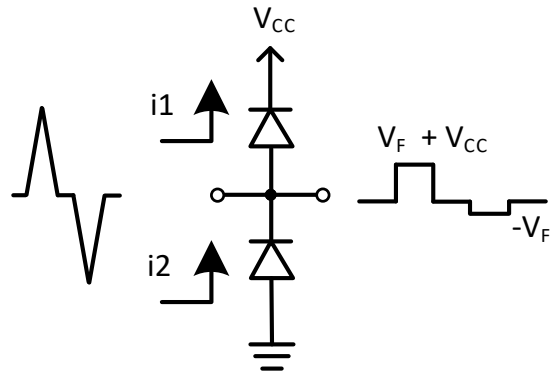


Figure 1 - Rail-To-Rail Protection Topology (First Approximation)

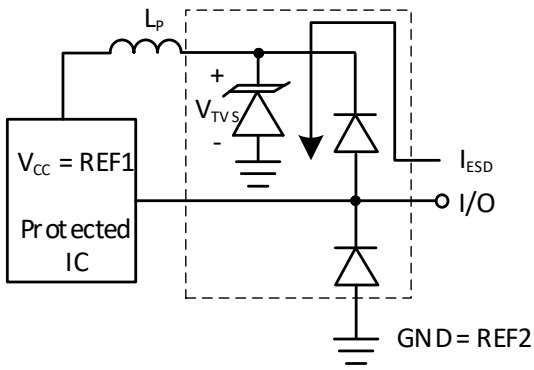


Figure 2 - The Effects of Parasitic Inductance When Using Discrete Components to Implement Rail-To-Rail Protection

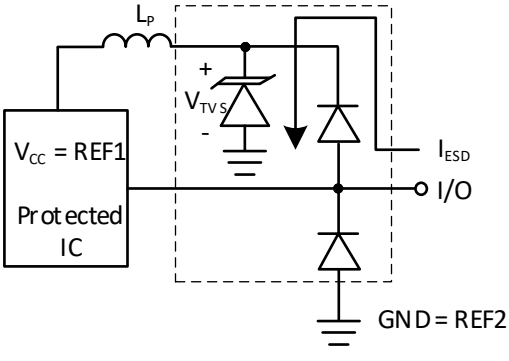


Figure 3 - Rail-To-Rail Protection Using RailClamp TVS Arrays

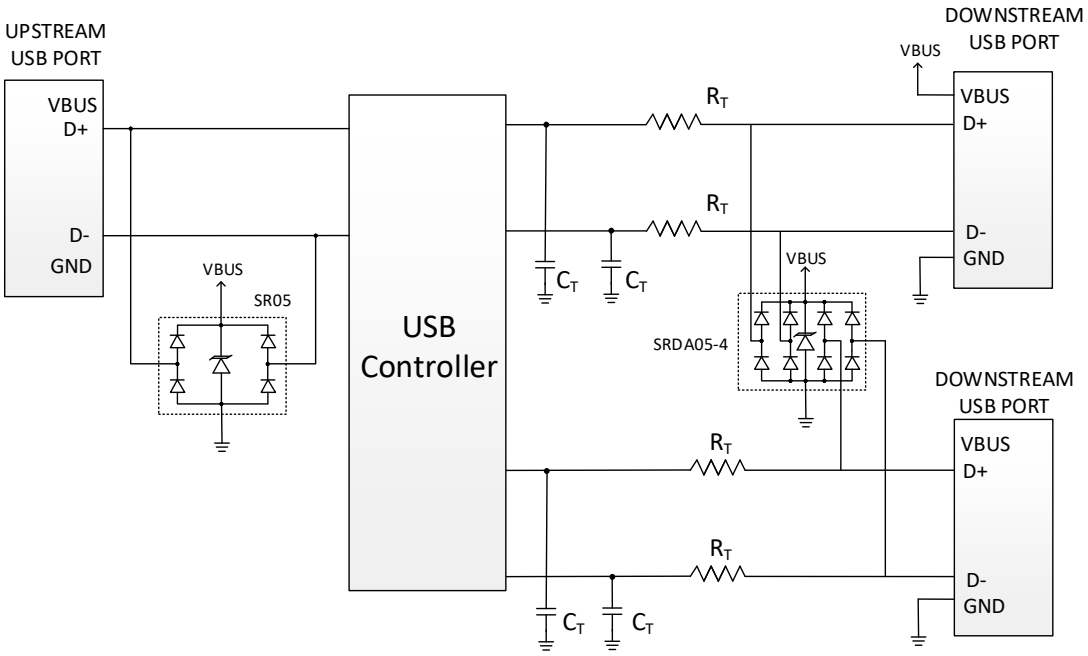
Application Information

The total clamping voltage seen by the protected IC due to this path will be:

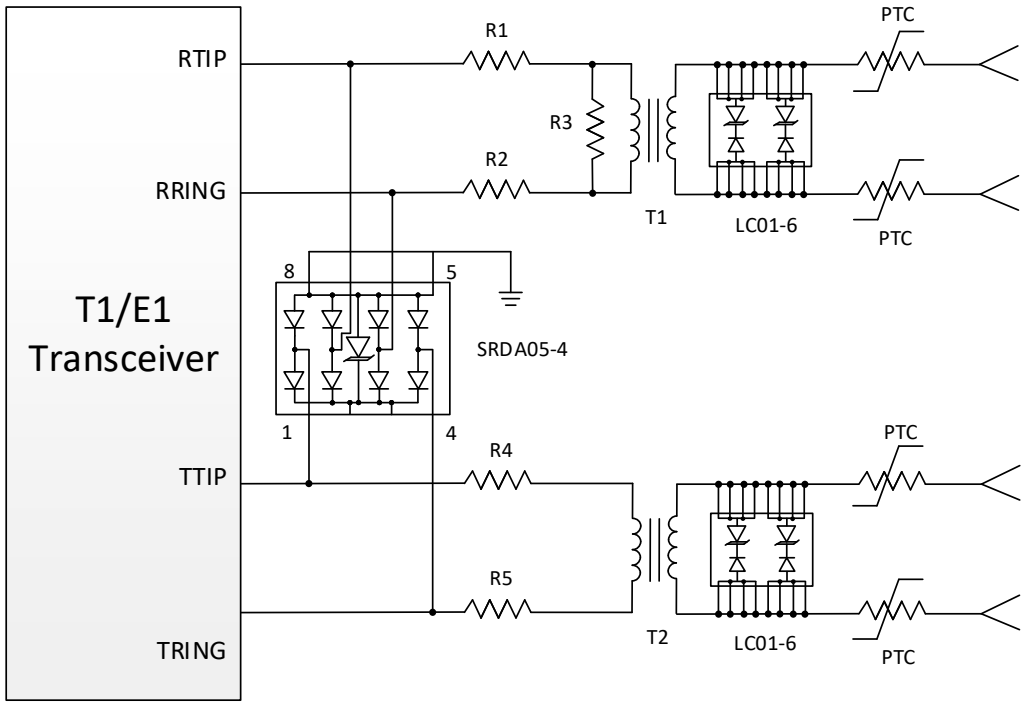
$V_C = V_F(\text{RailClamp}) + V_{TVS}$

This is given in the datasheet as the rated clamping voltage of the device. For an SRDA05-4 the typical clamping voltage is <16V at I_{PP}=30A. The diodes internal to the RailClamp are low capacitance, fast switching devices that are rated to handle high transient currents and maintain excellent forward voltage characteristics. Using the RailClamp does not negate the need for good board layout. All other inductive paths must be considered. The connection between the positive supply and the SRDA and from the ground plane to the SRDA must be kept as short as possible. The path between the SRDA and the protected line must also be minimized. The protected lines should be routed directly to the SRDA. Placement of the SRDA on the PC board is also critical for effective ESD protection. The device should be placed as close as possible to the input connector. The reason for this is twofold. First, inductance resists change in current flow. If a significant inductance exists between the connector and the TVS, the ESD current will be directed elsewhere (lower resistance path) in the system. Second, the effects of radiated emissions and transient coupling can cause upset to other areas of the board even if there is no direct path to the connector. By placing the TVS close to the connector, it will divert the ESD current immediately and absorb the ESD energy before it can be coupled into nearby traces.

Typical Application

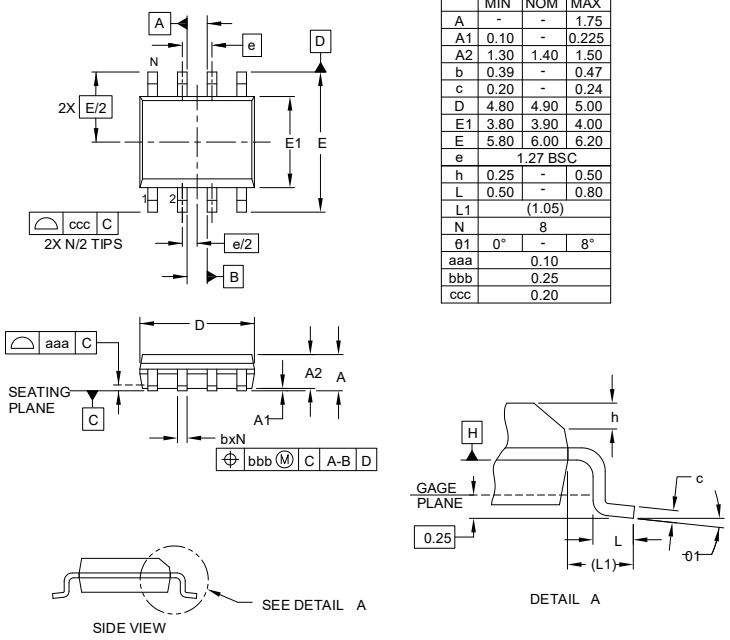


Univeral Serial Bus ESD Protection



T1/E1 Interface Protection (GR-1089 Long Haul)

Outline Drawing - SO-8

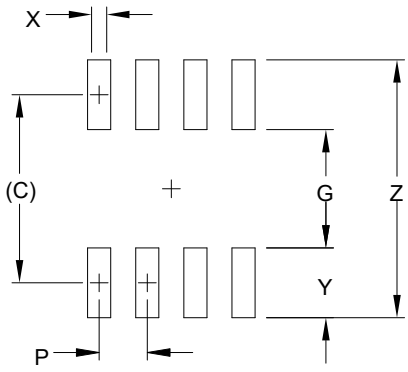


DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
b	0.39	-	0.47
c	0.20	-	0.24
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
E	5.80	6.00	6.20
e	1.27 BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	(1.05)		
N	8		
θ1	0°	-	8°
aaa	0.10		
bbb	0.25		
ccc	0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H- .
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AA.

Land Pattern - SO-8

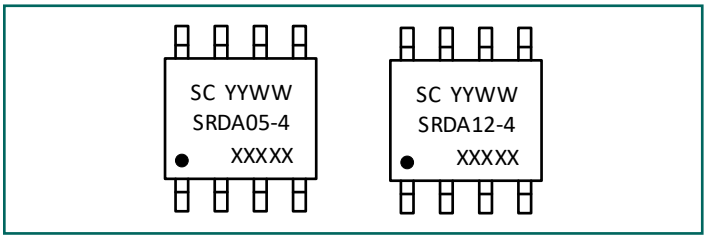


DIMENSIONS	
DIM	MILLIMETERS
C	(5.20)
G	3.00
P	1.27
X	0.60
Y	2.20
Z	7.40

NOTES:

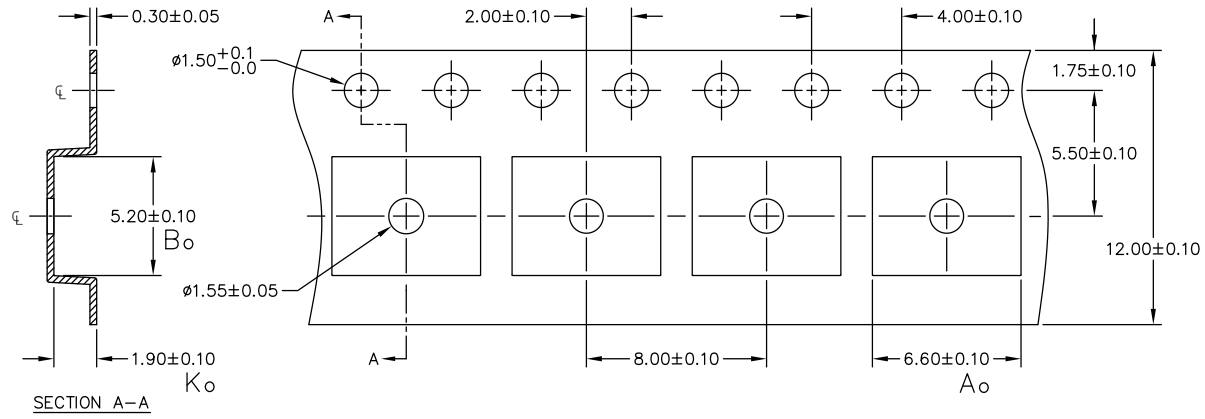
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.

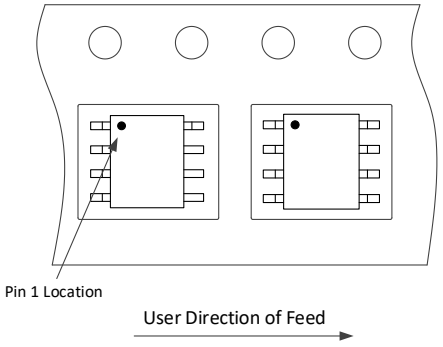
Marking Code



Notes:
YYWW = Date Code
XXXXX = Country of Assembly

Tape and Reel Specification





Ordering Information

Part Number	Qty per Reel	Reel Size
SRDA05-4.TLT	3000	13 Inch
SRDA12-4.TLT	3000	13 Inch

Important Notice

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Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com