MOSEL VITELIC

MS7200L/7201AL/7202AL
256 x 9, 512 x 9, 1K x 9
CMOS FIFO

Features

- First-In/First-Out static RAM based dual port memory
- Three densities in a x9 configuration
- Low power versions
- Includes empty, full, and half full status flags
- Direct replacement for industry standard Mostek and IDT
- Ultra high-speed 30 MHz FIFOs available with 33 ns cycle times.
- Fully expandable in both depth and width
- Simultaneous and asynchronous read and write
- Auto retransmit capability
- TTL compatible interface, single 5V ± 10% power supply
- Available in 28 pin 300 mil and 600 mil plastic DIP, 32 Pin PLCC and 330 mil SOG

Descriptions

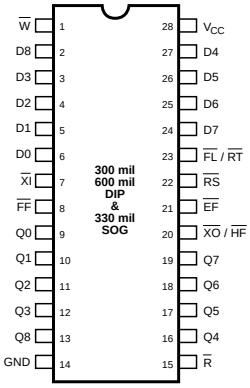
The MS7200L/7201AL/7202AL are dual-port static RAM based CMOS First-In/First-Out (FIFO) memories organized in nine-bit wide words. The devices are configured so that data is read out in the same sequential order that it was written in. Additional expansion logic is provided to allow for unlimited expansion of both word size and depth.

The dual-port RAM array is internally sequenced by independent Read and Write pointers with no external addressing needed. Read and write operations are fully asynchronous and may occur simultaneously, even with the device operating at full speed. Status flags are provided for full, empty, and half-full conditions to eliminate data underflow and overflow. The x9 architecture provides an additional bit which may be used as a parity or control bit. In addition, the devices offer a retransmit capability which resets the Read pointer and allows for retransmission from the beginning of the data.

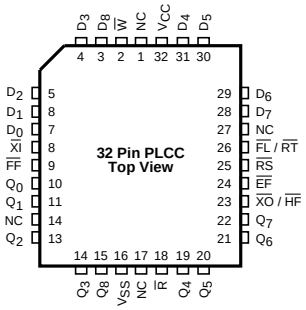
The MS7200L/7201AL/7202AL are available in a range of frequencies from 10 to 30 MHz (33 - 100 ns cycle times). A low power version with a 500µA power down supply current is available. They are manufactured on Mosel-Vitelic's high performance 1.2µ CMOS process and operate from a single 5V power supply.

Pin Configurations

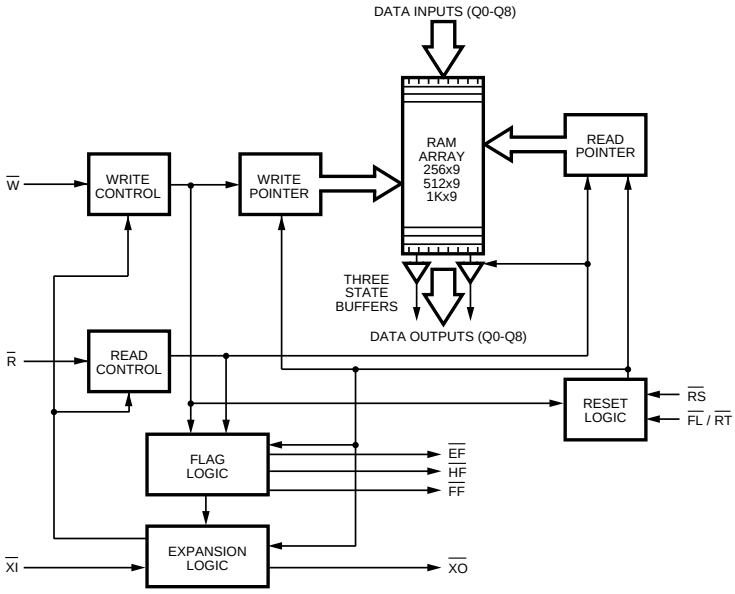
28-PIN PDIP



32-PIN PLCC



Block Diagram



Signal Descriptions

INPUTS:

Data In (D_0 - D_8)

These data inputs accept 9-bit data words for sequential storage in the FIFO during write operations.

CONTROLS:

Reset ($\overline{RS}$)

The reset input is active LOW. When asserted, the device is asynchronously reset, and both the read and write internal pointers are set to the first location in the FIFO. A Reset is required after power-up before a write operation can occur. Both Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be HIGH during Reset.

Read Enable ($\overline{R}$)

The read enable input is active LOW. As long as the Empty Flag ($\overline{EF}$) is not set, the read cycle is started on the falling edge of this signal. The data is accessed on a First-In/First-Out basis, independent of any write activity, and is presented on the Data Output pins (Q0 - Q8). When $\overline{R}$ goes HIGH the Data Output pins return to the high impedance state, and the read pointer is incremented. When the FIFO is empty or all of the data has been read, the Empty Flag will be set and further read operations are inhibited until a valid write operation has been performed.

Write Enable ($\overline{W}$)

The write enable input is active LOW. As long as the Full Flag ($\overline{FF}$) is not set, the write cycle is started on the falling edge of this signal. The data present on the Data Input pins (D0 - D8) is stored sequentially, independent of any read activity. When $\overline{W}$ goes HIGH the write cycle is terminated and the write pointer is incremented. When the maximum capacity of the FIFO has been reached the Full Flag will be set, and further write operations are inhibited until a valid read operation has been performed.

Expansion In ($\overline{XI}$)

This input pin serves two purposes. When grounded, it indicates that the device is being operated in the single device mode. In Depth Expansion mode, this pin is connected to the Expansion Out Output ($\overline{XO}$) of the previous device.

First Load/Retransmit ($\overline{FL}$/$\overline{RT}$)

This is a dual-purpose input. In single device mode (when Expansion In ($\overline{XI}$) is grounded) this pin acts as the retransmit input. A LOW pulse on this will reset the read pointer to the first memory location of the FIFO. The write pointer is unaffected. Both the read enable ($\overline{R}$) and write enable ($\overline{W}$) inputs must remain HIGH during the retransmit cycle.

In Depth Expansion mode this pin acts as a first load indicator. It must be grounded on the first device in the chain to indicate which device is the first to receive data.

OUTPUTS:

Data Output (Q_0 - Q_8)

A 9 bit data word from the FIFO is output on these pins during read operations. They are in the high impedance state whenever $\overline{R}$ is HIGH.

Empty Flag ($\overline{EF}$)

This output is active LOW. When all of the data has been read from the FIFO (defined as when the Read pointer is one location behind the Write pointer) this flag will be set. The Data Output pins will be forced into the high impedance state, and all further read operations will be inhibited until a valid write operation has been performed (which will reset this flag).

Full Flag ($\overline{FF}$)

This output is active LOW. To prevent data overflow, when the maximum capacity of the FIFO has been reached (defined as when the Write pointer is one location behind the Read pointer) this flag will be set. All further write operations will be inhibited until a valid read operation has been performed (which will reset this flag).

Expansion Out/Half Full Flag ($\overline{XO}$/$\overline{HF}$)

This dual-purpose output is active LOW. In single device mode (when Expansion In ($\overline{XI}$) is grounded) this flag will be set at the falling edge of the next write operation after the FIFO has reached one-half of its maximum capacity. This flag will remain set as long as the difference between the read pointer and the write pointer is greater than one-half of the maximum capacity of the FIFO.

In Depth Expansion mode, this output is connected to the Expansion In Input of the next device in the chain. The Expansion Out pin provides a pulse to the next device in the chain when the last memory location has been reached.

Absolute Maximum Ratings[1]

Symbol	Parameter	Condition	Unit
V_{TERM}	Terminal Voltage with Repect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-10 to +125	°C
T_{STG}	Storage Temperature	-60 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Range	Ambient Temperature	Vcc
Commercial	0°C to + 70°C	5V ± 10%

Capacitance[1] T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4	pF
C_O	Output Capacitance	V_{DQ} = 0V	6	pF

DC Electrical Characteristics (over the commercial operating range)

Test Parameter	Parameter	Test Conditions	MS7200L/7201AL 7202AL (-25, -35)			MS7200L/7201AL 7202AL (-50, -80)			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IL}	Input Low Voltage		-	-	0.8	-	-	0.8	V
V_{IH}	Input High Voltage		2.0	-	-	2.0	-	-	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0Vto V_{CC}	-1		1	-1		1	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, R= V_{IH}, V_{IN} = 0V toV_{CC}	-10		10	-10		10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 8mA	-	-	0.4	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -2mA	2.4	-	-	2.4	-	-	V
I_{CC1}	Operating Power Supply Current	V_{CC} = Max, $I_{I/O}$ = 0mA, F = F_{max}	-	-	125	-	50	80	mA
I_{CC2}	Average Standby Current	V_{CC} = Max, $\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ / $\overline{RT}$ = V_{IH}, $I_{I/O}$ = 0mA	-	-	15	-	5	8	mA
$I_{CCSB(S)}$	Power Down Power Supply Current (Standard Power)	V_{CC} = Max, $\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ / $\overline{RT}$ > V_{CC}-0.2V, V_{IN} > V_{CC}-0.2V or V_{IN} < 0.2V	-	-	5	-	-	5	mA
$I_{CCSB(L)}$	Power Down Power Supply Current (Low Power)	V_{CC} = Max, $\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ / $\overline{RT}$ > V_{CC}-0.2V, V_{IN} > V_{CC}-0.2V or V_{IN} < 0.2V	-	-	500	-	-	500	µA

Truth Tables

Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment[1]	Increment[1]	X	X	X

NOTE: 1. Pointer will increment if flag is high.

Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Unchanged	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE:

1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 15. $\overline{RS}$ = Reset Input. $\overline{FL}$/$\overline{RT}$ = First Load/Retransmit. $\overline{EF}$ = Empty Flag Output. $\overline{FF}$ Full Flag Output. $\overline{XI}$ = Expansion Input.

AC Electrical Characteristics (over the commercial operating range)

Parameter Name	Parameter	MS7200L-25 MS7201AL-25 MS7202AL-25		MS7200L-35 MS7201AL-35 MS7202AL-35		MS7200L-50 MS7201AL-50 MS7202AL-50		MS7200L-80 MS7201AL-80 MS7202AL-80		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_S	Shift Frequency	–	30	–	22.2	–	15	–	10	MHz
Read Cycle										
t_{RC}	Read Cycle Time	33	–	45	–	65	–	100	–	ns
t_A	Access Time	–	25	–	35	–	50	–	80	ns
t_{RPW}	Read Pulse Width	25	–	35	–	50	–	80	–	ns
t_{RR}	Read Recovery Time	8	–	10	–	15	–	20	–	ns
t_{RLZ} (2)	Read Pulse Low to Data Bus at Low Z	5	–	5	–	10	–	10	–	ns
t_{RHZ} (2,3)	Read Pulse High to Data Bus at High Z	–	18	–	20	–	30	–	30	ns
t_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	ns
Write Cycle										
t_{WC}	Write Cycle Time	33	–	45	–	65	–	100	–	ns
t_{WPW} (1)	Write Pulse Width	25	–	35	–	50	–	80	–	ns
t_{WR}	Write Recovery Time	8	–	10	–	15	–	20	–	ns
t_{DS}	Data Setup Time	15	–	18	–	30	–	40	–	ns
t_{DH}	Data Hold Time	0	–	0	–	5	–	10	–	ns
t_{WLZ} (2,3)	Write Pulse High to Data Bus at Low Z	5	–	10	–	15	–	20	–	ns
Flag Timing										
t_{REF}	Read Low to Empty Flag Low	–	25	–	30	–	45	–	60	ns
t_{RHF}	Read High to Half Full Flag High	–	33	–	45	–	65	–	100	ns
t_{RFF}	Read High to Full Flag High	–	25	–	30	–	45	–	60	ns
t_{WEF}	Write High to Empty Flag High	–	25	–	30	–	45	–	60	ns
t_{WFF}	Write Low to Full Flag Low	–	25	–	30	–	45	–	60	ns
t_{WHF}	Write Low to Half Full Flag Low	–	33	–	45	–	65	–	100	ns
t_{RPE}	Read Pulse Width After $\overline{EF}$ High	25	–	35	–	50	–	80	–	ns
t_{WPF}	Write Pulse Width After $\overline{FF}$ High	25	–	35	–	50	–	80	–	ns
Reset Timing										
t_{RSC}	Reset Cycle Time	33	–	45	–	65	–	100	–	ns
t_{RS} (1)	Reset Pulse Width	25	–	35	–	50	–	80	–	ns
t_{RSS}	Reset Set Up Time	25	–	35	–	50	–	80	–	ns
t_{RSR}	Reset Recovery Time	8	–	10	–	15	–	20	–	ns
t_{EFL}	Reset to Empty Flag Low	–	33	–	45	–	65	–	100	ns
t_{HFH}	Reset to Half Full Flag High	–	33	–	45	–	65	–	100	ns
t_{FFH}	Reset to Full Flag High	–	33	–	45	–	65	–	100	ns
Retransmit Timing										
t_{RTC}	Retransmit Cycle Time	33	–	45	–	65	–	100	–	ns
t_{RT} (1)	Retransmit Pulse Width	25	–	35	–	50	–	80	–	ns
t_{RTS}	Retransmit Set up Time	25	–	35	–	50	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	8	–	10	–	15	–	20	–	ns
Expansion Timing										
t_{XOL}	Read/Write to $\overline{XO}$ Low	–	25	–	35	–	50	–	80	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	–	25	–	35	–	50	–	80	ns
t_{XI}	$\overline{XI}$ Pulse Width	25	–	35	–	50	–	80	–	ns
t_{XIS}	$\overline{XI}$ Set up Time	15	–	15	–	15	–	15	–	ns
t_{XIR}	$\overline{XI}$ Recovery Time	8	–	10	–	10	–	10	–	ns

NOTES:
1. Pulse widths less than minimum value are not allowed.
2. Values guaranteed by design, not currently tested.
3. Only applies to read data flow-through mode.

AC Test Conditions

Input Pulse Levels	0V~ 3.0V
Input Rise and Fall Times	5 ns
Timing Reference Level	1.5V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC Test Loads and Waveforms

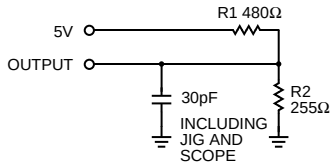


Figure 1a

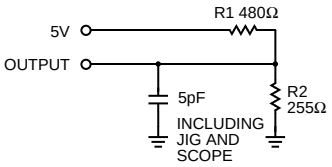
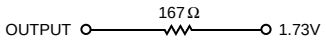


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

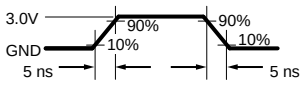
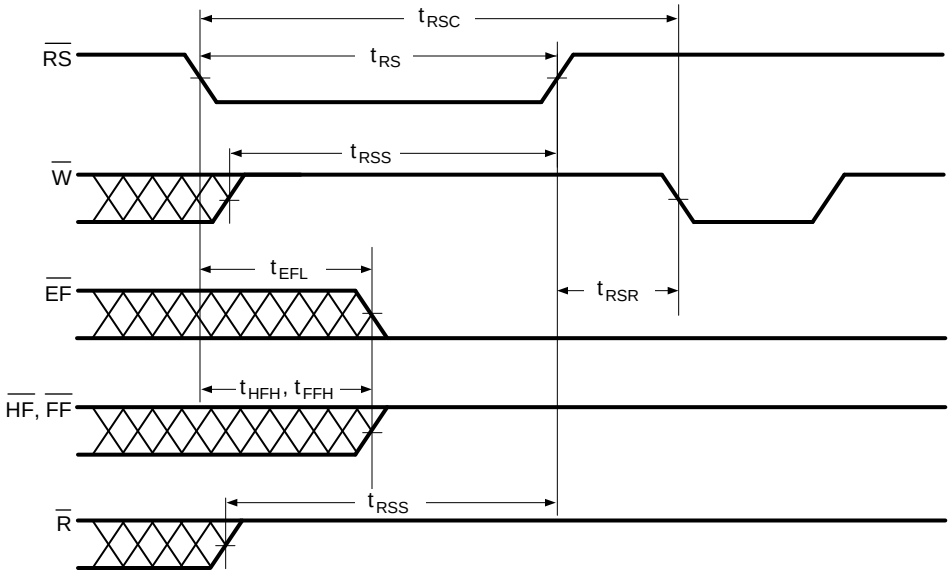


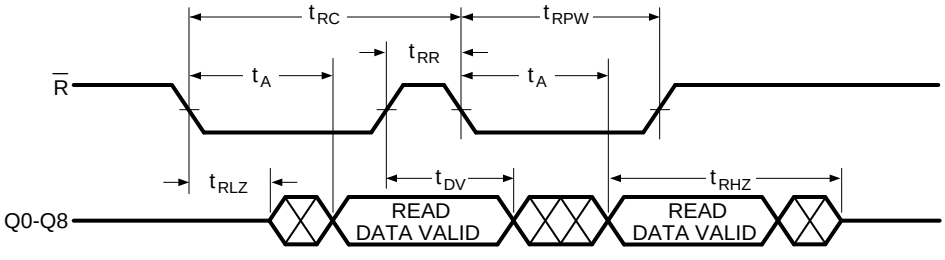
Figure 2

Timing Waveforms

RESET

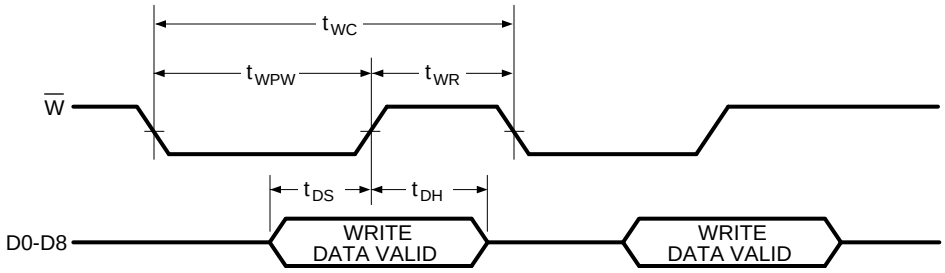


ASYNCHRONOUS READ OPERATION

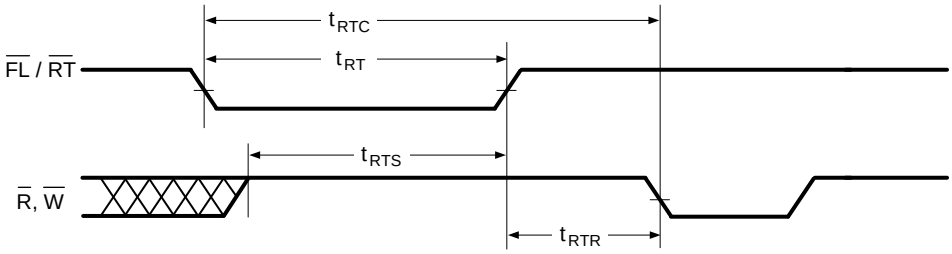


Timing Waveforms

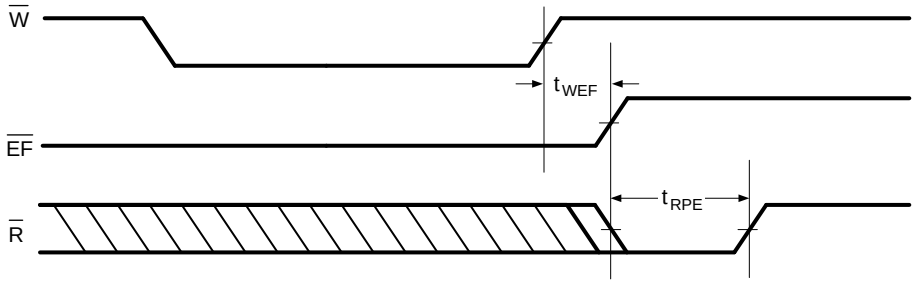
ASYNCHRONOUS WRITE OPERATION



RETRANSMIT



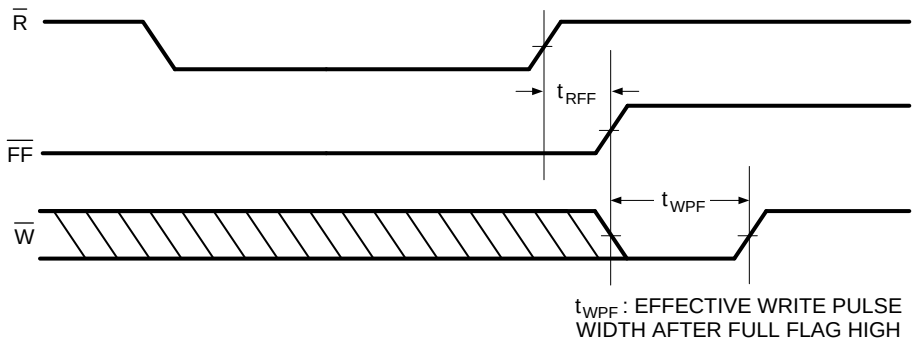
EMPTY FLAG TIMING



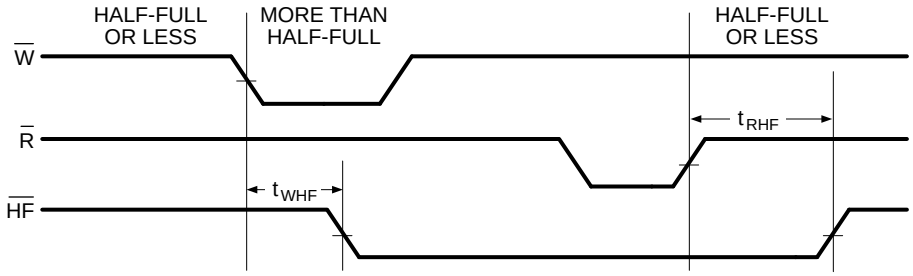
t_{RPE}: EFFECTIVE READ PULSE WIDTH AFTER EMPTY FLAG HIGH

Timing Waveforms

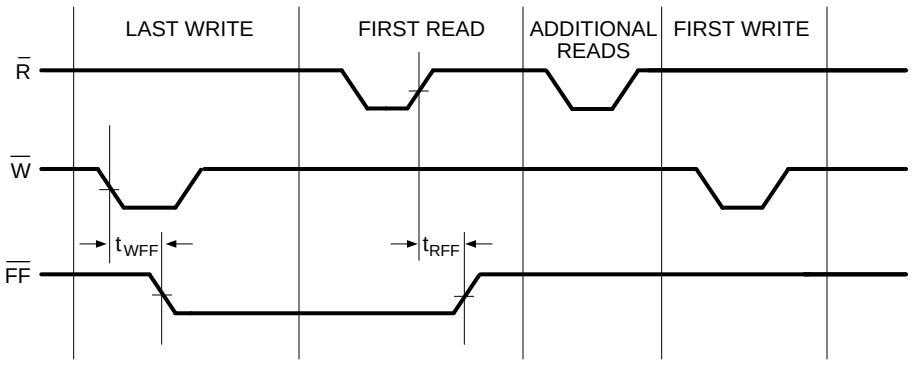
FULL FLAG TIMING



HALF-FULL FLAG TIMING

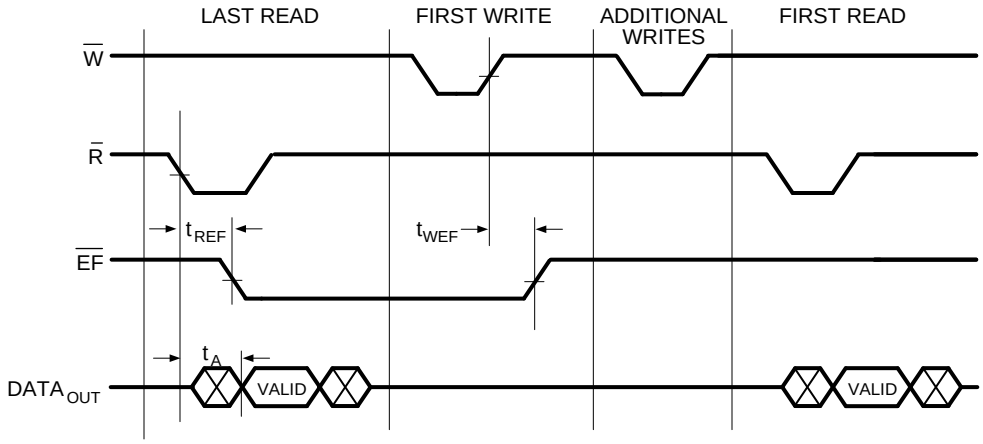


FULL FLAG FROM LAST WRITE TO FIRST READ

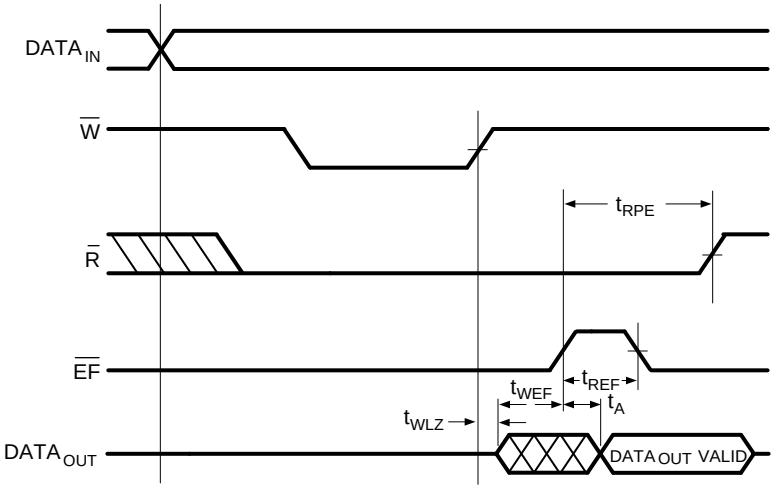


Timing Waveforms

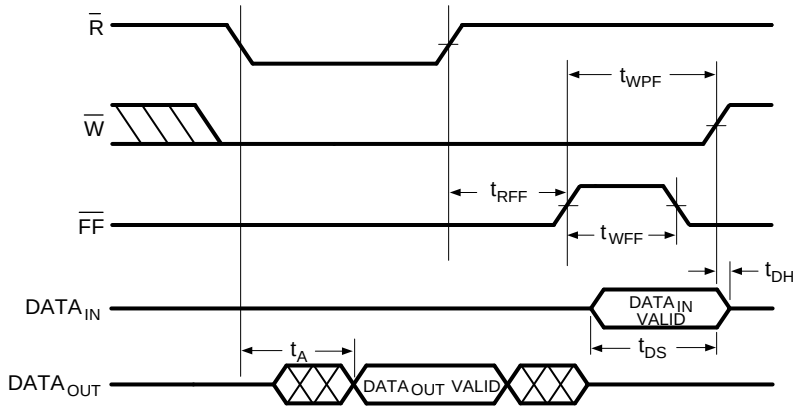
EMPTY FLAG FROM LAST READ TO FIRST WRITE



READ DATA FLOW-THROUGH MODE

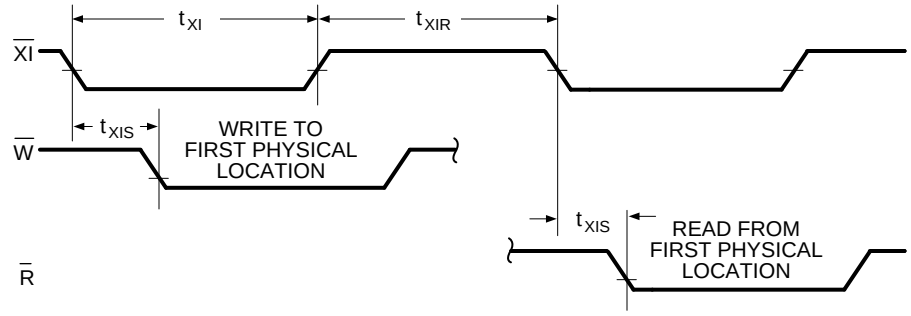


WRITE DATA FLOW-THROUGH MODE

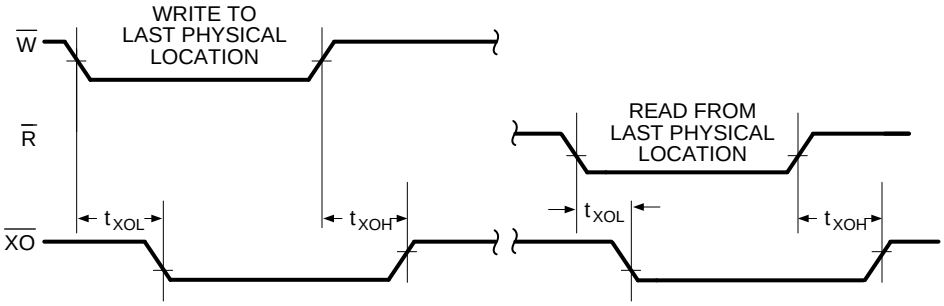


Timing Waveforms

EXPANSION IN



EXPANSION OUT



Operating Modes:

(Note: The7201A Lis used as example - these figures apply to all three devices, MS7200L/ 7201AL/7202AL

Single Device Mode

When one MS7201AL is used standalone in Single Device Mode, the Expansion In ($\overline{XI}$) control input pin must be grounded. See Figure 3.

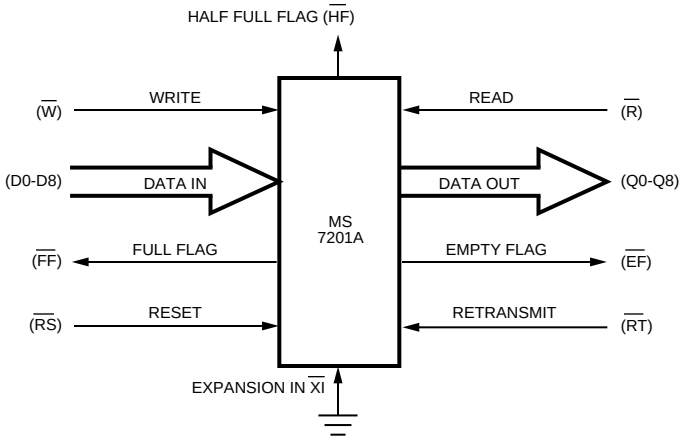


Figure 3. Single Device Mode

Width Expansion Mode

Word width may be expanded by connecting the corresponding control input signals of multiple devices together. The EMPTY, HALF FULL and FULL FLAGS ($\overline{EE}$, $\overline{HF}$ and $\overline{FF}$) can be detected by any particular device. Figure 4 shows an 18 bit wide configuration using two devices. They may be configured to any word width in this manner.

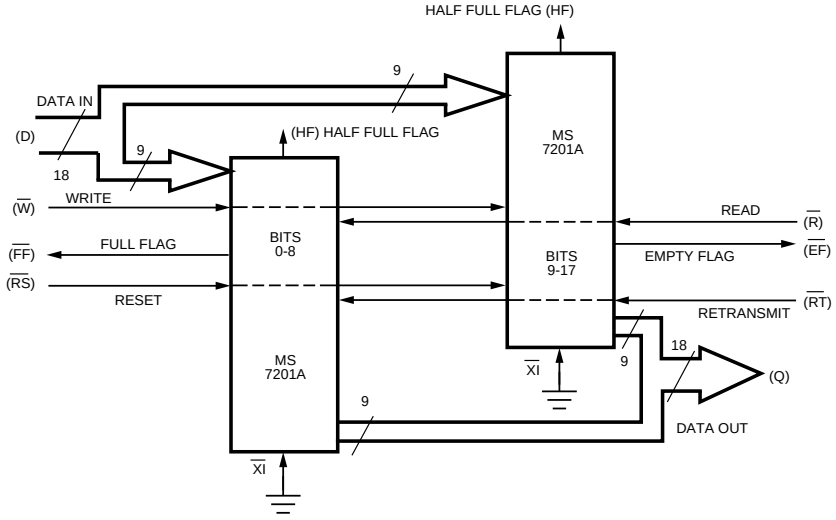


Figure 4. Width Expansion Mode

NOTES:
Flag detection is accomplished by monitoring the $\overline{EF}$, $\overline{HF}$ and $\overline{EF}$ pins on the device used in the Width Expansion Mode. Do not connect output control signals together.

Depth Expansion (Daisy Chain) Mode

Word depths may be expanded in multiples of 512 words by Daisy Chaining the devices together as follows:

1. The FIRST LOAD ($\overline{FL}$) control signal of the first device must be grounded. This FIFO represents word 1-512.
2. All other devices in the Daisy Chain must have the FIRST LOAD ($\overline{FL}$) control signal tied to V_{CC} in the inactive-high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be connected to the EXPANSION IN ($\overline{XI}$) pin of the next device as shown in Figure 5.
4. External logic is required to generate a common FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$) signal by ORing all of the $\overline{FF}$s together and ORing all of the $\overline{EF}$s together.
5. The RETRANSMIT ($\overline{RT}$) fuction and HALF FULL FLAG ($\overline{HF}$) are not available in Daisy Chain Mode.

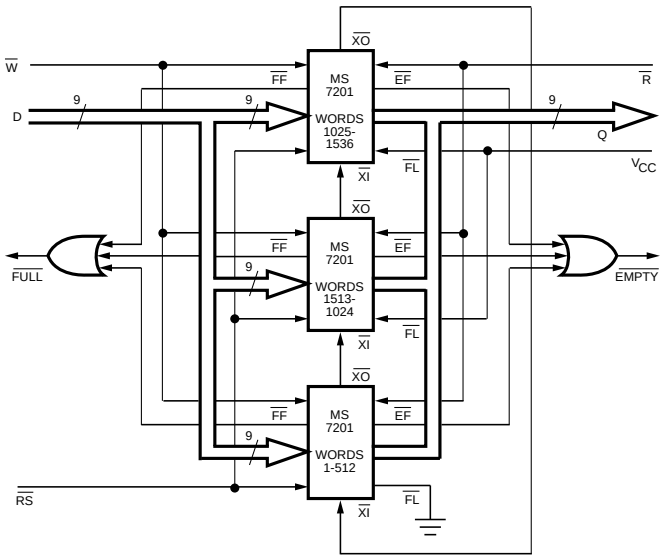


Figure 5. Diagram of a 1536 x 9 FIFO in Depth Expansion Mode

Bidirectional Mode

Data buffering between two systems can be achieved by pairing two FIFO arrays as shown in Figure 6. This allows each system to READ and WRITE shared data. The FULL FLAG ($\overline{FF}$) must be monitored on the FIFO where WRITE ENABLE ($\overline{W}$) is used and the EMPTY FLAG ($\overline{EF}$) must be monitored on the FIFO where READ ENABLE ($\overline{R}$) is used. Both Width Expansion and Depth Expansion Modes may be used in combination with Bidirectional Mode.

Compound Expansion Mode:

Both Width Expansion Mode and Depth Expansion (Daisy Chain) Mode can be used together to configure a large FIFO array (See Figure 4 and 5).

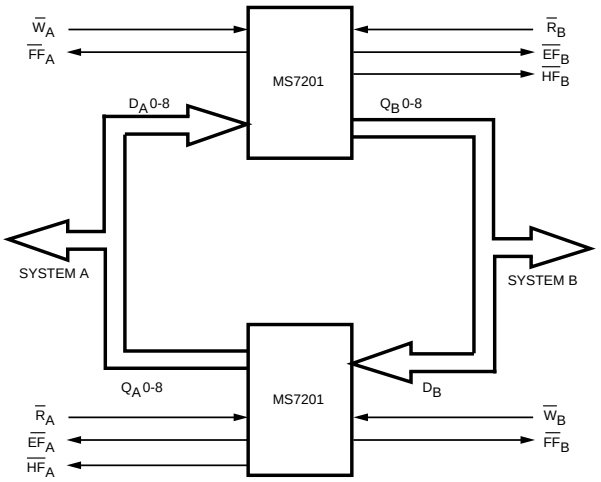


Figure 6. BiDirectional FIFO Mode

Ordering Information

Speed (ns)	Ordering Part Number			Package	Temperature Range
25		MS7201AL-25PC	MS7202AL-25PC	28 Pin Plastic DIP - 600 mil	0°C to +70°C
25	MS7200-25NC	MS7201AL-25NC	MS7202AL-25NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
25	MS7200-25JC	MS7201AL-25JC	MS7202AL-25JC	32 Pin Plastic PLCC	0°C to +70°C
25	MS7200-25FC	MS7201AL-25FC	MS7202AL-25FC	28 Pin Small Outline - 330 mil	0°C to +70°C
35		MS7201AL-35PC	MS7202AL-35PC	28 Pin Plastic DIP - 600 mil	0°C to +70°C
35	MS7200-35NC	MS7201AL-35NC	MS7202AL-35NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
35	MS7200-35JC	MS7201AL-35JC	MS7202AL-35JC	32 Pin Plastic PLCC	0°C to +70°C
35	MS7200-35FC	MS7201AL-35FC	MS7202AL-35FC	28 Pin Small Outline - 330 mil	0°C to +70°C
50		MS7201AL-50PC	MS7202AL-50PC	28 Pin Plastic DIP - 600 mil	0°C to +70°C
50	MS7200-50NC	MS7201AL-50NC	MS7202AL-50NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
50	MS7200-50JC	MS7201AL-50JC	MS7202AL-50JC	32 Pin Plastic PLCC	0°C to +70°C
50	MS7200-50FC	MS7201AL-50FC	MS7202AL-50FC	28 Pin Small Outline - 330 mil	0°C to +70°C
80		MS7201AL-80PC	MS7202AL-80PC	28 Pin Plastic DIP - 600 mil	0°C to +70°C
80	MS7200-80NC	MS7201AL-80NC	MS7202AL-80NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
80	MS7200-80JC	MS7201AL-80JC	MS7202AL-80JC	32 Pin Plastic PLCC	0°C to +70°C
80	MS7200-80FC	MS7201AL-80FC	MS7202AL-80FC	28 Pin Small Outline - 330 mil	0°C to +70°C