500mA, Linear Regulator with Precision Current Limit and Diagnostics

FEATURES

- **Output Current: 500mA**
- **Dropout Voltage: 350mV**
- **Input Voltage Range: 1.8V to 45V**
- **Programmable Precision Current Limit: ±10%**
- **Output Current Monitor: 1/500th of I_{OUT}**
- **Programmable Minimum I_{OUT} Monitor**
- **Temperature Monitor: 10mV/°C**
- **FAULT Indicator: Current Limit, Thermal Limit or Minimum I_{OUT}**
- **Low Noise: 25µV_{RMS} (10Hz to 100kHz)**
- Adjustable Output (V_{REF} = $V_{OUT(MIN)}$ = 0.6V)
- Output Tolerance: ±2% Over Load, Line and Temperature
- Stable with Low ESR, Ceramic Output Capacitors (3.3µF Minimum)
- Shutdown Current: <1µA
- Reverse Battery and Thermal Limit Protection
- 16-Lead 4mm × 3mm DFN and MSOP Packages

APPLICATIONS

- Protected Antenna Supplies
- Automotive Telematics
- Industrial Applications (Trucks, Forklifts, etc.)
- High Reliability Applications
- Noise-Sensitive RF or DSP Supplies

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DESCRIPTION

The LT®3055 series are micropower, low noise, low dropout voltage (LDO) linear regulators. The devices supply 500mA of output current with a dropout voltage of 350mV. A 10nF bypass capacitor reduces output noise to 25µV_{RMS} in a 10Hz to 100kHz bandwidth and soft starts the reference. The LT3055's ±45V input voltage rating combined with its precision current limit and diagnostic functions make the IC an ideal choice for robust, high reliability applications.

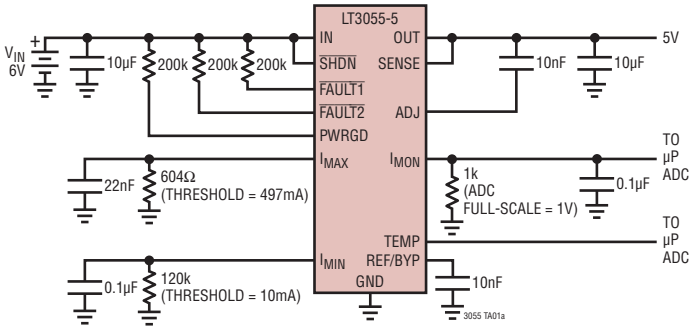
A single resistor programs the LT3055's current limit, accurate to ±10% over a wide input voltage and temperature range. Another resistor programs the LT3055's minimum output current monitor, useful for detecting open-circuit conditions. The current monitor function sources a current equal to 1/500th of output current. Logic fault pins assert low if the LT3055 is in current limit ($\overline{FAULT2}$), operating below its minimum output current ($\overline{FAULT1}$) or is in thermal limit (both $\overline{FAULT1}$ and $\overline{FAULT2}$). PWRGD indicates output regulation. The TEMP pin indicates average die temperature.

The LT3055 optimizes stability and transient response with low ESR ceramic capacitors, requiring a minimum of 3.3µF. Internal protection circuitry includes current limiting, thermal limiting, reverse battery protection, reverse current protection and reverse output protection.

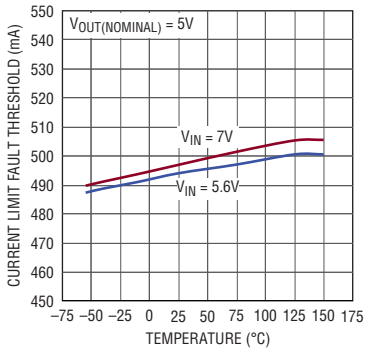
The LT3055 is available in fixed output voltages of 3.3V and 5V, and as an adjustable device with an output voltage range from 0.6V to 40V.

TYPICAL APPLICATION

5V Supply with 497mA Precision Current Limit, 10mA I_{MIN}



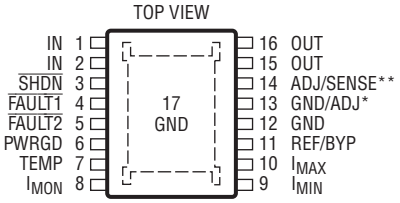
Precision Current Limit, R_{IMAX} = 604Ω



ABSOLUTE MAXIMUM RATINGS (Note 1)

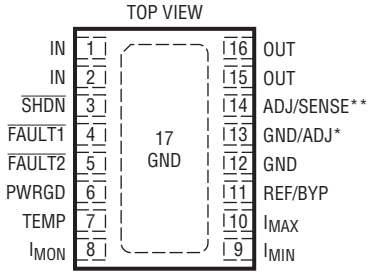
IN Pin Voltage ..... ±50V
OUT Pin Voltage ..... +40V, –50V
Input-to-Output Differential Voltage ..... +50V, –40V
ADJ Pin Voltage ..... ±50V
SENSE Pin Voltage ..... ±50V
SHDN Pin Voltage ..... ±50V
$\overline{FAULT1}$, $\overline{FAULT2}$, PWRGD Pin Voltage ..... –0.3V, 50V
I_{MON} Pin Voltage ..... –0.3V, 7V
I_{MIN} Pin Voltage ..... –0.3V, 7V
I_{MAX} Pin Voltage ..... –0.3V, 7V
TEMP Pin Voltage ..... –0.3V, 7V
REF/BYP Pin Voltage 1V
Output Short-Circuit Duration ..... Indefinite
Operating Junction Temperature Range (Notes 2, 3)
E-, I-Grades ..... –40°C to 125°C
MP-Grade ..... –55°C to 150°C
H-Grade ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature: (Soldering, 10 sec)
MSOP Package Only ..... 300°C

PIN CONFIGURATION



MSE PACKAGE
16-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 37°C/W, θ_{JC} = 5°C/W TO 10°C/W
T_{JMAX} = 150°C FOR H-GRADE
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB



DE PACKAGE
16-LEAD (4mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 38°C/W, θ_{JC} = 4.3°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

*PIN 13 IS GND FOR LT3055; PIN 13 IS ADJ FOR LT3055-3.3 AND LT3055-5.
**PIN 14 IS ADJ FOR LT3055; PIN 14 IS SENSE FOR LT3055-3.3 AND LT3055-5.

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3055EMSE#PBF	LT3055EMSE#TRPBF	3055	16-Lead Plastic MSOP	–40°C to 125°C
LT3055IMSE#PBF	LT3055IMSE#TRPBF	3055	16-Lead Plastic MSOP	–40°C to 125°C
LT3055MPMSE#PBF	LT3055MPMSE#TRPBF	3055	16-Lead Plastic MSOP	–55°C to 150°C
LT3055HMSE#PBF	LT3055HMSE#TRPBF	3055	16-Lead Plastic MSOP	–40°C to 150°C
LT3055EMSE-3.3#PBF	LT3055EMSE-3.3#TRPBF	305533	16-Lead Plastic MSOP	–40°C to 125°C
LT3055IMSE-3.3#PBF	LT3055IMSE-3.3#TRPBF	305533	16-Lead Plastic MSOP	–40°C to 125°C
LT3055MPMSE-3.3#PBF	LT3055MPMSE-3.3#TRPBF	305533	16-Lead Plastic MSOP	–55°C to 150°C
LT3055HMSE-3.3#PBF	LT3055HMSE-3.3#TRPBF	305533	16-Lead Plastic MSOP	–40°C to 150°C
LT3055EMSE-5#PBF	LT3055EMSE-5#TRPBF	30555	16-Lead Plastic MSOP	–40°C to 125°C
LT3055IMSE-5#PBF	LT3055IMSE-5#TRPBF	30555	16-Lead Plastic MSOP	–40°C to 125°C
LT3055MPMSE-5#PBF	LT3055MPMSE-5#TRPBF	30555	16-Lead Plastic MSOP	–55°C to 150°C
LT3055HMSE-5#PBF	LT3055HMSE-5#TRPBF	30555	16-Lead Plastic MSOP	–40°C to 150°C
LT3055EDE#PBF	LT3055EDE#TRPBF	3055	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3055IDE#PBF	LT3055IDE#TRPBF	3055	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3055EDE-3.3#PBF	LT3055EDE-3.3#TRPBF	05533	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3055IDE-3.3#PBF	LT3055IDE-3.3#TRPBF	05533	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3055EDE-5#PBF	LT3055EDE-5#TRPBF	30555	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3055IDE-5#PBF	LT3055IDE-5#TRPBF	30555	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage (Note 3, 11)	I_{LOAD} = 500mA	●		1.8	2.2	V
Regulated Output Voltage (Note 4)	LT3055-3.3: V_{IN} = 3.9V, I_{LOAD} = 1mA		3.267	3.3	3.333	V
	3.9V < V_{IN} < 45V, 1mA < I_{LOAD} < 500mA	●	3.234	3.3	3.336	V
	LT3055-5: V_{IN} = 3.9V, I_{LOAD} = 1mA		4.95	5	5.05	V
	5.6V < V_{IN} < 45V, 1mA < I_{LOAD} < 500mA	●	4.9	5	5.1	V
ADJ Pin Voltage (Note 3, 4)	LT3055: V_{IN} = 2.2V, I_{LOAD} = 1mA		594	600	606	mV
	2.2V < V_{IN} < 45V, 10mA < I_{LOAD} < 500mA	●	588		612	mV
Line Regulation (Note 3)	LT3055: ΔV_{IN} = 2.2V to 45V, I_{LOAD} = 1mA	●		0.25	3	mV
	LT3055-3.3: ΔV_{IN} = 3.9V to 45V, I_{LOAD} = 1mA	●		1.4	19.5	mV
	LT3055-5: ΔV_{IN} = 5.6V to 45V, I_{LOAD} = 1mA	●		2	30	mV
Load Regulation (Note 3)	LT3055: V_{IN} = 2.2V, I_{LOAD} = 1mA to 500mA	●		0.5	4	mV
	LT3055-3.3: V_{IN} = 4.3V, I_{LOAD} = 1mA to 500mA	●		3.5	22	mV
	LT3055-5: V_{IN} = 6V, I_{LOAD} = 1mA to 500mA	●		5.25	33	mV
Dropout Voltage, V_{IN} = $V_{OUT(NOMINAL)}$ (Notes 5, 6)	I_{LOAD} = 10mA			140	175	mV
		●			260	mV
	I_{LOAD} = 50mA			200	250	mV
		●			370	mV
	I_{LOAD} = 100mA			225	275	mV
		●			410	mV
	I_{LOAD} = 500mA			350	400	mV
		●			590	mV
GND Pin Current, V_{IN} = $V_{OUT(NOMINAL)}$ + 0.6V (Notes 6, 7)	I_{LOAD} = 0mA	●		65	130	µA
	I_{LOAD} = 1mA	●		100	200	µA
	I_{LOAD} = 10mA	●		270	550	µA
	I_{LOAD} = 100mA	●		1.8	4.5	mA
	I_{LOAD} = 500mA	●		11	25	mA
Quiescent Current in Shutdown	V_{IN} = 45V, $V_{\overline{SHDN}}$ = 0V			0.2	1	µA
ADJ Pin Bias Current (Notes 3,12)	V_{IN} = 12V	●		16	60	nA
Output Voltage Noise	C_{OUT} = 10µF, I_{LOAD} = 500mA, V_{OUT} = 600mV, BW = 10Hz to 100kHz			90		μV_{RMS}
	C_{OUT} = 10µF, C_{BYP} = 10nF, I_{LOAD} = 500mA, V_{OUT} = 600mV, BW = 10Hz to 100kHz			25		μV_{RMS}
Shutdown Threshold	V_{OUT} = Off to On	●		1.3	1.42	V
	V_{OUT} = On to Off	●	0.9	1.1		V
$\overline{SHDN}$ Pin Current (Note 13)	$V_{\overline{SHDN}}$ = 0V, V_{IN} = 45V	●			1	µA
	$V_{\overline{SHDN}}$ = 45V, V_{IN} = 45V	●		0.5	3	µA
Ripple Rejection	V_{IN}-V_{OUT} = 2V, V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 500mA					
	LT3055, V_{OUT} = 0.6V		70	85		dB
	LT3055-3.3		55	70		dB
	LT3055-5		51	66		dB
Input Reverse Leakage Current	V_{IN} = –45V, V_{OUT} = 0	●			300	µA
Reverse Output Current (Note 14)	V_{OUT} = 1.2V, V_{IN} = 0			0	10	µA
Internal Current Limit (Note 3)	V_{IN} = 2.2V, V_{OUT} = 0, V_{IMAX} = 0			900		mA
	V_{IN} = 2.2V, ΔV_{OUT} = –5%	●	520			mA
External Programmed Current Limit, V_{OUT} = 5V (Notes 6, 8)	5.6V < V_{IN} < 10V, V_{OUT} = 5V, R_{IMAX} = 1.5k, $\overline{FAULT2}$ Pin Threshold (I_{FAULT})	●	180	200	220	mA
	5.6V < V_{IN} < 7V, V_{OUT} = 5V, R_{IMAX} = 604Ω, $\overline{FAULT2}$ Pin Threshold (I_{FAULT})	●	445	495	545	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{FAULT}$, PWRGD Pins Logic Low Voltage	Pull-Up Current = 50µA	●		0.14	0.25	V
$\overline{FAULT}$, PWRGD Pins Leakage Current	$V_{\overline{FAULT1}}$, $V_{\overline{FAULT2}}$, V_{PWRGD} = 5V			0.01	1	µA
I_{MIN} Threshold Accuracy (Notes 6, 9)	5.6V < V_{IN} < 15V, V_{OUT} = 5V, R_{IMIN} = 1.2M 5.6V < V_{IN} < 15V, V_{OUT} = 5V, R_{IMIN} = 120K	● ●	0.9 9	1 10	1.1 11	mA mA
PWRGD Trip Point	% of Nominal Output Voltage, Output Rising	●	86	90	94	%
PWRGD Trip Point Hysteresis	% of Nominal Output Voltage			1		%
Current Monitor Ratio (Notes 6,10), Ratio = I_{OUT}/I_{MON}	I_{LOAD} = 10mA, 250mA, 500mA	●	450	500	550	mA/mA
TEMP Voltage (Note 16)	T_J = 25°C T_J = 125°C			0.25 1.25		V V
TEMP Error (Note 16)		●	–0.08		0.08	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. Absolute maximum input-to-output differential voltage is not achievable with all combinations of rated IN pin and OUT pin voltages. With the IN pin at 50V, the OUT pin may not be pulled below 0V. The total differential voltage from IN to OUT must not exceed +50V, –40V. If OUT is pulled above GND and IN, the total differential voltage from OUT to IN must not exceed 40V.

Note 2: The LT3055 is tested and specified under pulse load conditions such that $T_J \sim T_A$. The LT3055E is 100% production tested at T_A = 25°C and performance is guaranteed from 0°C to 125°C. Performance at –40°C and 125°C is assured by design, characterization and correlation with statistical process controls. The LT3055I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3055MP is 100% tested over the –55°C to 150°C operating junction temperature range. The LT3055H is 100% tested at 150°C operating junction temperature.

Note 3: The LT3055 adjustable version is tested and specified for these conditions with ADJ pin connected to the OUT pin.

Note 4: Maximum junction temperature limits operating conditions. Regulated output voltage specifications do not apply for all possible combinations of input voltage and output current. If operating at the maximum input voltage, limit the output current range. If operating at the maximum output current, limit the input voltage range. Current limit foldback limits the maximum output current as a function of input-to-output voltage. See Current Limit vs V_{IN}-V_{OUT} in the Typical Performance Characteristics section.

Note 5: Dropout voltage is the minimum differential IN-to-OUT voltage needed to maintain regulation at a specified output current. In dropout, the output voltage equals ($V_{IN} – V_{DROPOUT}$). For some output voltages, minimum input voltage requirements limit dropout voltage.

Note 6: To satisfy minimum input voltage requirements, the LT3055 adjustable version is tested and specified for these conditions with an external resistor divider (60k bottom, 440k top) which sets V_{OUT} to 5V. The external resistor divider adds 10µA of DC load on the output. This external current is not factored into GND pin current.

Note 7: GND pin current is tested with $V_{IN} = V_{OUT(NOMINAL)} + 0.6V$ and a current source load. GND pin current increases in dropout. For the fixed output voltage versions, an internal resistor divider adds about 10µA to GND pin current. See GND pin current curves in the Typical Performance Characteristics section.

Note 8: Current limit varies inversely with the external resistor value tied from the I_{MAX} pin to GND. For detailed information on how to set the I_{MAX} pin resistor value, please see the Operation section. If a programmed current limit is not needed, tie the I_{MAX} pin to GND and internal protection circuitry implements short-circuit protection as specified.

Note 9: The I_{MIN} fault condition asserts if the output current falls below the I_{MIN} threshold defined by an external resistor from the I_{MIN} pin to GND. For detailed information on how to set the I_{MIN} pin resistor value, please see the Operation section. If the I_{MIN} fault condition is not needed, the I_{MIN} pin must be left floating (unconnected).

Note 10: Current monitor ratio is tested with the I_{MON} pin fixed at $V_{OUT} – 0.5V$ and with the input range limited to $V_{OUT} + 0.6V < V_{IN} < V_{OUT} + 10V$ for I_{OUT} = 10mA; $V_{OUT} + 0.6V < V_{IN} < V_{OUT} + 4V$ for I_{OUT} = 250mA, and $V_{OUT} + 0.6V < V_{IN} < V_{OUT} + 2V$ for I_{OUT} = 500mA. Input voltage range conditions are set to limit power dissipation in the IC to 1W maximum for test purposes. The current monitor ratio varies slightly when in current limit or when the I_{MON} voltage exceeds $V_{OUT} – 0.5V$. Please see the Operation section for more information. If the current monitor function is not needed, tie the IMON pin to GND.

Note 11: To satisfy requirements for minimum input voltage, current limit is tested at $V_{IN} = V_{OUT(NOMINAL)} + 1V$ or V_{IN} = 2.2V, whichever is greater.

Note 12: ADJ pin bias current flows out of the ADJ pin.

Note 13: $\overline{SHDN}$ pin current flows into the $\overline{SHDN}$ pin.

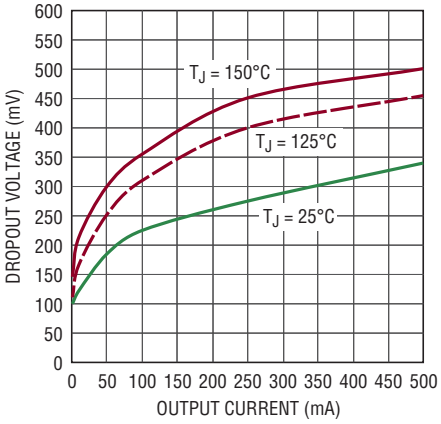
Note 14: Reverse output current is tested with the IN pin grounded and the OUT pin forced to the specified voltage. This current flows into the OUT pin and out of the GND pin.

Note 15: 500mA of output current does not apply to the full range of input voltage due to the internal current limit foldback.

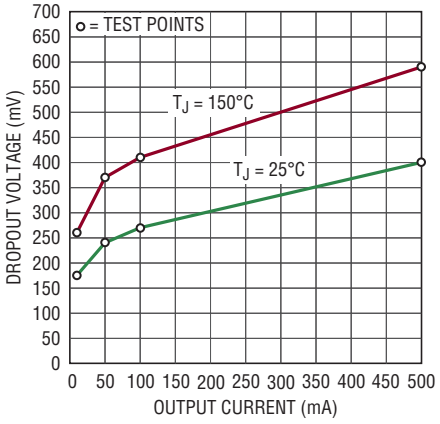
Note 16: The TEMP output voltage represents the average temperature of the die while dissipating quiescent power. Due to the pass device power dissipation and temperature gradients across the die, the TEMP output voltage measurement does not guarantee that absolute maximum junction temperature is not exceeded.

TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

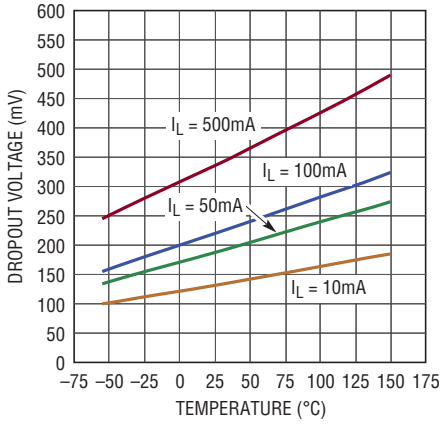
Typical Dropout Voltage



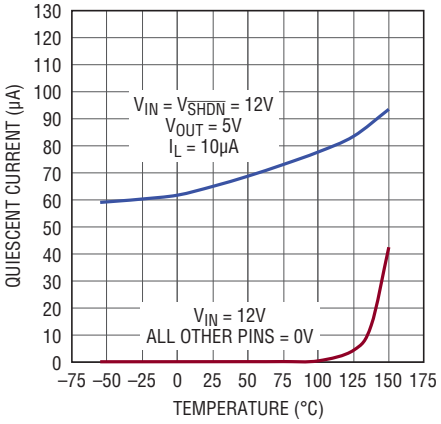
Guaranteed Dropout Voltage



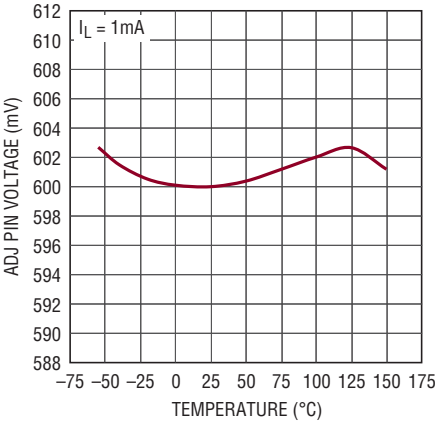
Dropout Voltage



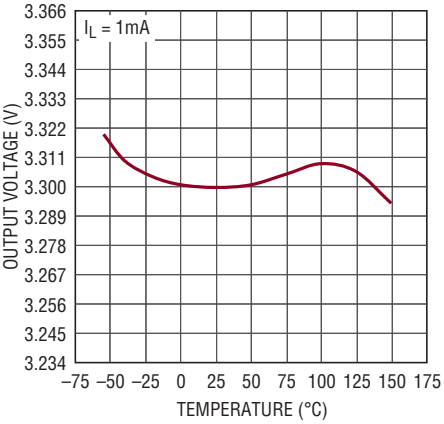
Quiescent Current



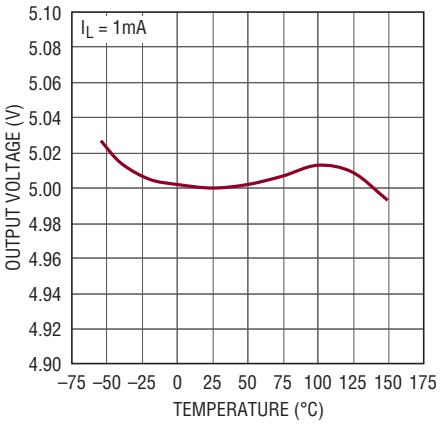
ADJ Pin Voltage



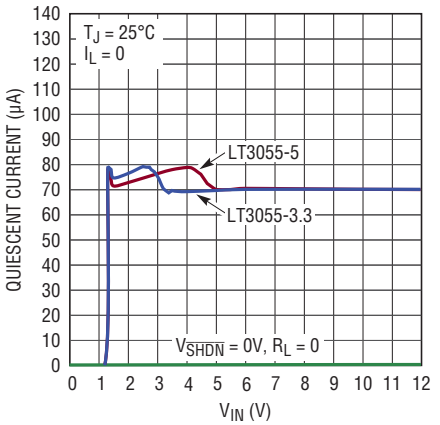
Output Voltage-LT3055-3.3



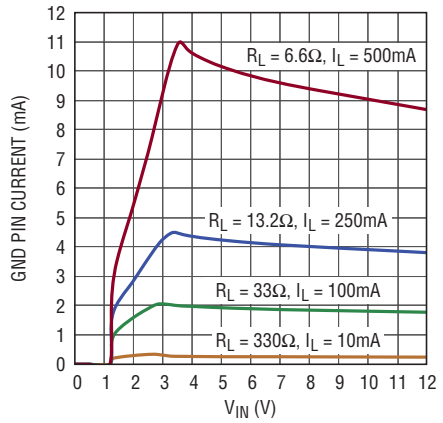
Output Voltage-LT3055-5



Quiescent Current

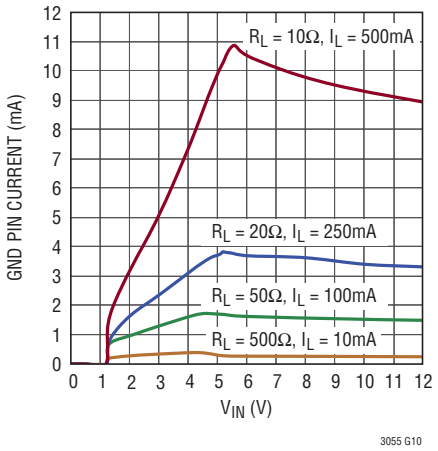


GND Pin Current-LT3055-3.3

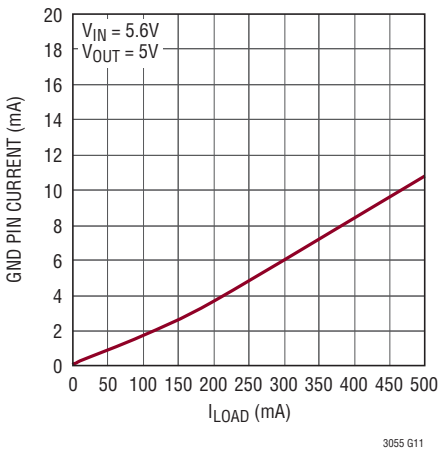


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

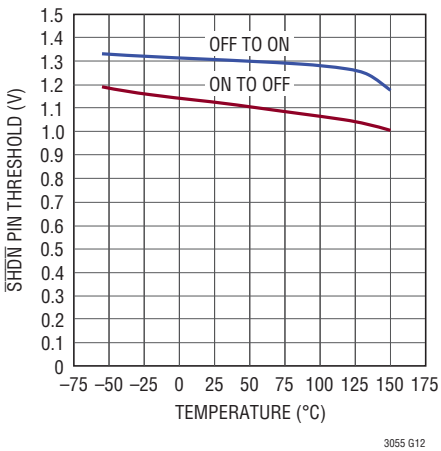
GND Pin Current-LT3055-5



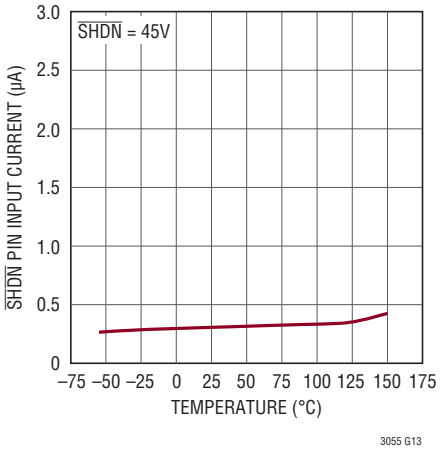
GND Pin Current vs I_{LOAD}



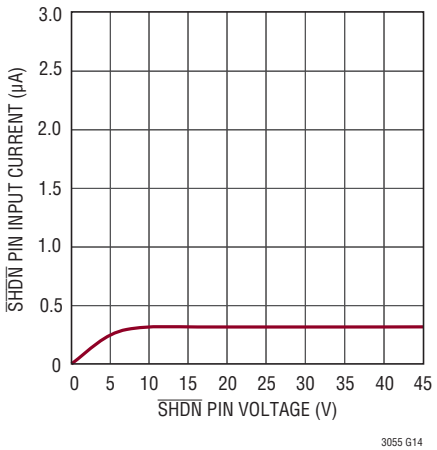
$\overline{SHDN}$ Pin Threshold



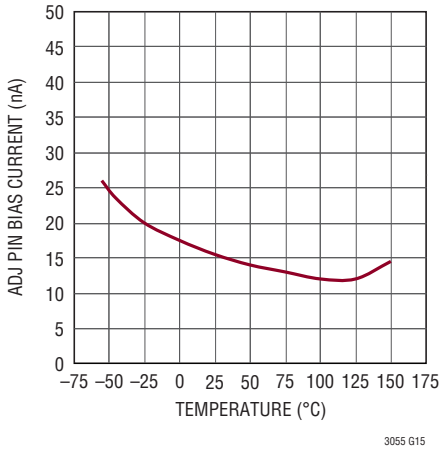
$\overline{SHDN}$ Pin Input Current



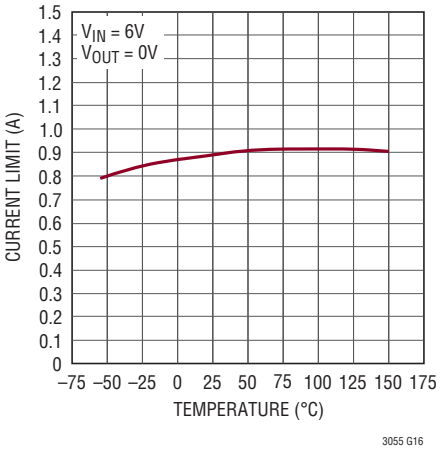
$\overline{SHDN}$ Pin Input Current



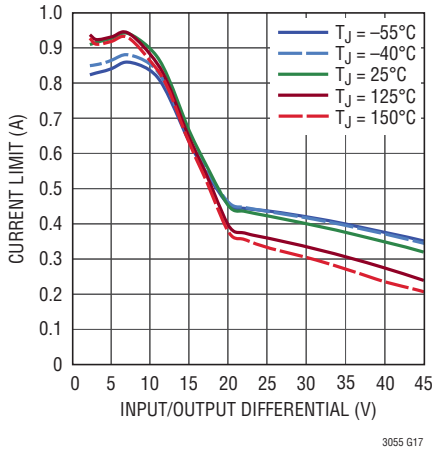
ADJ Pin Bias Current



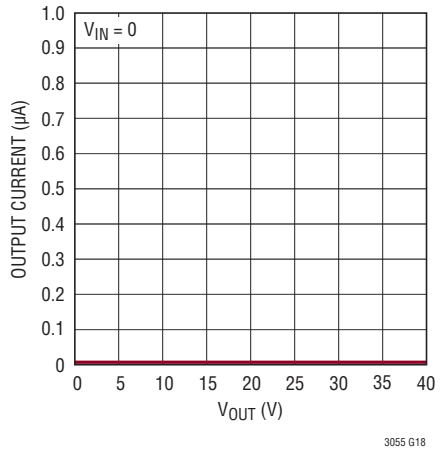
Internal Current Limit



Internal Current Limit

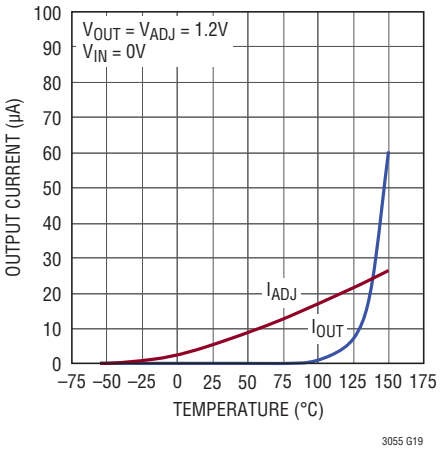


Reverse Output Current

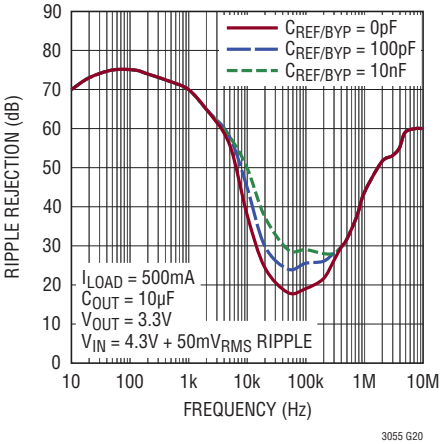


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

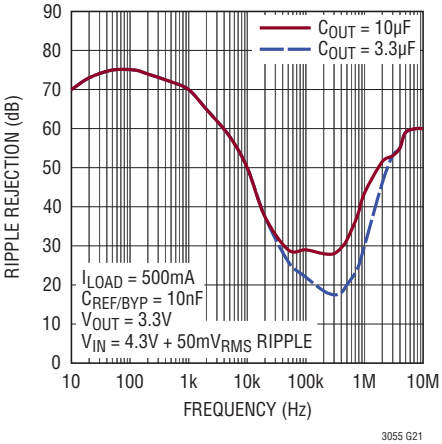
Reverse Output Current



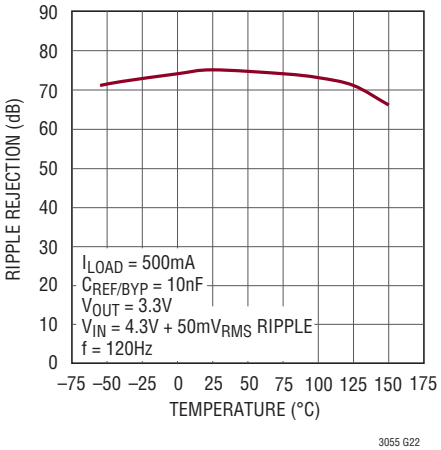
Input Ripple Rejection



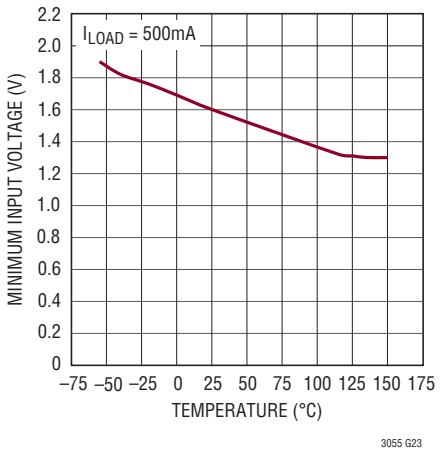
Input Ripple Rejection



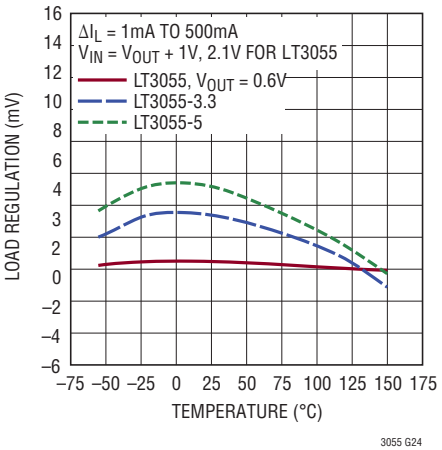
Input Ripple Rejection



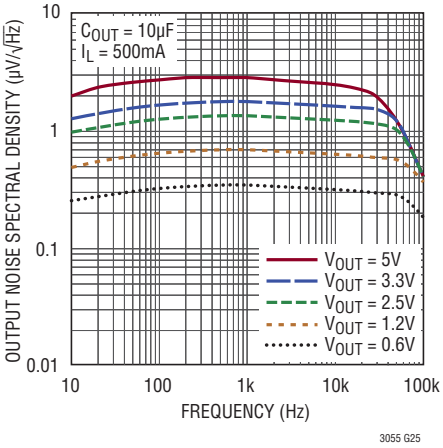
Minimum Input Voltage



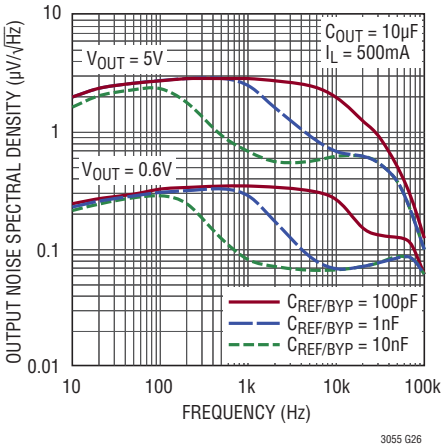
Load Regulation



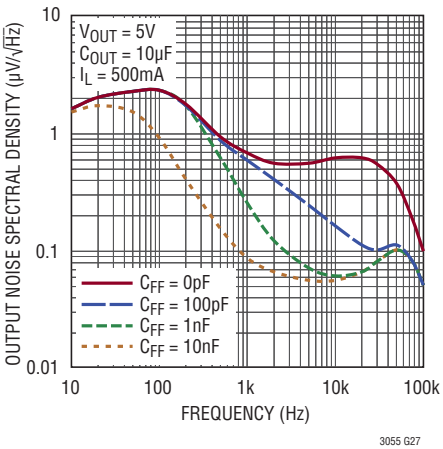
Output Noise Spectral Density
$C_{REF/BYP}$ = 0, C_{FF} = 0



Output Noise Spectral Density
vs $C_{REF/BYP}$, C_{FF} = 0

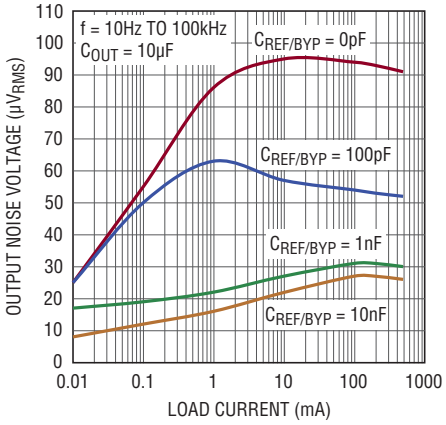


Output Noise Spectral Density
vs C_{FF}, $C_{REF/BYP}$ = 10nF

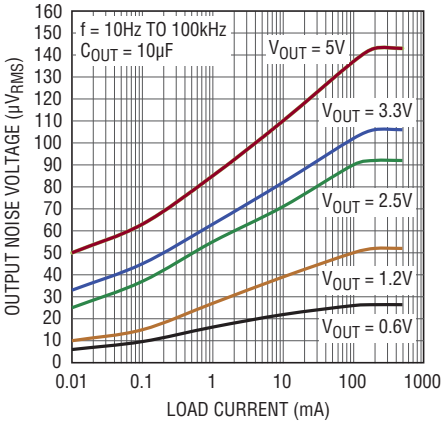


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

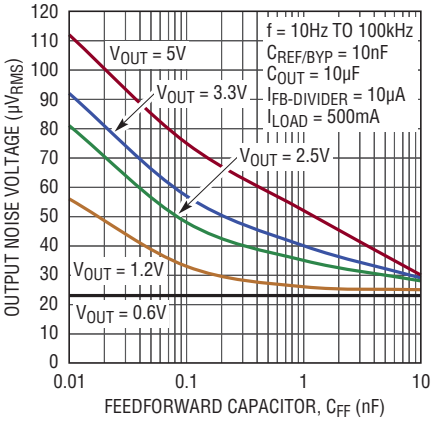
RMS Output Noise vs $C_{REF/BYP}$, V_{OUT} = 0.6V, C_{FF} = 0



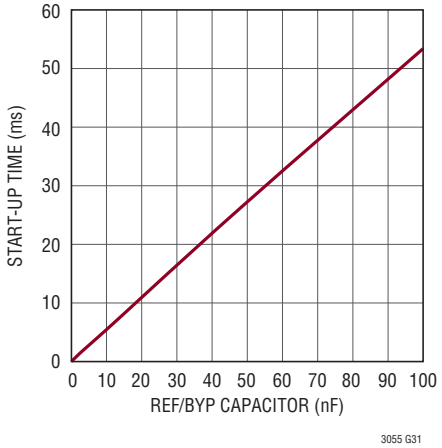
RMS Output Noise vs Load Current, $C_{REF/BYP}$ = 10nF, C_{FF} = 0



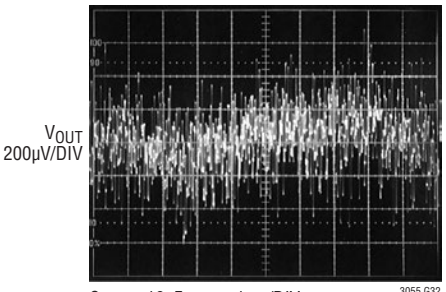
RMS Output Noise vs Feedforward Capacitor (C_{FF})



Start-Up Time vs REF/BYP Capacitor

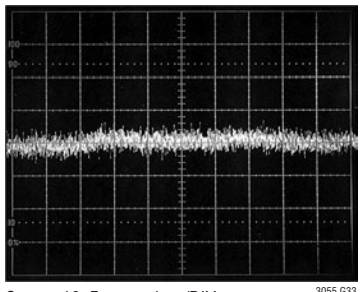


10Hz to 100kHz Output Noise $C_{REF/BYP}$ = 10nF, C_{FF} = 0



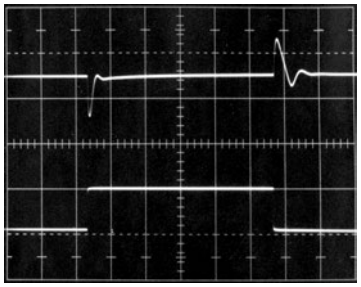
COUT = 10µF
ILOAD = 500mA
VOUT = 5V
1ms/DIV

10Hz to 100kHz Output Noise $C_{REF/BYP}$ = 10nF, C_{FF} = 10nF



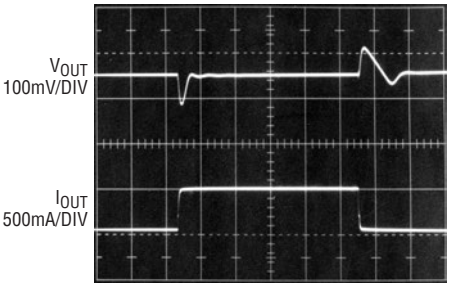
COUT = 10µF
ILOAD = 500mA
VOUT = 5V
1ms/DIV

5V Transient Response C_{FF} = 0, I_{OUT} = 50mA to 500mA



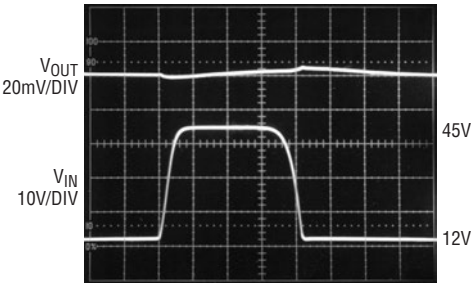
VIN = 6V
COUT = 10µF
IFB-DIVIDER = 10µA
VOUT = 5V
100µs/DIV

5V Transient Response C_{FF} = 10nF, I_{OUT} = 50mA to 500mA



VIN = 6V
COUT = 10µF
IFB-DIVIDER = 10µA
VOUT = 5V
20µs/DIV

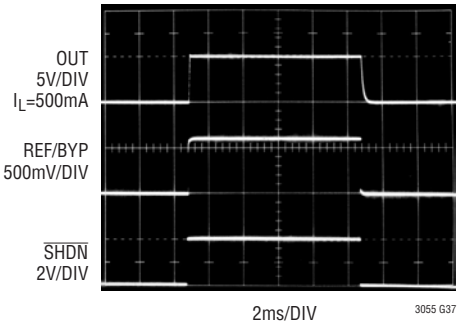
Transient Response (Load Dump)



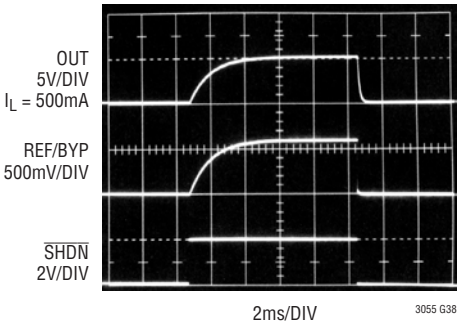
VOUT = 5V
IOUT = 100mA
COUT = 10µF
1ms/DIV

TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

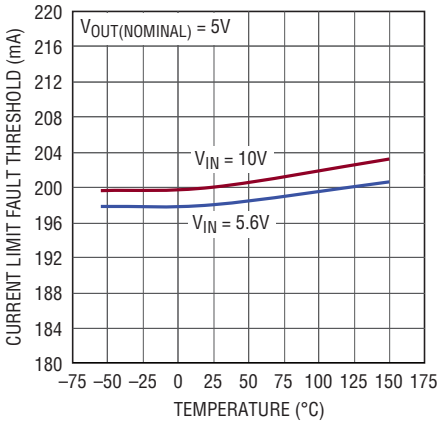
$\overline{SHDN}$ Transient Response $C_{REF/BYP}$ = 0



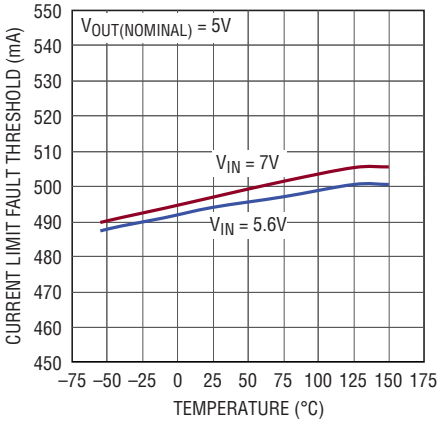
$\overline{SHDN}$ Transient Response $C_{REF/BYP}$ = 10nF



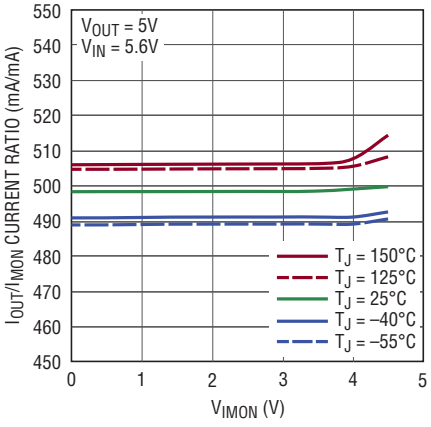
Precision Current Limit, R_{IMAX} = 1.5k



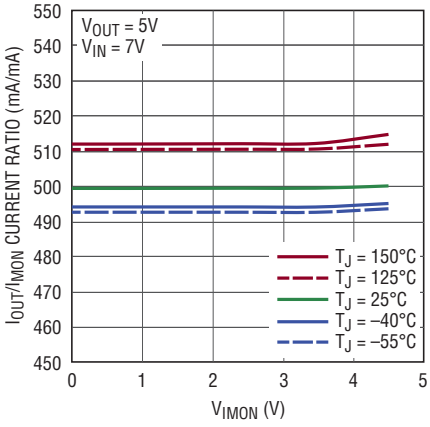
Precision Current Limit, R_{IMAX} = 604Ω



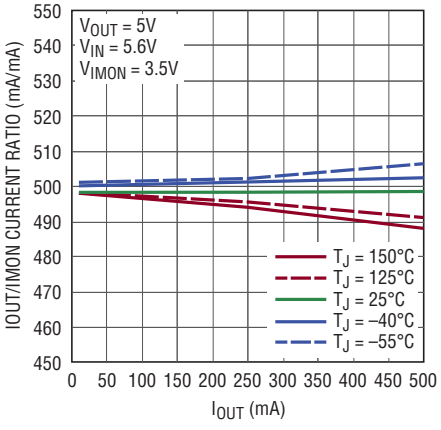
I_{OUT}/I_{MON} Ratio, I_{OUT} = 500mA



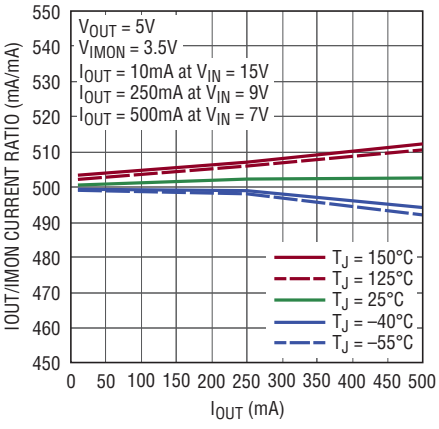
I_{OUT}/I_{MON} Ratio, I_{OUT} = 500mA



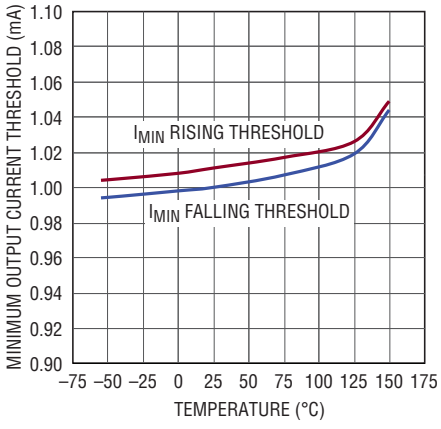
I_{OUT}/I_{MON} Current Ratio



I_{OUT}/I_{MON} Current Ratio

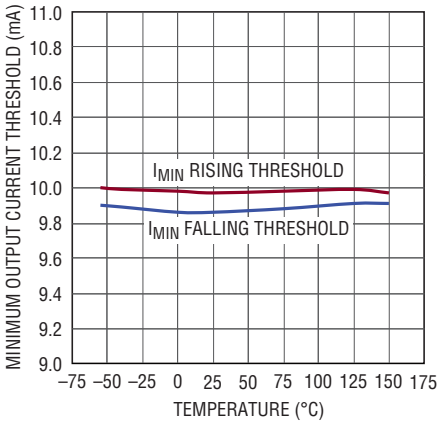


Minimum Output Current Threshold, R_{IMIN} = 1.2M

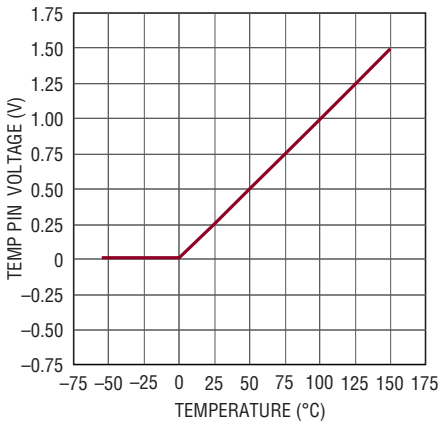


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

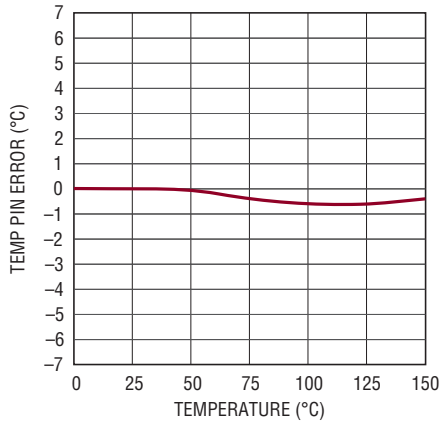
Minimum Output Current Threshold R_{IMIN} = 120k



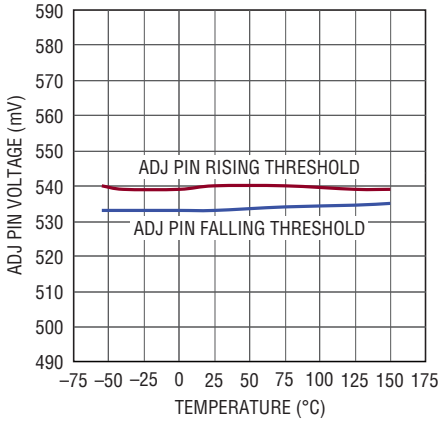
TEMP Output Voltage vs Temperature



TEMP Pin Error



PWRGD Threshold Voltage



PIN FUNCTIONS

IN (Pins 1, 2): Input. These pins supply power to the device. The LT3055 requires a local IN bypass capacitor if it is located more than six inches from the main input filter capacitor. In general, battery output impedance rises with frequency, so adding a bypass capacitor in battery-powered circuits is advisable. A bypass capacitor in the range of 1µF to 10µF is sufficient. See Input Capacitance and Stability in the Applications Information section for more information.

The LT3055 regulator withstands reverse voltages on the IN pins with respect to ground and the OUT pins. In the case of a reverse input, which can happen if a battery is plugged in backwards, the device acts as if there is a diode in series with its input. No reverse current flows into the regulator and no reverse voltage appears at the load.The device protects both itself and the load.

$\overline{\text{SHDN}}$ (Pin 3): Shutdown. Pulling the $\overline{\text{SHDN}}$ pin low puts the LT3055 into a low power state and turns the output off. Drive the $\overline{\text{SHDN}}$ pin with either logic or an open-collector/drain with a pull-up resistor. The resistor supplies the pull-up current to the open-collector/drain logic, normally several microamperes, and the $\overline{\text{SHDN}}$ pin current, typically less than 2µA. If unused, connect the $\overline{\text{SHDN}}$ pin to IN. The LT3055 does not function if the $\overline{\text{SHDN}}$ pin is not connected.

$\overline{\text{FAULT1}}$ (Pin 4), $\overline{\text{FAULT2}}$ (Pin 5): Fault Indicator Pins. $\overline{\text{FAULT1}}$ and $\overline{\text{FAULT2}}$ are open-collector logic pins. If the output current drops below the minimum current threshold, $\overline{\text{FAULT1}}$ asserts low. If the output current exceeds the current limit threshold, $\overline{\text{FAULT2}}$ asserts low. If the LT3055 enters thermal shutdown, both $\overline{\text{FAULT1}}$ and $\overline{\text{FAULT2}}$ assert low. The $\overline{\text{FAULT1}}$ and $\overline{\text{FAULT2}}$ pins are capable of sinking 50µA. There is no internal pull-up resistor; an external pull-up resistor must be used.

PWRGD (Pin 6): Power Good Pin. The PWRGD pin is an open-collector output that actively pulls low if the output is less than 90% of the nominal output value. The PWRGD pin is capable of sinking 50µA. There is no internal pull-up resistor, an external pull-up resistor must be used.

TEMP (Pin 7): Temperature Output. The TEMP pin outputs a voltage proportional to the average junction temperature. The pin voltage is 250mV for 25°C and has a slope of 10mV/°C.The TEMP pin output impedance is approximately 1500Ω. The TEMP pin is stable with no bypass capacitor or with a bypass capacitor with a value between 100pF and 1nF. A 100pF capacitor is recommended to improve TEMP pin power supply rejection. If not used, leave TEMP unconnected.

I_{MON} (Pin 8): Output Current Monitor. This pin is the collector of a PNP current mirror that outputs 1/500th of the power PNP current. The I_{MON} pin requires a small (22nF minimum) decoupling capacitor. In applications where the I_{MON} pin is used in an external feedback network (current sharing, cable drop compensation, etc.) smaller bypass capacitance values may be used to ensure stability of the external feedback network. If not used, tie I_{MON} to GND.

I_{MIN} (Pin 9): Minimum Output Current Programming Pin. This pin is the collector of a PNP current mirror that outputs 1/2000th of the power PNP load current. This pin is also the input to the minimum output current fault comparator. Connecting a resistor between I_{MIN} and GND sets the minimum output current fault threshold. For detailed information on how to set the I_{MIN} pin resistor value, please see the Operation section. A small external decoupling capacitor (10nF minimum) is required to improve I_{MIN} PSRR. If minimum output current programming is not required, float the I_{MIN} pin (unconnected).

I_{MAX} (Pin 10): Precision Current Limit Programming Pin. This pin is the collector of a current mirror PNP that is 1/500th the size of the output power PNP. This pin is also the input to the current limit amplifier. Current limit threshold is set by connecting a resistor between the I_{MAX} pin and GND. For detailed information on how to set the I_{MAX} pin resistor value, please see the Operation section. The I_{MAX} pin requires a 22nF decoupling capacitor to ground. If not used, tie I_{MAX} to GND.

PIN FUNCTIONS

REF/BYP (Pin 11): Bypass/Soft-Start. Connecting a capacitor from this pin to GND bypasses the LT3055's reference noise and soft starts the reference. A 10nF bypass capacitor typically reduces output voltage noise to 25μV_{RMS} in a 10Hz to 100kHz bandwidth. Soft-start time is directly proportional to BYP/SS capacitor value. If the LT3055 is placed in shutdown, BYP/SS is actively pulled low by an internal device to reset soft-start. If low noise or soft-start performance is not required, this pin must be left floating (unconnected). Do not drive this pin with any active circuitry. Because the REF/BYP pin is the reference input to the error amplifier, stray capacitance at this point should be minimized. Special attention should be given to any stray capacitances that can couple external signals onto the REF/BYP pin producing undesirable output transients or ripple. A minimum REF/BYP capacitance of 100pF is recommended.

GND (LT3055: Pin 12, Pin 13, Exposed Pad Pin 17): Ground. The exposed pad of the DFN and MSOP packages is an electrical connection to GND. To ensure proper electrical and thermal performance, solder Pin 17 to the PCB ground and tie it directly to Pins 12, 13. Connect the bottom of the output voltage setting resistor divider directly to GND (Pin 12) for optimum load regulation.

GND (LT3055-3.3, LT3055-5: Pin 12, Exposed Pad Pin 17): Ground. The exposed pad of the DFN and MSOP packages is an electrical connection to GND. To ensure proper electrical and thermal performance, solder Pin 17 to the PCB ground and tie it directly to Pin 12. Connect the bottom of the output voltage setting resistor divider directly to GND (Pin 12) for optimum load regulation.

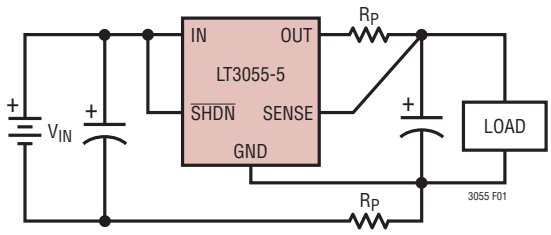


Figure 1. Kelvin Sense Connection

ADJ (LT3055: Pin 14): Adjust. This pin is the error amplifier's inverting terminal. The typical bias current of 16nA flows out of the pin (see the ADJ pin Bias Current vs Temperature curve in the Typical Performance Characteristics section). The ADJ pin voltage is 600mV referenced to GND.

Connecting a capacitor from ADJ to OUT reduces output noise and improves transient response for output voltages greater than 600mV. See the Applications information section for calculating the value of the feedforward capacitor.

ADJ (LT3055-3.3, LT3055-5: Pin 13): Adjust. This pin is the error amplifier's inverting terminal. The typical bias current of 16nA flows out of the pin (see the ADJ pin Bias Current vs Temperature curve in the Typical Performance Characteristics section). The ADJ pin voltage is 600mV referenced to GND.

Connecting a capacitor from ADJ to OUT reduces output noise and improves transient response for output voltages greater than 600mV. See the Applications information section for calculating the value of the feedforward capacitor.

SENSE (LT3055-3.3, LT3055-5: Pin 14): Sense. This pin is the top of the internal resistor divider network. SENSE should be connected directly to the load, as a Kelvin sense, for optimum load regulation and transient performance. Connecting this pin to the output pin, rather than directly to the load, can result in load regulation errors due to the current across the parasitic resistance of the PCB trace.

OUT (Pins 15,16): Output. These pins supply power to the load. Stability requirements demand a minimum 3.3μF ceramic output capacitor with an ESR < 1Ω to prevent oscillations. For output voltages less than 1.2V, a minimum 4.7μF ceramic output capacitor is required. Large load transient applications require larger output capacitors to limit peak voltage transients. See the Applications Information section for details on output capacitance and reverse output characteristics. Permissible output voltage range is 600mV to 40V.

BLOCK DIAGRAM

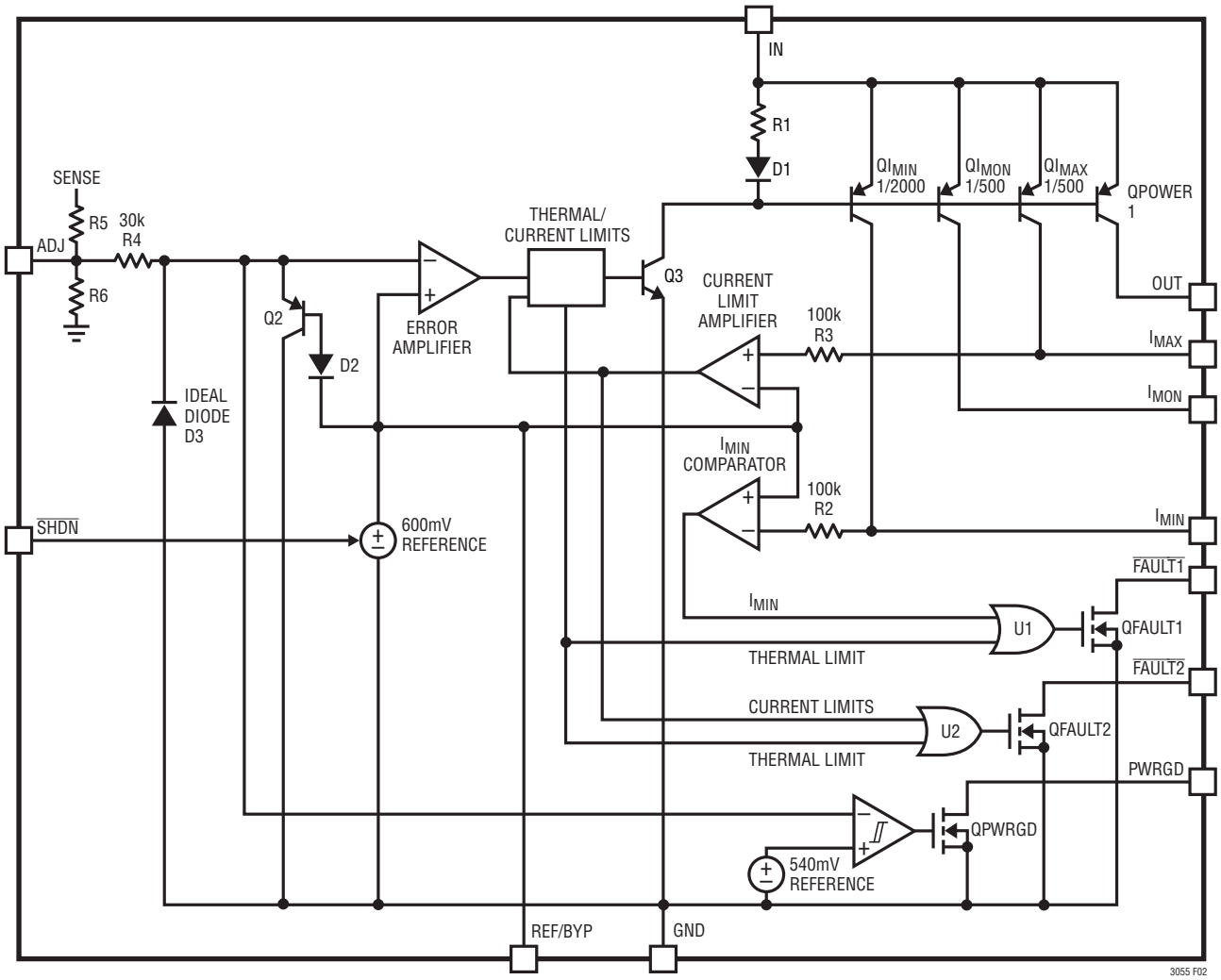


Figure 2

OPERATION

I_{MON} Pin Operation (Current Monitor)

The I_{MON} pin is the collector of a PNP which mirrors the LT3055 output PNP at a ratio of 1:500 (see Block Diagram). There is additional circuitry which compensates for early voltage variation by regulating the collector of the I_{MON} mirror PNP at the output voltage. This circuitry is active for $V_{IMON} \leq (V_{OUT} - 500mV)$. For the range where the early voltage compensation circuit is active, calculate the output current from the simple equation:

$$I_{OUT} = 500 \bullet \frac{V_{IMON}}{R_{IMON}}$$

For $V_{IMON} > (V_{OUT}\text{-}500mV)$, the I_{MON} mirror PNP collector is $V_{IMON} + VDS_{SAT}$ (500mV at 500mA). Early voltage effects increase the I_{OUT} to I_{MON} ratio as V_{IMON} increases.

OPERATION

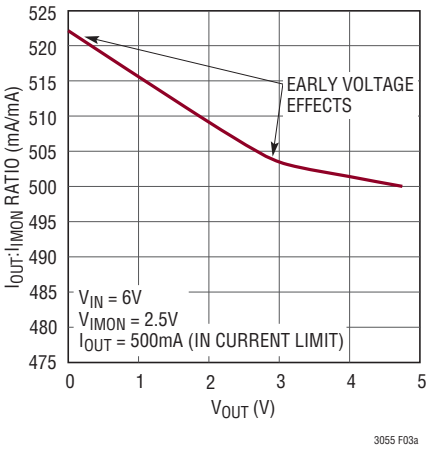


Figure 3a. I_{OUT}:I_{IMON} Ratio vs V_{OUT}

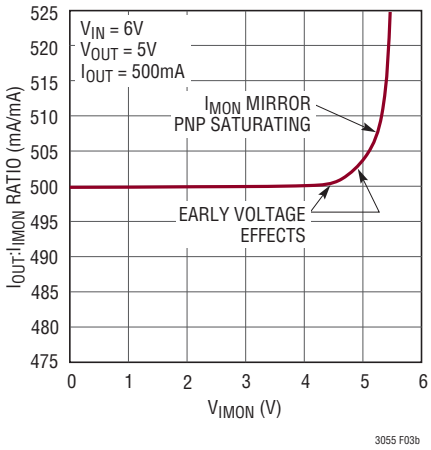


Figure 3b. I_{OUT}:I_{IMON} Ratio vs V_{IMON}

In addition, if $V_{IN} - V_{IMON} < 1V$, the I_{MON} mirror PNP saturates at high loads, causing the I_{OUT}-to-I_{MON} ratio to increase quickly. The I_{MON} mirror ratio is affected by power dissipation in the LT3055; it increases at a rate of approximately 0.5 percent per watt.

Open-Circuit Detection (I_{MIN} Pin)

The I_{MIN} pin is the collector of a PNP which mirrors the LT3055 output PNP at a ratio of 1:2000 (see Block Diagram). The I_{MIN} fault comparator asserts the $\overline{FAULT1}$ pin if the I_{MIN} pin voltage is below 0.6V. This low output current fault threshold voltage (I_{OPEN}) is set by attaching a resistor from I_{MIN} to GND:

$$R_{IMIN} = 2000 \bullet \frac{0.6V}{I_{OPEN}}$$

If the open-circuit detection function is not needed, the I_{MIN} pin must be left floating (unconnected). A small decoupling capacitor (10nF minimum) from I_{MIN} to GND is required to improve I_{MIN} pin power supply rejection and to prevent $\overline{FAULT1}$ pin glitches. See the Typical Performance Characteristics section for additional information.

I_{MAX} Pin Operation

The I_{MAX} pin is the collector of a PNP which mirrors the LT3055 output PNP at a ratio of 1:500 (see Block Diagram). The I_{MAX} pin is also the input to the precision current limit amplifier. If the output load increases to the point where it causes the I_{MAX} pin voltage to reach 0.6V, the current limit amplifier takes control of the output regulation so that the I_{MAX} pin regulates at 0.6V, regardless of the output voltage. The current limit threshold (I_{LIMIT}) is set by connecting a resistor (R_{IMAX}) from I_{MAX} to GND:

$$R_{IMAX} = 500 \bullet \frac{0.6V}{I_{LIMIT}}$$

In cases where the IN to OUT differential voltage exceeds 10V, fold-back current limit lowers the internal current limit level, possibly causing it to override the external programmable current limit. See the Internal Current Limit vs V_{IN}-V_{OUT} graph in the Typical Performance Characteristics section.

The I_{MAX} pin requires a 22nF decoupling capacitor. If the external programmable current limit is not needed, the I_{MAX} pin must be connected to GND. The I_{MAX} threshold is affected by power dissipation in the LT3055; it increases at a rate of approximately 0.5 percent per watt.

$\overline{FAULT}$ Pins Operation

The $\overline{FAULT1}$ and $\overline{FAULT2}$ pins are open-drain high voltage NMOS digital outputs. The $\overline{FAULT1}$ pin asserts during a low current fault (open circuit). The $\overline{FAULT2}$ pin asserts during a current limit fault (internal or externally programmed). Both $\overline{FAULT1}$ and $\overline{FAULT2}$ assert during thermal shutdown. There is no internal pull-up on the $\overline{FAULT}$ pins; an external pull-up resistor is required. The $\overline{FAULT}$ pins sink up to 50µA of pull-down current. Off state logic may be as high as 45V, regardless of the input voltage used.

OPERATION

Table 1. $\overline{\text{FAULT}}$ Pins Truth Table

STATUS	$\overline{\text{FAULT1}}$	$\overline{\text{FAULT2}}$
Open Circuit	Low	High
Current Limit	High	Low
Thermal Shutdown	Low	Low

Depending on the I_{MIN} capacitance, BYP capacitance, and OUT capacitance, the $\overline{\text{FAULT}}$ pins may assert during start-up. Consideration should be given to masking the fault signals during start-up. The $\overline{\text{FAULT}}$ pin circuitry is inactive (not asserted) during shutdown and when the OUT pin is pulled above IN pin.

PWRGD Pin Operation

The PWRGD pin is an open-drain high voltage NMOS digital output. The PWRGD pin deasserts and becomes high impedance if the output rises above 90% of its nominal value. If the output falls below 89% of its nominal value for more than 25µs, the PWRGD pin asserts low. The PWRGD comparator has 1% hysteresis and 25µs of deglitching. The PWRGD comparator has a dedicated reference that does not soft-start when a capacitor is added to the REF/BYP pin.

The use of a feed-forward capacitor, CFF, as shown in Figure 5, can result in the ADJ pin being pulled artificially high during start- up transients, which causes the PWRGD flag to assert early. To avoid this problem, ensure that the REF/BYP capacitor is significantly larger than the feed-forward capacitor, causing REF/BYP time constant to dominate over the time constant of the resistor divider network.

Operation in Dropout

There may be some degradation of the current mirror accuracy for output currents less than 50mA when operating in dropout.

APPLICATIONS INFORMATION

The LT3055 is a micropower, low noise and low dropout voltage, 500mA linear regulator with micropower shutdown, programmable current limit, and diagnostic functions. The device supplies up to 500mA at a typical dropout voltage of 350mV and operates over a 2.2V to 45V input range.

A single external capacitor provides low noise reference performance and output soft-start functionality. For example, connecting a 10nF capacitor from the REF/BYP pin to GND lowers output noise to 25µV_{RMS} over a 10Hz to 100kHz bandwidth. This capacitor also soft starts the reference and prevents output voltage overshoot at turn-on.

The LT3055's quiescent current is merely 65µA but provides fast transient response with a minimum low ESR 3.3µF ceramic output capacitor. In shutdown, quiescent current is less than 1µA and the reference soft-start capacitor is reset.

The LT3055 optimizes stability and transient response with low ESR, ceramic output capacitors. The regulator does not require the addition of ESR as is common with other regulators. The LT3055 typically provides 0.1% line regulation and 0.1% load regulation. Internal protection circuitry includes reverse battery protection, reverse output protection, reverse current protection, current limit with fold-back and thermal shutdown.

This "bullet-proof" protection set makes it ideal for use in battery-powered, automotive and industrial systems.

In battery backup applications where the output is held up by a backup battery and the input is pulled to ground, the LT3055 acts like it has a diode in series with its output and prevents reverse current flow.

APPLICATIONS INFORMATION

Adjustable Operation

The adjustable LT3055 has an output voltage range of 0.6V to 40V. The output voltage is set by the ratio of two external resistors, as shown in Figure 4. The device servos the output to maintain the ADJ pin voltage at 0.6V referenced to ground. The current in R1 is then equal to 0.6V/R1, and the current in R2 is the current in R1 minus the ADJ pin bias current.

The ADJ pin bias current, 16nA at 25°C, flows from the ADJ pin through R1 to GND. Calculate the output voltage using the formula in Figure 4. The value of R1 should be no greater than 62k to provide a minimum 10µA load current so that output voltage errors, caused by the ADJ pin bias current, are minimized. Note that in shutdown, the output is turned off and the divider current is zero. Curves of ADJ Pin Voltage vs Temperature and ADJ Pin Bias Current vs Temperature appear in the Typical Performance Characteristics section.

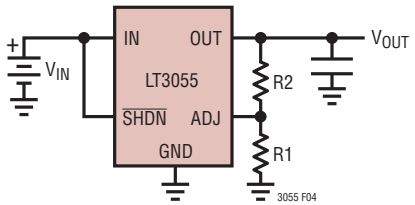
The LT3055 is tested and specified with the ADJ pin tied to the OUT pin, yielding V_{OUT} = 0.6V. Specifications for output voltages greater than 0.6V are proportional to the ratio of the desired output voltage to 0.6V: V_{OUT}/0.6V. For example, load regulation for an output current change of 1mA to 500mA is 0.5mV (typical) at V_{OUT} = 0.6V. At V_{OUT} = 12V, load regulation is:

$$\frac{12V}{0.6V} \bullet (0.5mV) = 10mV$$

Table 2 shows 1% resistor divider values for some common output voltages with a resistor divider current of 10µA.

Table 2. Output Voltage Resistor Divider Values

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.2	60.4	60.4
1.5	59	88.7
1.8	59	118
2.5	60.4	191
3	59	237
3.3	61.9	280
5	59	432



$$V_{OUT} = 0.6V\left(1+\frac{R2}{R1}\right)-(I_{ADJ} \bullet R2)$$

$V_{ADJ} = 0.6V$

I_{ADJ} = 16nA AT 25°C

OUTPUT RANGE = 0.6V TO 40V

Figure 4. Adjustable Operation

Bypass Capacitance and Output Voltage Noise

The LT3055 regulator provides low output voltage noise over a 10Hz to 100kHz bandwidth while operating at full load with the addition of a bypass capacitor ($C_{REF/BYP}$) from the REF/BYP pin to GND. A high quality low leakage capacitor is recommended. This capacitor bypasses the internal reference of the regulator, providing a low frequency noise pole for the internal reference. With the use of 10nF for $C_{REF/BYP}$, output voltage noise decreases to as low as 25µV_{RMS} when the output voltage is set for 0.6V. For higher output voltages (generated by using a feedback resistor divider), the output voltage noise gains up proportionately when using $C_{REF/BYP}$.

To lower the higher output voltage noise, include a feedforward capacitor (C_{FF}) from V_{OUT} to the ADJ pin. A high quality, low leakage capacitor is recommended. This capacitor bypasses the error amplifier of the regulator, providing an additional low frequency noise pole. With the use of 10nF for both C_{FF} and $C_{REF/BYP}$, output voltage noise decreases to 25µV_{RMS} when the output voltage is set to 5V by a 10µA feedback resistor divider. If the current in the feedback resistor divider is doubled, C_{FF} must also be doubled to achieve equivalent noise performance.

Higher values of output voltage noise can occur if care is not exercised with regard to circuit layout and testing. Crosstalk from nearby traces induces unwanted noise onto the LT3055's output. Power supply ripple rejection

APPLICATIONS INFORMATION

must also be considered. The LT3055 regulator does not have unlimited power supply rejection and passes a small portion of the input noise through to the output.

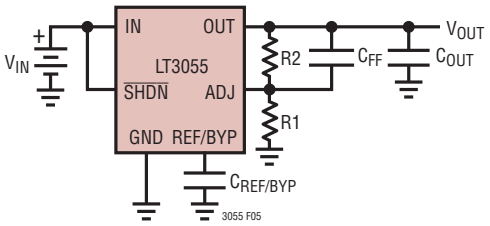
Using a feedforward capacitor (C_{FF}) from V_{OUT} to the ADJ pin has the added benefit of improving transient response for output voltages greater than 0.6V. With no feedforward capacitor, the settling time increases as the output voltage increases above 0.6V. Use the equation in Figure 5 to determine the minimum value of C_{FF} to achieve a transient response that is similar to the 0.6V output voltage performance regardless of the chosen output voltage (See Figure 6 and Transient Response in the Typical Performance Characteristics section).

During start-up, the internal reference soft-starts when a bypass capacitor is present. Regulator start-up time is directly proportional to the size of the bypass capacitor (See Start-Up Time vs REF/BYP Capacitor in the Typical Performance Characteristics section). The reference bypass capacitor is actively pulled low during shutdown to reset the internal reference.

Start-up time is also affected by the presence of a feedforward capacitor. Start-up time is directly proportional to the size of the feedforward capacitor and the output voltage, and is inversely proportional to the feedback resistor divider current, slowing to 15ms with a 10nF feedforward capacitor and a 10µF output capacitor for an output voltage set to 5V by a 10µA feedback resistor divider.

Output Capacitance and Transient Response

The LT3055 regulator is stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. Use a minimum output capacitor of 3.3µF with an ESR of 1Ω or less to prevent oscillations. If a feedforward capacitor is used with output voltages set for greater than 24V, use a minimum output capacitor of 10µF. The LT3055 is a micropower device and output load transient response is a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the LT3055, increase the effective output capacitor value. For applications with large load current transients, a low ESR ceramic



$$C_{FF} \geq \frac{10nF}{10\mu A} \bullet (I_{FB_DIVIDER})$$

$$I_{FB_DIVIDER} = \frac{V_{OUT}}{R1+R2}$$

Figure 5. Feedforward Capacitor for Fast Transient Response

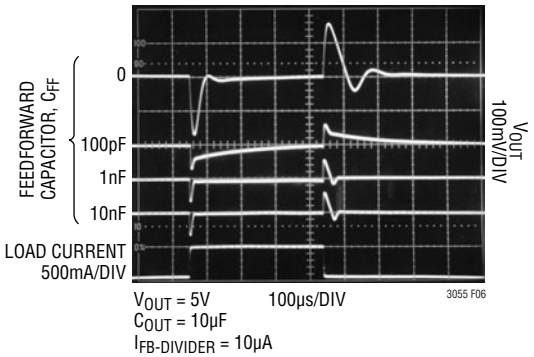


Figure 6. Transient Response vs Feedforward Capacitor

capacitor in parallel with a bulk tantalum capacitor often provides an optimally damped response.

Give extra consideration to the use of ceramic capacitors. Manufacturers make ceramic capacitors with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics provide high C-V products in a small package at low cost, but exhibit strong voltage and temperature coefficients, as shown in Figures 7 and 8. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied, and over the operating temperature range. The X5R and X7R dielectrics yield much more stable characteristics and are more suitable for use as the output capacitor.

The X7R type works over a wider temperature range and has better temperature stability, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R

APPLICATIONS INFORMATION

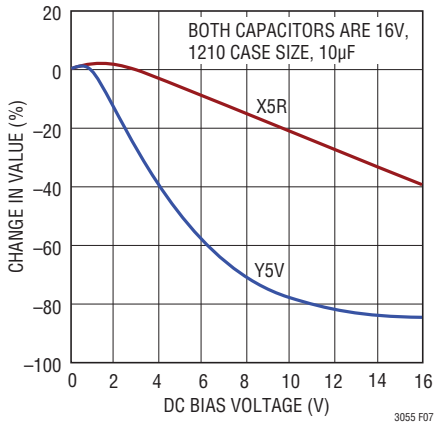


Figure 7. Ceramic Capacitor DC Bias Characteristics

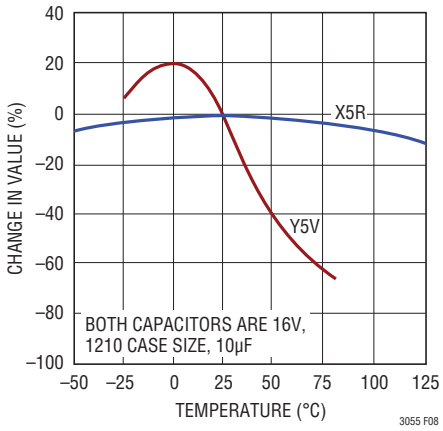


Figure 8. Ceramic Capacitor Temperature Characteristics

and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress is induced by vibrations in the system or thermal transients. The resulting voltages produced cause appreciable amounts of noise. A ceramic capacitor produced the trace in Figure 9 in response to light tapping from a pencil. Similar vibration induced behavior can masquerade as increased output voltage noise.

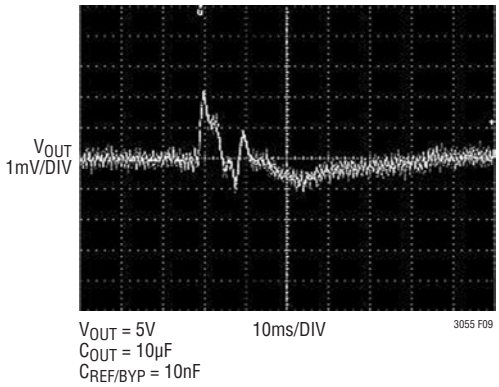


Figure 9. Noise Resulting from Tapping On a Ceramic Capacitor

Stability and Input Capacitance

Low ESR, ceramic input bypass capacitors are acceptable for applications without long input leads. However, applitions connecting a power supply to an LT3055 circuit's IN and GND pins with long input wires combined with a low ESR, ceramic input capacitors are prone to voltage spikes, reliability concerns and application-specific board oscillations.

The input wire inductance found in many battery-powered applications, combined with the low ESR ceramic input capacitor, forms a high Q LC resonant tank circuit. In some instances this resonant frequency beats against the output current dependent LDO bandwidth and interferes with proper operation. Simple circuit modifications/solutions are then required. This behavior is not indicative of LT3055 instability, but is a common ceramic input bypass capacitor application issue.

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. Wire diameter is not a major factor on its self-inductance. For example, the self-inductance of a 2-AWG isolated wire (diameter = 0.26") is about half the self-inductance of a 30-AWG wire (diameter = 0.01"). One foot of 30-AWG wire has approximately 465nH of self-inductance.

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Two methods can reduce wire self-inductance. One method divides the current flowing towards the LT3055 between two parallel conductors. In this case, the farther apart the wires are from each other, the more the self-inductance is reduced; up to a 50% reduction when placed a few inches apart. Splitting the wires connects two equal inductors in parallel, but placing them in close proximity creates mutual inductance adding to the self-inductance. The second and most effective way to reduce overall inductance is to place both forward and return current conductors (the input and GND wires) in very close proximity. Two 30-AWG wires separated by only 0.02", used as forward- and return-current conductors, reduce the overall self-inductance to approximately one-fifth that of a single isolated wire.

If a battery, mounted in close proximity, powers the LT3055, a 10µF input capacitor suffices for stability. However, if a distant supply powers the LT3055, use a larger value input capacitor. Use a rough guideline of 1µF (in addition to the 10µF minimum) per 8 inches of wire length. The minimum input capacitance needed to stabilize the application also varies with power supply output impedance variations. Placing additional capacitance on the LT3055's output also helps. However, this requires an order of magnitude more capacitance in comparison with additional LT3055 input bypassing. Series resistance between the supply and the LT3055 input also helps stabilize the application; as little as 0.1Ω to 0.5Ω suffices. This impedance dampens the LC tank circuit at the expense of dropout voltage. A better alternative is to use higher ESR tantalum or electrolytic capacitors at the LT3055 input in place of ceramic capacitors.

Paralleling Devices

Higher output current is obtained by paralleling multiple LT3055 together. Tie the individual OUT pins together and tie the individual IN pins together. An external NPN or NMOS current mirror is used in combination with the LT3055 I_{MON} pins to create a simple amplifier. This amplifier injects current into or out of the feedback divider of the slave LT3055 in order to ensure that the I_{MON} currents from each LT3055 are equal.

In Figure 10, this is implemented using inexpensive 2N3904 NPN devices. Precision 1k resistors provide 1V emitter degeneration at full load to guarantee good current mirror matching. The feedback resistors of the slave LT3055 are split into sections to ensure adequate headroom for the slave 2N3904. A 1nF capacitor added to the I_{MON} pin of the slave device frequency compensates the feedback loop.

This circuit architecture is scalable to as many LT3055s as are needed simply by extending the current mirror and adding slave LT3055 devices.

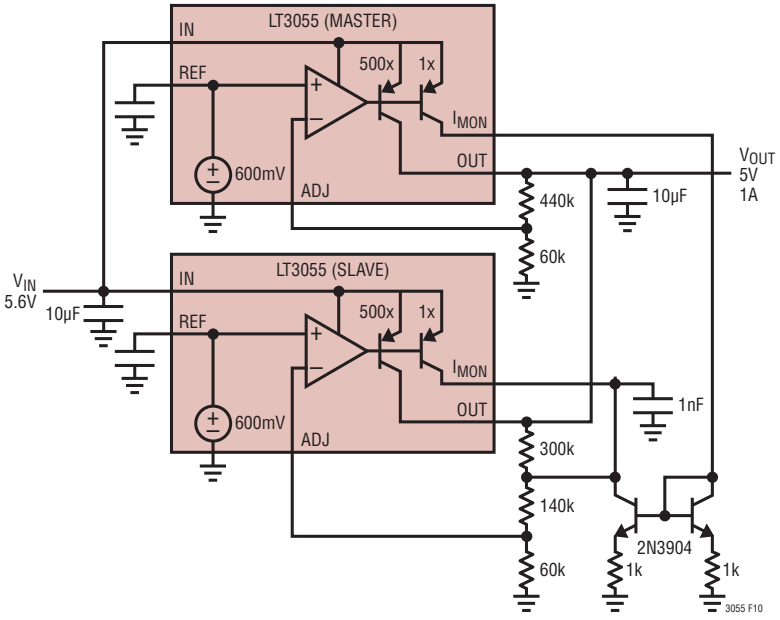


Figure 10. Parallel Devices

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Spreading the devices on the PC board also spreads the heat. Series input resistors can further spread the heat if the input-to-output differential is high.

Overload Recovery

Like many IC power regulators, the LT3055 has safe operating area protection. The safe area protection decreases current limit as input-to-output voltage increases, and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The LT3055 provides some output current at all values of input-to-output voltage up to the device breakdown.

When power is first applied, the input voltage rises and the output follows the input; allowing the regulator to start-up into very heavy loads. During start-up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein the removal of an output short will not allow the output to recover. Other regulators, such as the LT1083/LT1084/ LT1085 family and LT1764A also exhibit this phenomenon, so it is not unique to the LT3055. The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations are immediately after the removal of a short circuit or if the shutdown pin is pulled high after the input voltage is already turned on. The load line intersects the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply needs to be cycled down to zero and back up again to recover the output.

Thermal Considerations

The LT3055's maximum rated junction temperature of 125°C (E-, I-grades) or 150°C (MP-, H-grades) limits its power handling capability. Two components comprise the power dissipated by the device:

1. Output current multiplied by the input/output voltage differenvl:

   $I_{OUT} \bullet (V_{IN} – V_{OUT})$, and

2. GND pin current multiplied by the input voltage:

   $I_{GND} \bullet V_{IN}$

GND pin current is determined using the GND Pin Current curves in the Typical Performance Characteristics section. Power dissipation equals the sum of the two components listed above.

The LT3055 regulator has internal thermal limiting that protects the device during overload conditions. For continuous normal conditions, do not exceed the maximum junction temperature of 125°C (E-, I-grades) or 150°C (MP-, H-grades). Carefully consider all sources of thermal resistance from junction-to-ambient including other heat sources mounted in proximity to the LT3055.

The undersides of the LT3055 DFN and MSE packages have exposed metal from the lead frame to the die attachment. These packages allow heat to directly transfer from the die junction to the printed circuit board metal to control maximum operating junction temperature. The dual-in-line pin arrangement allows metal to extend beyond the ends of the package on the topside (component side) of a PCB. Connect this metal to GND on the PCB. The multiple IN and OUT pins of the LT3055 also assist in spreading heat to the PCB.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes also can spread the heat generated by power devices.

Tables 3 and 4 list thermal resistance as a function of copper area in a fixed board size. All measurements were taken in still air on a 4-layer FR-4 board with 1oz solid internal planes, and 2oz external trace planes with a total board thickness of 1.6mm. For further information on thermal resistance and using thermal information, refer to JEDEC standard JESD51, notably JESD51-12.

Table 3. MSOP Measured Thermal Resistance

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE	BACKSIDE		
2500 sq mm	2500 sq mm	2500 sq mm	35°C/W
1000 sq mm	2500 sq mm	2500 sq mm	36°C/W
225 sq mm	2500 sq mm	2500 sq mm	37°C/W
100 sq mm	2500 sq mm	2500 sq mm	39°C/W

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Table 4. DFN Measured Thermal Resistance

COPPER AREA TOPSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500 sq mm	2500 sq mm	36°C/W
1000 sq mm	2500 sq mm	37°C/W
225 sq mm	2500 sq mm	38°C/W
100 sq mm	2500 sq mm	40°C/W

Calculating Junction Temperature

Example: Given an output voltage of 5V, an input voltage range of 12V ±5%, a maximum output current range of 75mA and a maximum ambient temperature of 85°C, what is the maximum junction temperature?

The power dissipated by the device equals:

$$I_{OUT(MAX)} \bullet (V_{IN(MAX)} - V_{OUT}) + I_{GND} \bullet V_{IN(MAX)}$$

where:

$I_{OUT(MAX)} = 75mA$

$V_{IN(MAX)} = 12.6V$

I_{GND} at ($I_{OUT} = 75mA$, $V_{IN} = 12V$) = 3.5mA

So:

$$P = 75mA \bullet (12.6V - 5V) + 3.5mA \bullet 12.6V = 0.614W$$

Using a DFN package, the thermal resistance ranges from 36°C/W to 40°C/W depending on the copper area. So the junction temperature rise above ambient approximately equals:

$$0.614W \bullet 40°C/W = 24.6°C$$

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient or:

$$T_{JMAX} = 85°C + 24.6°C = 110°C$$

Protection Features

The LT3055 incorporates several protection features that make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device also protects against reverse input voltages, reverse output voltages and reverse output-to-input voltages.

Current limit protection and thermal overload protection protect the device against current overload conditions at the output of the device. For normal operation, do not exceed a junction temperature of 125°C (E-, I-grades) or 150°C (MP-, H-grades).

The LT3055 IN pin withstands reverse voltages of 50V. The device limits current flow to less than 1µA (typically less than 25nA) and no negative voltage appears at OUT. The device protects both itself and the load against batteries that are plugged in backwards.

The LT3055 incurs no damage if its output is pulled below ground. If the input is left open circuit or grounded, the output can be pulled below ground by 50V. No current flows through the pass transistor from the output. However, current flows in (but is limited by) the feedback resistor divider that sets the output voltage. Current flows from the bottom resistor in the divider and from the ADJ pin's internal clamp through the top resistor in the divider to the external circuitry pulling OUT below ground. If the input is powered by a voltage source, the output sources current equal to its current limit capability and the LT3055 protects itself by thermal limiting. In this case, grounding the $\overline{SHDN}$ pin turns off the device and stops the output from sourcing current.

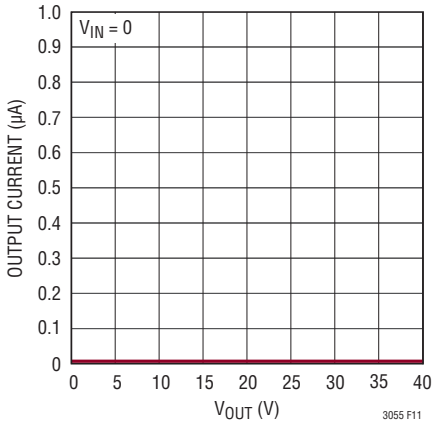
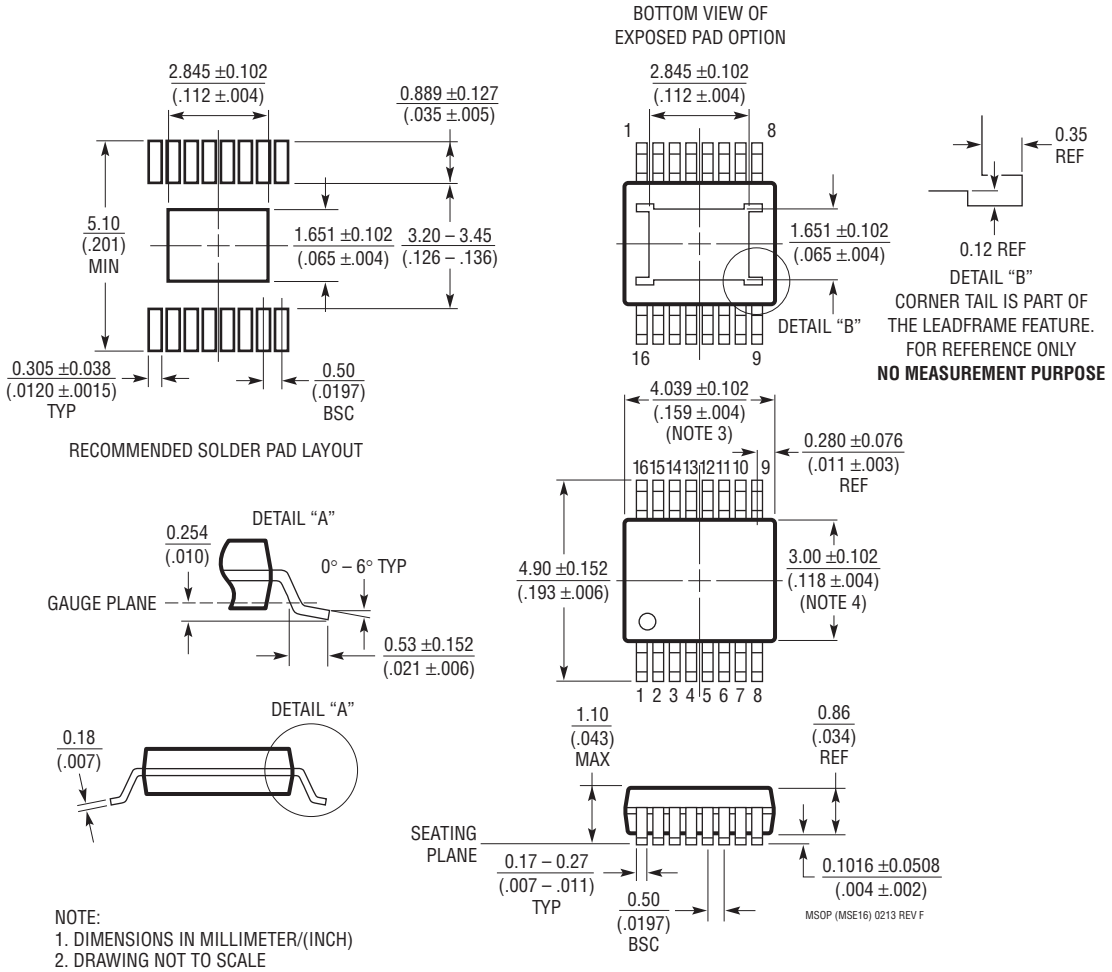


Figure 11. Reverse Output Current

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)

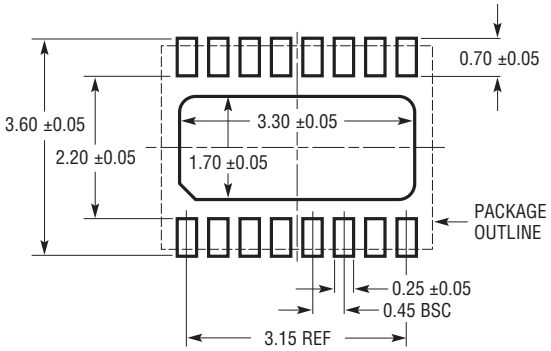


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

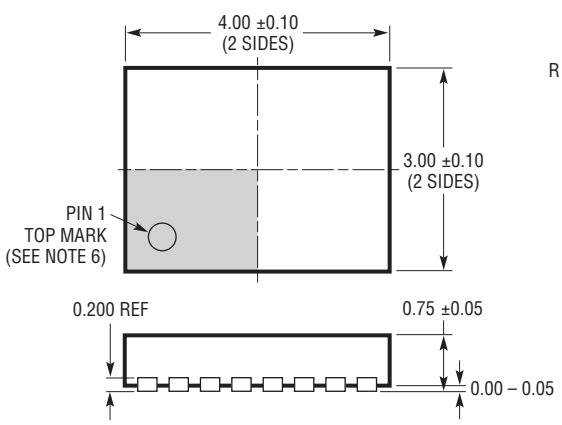
PACKAGE DESCRIPTION

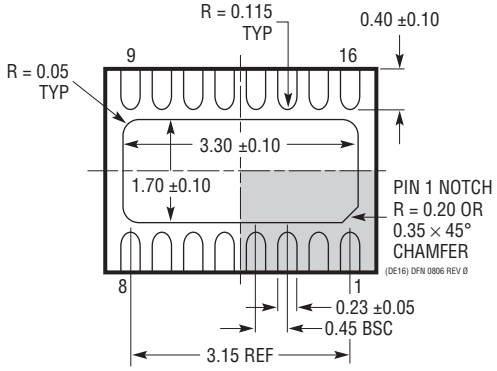
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DE Package
16-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1732 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

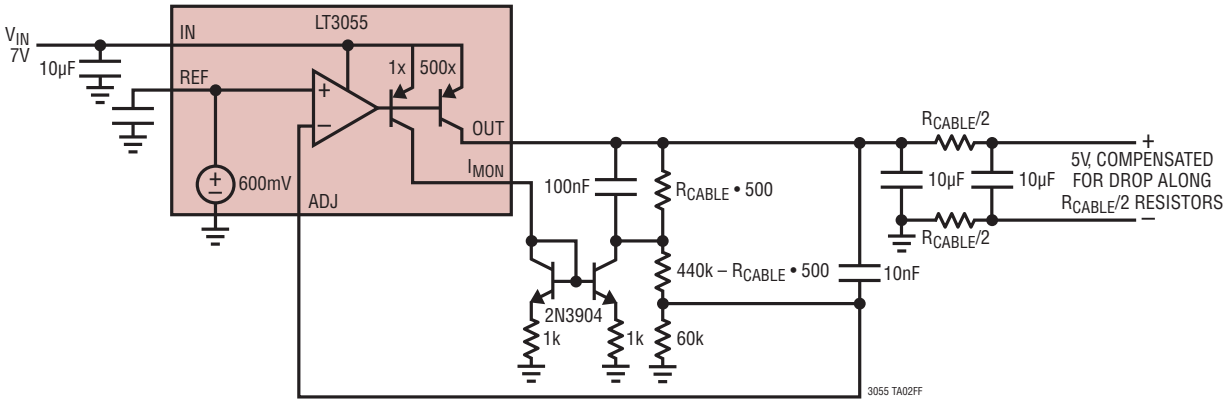
REV	DATE	DESCRIPTION	PAGE NUMBER
A	7/14	Modified Minimum V_{IN} to 1.8V	1
		Added 3.3V and 5V options, related specs, Typical Performance Characteristics and Pin Functions	Throughout
		Added specification for absolute maximum SENSE pin voltage	2
		Modified Pinouts to accommodate new fixed voltage options	2
		Modified Note 7	5
		Modified PWRGD applications section	16

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Cable Drop Compensation



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1761	100mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN}: 1.8V to 20V, ThinSOT™ Package
LT1762	150mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN}: 1.8V to 20V, MS8 Package
LT1763	500mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN}: 1.8V to 20V, SO-8 Package
LT1962	300mA, Low Noise LDO	270mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN}: 1.8V to 20V, MS8 Package
LT1964	200mA, Low Noise, Negative LDO	340mV Dropout Voltage, Low Noise: 30µV_{RMS}, V_{IN}: –1.8V to –20V, ThinSOT Package
LT1965	1.1A, Low Noise, Low Dropout Linear Regulator	290mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN}: 1.8V to 20V, V_{OUT}: 1.2V to 19.5V, Stable with Ceramic Capacitors, TO-220, DDPak, MSOP and 3mm × 3mm DFN Packages
LT3008	20mA, 45V, 3µA I_Q Micropower LDO	300mV Dropout Voltage, Low I_Q = 3µA, V_{IN}: 2.0V to 45V, V_{OUT}: 0.6V to 39.5V, ThinSOT and 2mm × 2mm DFN-6 Packages
LT3009	20mA, 3µA I_Q Micropower LDO	280mV Dropout Voltage, Low I_Q = 3µA, V_{IN}: 1.6V to 20V, 2mm × 2mm DFN-6 and SC-70 Packages
LT3010	50mA, High Voltage, Micropower LDO	V_{IN}: 3V to 80V, V_{OUT}: 1.275V to 60V, V_{DO} = 0.3V, I_Q = 30µA, I_{SD} < 1µA, Low Noise: <100µV_{RMSP-P}, Stable with 1µF Output Capacitor, Exposed MS8 Package
LT3011	50mA, High Voltage, Micropower LDO with PWRGD	V_{IN}: 3V to 80V, V_{OUT}: 1.275V to 60V, V_{DO} = 0.3V, I_Q = 46µA, I_{SD} < 1µA, Low Noise: <100µV_{RMS}, PowerGood, Stable with 1µF Output Capacitor, 3mm × 3mm DFN-10 and Exposed MS12E Packages
LT3012	250mA, 4V to 80V, Low Dropout Micropower Linear Regulator	V_{IN}: 4V to 80V, V_{OUT}: 1.24V to 60V, V_{DO} = 0.4V, I_Q = 40µA, I_{SD} < 1µA, TSSOP-16E and 4mm × 3mm DFN-12 Packages
LT3013	250mA, 4V to 80V, Low Dropout Micropower Linear Regulator with PWRGD	V_{IN}: 4V to 80V, V_{OUT}: 1.24V to 60V, V_{DO} = 0.4V, I_Q = 65µA, I_{SD} < 1µA, PowerGood Feature, TSSOP-16E and 4mm × 3mm DFN-12 Packages
LT3014/LT3014HV	20mA, 3V to 80V, Low Dropout Micropower Linear Regulator	V_{IN}: 3V to 80V (100V for 2ms, LT3014HV Version), V_{OUT}: 1.22V to 60V, V_{DO} = 0.35V, I_Q = 7µA, I_{SD} < 1µA, ThinSOT and 3mm × 3mm DFN-8 Packages
LT3080/LT3080-1	1.1A, Parallelable, Low Noise, Low Dropout Linear Regulator	300mV Dropout Voltage (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set, Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors, TO-220, SOT-223, MSOP and 3mm × 3mm DFN Packages, LT3080-1 Version Has Integrated Internal Ballast Resistor
LT3050	100mA LDO with Diagnostics and Precision Current Limit	340mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN}: 1.8V to 45V, DFN and MSOP Packages
LT3060	100mA, Low Noise LDO with Soft-Start	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN}: 1.8V to 45V, DFN Package

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LT3055

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