LMV981-N Single / LMV982 Dual 1.8V, RRIO Operational Amplifiers with Shutdown

Check for Samples: LMV981-N, LMV982-N

FEATURES

- **(Typical 1.8V Supply Values; Unless Otherwise Noted)**
- **Ensured 1.8V, 2.7V and 5V Specifications**
- **Output Swing**
  - **w/600Ω load 80mV from Rail**
  - **w/2kΩ load 30mV from Rail**
- **V_{CM} 200mV Beyond Rails**
- **Supply Current (Per Channel) 100µA**
- **Gain Bandwidth Product 1.4MHz**
- **Maximum V_{OS} 4.0mV**
- **Gain w/600Ω Load 101dB**
- **Ultra Tiny Package DSBGA 1.0mm x 1.5mm**
- **Turn-On Time from Shutdown 19µs**
- **Temperature Range −40°C to 125°C**

APPLICATIONS

- **Industrial and Automotive**
- **Consumer Communication**
- **Consumer Computing**
- **PDAs**
- **Portable audio**
- **Portable/Battery-Powered Electronic Equipment**
- **Supply Current Monitoring**
- **Battery Monitoring**

DESCRIPTION

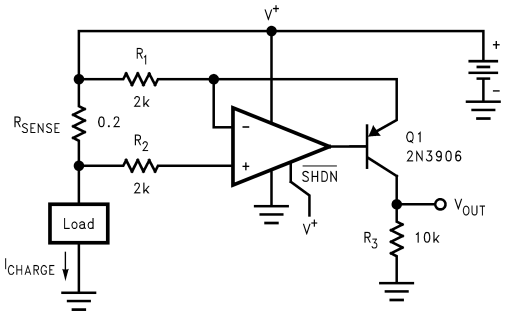
LMV981-N/LMV982 are low voltage, low power operational amplifiers. LMV981-N/LMV982 operate from +1.8V to +5.0V supply voltages and have rail-to-rail input and output. LMV981-N/LMV982 input common mode voltage extends 200mV beyond the supplies which enables user enhanced functionality beyond the supply voltage range. The output can swing rail-to-rail unloaded and within 105mV from the rail with 600Ω load at 1.8V supply. LMV981-N/LMV982 are optimized to work at 1.8V which make them ideal for portable two-cell battery powered systems and single cell Li-Ion systems.

LMV981-N/LMV982 offer a shutdown pin that can be used to disable the device and reduce the supply current. The device is in shutdown when the SHDN-pin = low. The output will be high impedance in shutdown.

LMV981-N/LMV982 exhibit excellent speed-power ratio, achieving 1.4MHz gain bandwidth product at 1.8V supply voltage with very low supply current. LMV981-N/LMV982 are capable of driving a 600Ω load and up to 1000pF capacitive load with minimal ringing. LMV981-N/LMV982 have a high DC gain of 101dB, making them suitable for low frequency applications.

LMV981-N is offered in space saving 6-Bump DSBGA, SC70-6 and SOT-23-6 packages. The 6-Bump DSBGA package has only a 1.006mm x 1.514mm x 0.945mm footprint. LMV982 is offered in space saving VSSOP-10 package. These small packages are ideal solutions for area constrained PC boards and portable electronics such as cellular phones and PDAs.

Typical Application



$$V_{OUT} = \frac{R_{SENSE} \bullet R_3}{R_1} \bullet I_{Charge} = 1\Omega \bullet I_{Charge}$$

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	
Machine Model	200V
Human Body Model	2000V
Supply Voltage (V^+–V^-)	5.5V
Differential Input Voltage	± Supply Voltage
Voltage at Input/Output Pins	V^++0.3V, V^--0.3V
Storage Temperature Range	−65°C to 150°C
Junction Temperature (4)	150°C
For soldering specifications:	
http://www.ti.com/lit/SNOA549f	

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}–T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Operating Ratings (1)

Supply Voltage Range	1.8V to 5.0V
Temperature Range	−40°C to 125°C
Thermal Resistance (θ_{JA})	
6-Bump DSBGA	286°C/W
SC70-6	414°C/W
SOT-23-6	265°C/W
VSSOP-10	235°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

1.8V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 1.8V, V^- = 0V, $V_{CM} = V^+/2$, $V_O = V^+/2$, R_L > 1 MΩ and $\overline{SHDN}$ tied to V^+. **Boldface** limits apply at the temperature extremes. See (1).

Parameter		Test Conditions	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage	LMV981-N (Single)		1	4 **6**	mV
		LMV982 (Dual)		1	5.5 **7.5**	
TCV_{OS}	Input Offset Voltage Average Drift			5.5		µV/°C
I_B	Input Bias Current			15	35 **50**	nA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Application Note section for information on temperature derating of this device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

1.8V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 1.8V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2, R_L > 1 MΩ and $\overline{SHDN}$ tied to V^+. **Boldface** limits apply at the temperature extremes. See (1).

Parameter		Test Conditions		Min (2)	Typ (3)	Max (2)	Units
I_{OS}	Input Offset Current				13	25 **40**	nA
I_S	Supply Current (per channel)				103	185 **205**	µA
		In Shutdown	LMV981-N (Single)		0.156	1 **2**	
			LMV982 (Dual)		0.178	3.5 **5**	
CMRR	Common Mode Rejection Ratio	LMV981-N, 0 ≤ V_{CM} ≤ 0.6V 1.4V ≤ V_{CM} ≤ 1.8V (4)		60 **55**	78		dB
		LMV982, 0 ≤ V_{CM} ≤ 0.6V 1.4V ≤ V_{CM} ≤ 1.8V (4)		55 **50**	76		
		−0.2V ≤ V_{CM} ≤ 0V 1.8V ≤ V_{CM} ≤ 2.0V		50	72		
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V		75 **70**	100		dB
CMVR	Input Common-Mode Voltage Range	For CMRR Range ≥ 50dB	T_A = 25°C	V^- −0.2	−0.2 to 2.1	V^+ +0.2	V
			T_A = −40°C to 85°C	V^-		V^+	
			T_A = 125°C	V^- +0.2		V^+ −0.2	
A_V	Large Signal Voltage Gain LMV981-N (Single)	R_L = 600Ω to 0.9V, V_O = 0.2V to 1.6V, V_{CM} = 0.5V		77 **73**	101		dB
		R_L = 2kΩ to 0.9V, V_O = 0.2V to 1.6V, V_{CM} = 0.5V		80 **75**	105		
	Large Signal Voltage Gain LMV982 (Dual)	R_L = 600Ω to 0.9V, V_O = 0.2V to 1.6V, V_{CM} = 0.5V		75 **72**	90		dB
		R_L = 2kΩ to 0.9V, V_O = 0.2V to 1.6V, V_{CM} = 0.5V		78 **75**	100		
V_O	Output Swing	R_L = 600Ω to 0.9V V_{IN} = ± 100mV		1.65 **1.63**	1.72		V
					0.077	0.105 **0.120**	
		R_L = 2kΩ to 0.9V V_{IN} = ± 100mV		1.75 **1.74**	1.77		
					0.024	0.035 **0.04**	
I_O	Output Short Circuit Current (5)	Sourcing, V_O = 0V V_{IN} = 100mV		4 **3.3**	8		mA
		Sinking, V_O = 1.8V V_{IN} = −100mV		7 **5**	9		
Ton	Turn-on Time from Shutdown				19		µs
V_{SHDN}	Turn-on Voltage to enable part				1.0		V
	Turn-off Voltage				0.55		

(4) For ensured temperature ranges, see Input Common-Mode Voltage Range specifications.
(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45mA over long term may adversely affect reliability.

1.8V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 1.8V, V^- = 0V, $V_{CM} = V^+/2$, $V_O = V^+/2$, R_L > 1 MΩ and $\overline{SHDN}$ tied to V^+. **Boldface** limits apply at the temperature extremes. See (1).

Parameter		Test Conditions	Min (2)	Typ (3)	Max (2)	Units
SR	Slew Rate	See (4)		0.35		V/µs
GBW	Gain-Bandwidth Product			1.4		MHz
Φ_m	Phase Margin			67		deg
G_m	Gain Margin			7		dB
e_n	Input-Referred Voltage Noise	f = 10 kHz, V_{CM} = 0.5V		60		nV/√Hz
i_n	Input-Referred Current Noise	f = 10 kHz		0.08		pA/√Hz
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_{IN} = 1 V_{PP}		0.023		%
	Amp-to-Amp Isolation	See (5)		123		dB

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Application Note section for information on temperature derating of this device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.
(5) Input referred, R_L = 100kΩ connected to $V^+/2$. Each amp excited in turn with 1kHz to produce $V_O = 3V_{PP}$. (For Supply Voltages <3V, $V_O = V^+$).

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 2.7V, V^- = 0V, $V_{CM} = V^+/2$, $V_O = V^+/2$, R_L > 1 MΩ and $\overline{SHDN}$ tied to V^+. **Boldface** limits apply at the temperature extremes. See (1).

Parameter		Test Conditions		Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage	LMV981-N (Single)			1	4 **6**	mV
		LMV982 (Dual)			1	6 **7.5**	mV
TCV_{OS}	Input Offset Voltage Average Drift				5.5		µV/°C
I_B	Input Bias Current				15	35 **50**	nA
I_{OS}	Input Offset Current				8	25 **40**	nA
I_S	Supply Current (per channel)				105	190 **210**	µA
		In Shutdown	LMV981-N (Single)		0.061	1 **2**	
			LMV982 (Dual)		0.101	3.5 **5**	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Application Note section for information on temperature derating of this device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

2.7V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2, R_L > 1 MΩ and $\overline{SHDN}$ tied to V^+. **Boldface** limits apply at the temperature extremes. See (1).

Parameter		Test Conditions		Min (2)	Typ (3)	Max (2)	Units
CMRR	Common Mode Rejection Ratio	LMV981-N, 0 ≤ V_{CM} ≤ 1.5V 2.3V ≤ V_{CM} ≤ 2.7V (4)		60 **55**	81		dB
		LMV982, 0 ≤ V_{CM} ≤ 1.5V 2.3V ≤ V_{CM} ≤ 2.7V (4)		55 **50**	80		
		−0.2V ≤ V_{CM} ≤ 0V 2.7V ≤ V_{CM} ≤ 2.9V		50	74		
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V V_{CM} = 0.5V		75 **70**	100		dB
CMVR	Input Common-Mode Voltage Range	For CMRR Range ≥ 50dB	T_A = 25°C	V^- −0.2	−0.2 to 3.0	V^++0.2	V
			T_A = −40°C to 85°C	V^-		V^+	
			T_A = 125°C	V^- +0.2		V^+−0.2	
A_V	Large Signal Voltage Gain LMV981-N(Single)	R_L = 600Ω to 1.35V, V_O = 0.2V to 2.5V		87 **86**	104		dB
		R_L = 2kΩ to 1.35V, V_O = 0.2V to 2.5V		92 **91**	110		
	Large Signal Voltage Gain LMV982 (Dual)	R_L = 600Ω to 1.35V, V_O = 0.2V to 2.5V		78 **75**	90		
		R_L = 2kΩ to 1.35V, V_O = 0.2V to 2.5V		81 **78**	100		
V_O	Output Swing	R_L = 600Ω to 1.35V V_{IN} = ±100mV		2.55 **2.53**	2.62		V
					0.083	0.110 **0.130**	
		R_L = 2kΩ to 1.35V V_{IN} = ±100mV		2.65 **2.64**	2.675		
					0.025	0.04 **0.045**	
I_O	Output Short Circuit Current (5)	Sourcing, V_O = 0V V_{IN} = 100mV		20 **15**	30		mA
		Sinking, V_O = 0V V_{IN} = −100mV		18 **12**	25		
Ton	Turn-on Time from Shutdown				12.5		µs
V_{SHDN}	Turn-on Voltage to enable part				1.9		V
	Turn-off Voltage				0.8		

(4) For ensured temperature ranges, see Input Common-Mode Voltage Range specifications.
(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45mA over long term may adversely affect reliability.

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V, R_L > 1 MΩ and $\overline{SHDN}$ tied to V^+. **Boldface** limits apply at the temperature extremes. See (1).

Parameter		Test Conditions	Min (2)	Typ (3)	Max (2)	Units
SR	Slew Rate	(4)		0.4		V/µs
GBW	Gain-Bandwidth Product			1.4		MHz
Φ_m	Phase Margin			70		deg
G_m	Gain Margin			7.5		dB
e_n	Input-Referred Voltage Noise	f = 10 kHz, V_{CM} = 0.5V		57		nV/√Hz
i_n	Input-Referred Current Noise	f = 10 kHz		0.08		pA/√Hz
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_{IN} = $1V_{PP}$		0.022		%
	Amp-to-Amp Isolation	(5)		123		dB

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Application Note section for information on temperature derating of this device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.
(5) Input referred, R_L = 100kΩ connected to $V^+/2$. Each amp excited in turn with 1kHz to produce $V_O = 3V_{PP}$. (For Supply Voltages <3V, $V_O = V^+$).

5V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 5V, V^- = 0V, $V_{CM} = V^+/2$, $V_O = V^+/2$, R_L > 1 MΩ and $\overline{SHDN}$ tied to V^+. **Boldface** limits apply at the temperature extremes. See (1).

Parameter		Test Conditions		Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage	LMV981-N (Single)			1	4 **6**	mV
		LMV982 (Dual)			1	5.5 **7.5**	
TCV_{OS}	Input Offset Voltage Average Drift				5.5		µV/°C
I_B	Input Bias Current				14	35 **50**	nA
I_{OS}	Input Offset Current				9	25 **40**	nA
I_S	Supply Current (per Channel)				116	210 **230**	µA
		In Shutdown	LMV981-N (Single)		0.201	1 **2**	µA
			LMV982 (Dual)		0.302	3.5 **5**	
CMRR	Common Mode Rejection Ratio	0 ≤ V_{CM} ≤ 3.8V 4.6V ≤ V_{CM} ≤ 5.0V (4)		60 **55**	86		dB
		−0.2V ≤ V_{CM} ≤ 0V 5.0V ≤ V_{CM} ≤ 5.2V		50	78		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Application Note section for information on temperature derating of this device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) For ensured temperature ranges, see Input Common-Mode Voltage Range specifications.

5V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2, R_L > 1 MΩ and $\overline{SHDN}$ tied to V^+. **Boldface** limits apply at the temperature extremes. See (1).

Parameter		Test Conditions		Min (2)	Typ (3)	Max (2)	Units
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V V_{CM} = 0.5V		75 **70**	100		dB
CMVR	Input Common-Mode Voltage Range	For CMRR Range ≥ 50dB	T_A = 25°C	V^- −0.2	−0.2 to 5.3	V^+ +0.2	V
			T_A = −40°C to 85°C	V^-		V^+	
			T_A = 125°C	V^- +0.3		V^+ −0.3	
A_V	Large Signal Voltage Gain (LMV981-N Single)	R_L = 600Ω to 2.5V, V_O = 0.2V to 4.8V		88 **87**	102		dB
		R_L = 2kΩ to 2.5V, V_O = 0.2V to 4.8V		94 **93**	113		
	Large Signal Voltage Gain LMV982 (Dual)	R_L = 600Ω to 2.5V, V_O = 0.2V to 4.8V		81 **78**	90		dB
		R_L = 2kΩ to 2.5V, V_O = 0.2V to 4.8V		85 **82**	100		
V_O	Output Swing	R_L = 600Ω to 2.5V V_{IN} = ±100mV (4)		4.855 **4.835**	4.890		V
					0.120	0.160 **0.180**	
		R_L = 2kΩ to 2.5V V_{IN} = ±100mV		4.945 **4.935**	4.967		
					0.037	0.065 **0.075**	
I_O	Output Short Circuit Current (5)	LMV981-N, Sourcing, V_O = 0V V_{IN} = 100mV		80 **68**	100		mA
		Sinking, V_O = 5V V_{IN} = −100mV		58 **45**	65		
Ton	Turn-on Time from Shutdown				8.4		µs
V_{SHDN}	Turn-on Voltage to enable part				4.2		V
	Turn-off Voltage				0.8		

(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45mA over long term may adversely affect reliability.

5V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_O = 2.5V, R_L > 1 MΩ and $\overline{SHDN}$ tied to V^+.**Boldface** limits apply at the temperature extremes. See (1).

Parameter		Test Conditions	Min (2)	Typ (3)	Max (2)	Units
SR	Slew Rate	(4)		0.42		V/µs
GBW	Gain-Bandwidth Product			1.5		MHz
Φ_m	Phase Margin			71		deg
G_m	Gain Margin			8		dB
e_n	Input-Referred Voltage Noise	f = 10 kHz, V_{CM} = 1V		50		nV/√Hz
i_n	Input-Referred Current Noise	f = 10 kHz		0.08		pA/√Hz

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_J > T_A. See Application Note section for information on temperature derating of this device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.

5V AC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 5V, V^- = 0V, $V_{CM} = V^+/2$, V_O = 2.5V, R_L > 1 MΩ and $\overline{SHDN}$ tied to V^+. **Boldface** limits apply at the temperature extremes. See (1).

Parameter		Test Conditions	Min (2)	Typ (3)	Max (2)	Units
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_O = 1 V_{PP}		0.022		%
	Amp-to-Amp Isolation	(5)		123		dB

(5) Input referred, R_L = 100kΩ connected to $V^+/2$. Each amp excited in turn with 1kHz to produce $V_O = 3V_{PP}$. (For Supply Voltages <3V, $V_O = V^+$).

Connection Diagrams

Top View

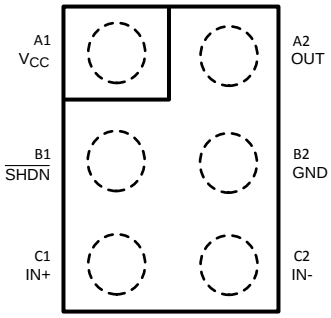


Figure 1. 6-Bump DSBGA Package
See Package Number YZR0006BBA

Top View

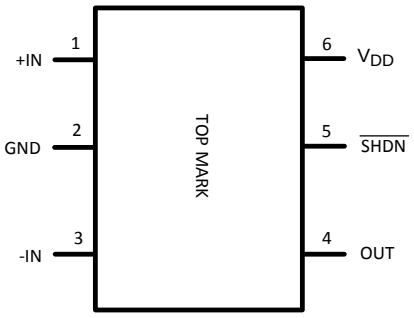


Figure 2. 6-Pin SC70 and SOT-23
See Package Numbers DCK0006A and DBV0006A

Top View

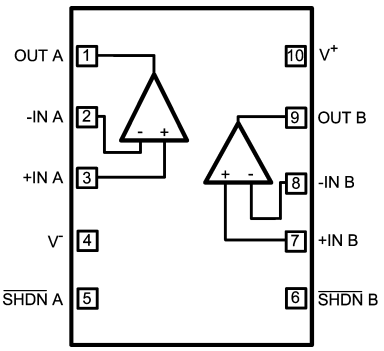


Figure 3. 10-Pin VSSOP Package
See Package Number DGS0010A

Typical Performance Characteristics

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Supply Current vs. Supply Voltage (LMV981-N)

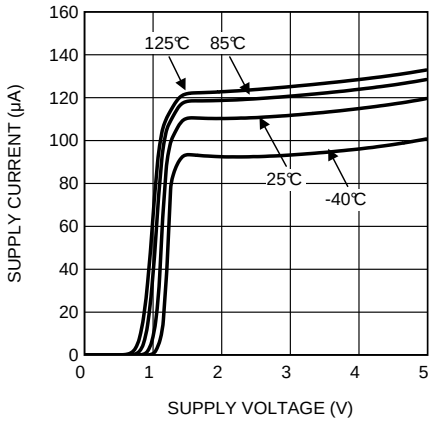


Figure 4.

Sourcing Current vs. Output Voltage

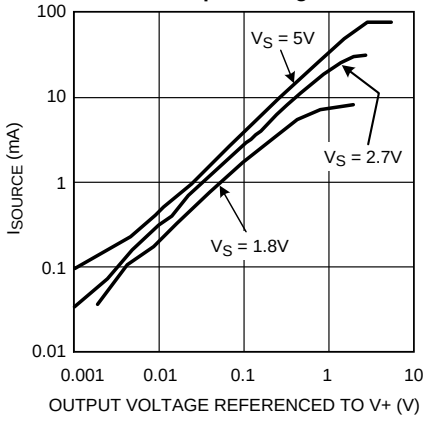


Figure 5.

Sinking Current vs. Output Voltage

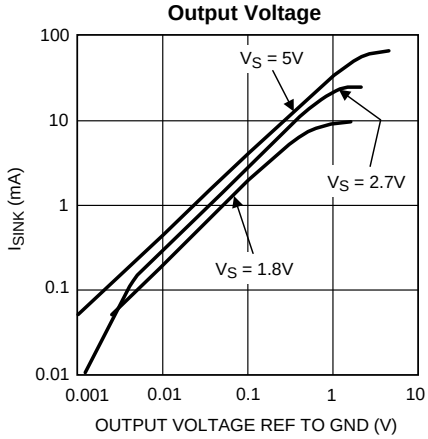


Figure 6.

Output Voltage Swing vs. Supply Voltage

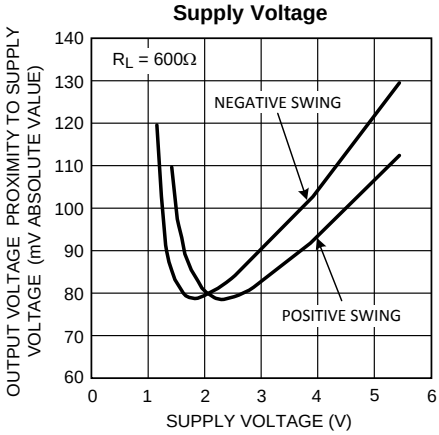


Figure 7.

Output Voltage Swing vs. Supply Voltage

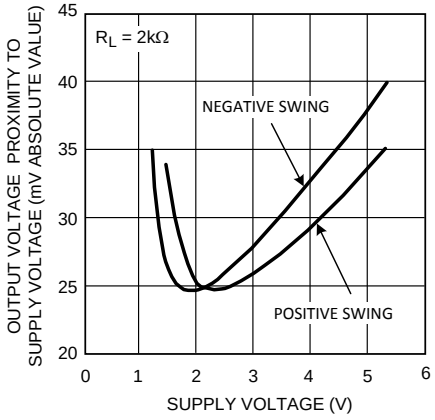


Figure 8.

Gain and Phase vs. Frequency

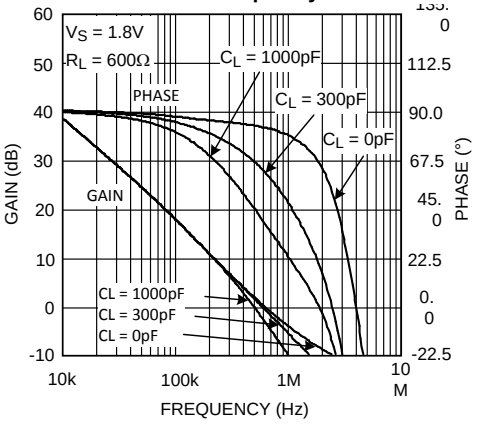


Figure 9.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Gain and Phase vs. Frequency

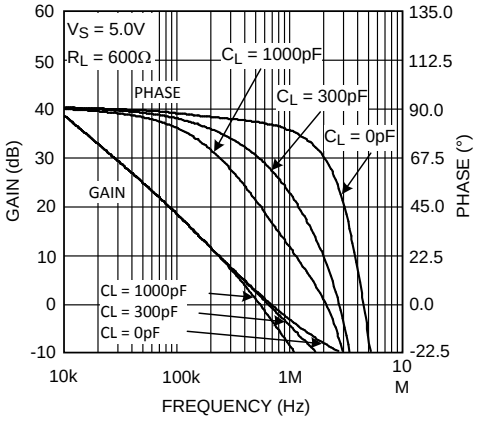


Figure 10.

Gain and Phase vs. Frequency

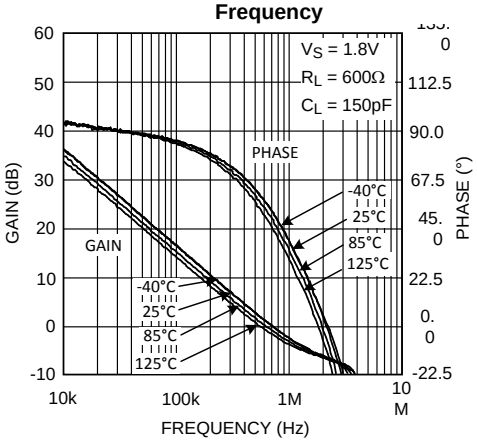


Figure 11.

Gain and Phase vs. Frequency

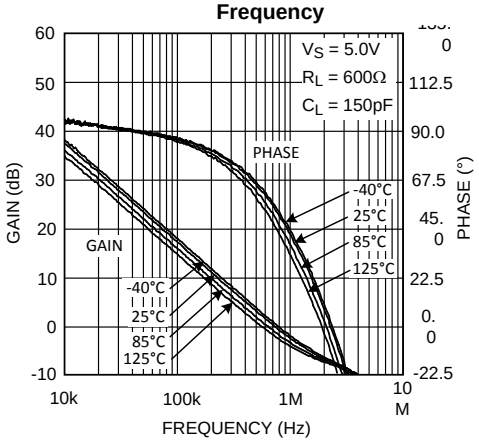


Figure 12.

CMRR vs. Frequency

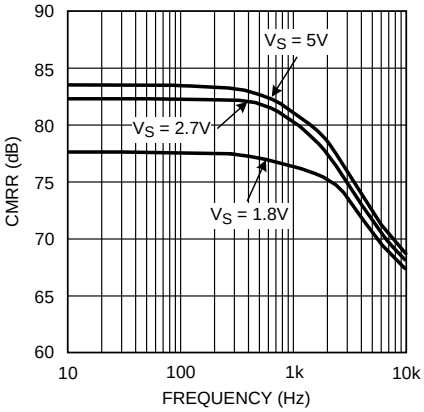


Figure 13.

PSRR vs. Frequency

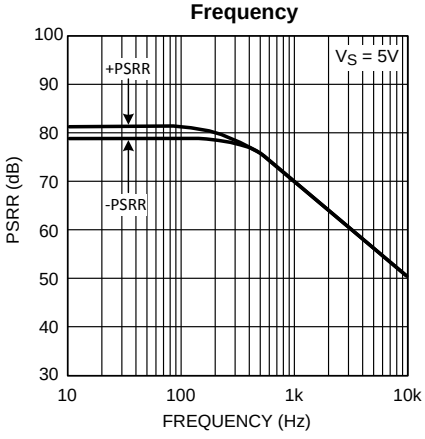


Figure 14.

Input Voltage Noise vs. Frequency

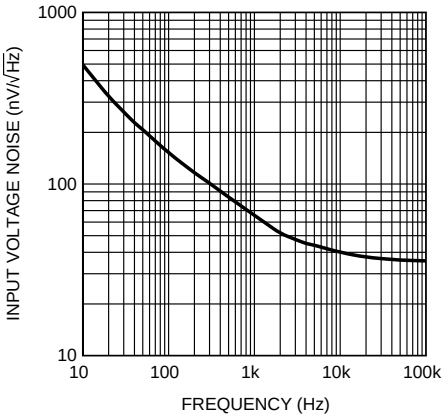


Figure 15.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Input Current Noise vs. Frequency

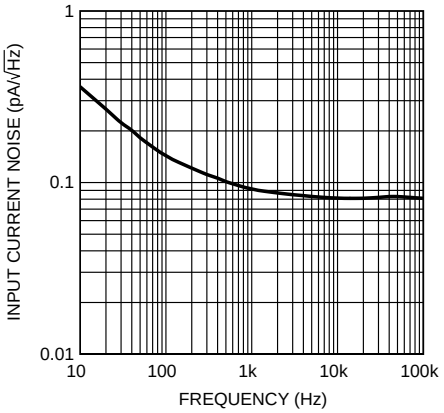


Figure 16.

THD vs. Frequency

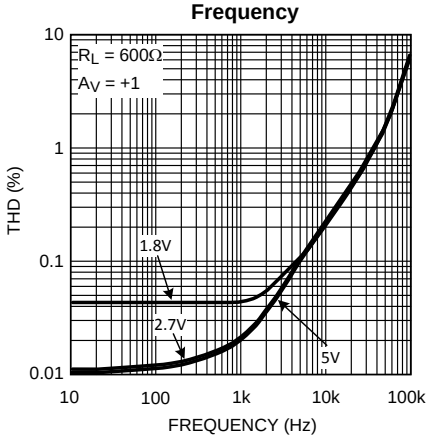


Figure 17.

THD vs. Frequency

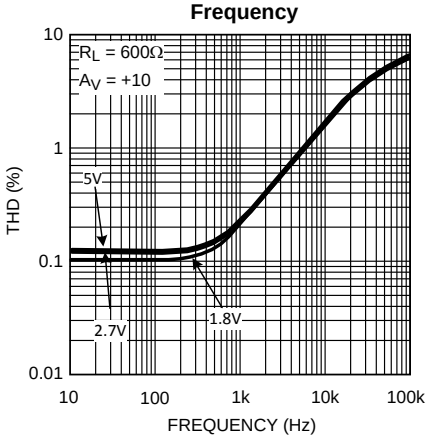


Figure 18.

Slew Rate vs. Supply Voltage

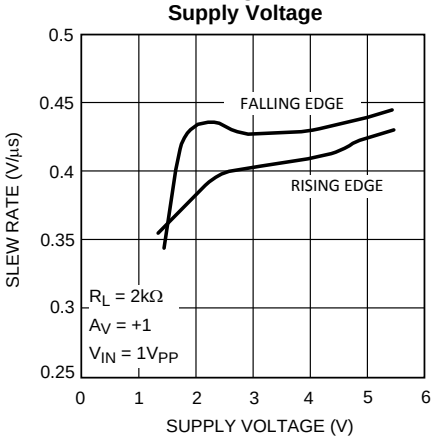


Figure 19.

Small Signal Non-Inverting Response

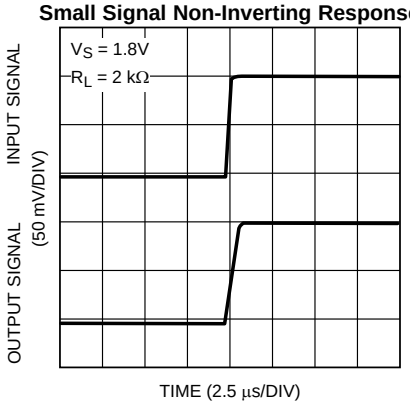


Figure 20.

Small Signal Non-Inverting Response

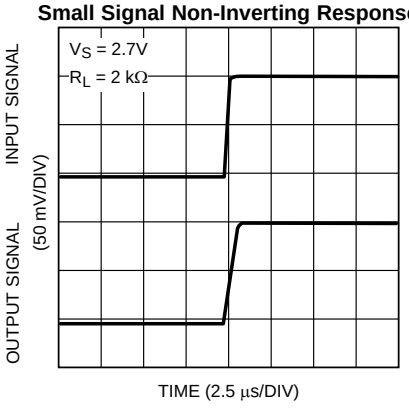


Figure 21.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Small Signal Non-Inverting Response

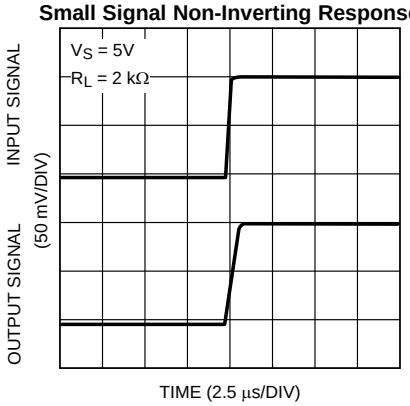


Figure 22.

Large Signal Non-Inverting Response

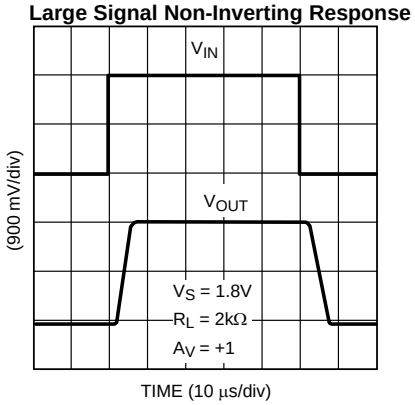


Figure 23.

Large Signal Non-Inverting Response

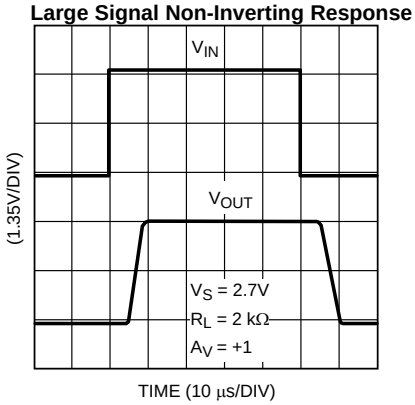


Figure 24.

Large Signal Non-Inverting Response

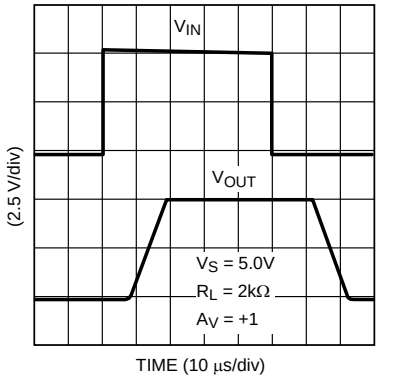


Figure 25.

Short Circuit Current vs. Temperature (Sinking)

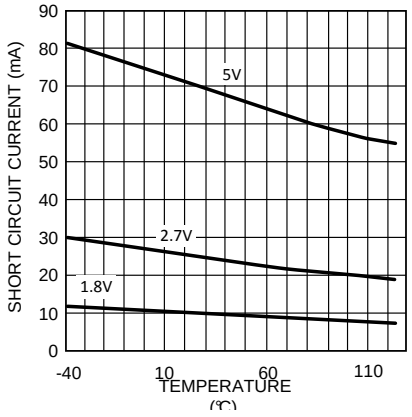


Figure 26.

Short Circuit Current vs. Temperature (Sourcing)

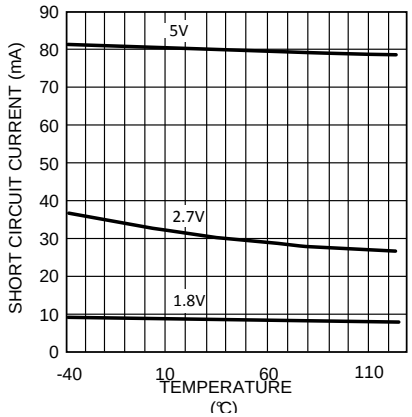


Figure 27.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Offset Voltage vs. Common Mode Range

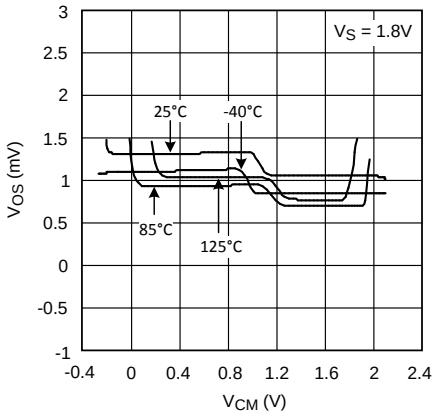


Figure 28.

Offset Voltage vs. Common Mode Range

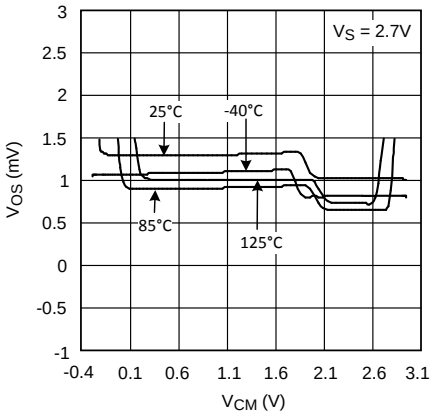


Figure 29.

Offset Voltage vs. Common Mode Range

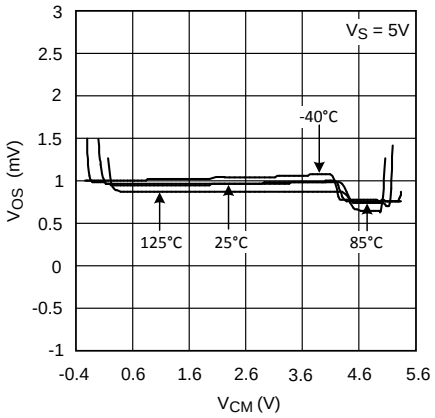


Figure 30.

APPLICATION NOTE

Input and Output Stage

The rail-to-rail input stage of this family provides more flexibility for the designer. The LMV981-N/LMV982 use a complimentary PNP and NPN input stage in which the PNP stage senses common mode voltage near V^- and the NPN stage senses common mode voltage near V^+. The transition from the PNP stage to NPN stage occurs 1V below V^+. Since both input stages have their own offset voltage, the offset of the amplifier becomes a function of the input common mode voltage and has a crossover point at 1V below V^+.

This V_{OS} crossover point can create problems for both DC and AC coupled signals if proper care is not taken. Large input signals that include the V_{OS} crossover point will cause distortion in the output signal. One way to avoid such distortion is to keep the signal away from the crossover. For example, in a unity gain buffer configuration and with V_S = 5V, a 5V peak-to-peak signal will contain input-crossover distortion while a 3V peak-to-peak signal centered at 1.5V will not contain input-crossover distortion as it avoids the crossover point. Another way to avoid large signal distortion is to use a gain of −1 circuit which avoids any voltage excursions at the input terminals of the amplifier. In that circuit, the common mode DC voltage can be set at a level away from the V_{OS} cross-over point. For small signals, this transition in V_{OS} shows up as a V_{CM} dependent spurious signal in series with the input signal and can effectively degrade small signal parameters such as gain and common mode rejection ratio. To resolve this problem, the small signal should be placed such that it avoids the V_{OS} crossover point. In addition to the rail-to-rail performance, the output stage can provide enough output current to drive 600Ω loads. Because of the high current capability, care should be taken not to exceed the 150°C maximum junction temperature specification.

Shutdown Mode

The LMV981-N/LMV982 have a shutdown pin. To conserve battery life in portable applications, the LMV981-N/LMV982 can be disabled when the shutdown pin voltage is pulled low.

The shutdown pin can't be left unconnected. In case shut-down operation is not needed, the shutdown pin should be connected to V^+ when the LMV981-N/LMV982 are used. Leaving the shutdown pin floating will result in an undefined operation mode, either shutdown or active, or even oscillating between the two modes.

Input Bias Current Consideration

The LMV981-N/LMV982 family has a complementary bipolar input stage. The typical input bias current (I_B) is 15nA. The input bias current can develop a significant offset voltage. This offset is primarily due to I_B flowing through the negative feedback resistor, R_F. For example, if I_B is 50nA and R_F is 100kΩ, then an offset voltage of 5mV will develop ($V_{OS} = I_B \times R_F$). Using a compensation resistor (R_C), as shown in Figure 31, cancels this effect. But the input offset current (I_{OS}) will still contribute to an offset voltage in the same manner.

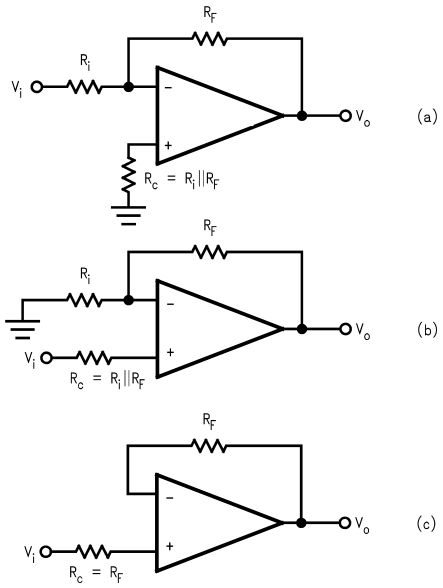


Figure 31. Canceling the Offset Voltage due to Input Bias Current

Typical Applications

High Side Current Sensing

The high side current sensing circuit (Figure 32) is commonly used in a battery charger to monitor charging current to prevent over charging. A sense resistor R_{SENSE} is connected to the battery directly. This system requires an op amp with rail-to-rail input. The LMV981-N/LMV982 are ideal for this application because the common mode input range goes up to the rail.

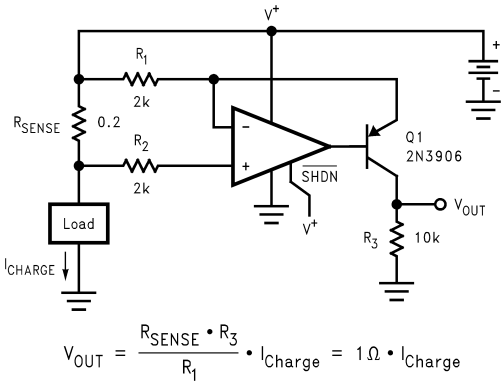


Figure 32. High Side Current Sensing

Half-Wave Rectifier with Rail-to-Ground Output Swing

Since the LMV981-N/LMV982 input common mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction is an easy task. All that is needed are two external resistors; there is no need for diodes or matched resistors. The half wave rectifier can have either positive or negative going outputs, depending on the way the circuit is arranged.

In Figure 33 the circuit is referenced to ground, while in Figure 34 the circuit is biased to the positive supply. These configurations implement the half wave rectifier since the LMV981-N/LMV982 can not respond to one-half of the incoming waveform. It can not respond to one-half of the incoming because the amplifier can not swing the output beyond either rail therefore the output disengages during this half cycle. During the other half cycle, however, the amplifier achieves a half wave that can have a peak equal to the total supply voltage. R_I should be large enough not to load the LMV981-N/LMV982.

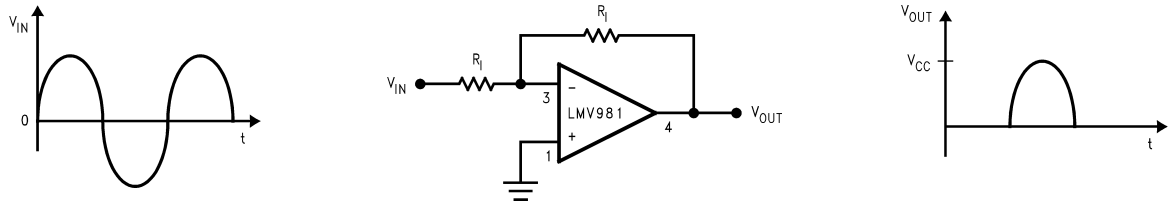


Figure 33. Half-Wave Rectifier with Rail-to-Ground Output Swing Referenced to Ground

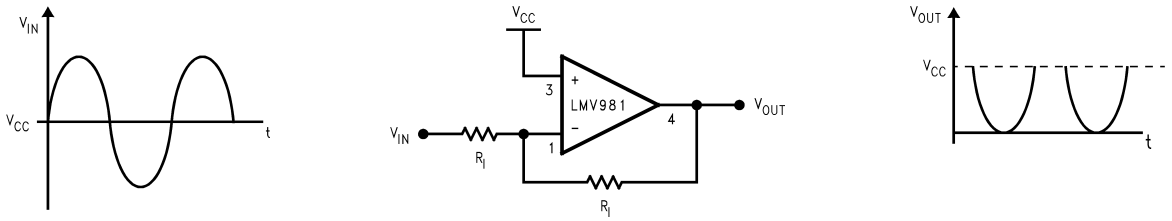


Figure 34. Half-Wave Rectifier with Negative-Going Output Swing Referenced to V_{CC}

Instrumentation Amplifier with Rail-to-Rail Input and Output

Some manufactures make a non-“rail-to-rail”-op amp rail-to-rail by using a resistive divider on the inputs. The resistors divide the input voltage to get a rail-to-rail input range. The problem with this method is that it also divides the signal, so in order to get the obtained gain, the amplifier must have a higher closed loop gain. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMRR as well. The LMV981-N/LMV982 is rail-to-rail and therefore doesn't have these disadvantages.

Using three of the LMV981-N/LMV982 amplifiers, an instrumentation amplifier with rail-to-rail inputs and outputs can be made as shown in Figure 35.

In this example, amplifiers on the left side act as buffers to the differential stage. These buffers assure that the input impedance is very high and require no precision matched resistors in the input stage. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMRR set by the matching R_1-R_2 with R_3-R_4. The gain is set by the ratio of R_2/R_1 and R_3 should equal R_1 and R_4 equal R_2. With both rail-to-rail input and output ranges, the input and output are only limited by the supply voltages. Remember that even with rail-to-rail outputs, the output can not swing past the supplies so the combined common mode voltages plus the signal should not be greater that the supplies or limiting will occur. For additional applications, see Texas Instruments application notes AN–29, AN–31, AN–71, and AN–127.

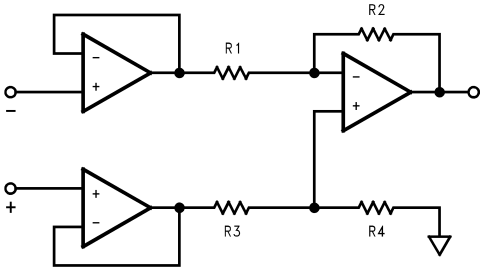
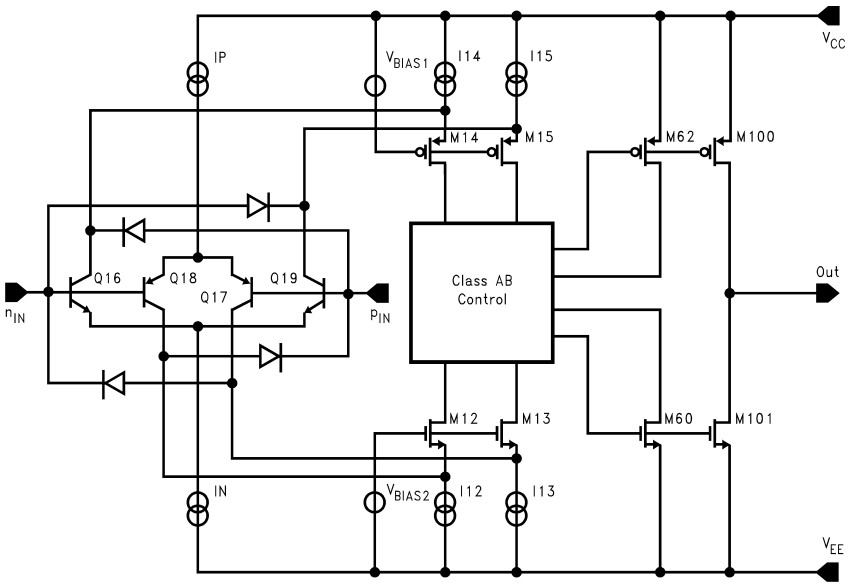


Figure 35. Rail-to-rail instrumentation amplifier

Simplified Schematic



REVISION HISTORY

Changes from Revision K (March 2013) to Revision L	Page
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV981MF	NRND	SOT-23	DBV	6	1000	TBD	Call TI	Call TI	-40 to 125	A78A	
LMV981MF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A78A	Samples
LMV981MFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A78A	Samples
LMV981MG	NRND	SC70	DCK	6	1000	TBD	Call TI	Call TI	-40 to 125	A77	
LMV981MG/NOPB	ACTIVE	SC70	DCK	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A77	Samples
LMV981MGX/NOPB	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A77	Samples
LMV981TL/NOPB	ACTIVE	DSBGA	YZR	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	A H	Samples
LMV981TLX/NOPB	ACTIVE	DSBGA	YZR	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	A H	Samples
LMV982MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A87A	Samples
LMV982MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A87A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

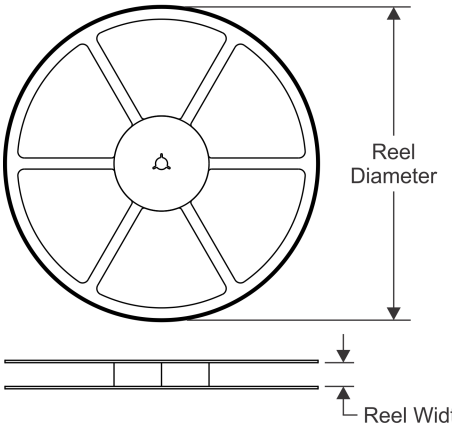
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

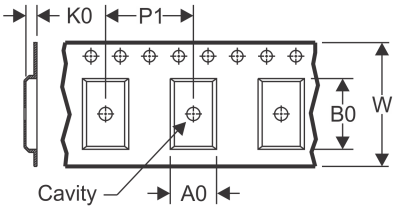
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

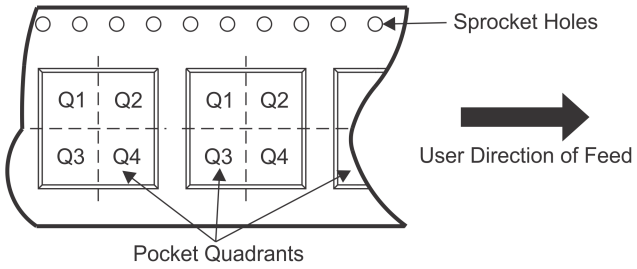


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

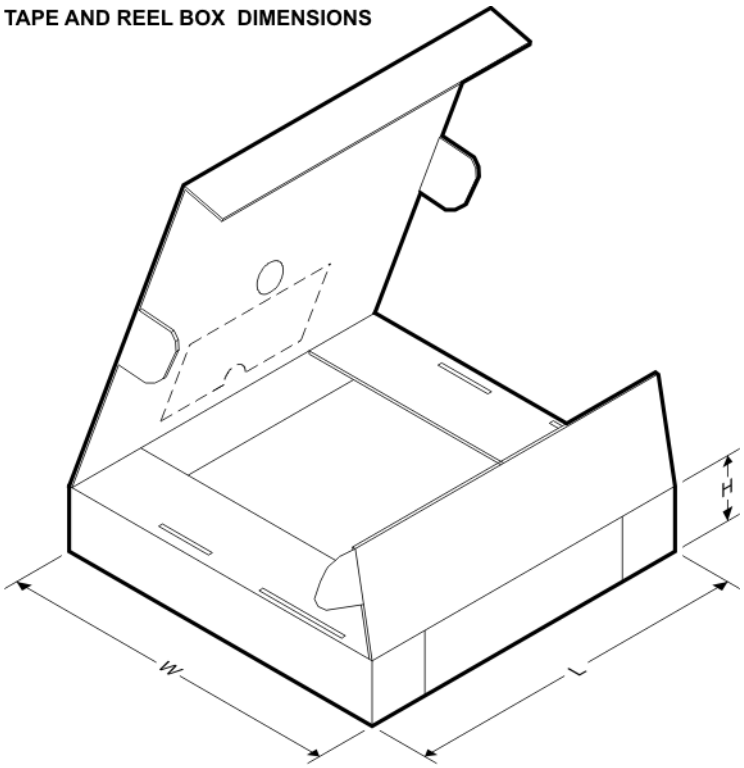
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV981MF	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV981MF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV981MFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV981MG	SC70	DCK	6	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV981MG/NOPB	SC70	DCK	6	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV981MGX/NOPB	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV981TL/NOPB	DSBGA	YZR	6	250	178.0	8.4	1.12	1.63	0.76	4.0	8.0	Q1
LMV981TLX/NOPB	DSBGA	YZR	6	3000	178.0	8.4	1.12	1.63	0.76	4.0	8.0	Q1
LMV982MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV982MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

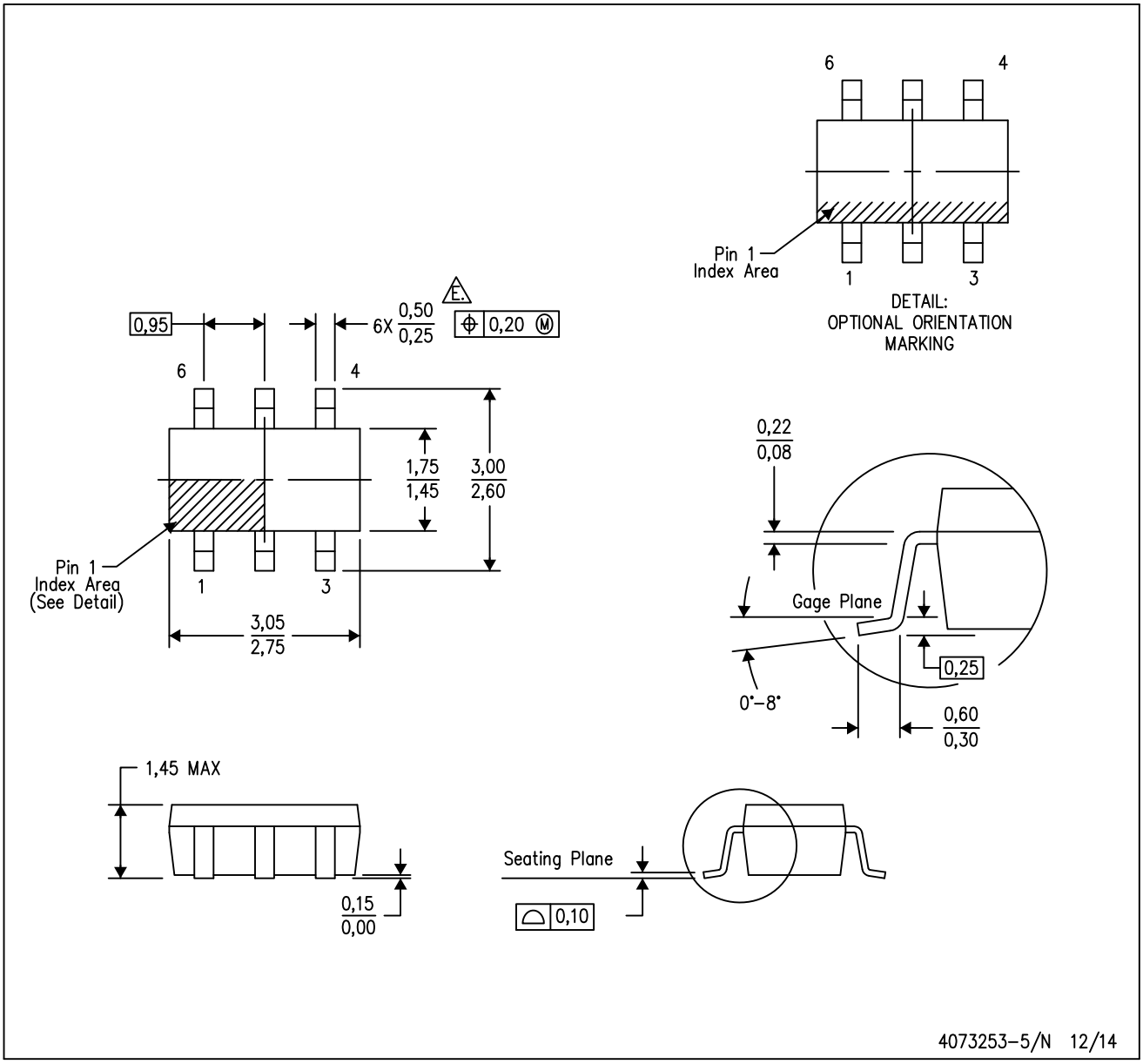
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

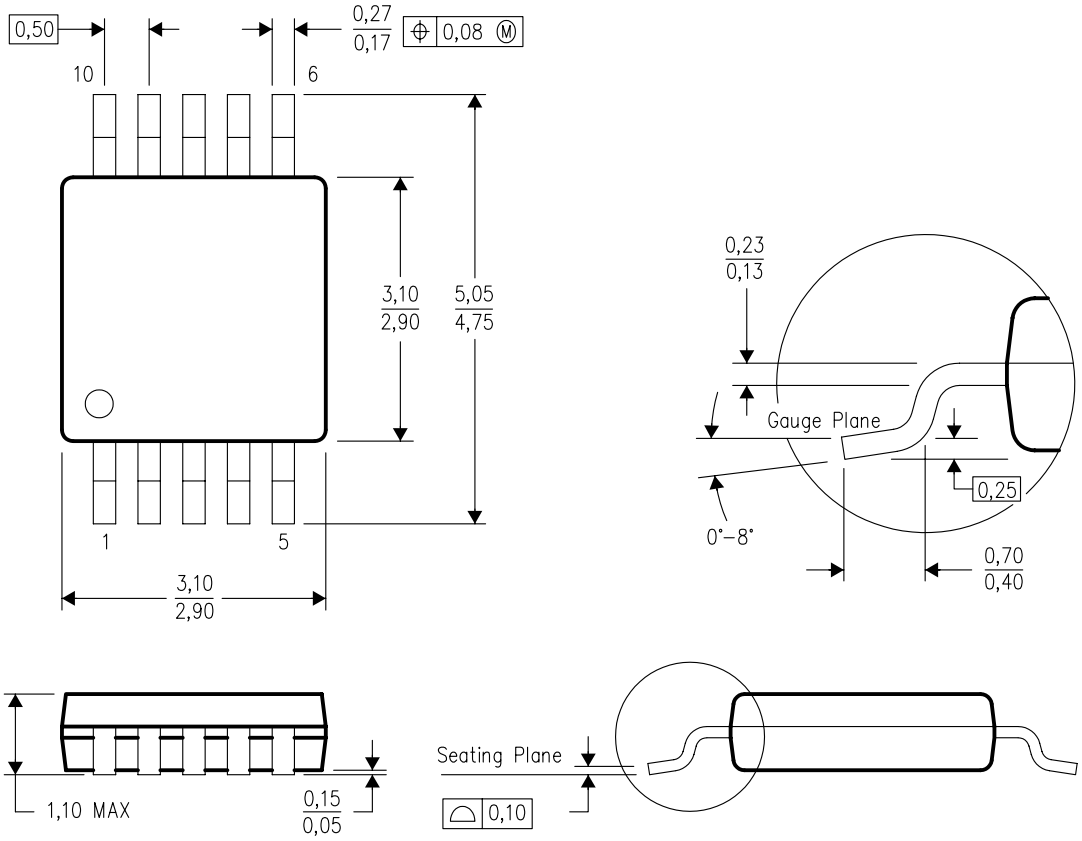
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV981MF	SOT-23	DBV	6	1000	210.0	185.0	35.0
LMV981MF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LMV981MFX/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0
LMV981MG	SC70	DCK	6	1000	210.0	185.0	35.0
LMV981MG/NOPB	SC70	DCK	6	1000	210.0	185.0	35.0
LMV981MGX/NOPB	SC70	DCK	6	3000	210.0	185.0	35.0
LMV981TL/NOPB	DSBGA	YZR	6	250	210.0	185.0	35.0
LMV981TLX/NOPB	DSBGA	YZR	6	3000	210.0	185.0	35.0
LMV982MM/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LMV982MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

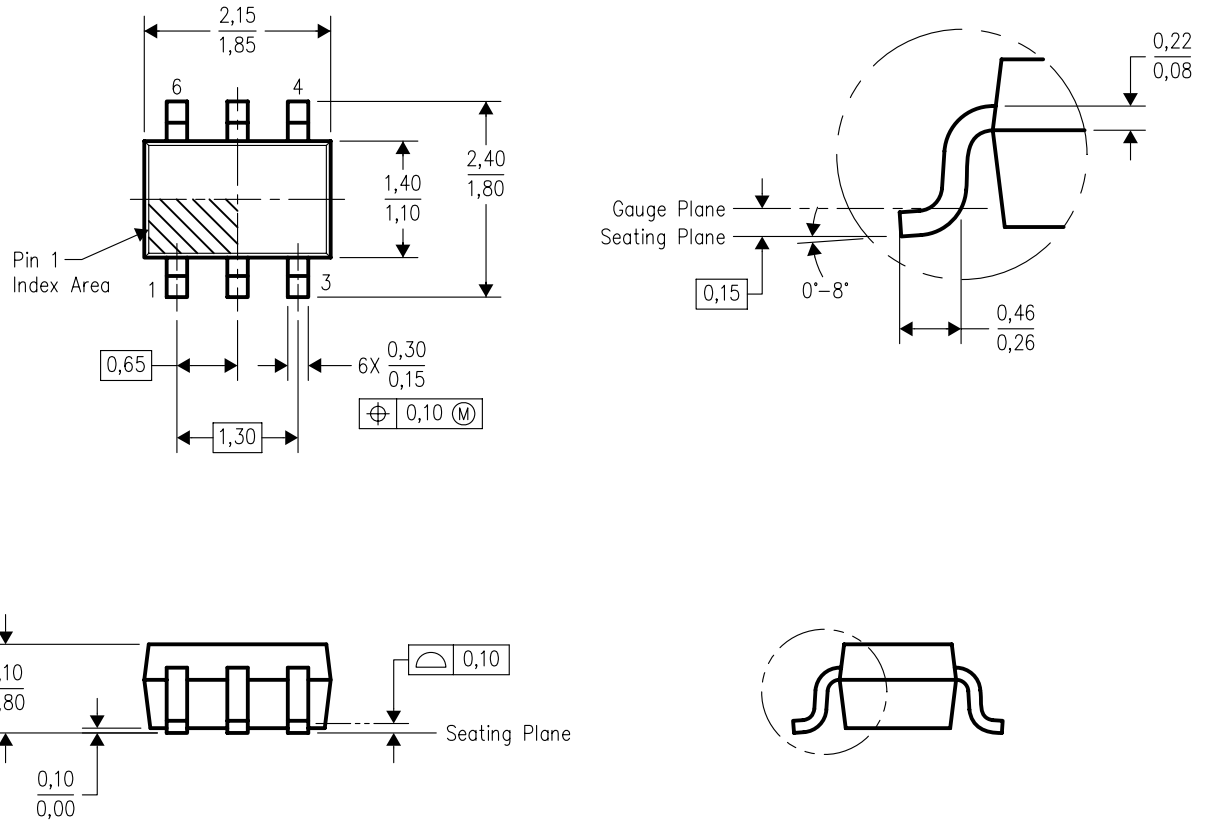
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

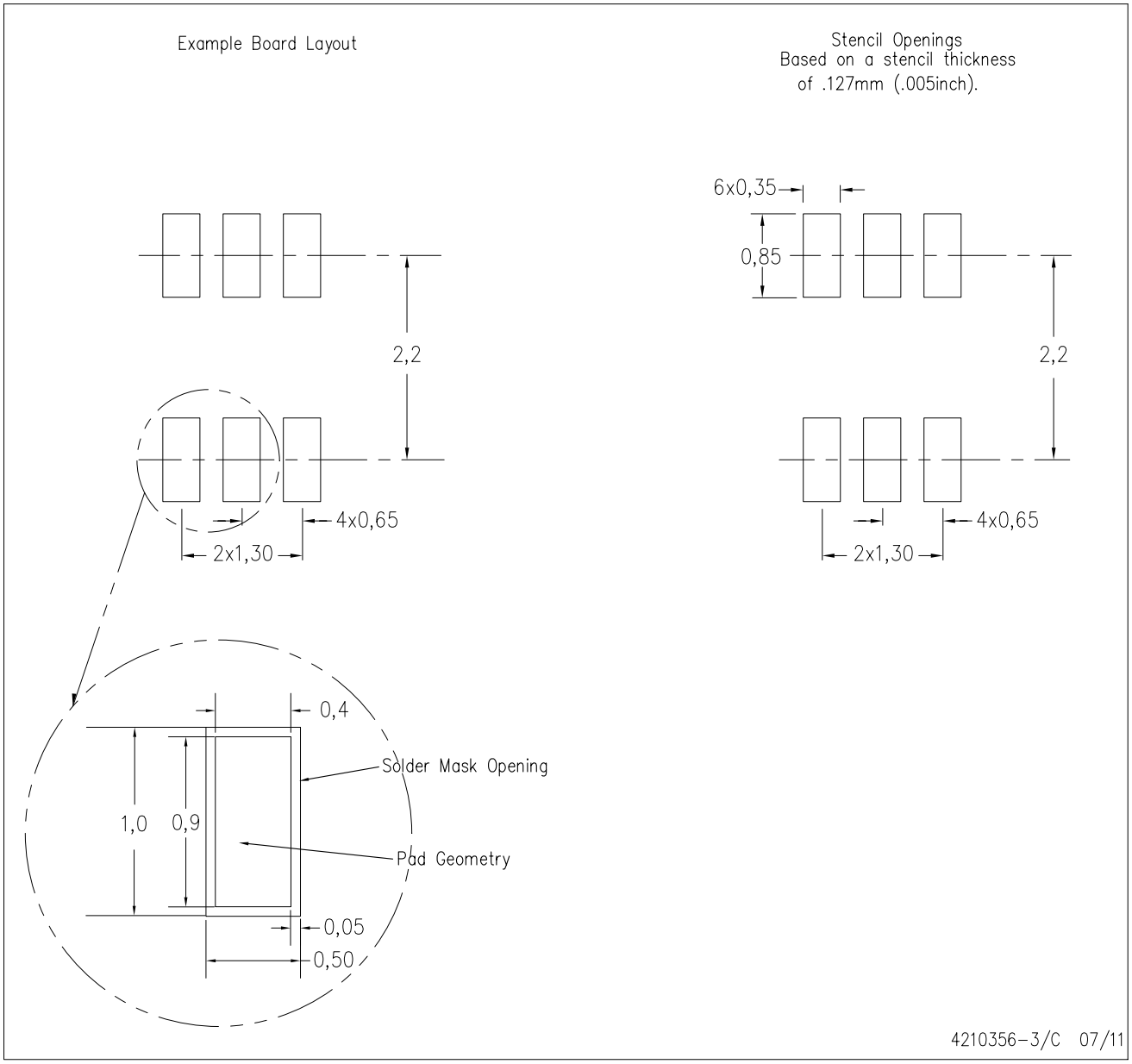
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

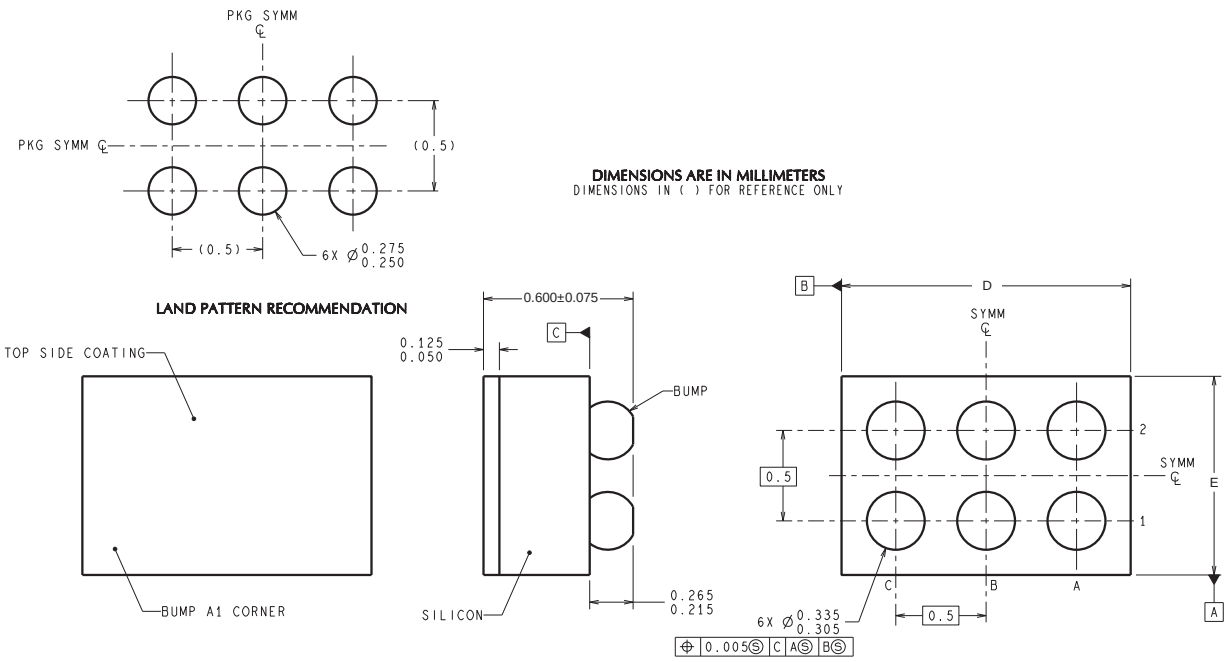
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

YZR0006



TLA06XXX (Rev C)

D: Max = 1.565 mm, Min =1.504 mm

E: Max = 1.057 mm, Min =0.996 mm

4215044/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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