5-Bit Programmable Synchronous Controller for Pentium® III Processors

ADP3157

FEATURES

- Active Voltage Positioning with Gain and Offset Adjustment
- Optimal Compensation for Superior Load Transient Response
- VRM 8.2, VRM 8.3 and VRM 8.4 Compliant
- 5-Bit Digitally Programmable 1.3 V to 3.5 V Output
- Dual N-Channel Synchronous Driver
- Total Output Accuracy ±1% Over Temperature
- High Efficiency, Current-Mode Operation
- Short Circuit Protection
- Overvoltage Protection Crowbar Protects Microprocessors with No Additional External Components
- Power Good Output
- SO-16 Package

APPLICATIONS

- Desktop PC Power Supplies for:
  - Pentium II and Pentium III Processor Families
  - AMD-K6 Processors
  - VRM Modules

GENERAL DESCRIPTION

The ADP3157 is a highly efficient synchronous buck switching regulator controller optimized for converting the 5 V main supply into the core supply voltage required by the Pentium III and other high performance processors. The ADP3157 uses an internal 5-bit DAC to read a voltage identification (VID) code directly from the processor, which is used to set the output voltage between 1.3 V and 3.5 V. The ADP3157 uses a current mode, constant off-time architecture to drive two external N-channel MOSFETs at a programmable switching frequency that can be optimized for size and efficiency. It also uses a unique supplemental regulation technique called active voltage positioning to enhance load transient performance.

Active voltage positioning results in a dc/dc converter that meets the stringent output voltage specifications for Pentium II and Pentium III processors, with the minimum number of output capacitors and smallest footprint. Unlike voltage-mode and standard current-mode architectures, active voltage positioning adjusts the output voltage as a function of the load current so that it is always optimally positioned for a system transient.

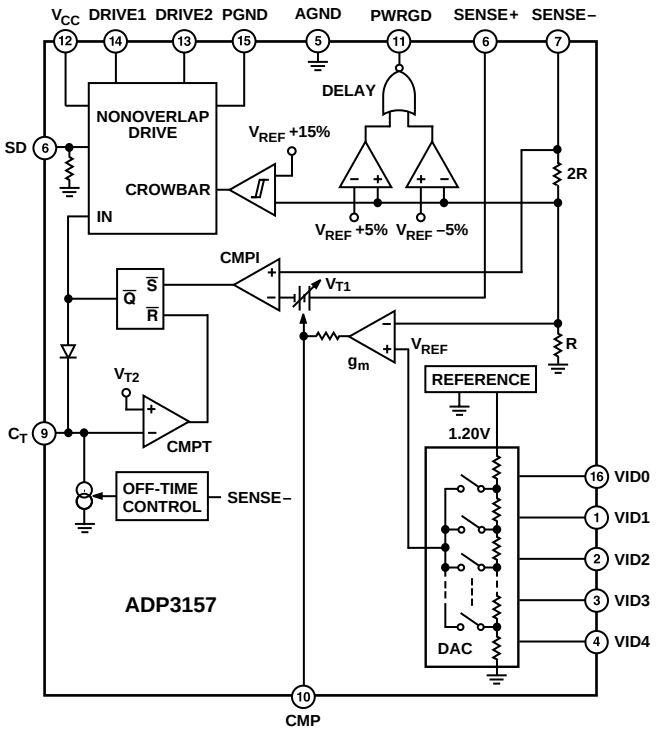
The ADP3157 provides accurate and reliable short circuit protection and adjustable current limiting. It also includes an integrated overvoltage crowbar function to protect the microprocessor from destruction in case the core supply exceeds the nominal programmed voltage by more than 15%.

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FUNCTIONAL BLOCK DIAGRAM



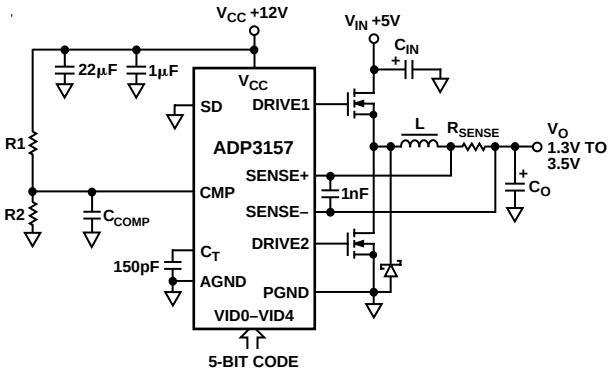


Figure 1. 5-Bit Code Typical Application

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ADP3157–SPECIFICATIONS ($0°C \le T_A \le +70°C$, V_{CC} = 12 V, V_{IN} = 5 V, unless otherwise noted)[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OUTPUT ACCURACY						
1.3 V Output Voltage	V_O	(Figure 13)	1.283	1.3	1.317	V
2.0 V Output Voltage			1.980	2.0	2.020	V
3.5 V Output Voltage			3.465	3.5	3.535	V
OUTPUT VOLTAGE LINE REGULATION	ΔV_O	I_{LOAD} = 10 A (Figure 2) V_{IN} = 4.75 V to 5.25 V		0.05		%
INPUT DC SUPPLY CURRENT[2]						
Normal Mode	I_Q	V_{SD} = 0.6 V		4.1	5.5	mA
Shutdown		T_A = +25°C, VID Pins Floating		140	250	µA
CURRENT SENSE THRESHOLD VOLTAGE	$V_{SENSE(TH)}$	V_{SENSE-} Forced to V_{OUT} – 3%	125	145	165	mV
VID0–VID4 THRESHOLD	$VID_{(TH)}$					
Low					0.6	V
High			2.0			V
VID0–VID4 INPUT CURRENT	I_{VID}	VID = 0 V		110	220	µA
VID0–VID4 PULL-UP RESISTANCE	R_{VID}		20	30		kΩ
C_T PIN DISCHARGE CURRENT	I_{12}	T_A = +25°C				
		V_{OUT} in Regulation		65		µA
		V_{OUT} = 0 V		2	10	µA
OFF-TIME	t_{OFF}	C_T = 150 pF	1.8	2.45	3.2	µs
DRIVER OUTPUT TRANSITION TIME	t_R, t_F	C_L = 7000 pF (Drive 1, 2) T_A = +25°C		120	200	ns
POSITIVE POWER GOOD TRIP POINT[3]	V_{PWRGD}	% Above Output Voltage		5	8	%
NEGATIVE POWER GOOD TRIP POINT[3]	V_{PWRGD}	% Below Output Voltage	–8	–5		%
POWER GOOD RESPONSE TIME	t_{PWRGD}			500		µs
CROWBAR TRIP POINT	$V_{CROWBAR}$	% Above Output Voltage	9	15	24	%
ERROR AMPLIFIER OUTPUT IMPEDANCE	RO_{ERR}			275		kΩ
ERROR AMPLIFIER TRANSCONDUCTANCE	$g_{m(ERR)}$			2.2		mmho
ERROR AMPLIFIER MINIMUM OUTPUT VOLTAGE	V_{CMPMIN}	V_{SENSE+} Forced to V_{OUT} + 3%		0.8		V
ERROR AMPLIFIER MAXIMUM OUTPUT VOLTAGE	V_{CMPMAX}	V_{SENSE+} Forced to V_{OUT} – 3%		2.4		V
ERROR AMPLIFIER BANDWIDTH –3 dB	BW_{ERR}	CMP = Open		500		kHz
SHUTDOWN (SD) PIN						
Low Threshold	SD_L	Part Active			0.6	V
High Threshold	SD_H	Part in Shutdown	2.0			V
Input Current	SD_{IC}			10		µA

NOTES

[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

[2]Dynamic supply current is higher due to the gate change being delivered to the external MOSFETs.

[3]The trip point is for the output voltage coming into regulation.

Specifications subject to change without notice.

PIN FUNCTION DESCRIPTIONS

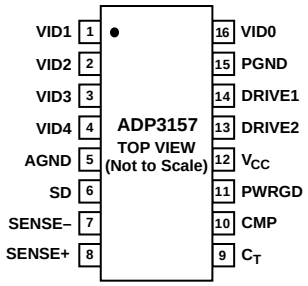
Pin No.	Mnemonic	Function
1–4, 16	VID1–VID4, VID0	Voltage Identification DAC Inputs. These pins are pulled up to an internal reference, providing a logic one if left open. The DAC output programs the SENSE– regulation voltage from 1.3 V to 3.5 V. Leaving all five DAC inputs open results in placing the ADP3157 into shutdown.
5	AGND	Analog Ground. All internal signals of the ADP3157 are reference to this ground.
6	SD	Shutdown. A logic high will place the ADP3157 in shutdown and disable both outputs. This pin is internally pulled down.
7	SENSE–	Connects to the internal resistor divider that senses the output voltage. This pin is also the (–) input for the current comparator.
8	SENSE+	The (+) input for the current comparator. The output current is sensed as a voltage at this pin with respect to SENSE–.
9	C_T	External capacitor C_T connection to ground sets the off time of the device.
10	CMP	Error Amplifier output and compensation point. The voltage at this output programs the output current control level between the SENSE pins.
11	PWRGD	Power Good. An open drain signal indicates that the output voltage is within a ±5% regulation band.
12	V_{CC}	Supply Voltage to ADP3157.
13	DRIVE2	Gate Drive for the (bottom) synchronous rectifier N-channel MOSFET. The voltage at DRIVE2 swings from ground to V_{CC}.
14	DRIVE1	Gate Drive for the buck switch N-channel MOSFET. The voltage at DRIVE1 swings from ground to V_{CC}.
15	PGND	Power Ground. The drivers turn off the buck and synchronous MOSFETs by discharging their gate capacitances to this pin. PGND should have a low impedance path to the source of the synchronous MOSFET.

ABSOLUTE MAXIMUM RATINGS*

Input Supply Voltage (V_{CC}) . . . . . –0.3 V to +16 V
VID0–VID4, SD, PWRGD, CMP, C_T . . . . . –0.3 V to V_{CC}
DRIVE1, DRIVE2, SENSE+, SENSE– . . . . . –0.3 V to V_{CC}
Operating Ambient Temperature Range . . . . . 0°C to +70°C
Junction Temperature Range . . . . . 0°C to +150°C
θ_{JA} . . . . . 110°C/W
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
ADP3157JR	0°C to +70°C	16-Lead SOIC	R-16A/SO-16

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3157 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



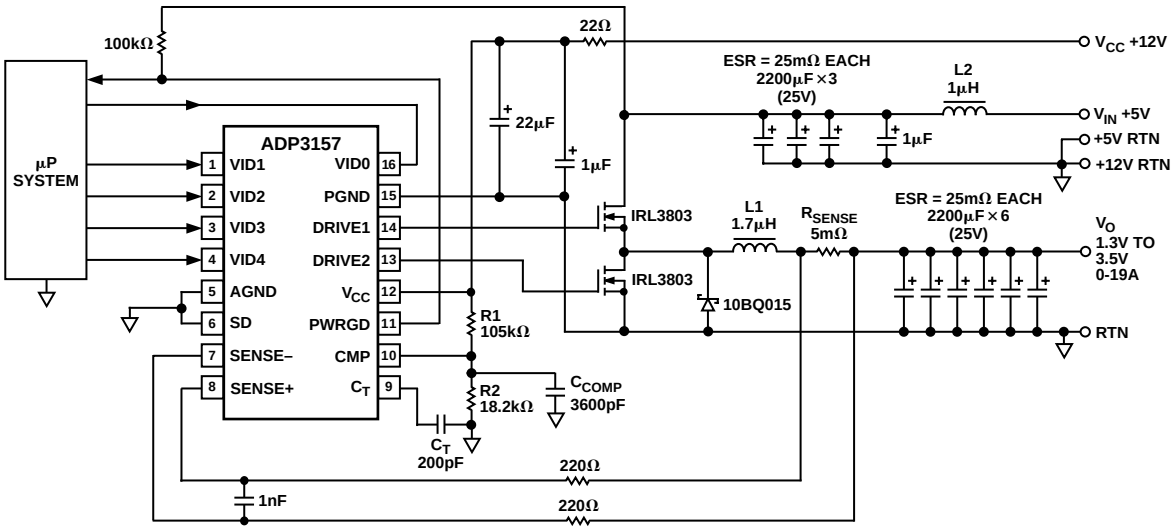


Figure 2. Typical VRM8.2/8.3/8.4 Compliant Core DC/DC Converter Circuit

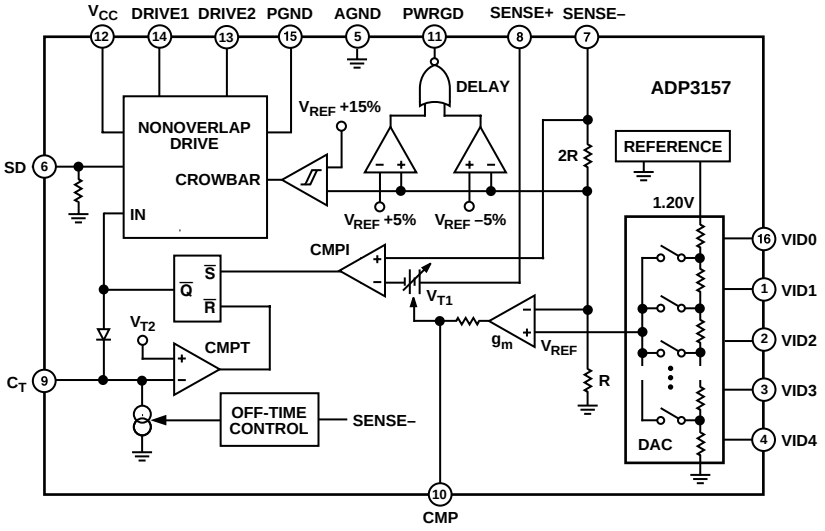


Figure 3. Functional Block Diagram

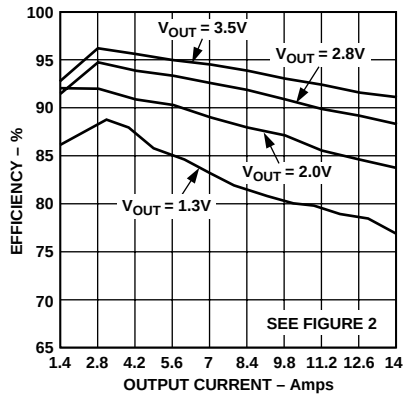


Figure 4. Efficiency vs. Output Current

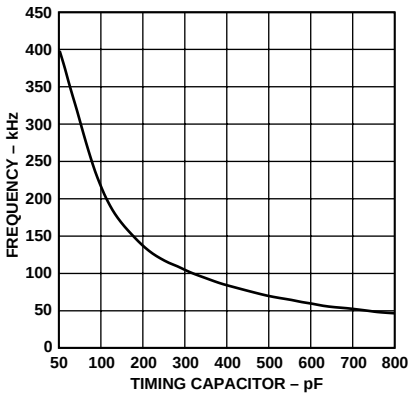


Figure 5. Frequency vs. Timing Capacitor

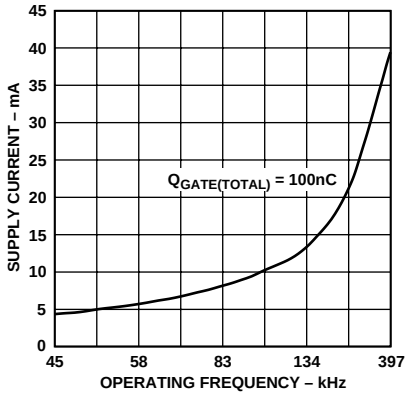


Figure 6. Supply Current vs. Operating Frequency

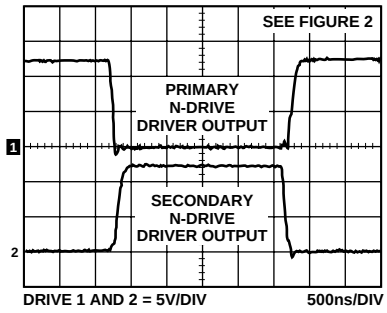


Figure 7. Gate Switching Waveforms

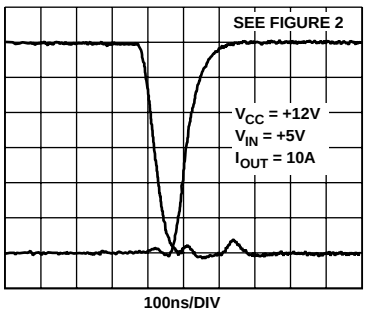


Figure 8. Driver Transition Waveforms

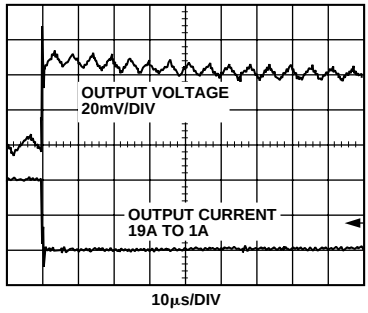


Figure 9. Load Transient Response, 19 A–1 A of Figure 2 Circuit

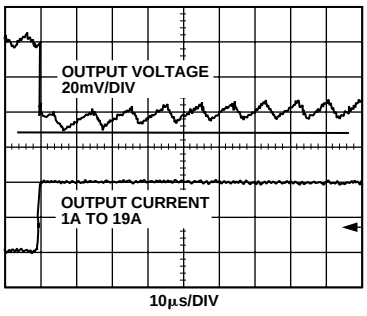


Figure 10. Load Transient Response, 1 A–19 A of Figure 2 Circuit

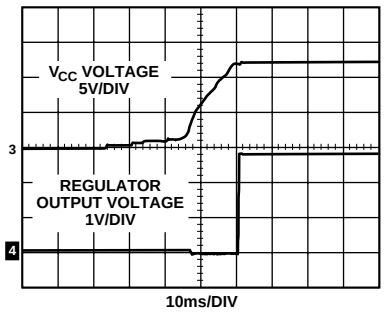


Figure 11. Power-On Start-Up Waveform

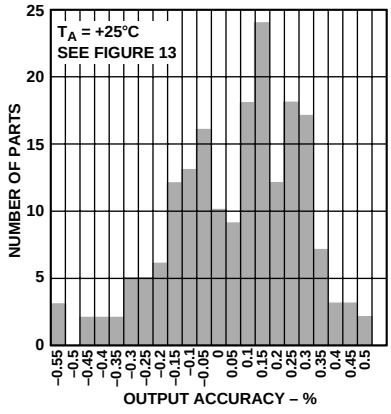


Figure 12. Output Accuracy Distribution, V_{OUT} = 2.0 V

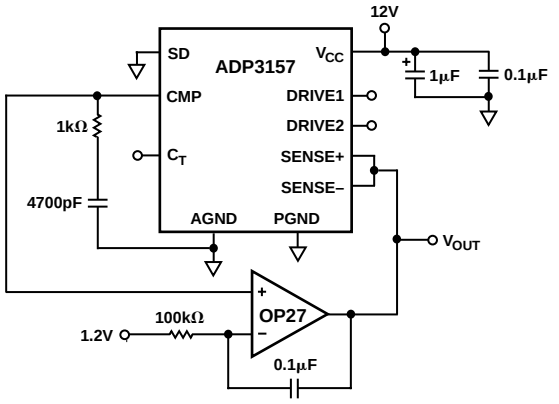


Figure 13. Closed-Loop Test Circuit for Accuracy

THEORY OF OPERATION

The ADP3157 uses a current-mode, constant-off-time control technique to switch a pair of external N-channel MOSFETs in a synchronous buck topology. Constant off-time operation offers several performance advantages, including that no slope compensation is required for stable operation. A unique feature of the constant-off-time control technique is that since the off-time is fixed, the converter's switching frequency is a function of the ratio of input voltage to output voltage. The fixed off-time is programmed by the value of an external capacitor connected to the C_T pin. The on-time varies in such a way that a regulated output voltage is maintained as described below in the cycle-by-cycle operation. Under fixed operating conditions the on-time does not vary, and it only varies slightly as a function of load. This means that switching frequency is fairly constant in standard VRM applications. In order to maintain a ripple current in the inductor that is independent of the output voltage (which also helps control losses and simplify the inductor design), the off-time is made proportional to the value of the output voltage. Normally, the output voltage is constant and therefore the off-time is constant as well.

Active Voltage Positioning

The output voltage is sensed at the SENSE– pin. A voltage-error amplifier, (g_m), amplifies the difference between the output voltage and a programmable reference voltage. The reference voltage is programmed to between 1.3 V and 3.5 V by an internal 5-bit DAC, which reads the code at the voltage identification (VID) pins. Refer to Table I for output voltage vs. VID pin code information. A unique supplemental regulation technique called active voltage positioning with optimal compensation adjusts the output voltage as a function of the load current so that it is always optimally positioned for a load transient. Standard (passive) load voltage positioning, sometimes recommended for use with other architectures, has poor dynamic performance which renders it ineffective under the stringent repetitive transient conditions specified in Intel VRM documents. Consequently, such techniques do not allow the minimum possible number of output capacitors to be used. Optimally compensated active voltage positioning as used in the ADP3157 provides a bandwidth for transient response that is limited only by parasitic output inductance. This yields optimal load transient response with the minimum number of output capacitors.

Table I. Output Voltage vs. VID Code

VID4	VID3	VID2	VID1	VID0	V_{OUT}
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05
1	1	1	1	1	No CPU—Shutdown
1	1	1	1	0	2.10
1	1	1	0	1	2.20
1	1	1	0	0	2.30
1	1	0	1	1	2.40
1	1	0	1	0	2.50
1	1	0	0	1	2.60
1	1	0	0	0	2.70
1	0	1	1	1	2.80
1	0	1	1	0	2.90
1	0	1	0	1	3.00
1	0	1	0	0	3.10
1	0	0	1	1	3.20
1	0	0	1	0	3.30
1	0	0	0	1	3.40
1	0	0	0	0	3.50

Cycle-by-Cycle Operation

During normal operation (when the output voltage is regulated), the voltage-error amplifier and the current comparator (CMPI) are the main control elements. (See the block diagram of Figure 3.) During the on-time of the high side MOSFET, CMPI monitors the voltage between the SENSE+ and SENSE– pins. When the voltage level between the two pins reaches the threshold level V_{T1}, the high side drive output is switched to ground, which turns off the high side MOSFET. The timing capacitor C_T is then discharged at a rate determined by the off-time controller. While the timing capacitor is discharging, the low side drive output goes high, turning on the low side MOSFET. When the voltage level on the timing capacitor has discharged to the threshold voltage level V_{T2}, comparator CMPT resets the SR flip-flop. The output of the flip-flop forces the low side drive output to go low and the high side drive output to go high. As a result, the low side switch is turned off and the high side switch is turned on. The sequence is then repeated. As the load current increases, the output voltage starts to decrease. This causes an increase in the output of the voltage-error amplifier, which, in turn, leads to an increase in the current comparator threshold V_{T1}, thus tracking the load current. To prevent cross conduction of the external MOSFETs, feedback is incorporated to sense the state of the driver output pins. Before the low side drive output can go high, the high side drive output must be low. Likewise, the high side drive output is unable to go high while the low side drive output is high.

Power Good

The ADP3157 has an internal monitor that senses the output voltage and drives the PWRGD pin of the device. This pin is an open drain output whose high level (when connected to a pull-up resistor) indicates that the output voltage has been within a ±5% regulation band of the targeted value for more than 500 µs. The PWRGD pin will go low if the output is outside the regulation band for more than 500 µs.

Output Crowbar

An added feature of using an N-channel MOSFET as the synchronous switch is the ability to crowbar the output with the same MOSFET. If the output voltage is 15% greater than the targeted value, the ADP3157 will turn on the lower MOSFET, which will current-limit the source power supply or blow its fuse, pull down the output voltage, and thus save the microprocessor from destruction. The crowbar function releases at approximately 50% of the nominal output voltage. For example, if the output is programmed to 2.0 V, but is pulled up to 2.3 V or above, the crowbar will turn on the lower MOSFET. If in this case the output is pulled down to less than 1.0 V, the crowbar will release, allowing the output voltage to recover to 2.0 V if the fault condition has been removed.

Shutdown

The ADP3157 has a shutdown (SD) pin that is pulled down by an internal resistor. In this condition the device functions normally. This pin should be pulled high to disable the output drives.

APPLICATION INFORMATION

Specifications for a Design Example

The design parameters for a typical 550 MHz Pentium III application (Figure 2) are as follows:

Input voltage: V_{IN} = 5 V
Auxiliary input: V_{CC} = 12 V
Output voltage: V_O = 2.0 V

Maximum output current:
I_{OMAX} = 17.0 A dc

Minimum output current:
I_{OMIN} = 1.0 A dc

Static tolerance of the supply voltage for the processor core:
ΔV_{OST+} = +70 mV
ΔV_{OST-} = –70 mV

Transient tolerance (for less than 2 µs) of the supply voltage for the processor core when the load changes between the minimum and maximum values with a di/dt of 30 A/µs:

ΔV_{OTR+} = +140 mV
ΔV_{OTR-} = –140 mV

Input current di/dt when the load changes between the minimum and maximum values: less than 8 A/µs

The above requirements correspond to Intel's published power supply requirements based on Intel Pentium III specifications.

C_T Selection for Operating Frequency

The ADP3157 uses a constant-off-time architecture with t_{OFF} determined by an external timing capacitor C_T. Each time the high side N-channel MOSFET switch turns on, the voltage across C_T is reset to approximately 3.3 V. During the off time, C_T is discharged by a constant current of 65 µA. Once C_T reaches 2.3 V, a new on-time cycle is initiated. The value of the off-time is calculated using the continuous-mode operating frequency. Assuming a nominal operating frequency of f_{NOM} = 200 kHz at an output voltage of 2.0 V, the corresponding off time is:

$$t_{OFF} = \left(1 - \frac{V_O}{V_{IN}}\right)\frac{1}{f_{NOM}} = 3.0\ \mu s$$

The timing capacitor can be calculated from the equation:

$$C_T = \frac{t_{OFF} \times 65\ \mu A}{1\ V} = 200\ pF$$

The converter operates at the nominal operating frequency only at the above specified V_{OUT} and at light load. At higher V_{OUT} or heavy load, the operating frequency decreases due to the parasitic voltage drops across the power devices. The actual minimum frequency at V_{OUT} = 2.0 V is calculated to be 180 kHz (see Equation 1), where:

I_{IN}	is the input dc current (assuming an efficiency of 90%, I_{IN} = 7.5 A)
R_{IN}	is the resistance of the input filter (estimated value: 7 mΩ)
$R_{DS(ON)HSF}$	is the resistance of the high side MOSFET (estimated value: 10 mΩ)
$R_{DS(ON)LSF}$	is the resistance of the low side MOSFET (estimated value: 10 mΩ)
R_{SENSE}	is the resistance of the sense resistor (estimated value: 5 mΩ)
R_L	is the resistance of the inductor (estimated value: 6 mΩ)

C_{OUT} Selection–Determining the ESR

The required ESR and capacitance drive the selection of the type and quantity of the output capacitors. The ESR must be small enough that both the resistive voltage deviation due to a step change in the load current and the output ripple voltage stay below the values defined in the specification of the supplied microprocessor. The capacitance must be large enough that the output is held up while the inductor current ramps up or down to the value corresponding to the new load current.

The total static tolerance of the Pentium III processor is 140 mV. Taking into account the ±1% setpoint accuracy of the ADP3157, and assuming a 0.5% (or 10 mV) peak-to-peak ripple, the allowed static voltage deviation of the output voltage when the load changes between the minimum and maximum values is 90 mV. Assuming a step change of $\Delta I = I_{OMAX} - I_{OMIN}$ = 16 A, and allocating all of the total allowed static deviation to the contribution of the ESR sets the following limit:

$$R_{E(MAX)} = ESR_{MAX1} = \frac{90\ mV}{16\ A} = 5.6\ m\Omega$$

The output filter capacitor must have an ESR of less than 5.6 mΩ. One can use, for example, two SP-Type OS-CON capacitors from Sanyo, with 2200 µF capacitance, 7 V voltage rating, and

$$f_{MIN} = \frac{1}{t_{OFF}} \times \frac{V_{IN} - I_{IN}R_{IN} - I_{OMAX}(R_{DS(ON)HSF} + R_{SENSE} + R_L) - V_O}{V_{IN} - I_{IN}R_{IN} - I_{OMAX}(R_{DS(ON)HSF} + R_{SENSE} + R_L - R_{DS(ON)LSF})} = 180\ kHz \quad (1)$$

10 mΩ ESR. The two capacitors have a total ESR of 5.0 mΩ when connected in parallel, which gives adequate margin.

Inductor Selection

The minimum inductor value can be calculated from ESR, off-time, dc output voltage and allowed peak-to-peak ripple voltage using the following equation:

$$L_{MIN1} = \frac{V_O t_{OFF} R_{E(MAX)}}{V_{RIPPLE,\ p-p}} = \frac{2.0\ V \times 3\ \mu s \times 5.3\ m\Omega}{10\ mV} = 3.2\ \mu H$$

The minimum inductance gives a peak-to-peak ripple current of 2.55 A, or 15% of the maximum dc output current I_{OMAX}.

The inductor peak current in normal operation is:

$$I_{LPEAK} = I_{OMAX} + I_{RPP}/2 = 19.5\ A$$

The inductor valley current is:

$$I_{LVALLEY} = I_{LPEAK} - I_{RPP} = 14.5\ A$$

The inductor for this application should have an inductance of 3.3 µH at full load current and should not saturate at the worst-case overload or short circuit current at the maximum specified ambient temperature.

Tips for Selecting the Inductor Core

Ferrite designs have very low core loss, so the design should focus on copper loss and on preventing saturation. Molypermalloy, or MPP, is a low loss core material for toroids, and it yields the smallest size inductor, but MPP cores are more expensive than ferrite cores or the Kool Mµ® cores from Magnetics, Inc.

C_{OUT} Selection–Determining the Capacitance

The minimum capacitance of the output capacitor is determined from the requirement that the output be held up while the inductor current ramps up (or down) to the new value. The minimum capacitance should produce an initial dv/dt which is equal (but opposite in sign) to the dv/dt obtained by multiplying the di/dt in the inductor and the ESR of the capacitor:

$$C_{MIN} = \frac{\left(I_{OMAX} - I_{OMIN}\right) \times 0.8}{R_E(di/dt)} = \frac{\left(17\ A - 1\ A\right) \times 0.8}{5\ m\Omega \times (2.0\ V/\ 3.0 \mu H)} = 3840\ \mu F$$

In the above equation the value of di/dt is calculated as the smaller voltage across the inductor (i.e., V_{IN}–V_{OUT} rather than V_{OUT}) divided by the maximum inductance inductor. The two parallel-connected 2200 µF capacitors have a total capacitance of 4400 µF, so the minimum capacitance requirement is met with ample margin.

R_{SENSE}

The value of R_{SENSE} is based on the required output current. The current comparator of the ADP3157 has a threshold range that extends from 0 mV to 125 mV (minimum). Note that the full 125 mV range cannot be used for the maximum specified nominal current, as headroom is needed for current ripple, and transients.

The current comparator threshold sets the peak of the inductor current yielding a maximum output current, I_{OMAX}, which equals the peak value less half of the peak-to-peak ripple current. Solving for R_{SENSE}, allowing a 20% margin for overhead, and using the minimum current sense threshold of 125 mV, yields:

$$R_{SENSE} = (125\ mV)/[1.2(I_{OMAX} + I_{RPP}/2)] = 5.0\ m\Omega$$

Once R_{SENSE} has been chosen, the peak short-circuit current $I_{SC(PK)}$ can be predicted from the following equation:

$$I_{SC(PK)} = (145\ mV)/R_{SENSE} = (145\ mV)/(5.0\ m\Omega) = 29\ A$$

The actual short-circuit current is less than the above calculated $I_{SC(PK)}$ value because the off-time rapidly increases when the output voltage drops below 1 V. The relationship between the off-time and the output voltage is:

$$t_{OFF} \approx \frac{C_T \times 1V}{\frac{V_O}{360\ k\Omega} + 2\ \mu A}$$

With a short circuit across the output, the off-time will be about 70 µs. During that time the inductor current gradually decays. The amount of decay depends on the L/R time constant in the output circuit. With an inductance of 3.3 µH and total resistance of 22 mΩ, the time constant will be 73 µs. This yields an average short-circuit current of about 20 A. To safely carry the short-circuit current, the sense resistor must have a power rating of at least 20 $A^2 \times 5.0$ mΩ = 2.0 W.

Current Transformer Option

An alternative to using a low value and high power current sense resistor is to reduce the sensed current by using a low cost current transformer and a diode. The current can then be sensed with a small-size, low cost SMT resistor. Using a transformer with one primary and 50 secondary turns reduces the worst-case resistor dissipation to a few mW. Another advantage of using this option is the separation of the current and voltage sensing, which makes the voltage sensing more accurate.

Power MOSFETs

Two external N-channel power MOSFETs must be selected for use with the ADP3157, one for the main switch, and an identical one for the synchronous switch. The main selection parameters for the power MOSFETs are the threshold voltage $V_{GS(TH)}$ and the on resistance $R_{DS(ON)}$.

The minimum input voltage dictates whether standard threshold or logic-level threshold MOSFETs must be used. For V_{IN} > 8 V, standard threshold MOSFETs ($V_{GS(TH)}$ < 4 V) may be used. If V_{IN} is expected to drop below 8 V, logic-level threshold MOSFETs ($V_{GS(TH)}$ < 2.5 V) are strongly recommended. Only logic-level MOSFETs with V_{GS} ratings higher than the absolute maximum of V_{CC} should be used.

The maximum output current I_{OMAX} determines the $R_{DS(ON)}$ requirement for the two power MOSFETs. When the ADP3157 is operating in continuous mode, the simplifying assumption can be made that one of the two MOSFETs is always conducting the average load current. For V_{IN} = 5 V and V_{OUT} = 2.8 V, the maximum duty ratio of the high side FET is:

$$D_{MAXHF} = (1 - f_{MIN} \times t_{OFF}) = (1\ kHz - 180\ kHz \times 3.0\ \mu s) = 46\%$$

The maximum duty ratio of the low side (synchronous rectifier) FET is:

$$D_{MAXLF} = 1 - D_{MAXHF} = 54\%$$

The maximum rms current of the high side FET is:

$$I_{RMSHS} = [D_{MAXHF}\ (I_{LVALLEY}2 + I_{LPEAK}2 + I_{LVALLEY}I_{LPEAK})/3]^{0.5}$$
$$= 11.6\ A\ rms$$

The maximum rms current of the low side FET is:

$$I_{RMSLS} = [D_{MAXLF} (I_{LVALLEY}2 + I_{LPEAK}2 + I_{LVALLEY}I_{LPEAK})/3]^{0.5} = 12.5\ A\ rms$$

The $R_{DS(ON)}$ for each FET can be derived from the allowable dissipation. If 5% of the maximum output power is allowed for FET dissipation, the total dissipation will be:

$$P_{FETALL} = 0.05\ V_O I_{OMAX} = 1.7\ W$$

Allocating half of the total dissipation for the high side FET and half for the low side FET, the required minimum FET resistances will be:

$$R_{DS(ON)HSF(MIN)} = 0.85\ W/(11.6\ A)^2 = 6\ m\Omega$$
$$R_{DS(ON)LSF(MIN)} = 0.85\ W/(12.5\ A)^2 = 5.5\ m\Omega$$

Note that there is a trade-off between converter efficiency and cost. Larger FETs reduce the conduction losses and allow higher efficiency, but increase the system cost. If efficiency is not a major concern, the International Rectifier IRL3803 is an economical choice for both the high side and low side positions. Those devices have an $R_{DS(ON)}$ of 6 mΩ at V_{GS} = 10 V and at +25°C. The low side FET is turned on with at least 10 V. The high side FET, however, is turned on with only 12 V – 5 V = 7 V. The specified $R_{DS(ON)}$ at the expected highest FET junction temperature of +140°C must be modified by:

$$R_{DS(ON)MULT} = 1.7$$

Using this multiplier, the expected $R_{DS(ON)}$ at +140°C is 1.7 × 6 mΩ = 10 mΩ.

The high side FET dissipation is:

$$P_{DFETHS} = I_{RMSHS}^2 R_{DS(ON)} + 0.5\ V_{IN} I_{LPEAK} Q_G f_{MIN}/I_G \sim 2.3\ W$$

where the second term represents the turn-off loss of the FET. (In the second term, Q_{GS} is the gate charge to be removed from the gate for turn-off and I_G is the gate current. From the data sheet, Q_{GS} is a 41 nC and the peak gate drive current provided by the ADP3157 is about 1 A.)

The low side FET dissipation is:

$$P_{DFETLS} = I_{RMSLS}^2 R_{DS(ON)} = 1.6\ W$$

(Note that there are no switching losses in the low side FET.)

To maintain an acceptable MOSFET junction temperature, proper heat sinks should be used. The Thermalloy 6030 heat sink has a thermal impedance of 13°C/W with convection cooling. With this heat sink, the junction-to-ambient thermal impedance of the chosen high side FET θ_{JAHS} will be 13°C/W (heat sink-to-ambient) + 2°C/W (junction-to-case) + 0.5°C/W (case-to-heat sink) = 15.5°C/W.

At full load, and at +50°C ambient temperature, the junction temperature of the high side FET is:

$$T_{JHSMAX} = T_A + \theta_{JAHS} P_{DFETHS} = +86°C$$

The same heat sink may be used for the low side FET, e.g., the Thermalloy type 7141 (θ = 20.3°C/W). With this heat sink, the junction temperature of the low side FET is:

$$T_{JLSMAX} = T_A + \theta_{JALS} P_{DFETLS} = +82.5°C$$

All of the above-calculated junction temperatures are safely below the +175°C maximum specified junction temperature of the selected FETs.

The maximum operating junction temperature of the ADP3157 is calculated as follows:

$$T_{JICMAX} = T_A + \theta_{JA} (I_{IC} V_{CC} + P_{DR})$$

where θ_{JA} is the junction-to-ambient thermal impedance of the ADP3157 and P_{DR} is the drive power. From the data sheet, θ_{JA} is equal to 110°C/W and I_{IC} = 2.7 mA. P_{DR} can be calculated as follows:

$$P_{DR} = (C_{RSS} + C_{ISS}) V_{CC}^2 f_{MAX} = 307\ mW$$

The result is:

$$T_{JICMAX} = +86°C$$

C_{IN} Selection and Input Current di/dt Reduction

In continuous inductor-current mode, the source current of the high side MOSFET is a square wave with a duty ratio of V_{OUT}/V_{IN}. To keep the input ripple voltage at a low value, one or more capacitors with low equivalent series resistance (ESR) and adequate ripple-current rating must be connected across the input terminals. The maximum rms current of the input bypass capacitors is:

$$I_{CINRMS} = 0.5\ I_{OMAX} = 8.5\ A\ rms$$

For an FA-type capacitor with 2700 µF capacitance and 10 V voltage rating, the ESR is 34 mΩ and the allowed ripple current at 100 kHz is 1.94 A. At +105°C, at least four such capacitors must be connected in parallel to handle the calculated ripple current. At +50°C ambient, however, a higher ripple current can be tolerated, so three capacitors in parallel are adequate.

The ripple voltage across the three paralleled capacitors is:

$$V_{CINRPL} = I_{OMAX} [ESR_{IN}/3 + D_{MAXHF}/(3\ C_{IN}\ f_{MIN})] = 100\ mV\ p\text{-}p$$

To further reduce the effect of the ripple voltage on the system supply voltage bus and to reduce the input-current di/dt to below the recommended maximum of 0.1 A/µs, an additional small inductor (L > 1.7 µH @ 10 A) should be inserted between the converter and the supply bus (see Figure 2).

Feedback Loop Compensation Design for Active Voltage Positioning

Optimized compensation of the ADP3157 allows the best possible containment of the peak-to-peak output voltage deviation. Any practical switching power converter is inherently limited by the inductor in its output current slew rate to a value much less than the slew rate of the load. Therefore, any sudden change of load current will initially flow through the output capacitors, and this will produce an output voltage deviation equal to the ESR of the output capacitor array times the load current change.

To correctly implement active voltage positioning, the low frequency output impedance (i.e., the output resistance) of the converter should be made equal to the maximum ESR of the output capacitor array. This can be achieved by having a single pole roll-off of the voltage gain of the g_m error amplifier, where the pole frequency coincides with the ESR zero of the output capacitor. A gain with single pole roll-off requires that the g_m amplifier output pin be terminated by the parallel combination of a resistor and capacitor. The required resistor value can be calculated from the equation:

$$R_C = \frac{275\ k\Omega \times Rt_{TOTAL}}{275\ k\Omega - Rt_{TOTAL}}$$

where

$$Rt_{TOTAL} = \frac{16.4\,k\Omega \times R_{CS} \times I_{OMAX}}{V_{HI} - V_{LO}}$$

and where the quantities 16.4 $k\Omega$ and 275 $k\Omega$ are characteristics of the ADP3157 and the value of the current sense resistor, R_{CS}, has already been determined as above.

Although a single termination resistor equal to R_C would yield the proper voltage positioning gain, the dc biasing of that resistor would determine how the regulation band is centered (i.e., offset). Note that sometimes the specified regulation band is asymmetrical with respect to the nominal VID voltage. With the ADP3157, the offset is already considered as part of the design procedure—no special provision is required. To accomplish the dc biasing, it is simplest to use two resistors to terminate the g_m amplifier output, with the lower resistor tied to ground and the upper resistor to the 12 V supply of the IC. The values of these resistors can be calculated using:

$$R_{UPPER} = R_C \times \frac{V_{DIV}}{V_{OS}}$$

and

$$R_{LOWER} = R_C \times \frac{V_{OS}}{V_{DIV} - V_{OS}}$$

where V_{DIV} is the resistor divider supply voltage (e.g., the recommended 12 V), and V_{OS} is the offset voltage required on the amplifier to produce the desired offset at the output. V_{OS} is calculated using Equation 2 below, where $V_{OUT(OS)}$ is the offset from the nominal VID-programmed value to the center of the specified regulation window for the output voltage. (Note this may be either positive or negative.) For clarification, that offset is given by:

$$V_{OUT(OS)} = \frac{1}{2}(V_{HI} + V_{LO}) - VID$$

where V_{HI} and V_{LO} are the respective upper and lower limits allowed for regulation.

$$V_{OS} = \frac{R_C}{Rt_{TOTAL}} \times \left[0.8\ V + V_{OUT(OS)} \left(\frac{Rt_{TOTAL}}{1.36\ k\Omega} \right) - 1.7\ V \left(\frac{Rt_{TOTAL}}{275\ k\Omega} \right) + 6\ R_{CS} I_{OMAX} \right] \quad (2)$$

Finally, the compensating capacitance is determined from the equality of the pole frequency of the error amplifier gain and the zero frequency of the impedance of the output capacitor:

$$C_{COMP} = \frac{C_O \times ESR}{Rt_{TOTAL}}$$

Trade-Offs Between DC Load Regulation and AC Load Regulation

Casual observation of the circuit operation—e.g., with a voltmeter—would make it appear that the dc load regulation appears to be rather poor compared to a conventional regulator. This would be especially noticeable under very light or very heavy loads where the voltage is "positioned" near one of the extremes of the regulation window rather than near the nominal center value. It must be noted and understood that this low gain characteristic (i.e., loose dc load regulation) is inherently required to allow improved transient containment (i.e., to achieve tighter ac load regulation). That is, the dc load regulation is intentionally sacrificed (but kept within specification) in order to minimize the number of capacitors required to contain the load transients produced by the CPU.

LAYOUT AND COMPONENT PLACEMENT GUIDELINES

The following guidelines are recommended for optimal performance of a switching regulator in a PC system:

General Recommendations

1. For best results, a four-layer (minimum) PCB is recommended. This should allow the needed versatility for control circuitry interconnections with optimal placement, a signal ground plane, power planes for both power ground and the input power (e.g., 5 V), and wide interconnection traces in the rest of the power delivery current paths. Each square unit of 1 ounce copper trace has a resistance of ~0.53 mW at room temperature.
2. Whenever high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.
3. The power and ground planes should overlap each other as little as possible. It is generally easiest (although not necessary) to have the power and signal ground planes on the same PCB layer. The planes should be connected nearest to the first input capacitor where the input ground current flows from the converter back to the power source (e.g., 5 V).

4. If critical signal lines (including the voltage and current sense lines of the ADP3157) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.
5. The PGND pin of the ADP3157 should connect first to a ceramic bypass capacitor (on the V_{CC} pin) and then into the power ground plane using the shortest possible trace. However, the power ground plane should not extend under other signal components, including the ADP3157 itself. If necessary, follow the preceding guideline to use the signal plane as a shield between the power ground plane and the signal circuitry.
6. The AGND pin of the ADP3157 should connect first to the timing capacitor (on the C_T pin), and then into the signal ground plane. In cases where no signal ground plane can be used, short interconnections to other signal ground circuitry in the power converter should be used—the compensation capacitor being the next most critical.
7. The output capacitors of the power converter should be connected to the signal ground plan even though power current flows in the ground of these capacitors. For this reason, it is advised to avoid critical ground connections (e.g., the signal circuitry of the power converter) in the signal ground plane between the input and output capacitors. It is also advised to keep the planar interconnection path short (i.e., have input and output capacitors close together).
8. The output capacitors should also be connected as closely as possible to the load (or connector) that receives the power (e.g., a microprocessor core). If the load is distributed, the capacitors also should be distributed, and generally in proportion to where the load tends to be more dynamic.
9. Absolutely avoid crossing any signal lines over the switching power path loop, described below.

Power Circuitry

10. The switching power path should be routed on the PCB to encompass the smallest possible area in order to minimize radiated switching noise energy (i.e., EMI). Failure to take proper precaution often results in EMI problems for the entire PC system as well as noise related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors, the two FETs, and the power Schottky diode if used, including all interconnecting PCB traces and planes. The use of short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high-energy ringing, and it accommodates the high current demand with minimal voltage loss.
11. A power Schottky diode (1 ~ 2 A dc rating) placed from the lower FET's source (anode) to drain (cathode) will help to minimize switching power dissipation in the upper FET. In the absence of an effective Schottky diode, this dissipation occurs through the following sequence of switching events. The lower FET turns off in advance of the upper FET turning on (necessary to prevent cross-conduction). The circulating current in the power converter, no longer finding a path for current through the channel of the lower FET, draws current through the inherent body-drain diode of the FET. The upper FET turns on, and the reverse recovery characteristic of the lower FET's body-drain diode prevents the drain voltage from being pulled high quickly. The upper FET then conducts very large current while it momentarily has a high voltage forced across it, which translates into added power dissipation in the upper FET. The Schottky diode minimizes this problem by carrying a majority of the circulating current when the lower FET is turned off, and by virtue of its essentially nonexistent reverse recovery time.
12. A small ferrite bead inductor placed in series with the drain of the lower FET can also help to reduce this previously described source of switching power loss.
13. Whenever a power dissipating component (e.g., a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are: improved current rating through the vias (if it is a current path), and improved thermal performance—especially if the vias extended to the opposite side of the PCB where a plane can more readily transfer the heat to the air.
14. The output power path, though not as critical as the switching power path, should also be routed to encompass a small area. The output power path is formed by the current path through the inductor, the current sensing resistor, the output capacitors, and back to the input capacitors.
15. For best EMI containment, the power ground plane should extend fully under all the power components except the output capacitors. These are: the input capacitors, the power MOSFETs and Schottky diode, the inductor, the current sense resistor and any snubbing elements that might be added to dampen ringing. Avoid extending the power ground under any other circuitry or signal lines, including the voltage and current sense lines.

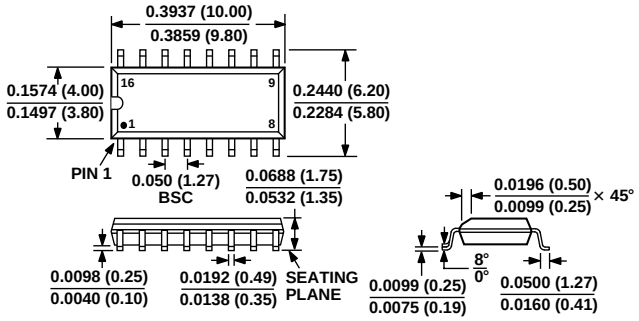
Signal Circuitry

16. The output voltage is sensed and regulated between the AGND pin (which connects to the signal ground plane) and the SENSE– pin. The output current is sensed (as a voltage) and regulated between the SENSE– pin and the SENSE+ pin. In order to avoid differential mode noise pickup in those sensed signals, their loop areas should be small. Thus the SENSE– trace should be routed atop the signal ground plane, and the SENSE+ and SENSE– traces should be routed as a closely coupled pair (SENSE+ should be over the signal ground plane as well).
17. The SENSE+ and SENSE– traces should be Kelvin connected to the current sense resistor so that the additional voltage drop due to current flow on the PCB at the current sense resistor connections does not affect the sensed voltage. It is desirable to have the ADP3157 close to the output capacitor bank and not in the output power path, so that any voltage drop between the output capacitors and the AGND pin is minimized, and voltage regulation is not compromised.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead SOIC
(R-16A/SO-16)



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