ESD Protection Diodes Silicon Epitaxial Planar

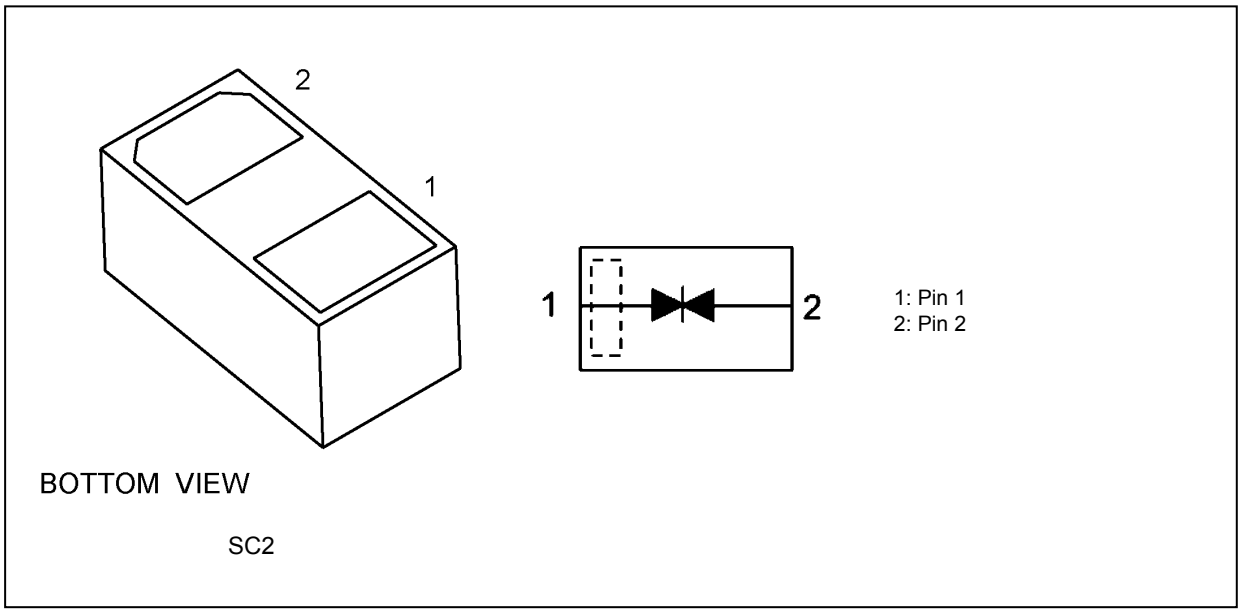
# DF2B6.8M2SC

## 1. Applications

- ESD Protection

Note: This product is designed for protection against electrostatic discharge (ESD) and is not intended for any other purpose, including, but not limited to, voltage regulation.

## 2. Packaging and Internal Circuit




## 3. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a$ = 25°C)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Electrostatic discharge voltage (IEC61000-4-2)(Contact) | $V_{ESD}$ | ±8 | kV |
| Junction temperature | $T_j$ | 150 | °C |
| Storage temperature | $T_{stg}$ | -55 to 150 | °C |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## 4. Electrical Characteristics (Unless otherwise specified, $T_a$ = 25°C)

$V_{RWM}$: Working peak reverse voltage
$V_{BR}$: Reverse breakdown voltage
$I_{BR}$: Reverse breakdown current
$I_R$: Reverse current
$V_C$: Clamp voltage
$I_{PP}$: Peak pulse current
$R_{DYN}$: Dynamic resistance

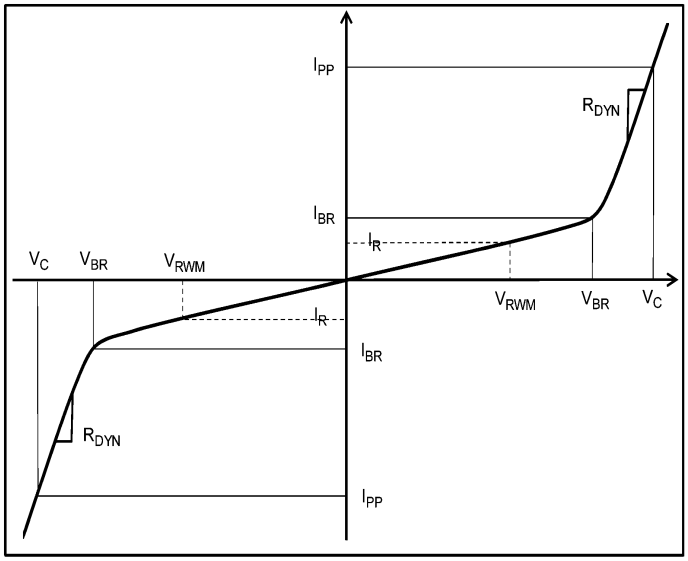



**Fig. 4.1 Definitions of Electrical Characteristis**

| Characteristics | Symbol | Note | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Working peak reverse voltage | $V_{RWM}$ | | — | — | — | 5 | V |
| Reverse breakdown voltage | $V_{BR}$ | | $I_{BR}$ = 1 mA | 6 | — | — | V |
| Reverse current | $I_R$ | | $V_{RWM}$ = 5 V | — | — | 0.05 | μA |
| Clamp voltage | $V_C$ | (Note 1) | $I_{PP}$ = 1 A | — | 13 | — | V |
| Dynamic resistance | $R_{DYN}$ | (Note 2) | — | — | 1.15 | — | Ω |
| Total capacitance | $C_t$ | (Note 3) | $V_R$ = 0 V, f = 1 MHz | — | 0.2 | 0.4 | pF |

Note 1: Based on IEC61000-4-5 8/20 μs pulse.
Note 2: TLP parameter: Z0 = 50 Ω, tp = 100 ns, tr = 300 ps, averaging window: t1 = 30 ns to t2 = 60 ns, extraction of dynamic resistance using a least-squares fit of TLP characteristics at $I_{PP}$ between 3 A to 8 A.
Note 3: Guaranteed by design.

## 5. Guaranteed ESD Protection (Note)

| Test Condition | ESD Protection |
|---|---|
| IEC61000-4-2 (Contact discharge) | ±8 kV |

Note: Criterion: No damage to devices.

## 6. Marking

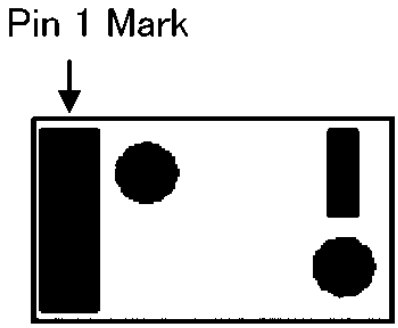



Fig. 6.1 Marking

| Marking Code | Part Number |
|---|---|
| (Dot designation) | DF2B6.8M2SC |

## 7. Land Pattern Dimensions (for reference only)

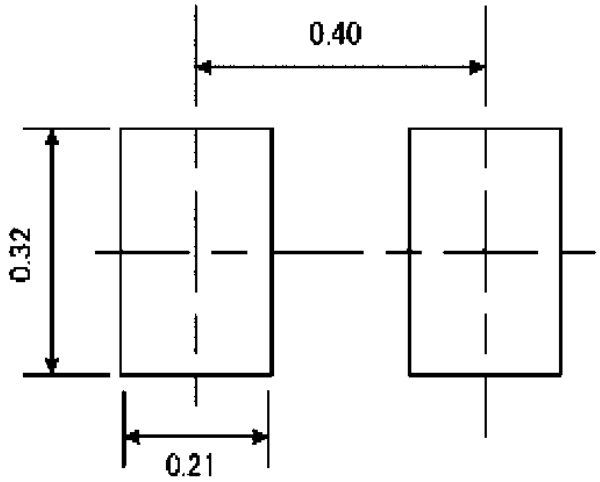



Fig. 7.1 Land Pattern Dimensions (Unit: mm)

## 8. Characteristics Curves (Note)

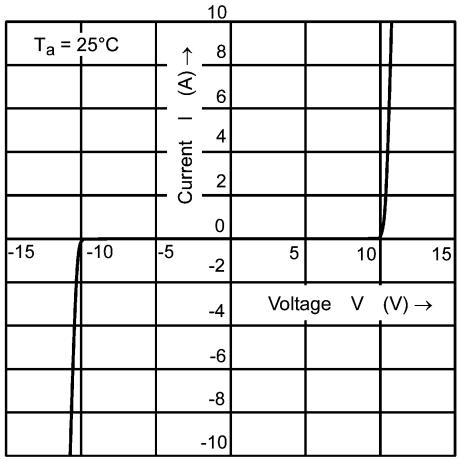



Fig. 8.1 I - V

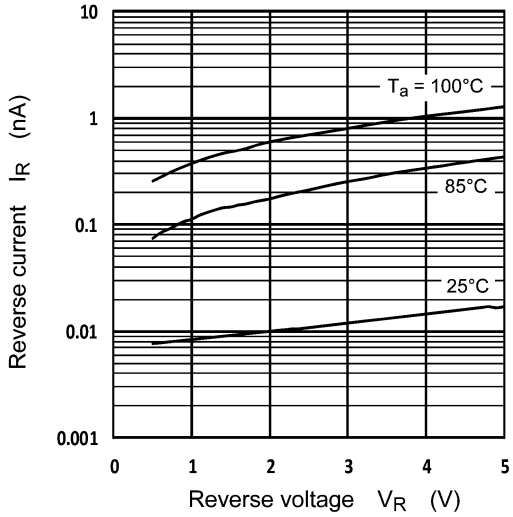



Fig. 8.2 $I_R$ - $V_R$

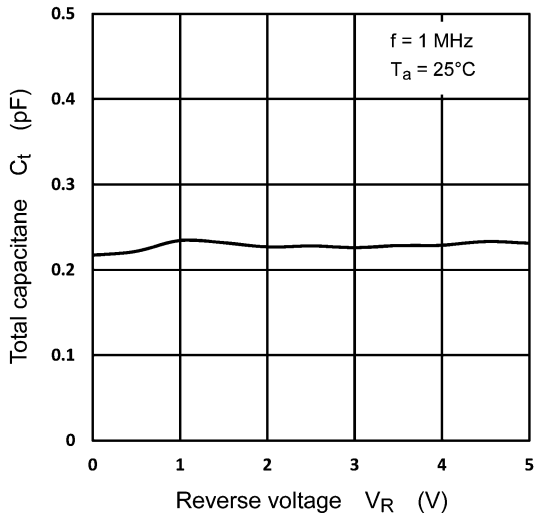



Fig. 8.3 $C_t$ - $V_R$

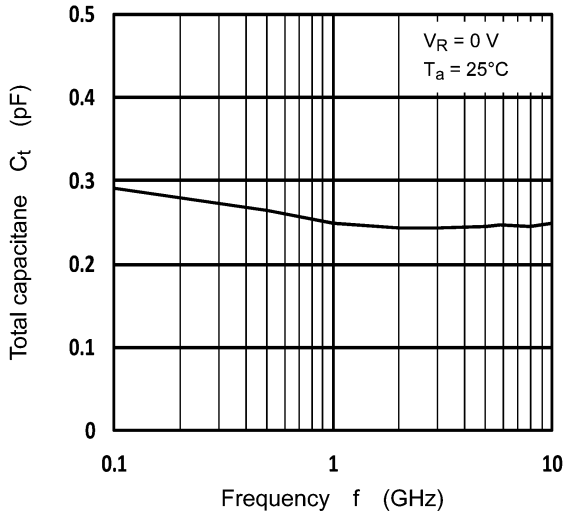



Fig. 8.4 $C_t$ - f

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

## 9. Clamp Voltage $V_C$ - Peak Pulse Current ($I_{PP}$) (Note)

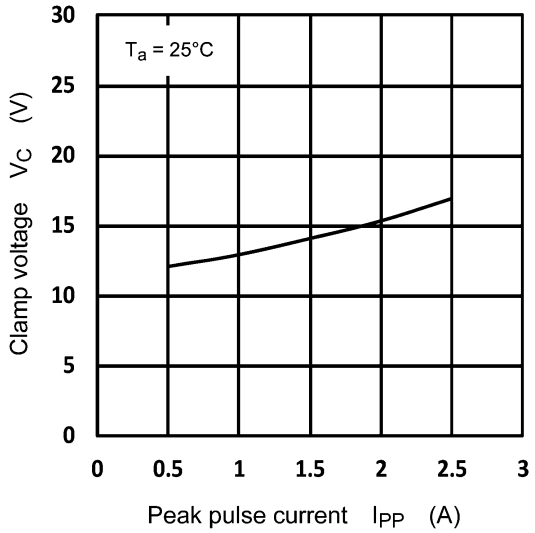



Fig. 9.1 $V_C$ - $I_{PP}$

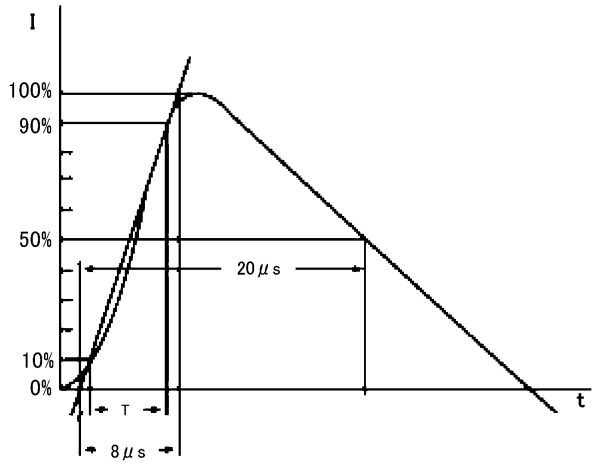



Fig. 9.2 Based on IEC61000-4-5 8/20 μs pulse.

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

## 10. Insertion Loss (S21) (Note)

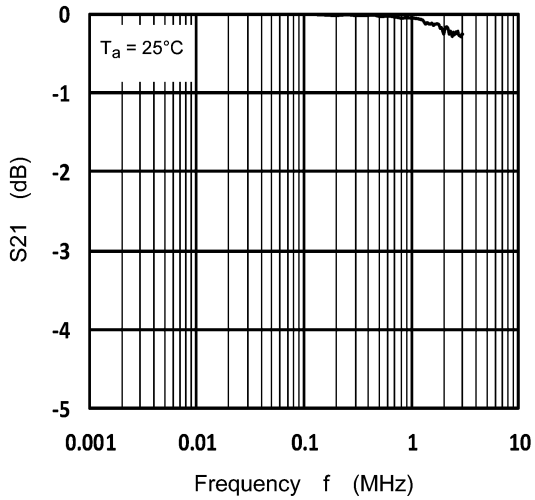
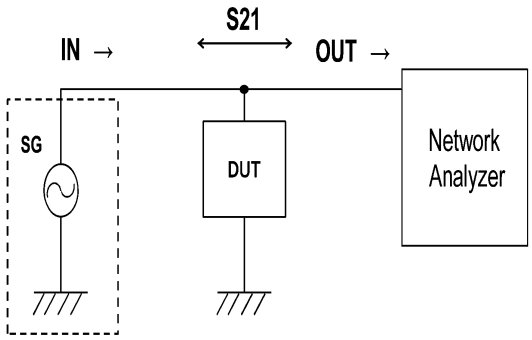



Fig. 10.1 S21 - f




Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

## 11. ESD Clamp Waveform (Note)

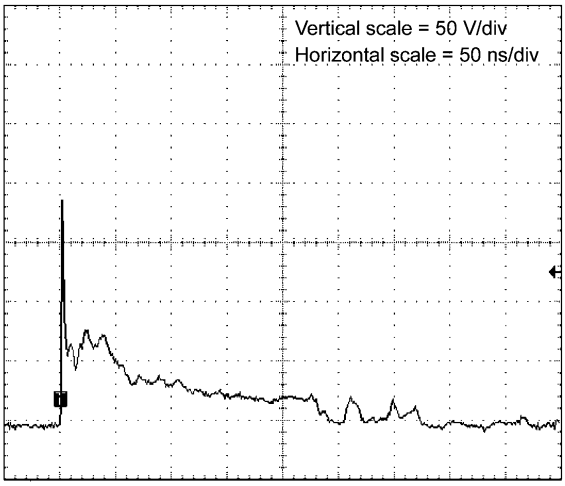



Fig. 11.1 +8 kV

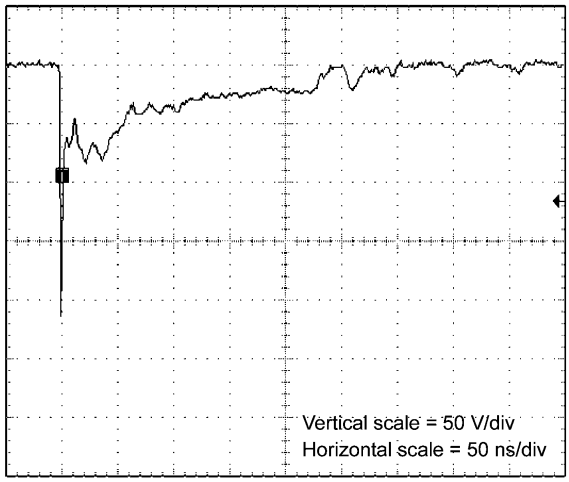



Fig. 11.2 -8 kV

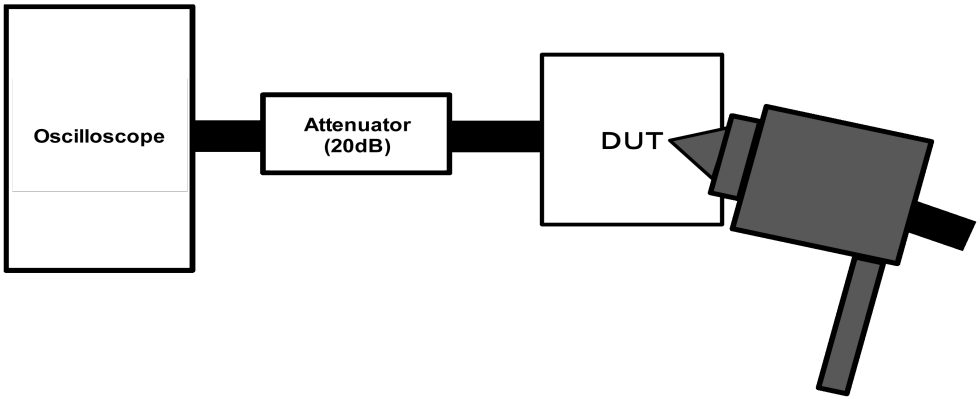
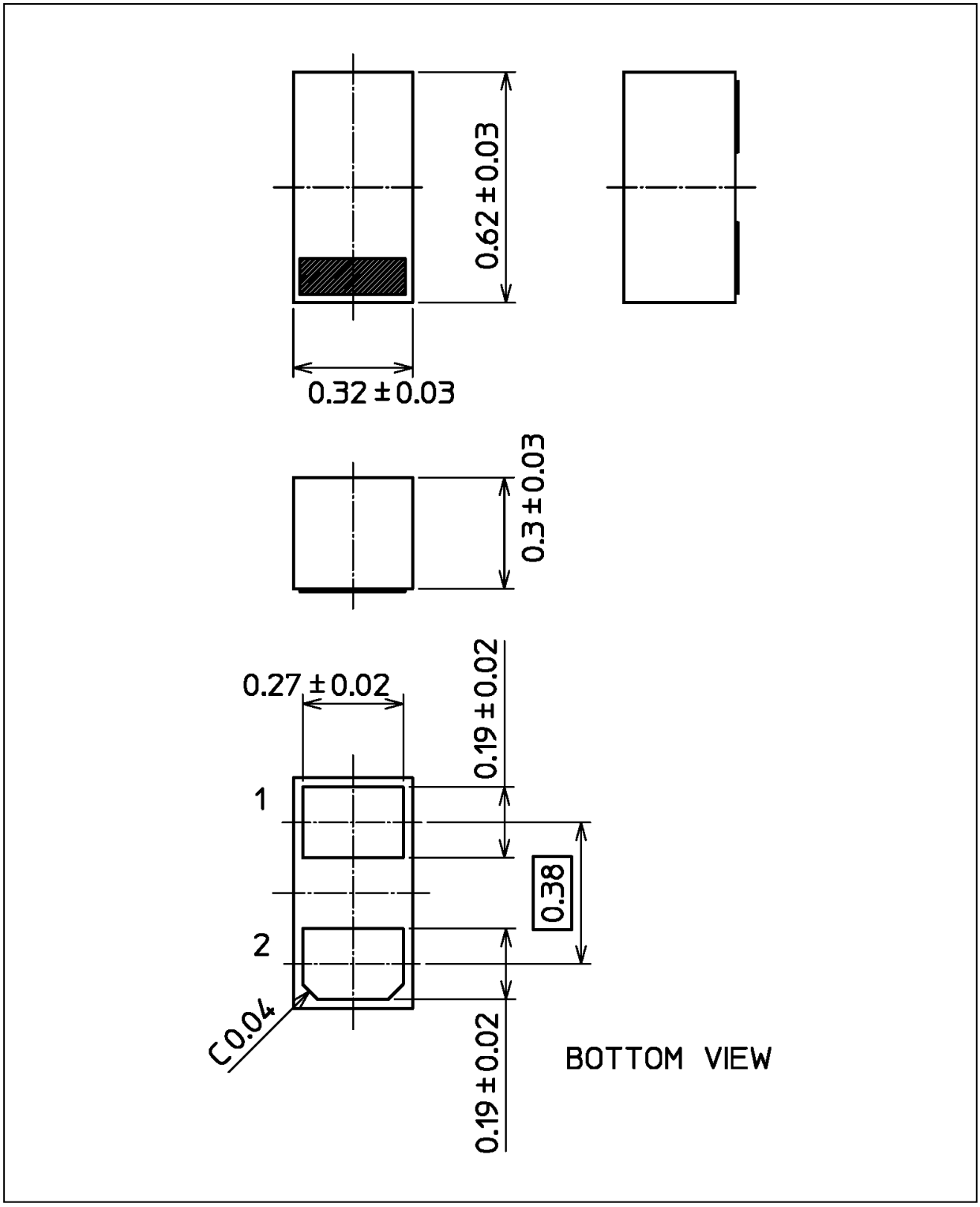



Fig. 11.3 IEC61000-4-2 (Contact)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

## Package Dimensions

Unit: mm




Weight: 0.17 mg (typ.)

| Package Name(s) |
|---|
| TOSHIBA: 1-1R1S |
| Nickname: SC2 |

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