ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089

NTE981
Integrated Circuit
Positive 3 Terminal Voltage Regulator, 100mA

Description:

The NTE981 is a positive 3–terminal voltage regulator available in a TO92 type package. With adequate heat sinking this device can deliver 100mA output current. Current limiting is included to limit peak output current to safe value. Safe area protection for the output transistors is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

When used as a zener diode/resistor combination replacement, the NTE981 usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. These regulators can provide local on card regulation, eliminating the distribution problems associated with single point regulation. Typical applications include use in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulator this device can be used with external components to obtain adjustment voltages and currents.

Features:

- Output Voltage Tolerances of ±5% over the Temperature Range
- Output Current of 100mA
- Internal Thermal Overload Protection
- Output Transistor Safe Area Protection
- Internal Short Circuit Current Limit

Absolute Maximum Ratings:

Output Voltage, V_{OUT} 8V
Input Voltage, V_{IN} 30V
Internal Power Dissipation (Note 1), P_D . . . . . Internally Limited
Operating Temperature Range, T_{opr} . . . . . 0°C to +70°C
Maximum Junction Temperature, T_J . . . . . +125°C
Storage Temperature Range, T_{stg} . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec), T_L . . . . . +260°C

Note 1. Thermal resistance is +180°C/W junction–to–ambient with 0.4” leads from a P.C. board and +160°C/W junction–to–ambient with 0.125” lead length to a P.C. board.

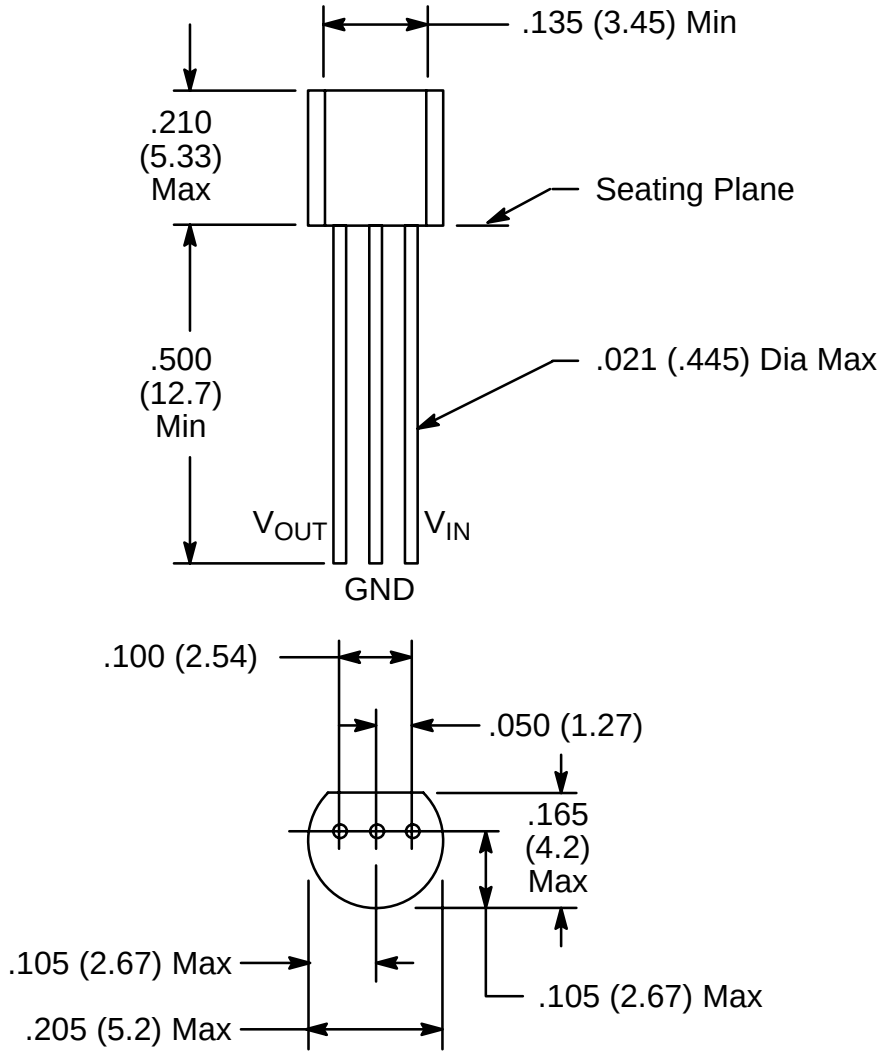
Electrical Characteristics: (T_J = 0° to +125°C, V_{IN} = 14V, I_O = 40mA, C_{IN} = 0.33µF, C_O = 0.1µF, Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage (Note 4)	V_O	T_J = +25°C	7.7	8.0	8.3	V
		1mA ≤ I_O ≤ 70mA	7.6	–	8.4	V
		1mA ≤ I_O ≤ 70mA	7.6	–	8.4	V
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(7 ≤ V_{IN} ≤ 20)			
Line Regulation	ΔV_O	T_J = +25°C	–	12	85	mV
			(11 ≤ V_{IN} ≤ 23)			V
			–	20	100	mV
			(10.5 ≤ V_{IN} ≤ 23)			V
Load Regulation	ΔV_O	T_J = +25°C, 1mA ≤ I_O ≤ 40mA	–	8	40	mV
		T_J = +25°C, 1mA ≤ I_O ≤ 100mA	–	25	80	mV
Long Term Stability	ΔV_O		–	20	–	$\frac{mV}{1000Hrs}$
Quiescent Current	I_Q	T_J = +25°C	–	3	5	mA
		T_J = +125°C	–	–	4.7	mA
Quiescent Current Change	ΔI_Q	1mA ≤ I_O ≤ 40mA	–	–	0.1	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	–	–	1.0	mA
			(11 ≤ V_{IN} ≤ 23)			V
Output Noise Voltage	V_n	T_J = +25°C, Note 3, f = 10Hz to 10kHz	–	60	–	µV
Ripple Rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	f = 120Hz	43	57	–	dB
			(12 ≤ V_{IN} ≤ 23)			V
Input Voltage Required to Maintain Line Regulation		T_J = +25°C	10.5	–	–	V

Note 2. The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of test.

Note 3. Recommended minimum load capacitance of 0.01µF to limit high frequency noise bandwidth.

Note 4. The temperature coefficient of V_{OUT} is typically within ±0.01% V_O/°C.


.135 (3.45) Min
.210
(5.33)
Max
Seating Plane
.500
(12.7)
Min
.021 (.445) Dia Max
V_{OUT}
V_{IN}
GND
.100 (2.54)
.050 (1.27)
.165
(4.2)
Max
.105 (2.67) Max
.105 (2.67) Max
.205 (5.2) Max