



2N65K

Power MOSFET

2A, 650V N-CHANNEL POWER MOSFET

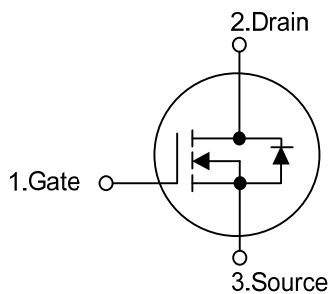
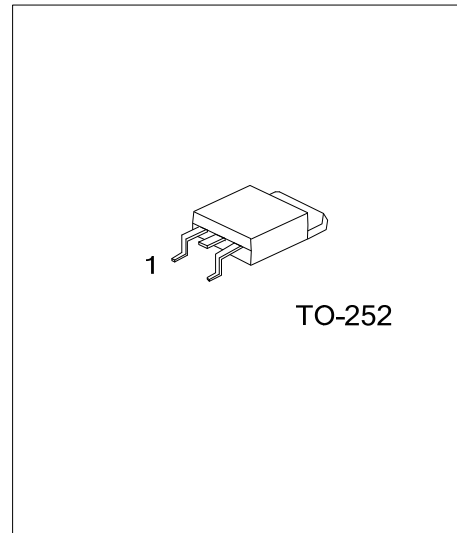
DESCRIPTION

The UTC **2N65K** is a high voltage power MOSFET and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in power supplies, PWM motor controls, high efficient DC to DC converters and bridge circuits.

FEATURES

- * $R_{DS(ON)} = 5.0\Omega @ V_{GS} = 10V$
- * Ultra Low gate charge (typical 9.0nC)
- * Low reverse transfer capacitance (C_{RSS} = typical 5.0 pF)
- * Fast switching capability
- * Avalanche energy specified
- * Improved dv/dt capability, high ruggedness

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
2N65KL-TN3-R	2N65KG-TN3-R	TO-252	G	D	S	Tape Reel
2N65KL-TN3-T	2N65KG-TN3-T	TO-252	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>2N65KL-TN3-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Lead Free</p>	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) TN3: TO-252</p> <p>(3) L: Lead Free, G: Halogen Free</p>
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■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	650	V
Gate-Source Voltage		V_{GSS}	± 30	V
Avalanche Current (Note 2)		I_{AR}	2.0	A
Drain Current	Continuous	I_D	2.0	A
	Pulsed (Note 2)	I_{DM}	8.0	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	60	mJ
	Repetitive (Note 2)	E_{AR}	4.5	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.5	V/ns
Power Dissipation		P_D	28	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Operating Temperature		T_{OPR}	-55 ~ +150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by T_J

3. $L=64\text{mH}$, $I_{AS}=2.0\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD}\leq 2.4\text{A}$, $di/dt\leq 200\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	4.53	$^\circ\text{C}/\text{W}$

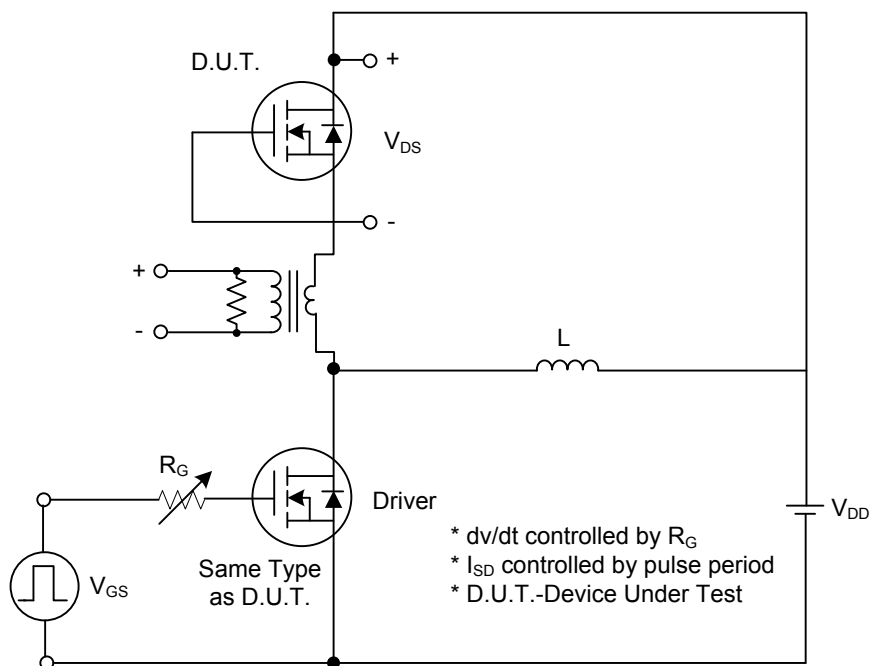
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} = 0V, I _D = 250μA	650			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} = 650V, V _{GS} = 0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} = 30V, V _{DS} = 0V			100	nA
	Reverse		V _{GS} = -30V, V _{DS} = 0V			-100	nA
Breakdown Voltage Temperature Coefficient		ΔBV _{DSS} /ΔT _J	I _D =250μA, Referenced to 25°C		0.4		V/°C
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250μA	2.0		5.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} = 10V, I _D =1A		5.0	6.0	Ω
DYNAMIC CHARACTERISTICS							
Input Capacitance		C _{ISS}	V _{DS} =25V, V _{GS} =0V, f =1MHz		270	350	pF
Output Capacitance		C _{OSS}			40	50	pF
Reverse Transfer Capacitance		C _{RSS}			5	7	pF
SWITCHING CHARACTERISTICS							
Turn-On Delay Time		t _{D (ON)}	V _{DD} =325V, I _D =2.4A, R _G =25Ω (Note 1, 2)		10	30	ns
Turn-On Rise Time		t _R			25	60	ns
Turn-Off Delay Time		t _{D (OFF)}			20	50	ns
Turn-Off Fall Time		t _F			25	60	ns
Total Gate Charge		Q _G	V _{DS} =520V, V _{GS} =10V, I _D =2.4A (Note 1, 2)		9.0	11	nC
Gate-Source Charge		Q _{GS}			1.6		nC
Gate-Drain Charge		Q _{GD}			4.3		nC
DRAIN-SOURCE DIODE CHARACTERISTICS							
Drain-Source Diode Forward Voltage		V _{SD}	V _{GS} = 0 V, I _{SD} = 2.0 A			1.4	V
Continuous Drain-Source Current		I _{SD}				2.0	A
Pulsed Drain-Source Current		I _{SM}				8.0	A
Reverse Recovery Time		t _{rr}	V _{GS} = 0 V, I _{SD} = 2.4A,		180		ns
Reverse Recovery Charge		Q _{RR}	di/dt = 100 A/μs (Note1)		0.72		μC

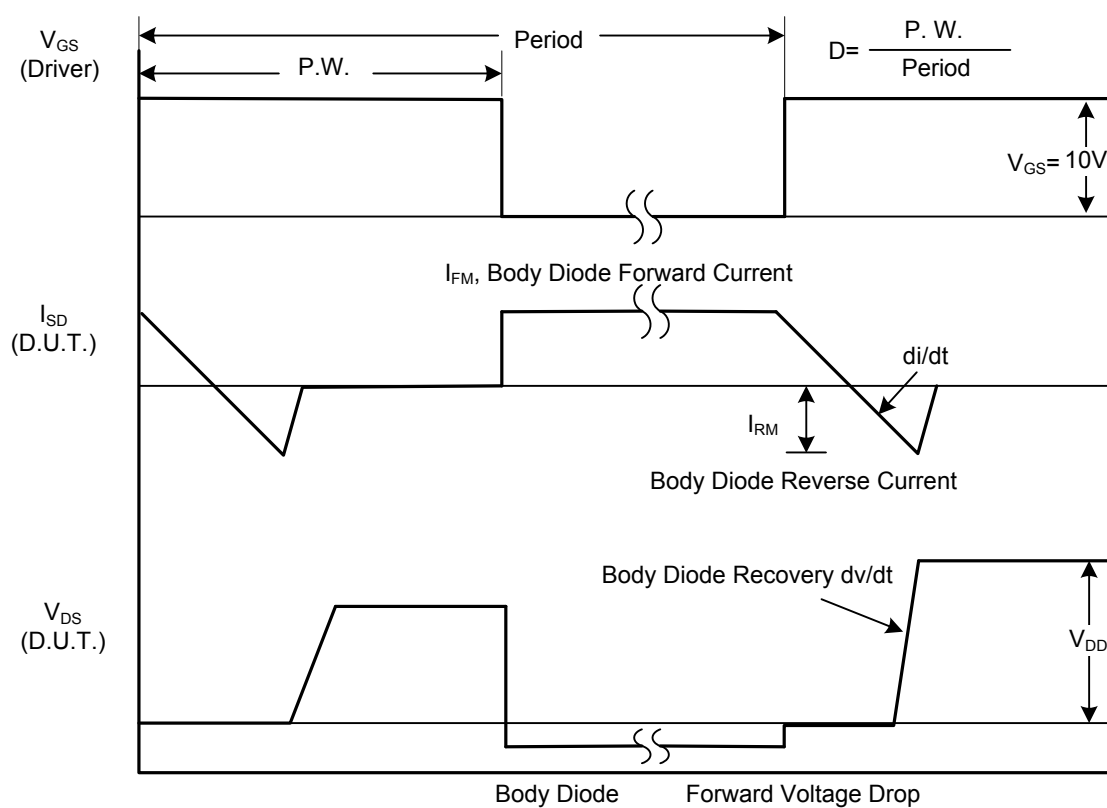
Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$

2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

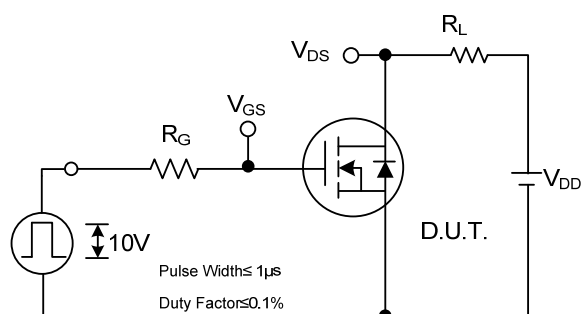


Peak Diode Recovery dv/dt Test Circuit

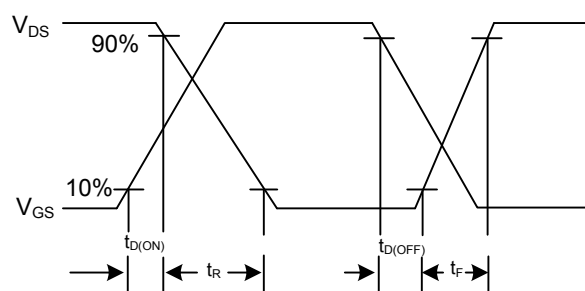


Peak Diode Recovery dv/dt Waveforms

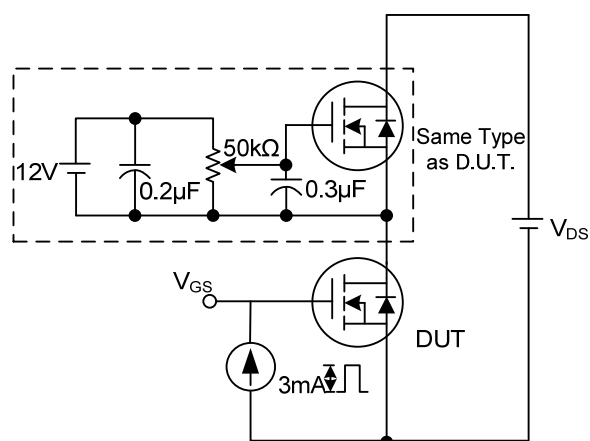
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



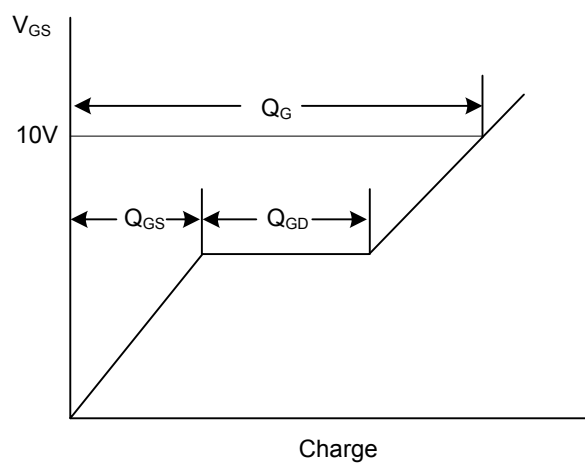
Switching Test Circuit



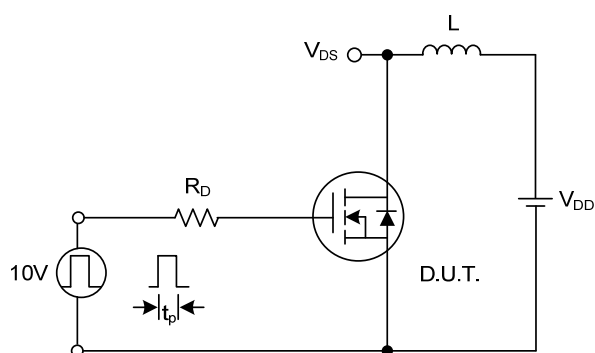
Switching Waveforms



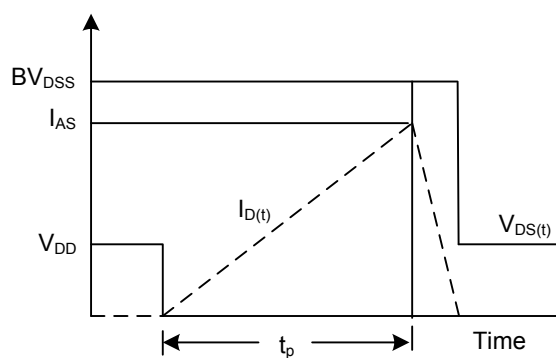
Gate Charge Test Circuit



Gate Charge Waveform

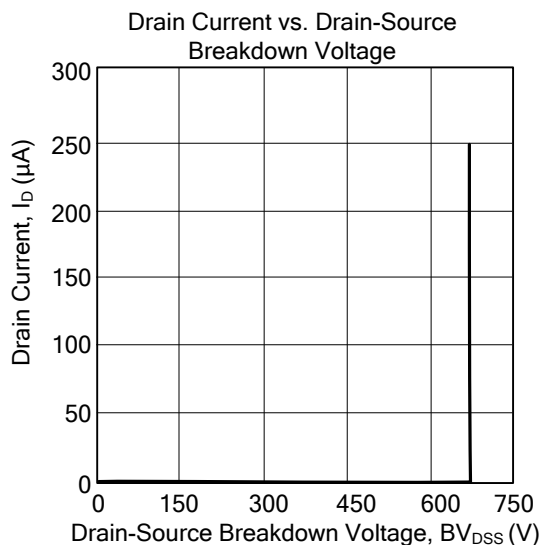
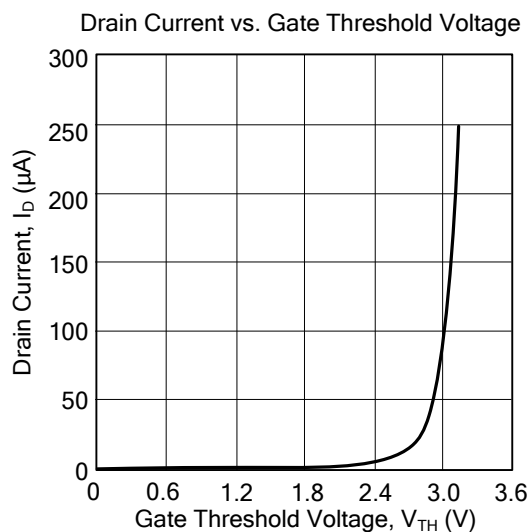
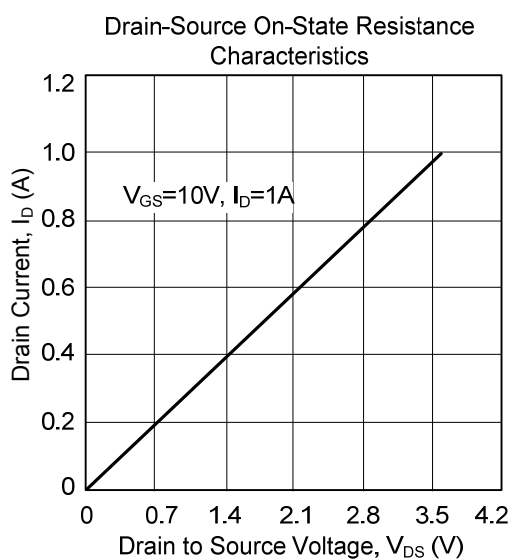
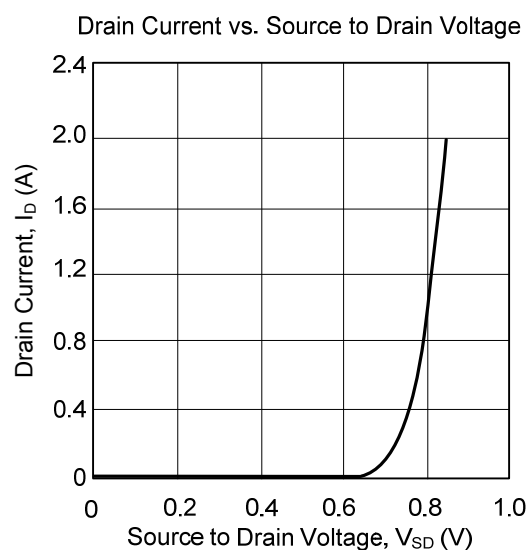


Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

TYPICAL CHARACTERISTICS



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