GENERAL DESCRIPTION

The XRT71D00 is a single channel, single chip Jitter Attenuator, that meets the Jitter transfer characteristic requirements specified in the ETSI TBR-24, Bellcore GR-499-CORE and GR-253-CORE standards.

In addition, the XRT71D00 also meets the Output Jitter and Wander specifications described in the ANSI T1.105.03b 1997, Bellcore GR-253-CORE and GR-499-CORE standards.

FEATURES

- Meets E3/DS3/STS-1 jitter transfer requirements
- No external components required
- Compliant with the jitter transfer characteristic requirements specified in ITU G.751, G.752, and G.755 for E3 applications
- Meets jitter transfer characteristic requirement as specified by ETSI TBR24 (for E3 applications).
- Meets the Output Jitter and Wander specifications described in ANSI T1.105.03b, Bellcore GR-253-CORE and Bellcore GR-499-CORE standards.
- Selectable buffer size of 16 and 32 bits
- Jitter attenuator can be disabled
- Available in a 32 pin TQFP package.
- Single 3.3V or 5.0V supply.
- Operates over - 40^0 C to 85^0 C temperature range.

APPLICATIONS

- E3/DS3 Access Equipment.
- DSLAMs

FIGURE 1. BLOCK DIAGRAM OF THE XRT71D00

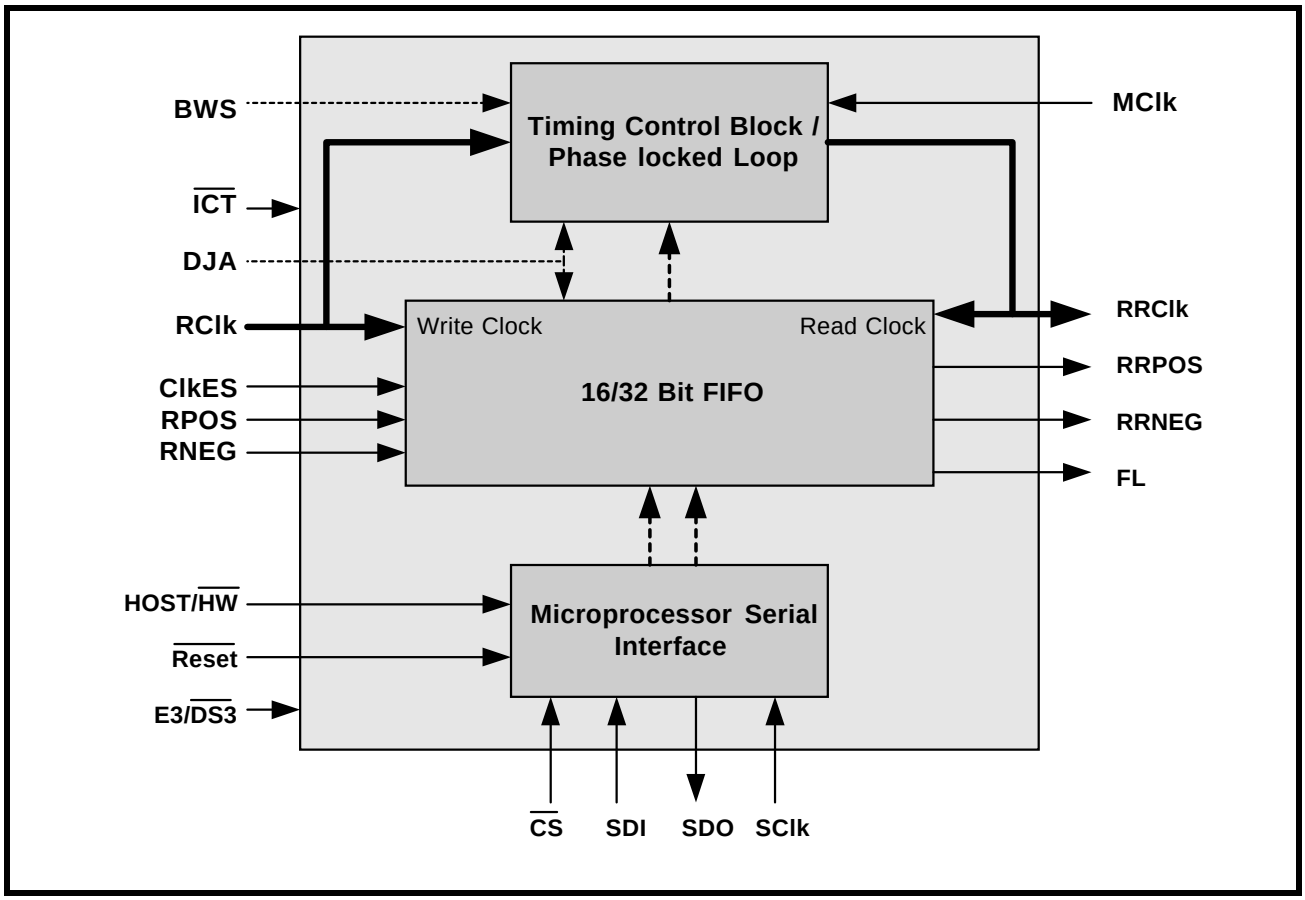
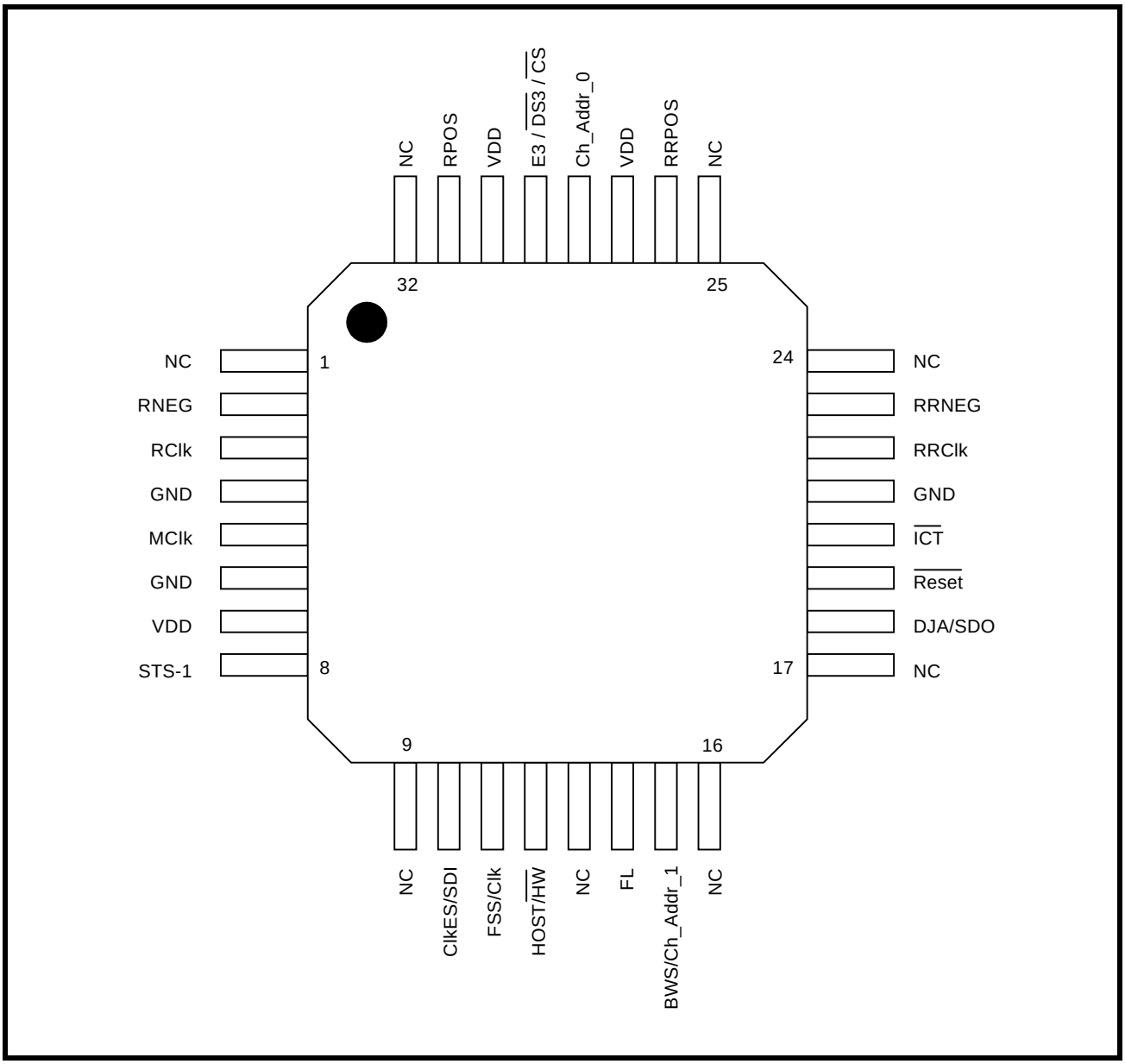


FIGURE 2. PIN OUT OF THE XRT71D00 (32 LEAD TFQP PACKAGE)



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT71D00IQ	32 Lead TQFP	-40^0C to $+85^0$C

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PIN DESCRIPTIONS

PIN DESCRIPTION

PIN #	NAME	TYPE	DESCRIPTION
1	NC	***	**This pin is not connected internally**
2	RNEG	I	**Receive Negative Data (Jittery) Input** The input jittery negative data is sampled either on the rising or falling edge of RClk depending on the setting of ClkES (pin 10). This data will ultimately be output via the RRNEG output pin. If ClkES is "high", then RNEG will be sampled on the falling edge of RClk. If ClkES is "low", then RPOS will be sampled on the rising edge of RClk. This pin is typically tied to the "RNEG" output pin of the LIU. ***NOTES:*** 1. *For "Jitter Attenuator" applications, this pin is typically connected to the "RNEG" output pin of the corresponding LIU IC.* 2. *The user should tie this input pin to "GND" for "SONET De-Synchronization" and "Single-Rail Jitter Attenuator" Applications.*
3	RClk	I	**Receive Clock (Jittery) Input** The user is expected to supply the "jittery" clock signal (e.g., the clock signal that needs to be "smoothed") to this input pin. **For Jitter Attenuation Applications:** The user should connect the "Recovered Line Clock" (RCLK) output signal (of the DS3, E3 or STS-1 LIU IC) to this input pin. **For SONET De-synchronizer Applications:** The user should connect the "Receive DS3 Output" clock signal (of the OC-N to DS3 Mapper/De-Mapper IC) to this input pin. The XRT71D00 device will use this clock signal to latch the data, residing on the "RPOS" and "RNEG" input pins, into the chip. If the "CLKES" input pin (or bit-field) is "high", then the XRT71D00 device will sample the data on the "RPOS" and "RNEG" input pins, on the falling edge of the "RCLK" clock signal. If the "CLKES" input pin (or bit-field) is "low", then the XRT71D00 device will sample the data on the "RPOS" and "RNEG" input pins, on the rising edge of the "RCLK" clock signal.
4	GND	***	Digital Ground
5	MClk	I	**Master Clock Input.** This input pin functions as the reference clock for the internal PLL. The user is expected to apply a 44.736MHz+/-20ppm (for DS3 applications), 34.368MHz+/-20ppm (for E3 applications) or a 51.84MHz+/- 20ppm (for STS-1 applications) to this input pin. This clock must be continuous and jitter free with duty cycle between 30 to 70%.
6	GND	***	Analog Ground
7	VDD	***	**Analog Positive Supply**: 3.3V or 5.0V ± 5%

PIN DESCRIPTION

PIN #	NAME	TYPE	DESCRIPTION
8	STS-1	I	**SONET STS-1 Mode Select:** This pin along with the E3/DS3* select pin (pin 29) configures the XRT71D00 either in E3, DS3 or STS-1 mode. A table relating the setting of these two input pins to the operating modee of the XRT71D00 device is given below: **STS-1 / E3/DS3* / XRT71D00 Operating Mode** 0 / 0 / DS3 (44.736 MHz) 0 / 1 / E3 (34.368 MHz) 1 / 0 / STS-1 (51.84 MHz) 1 / 1 / E3 (34.368 MHz) ***NOTES:*** *1. For "SONET De-Synchronization" Applications, the user should configure the XRT71D00 device to operate in the "DS3" Mode.* *2. This input pin is active only in the Hardware Mode* *3. This pin contains an Internal 50 K Ohm pull-up resistor.*
9	NC	***	**This pin is not connected internally**

PIN DESCRIPTION

PIN #	NAME	TYPE	DESCRIPTION
10	ClkES/(SDI)	I	**Clock Edge Select Input/Serial Data Input Pin.** The function of this pin depends on whether XRT71D00 is configured in Harware or Host Mode. **Hardware Mode—Clock Edge Select Input** This input pin permits the user to do the following. **1.** To configure the XRT71D00 device to latch the data, on the RPOS and RNEG input pin, upon either the rising or falling edge of the RCLK input signal. **2.** To configure the XRT71D00 device to update the data, which is output via the "RRPOS" and "RRNEG" pins, upon either the rising or falling edge of the RRCLK output signal. Setting this input pin LOW configures the XRT71D00 device to do the following. **1.** Sample and latch the RPOS and RNEG input signals upon the rising edge of the RCLK input signal. **2.** Update the data, output via the RRPOS and RRNEG output pins, upon the falling edge of the RRCLK output signal. Conversely, setting this input pin HIGH configures the XRT71D00 device to do the following. **1.** Same and latch the RPOS and RNEG input signals upon the falling edge of the RCLK input signal. **2.** Update the data, output via the RRPOS and RRNEG output pins, upon the rising edge of the RRCLK output signal. **Host Mode—Serial Data Input** When the Microprocessor/Microcontroller is executing a READ operation, with the Microprocessor Serial Interface (of the XRT71D00 device) then it is expected to apply the address value (of the "Target" Command Register) to this input pin, in a serial manner. When the Microprocessor/Microcontroller is executing a WRITE operation, with the Microprocessor Serial Interface, then it is expected to do the following. **1.** Apply the address value (of the "Target" Command Register) to this input pin, in a serial manner. **2.** Apply the data (to be written into the "Target" Command Register) to this input pin. ***NOTE:*** *A detailed description on how to read and write data into the Command Registers of the XRT71D00 device (via the Microprocessor Serial Interface) is presented in Section _.*
11	FSS/(SClk)	I	**FIFO Size Select Input/Serial Clock Input.** The function of this input pin depends on whether XRT71D00 is configured in Hardware or Host mode. **Hardware Mode—FIFO Size Select Input** This input pin permits the user to select the operating depth of the "on-chip" FIFO. When high: Selects 32 bits FIFO. When low: Selects 16 bits FIFO. ***NOTE:*** *For SONET De-synchronizer applications, the user is advised to configure the FIFO Depth to 32 bits.* **Host Mode—Microprocessor Serial Interface Clock Signal** This signal will be used to sample the data, on the SDI pin, on the rising edge of this signal. Additionally, during "Read" operations, the Microprocessor Serial Interface will update the SDO output on the falling edge of this signal.

PIN DESCRIPTION

PIN #	NAME	TYPE	DESCRIPTION
12	HOST/$\overline{HW}$	I	**Host/Hardware Mode Select:** This input pin permits the user to configure the XRT71D00 device to operate in either the "Host" or "Hardware" Mode. Setting this input pin "high" configures the XRT71D00 device to operate in the "Host" Mode (e.g., enables the Microprocessor Serial Interface). In this mode, the user is expected to configure the XRT71D00 device by writing data into the "on-chip" Command Registers via the Microprocessor Serial Interface. As a consequence, when the XRT71D00 device is operating in the "Host" Mode, then it will ignore the states of many of the discrete input pins. Setting this input pin "low" configures the XRT71D00 device to operate in the "Hardware" Mode. When the XRT71D00 device is operating in the "Hardware" Mode, then the Microprocessor Serial Interface will be disabled. In this mode, many of the external input control pins will be functional.
13	NC	***	**This pin is not connected internally.**
14	FL	O	**FIFO Limit Alarm Output Indicator.** This output pin is driven high whenever the internal FIFO comes within two-bits of being completely full or completely depleted. When this output pin is asserted, it will be driven "high" for at least one "RRCLK" cycle period.
15	BWS/ Ch_Addr_1	I	**Bandwidth Select Input/Channel Addr_1 Assignment Input.** The function of this input pin depends on whether XRT71D00 is configured in Host or Hardware mode. **Hardware Mode—Bandwidth Select Input:** This input pin permits the user to configure the PLL (within the XRT71D00 device) to operate with either a wide or narrow bandwidth. Setting this input pin "high" configures the PLL to operate with a wide bandwidth Conversely, setting this input pin "low" configures the PLL to operate with a "narrow-bandwidth". **Host Mode—Channel_Addr_1 Assignment Input:** This input pin, along with pin 28 permits the user to assign a "Channel Address" to the XRT71D00 device. ***NOTE:*** *A detailed discussion on "Channel Assignment" is presented in Section _.*
16	NC	***	**This pin is not connected internally.**
17	NC	***	**This pin is not connected internally.**

PIN DESCRIPTION

PIN #	NAME	TYPE	DESCRIPTION
18	DJA/ (SDO)	I/(O)	**Disable Jitter Attenuator Input/Serial Data Output pin:** The function of this pin depends on whether XRT71D00 is configured in Host or Hardware mode. **Hardware Mode—Disable Jitter Attenuator:** This input pin permits the user to enable or disable the Jitter Attenuator function within the XRT71D00 device. Setting this input pin "high" disables the jitter attenuator PLL. Whenever the Jitter Attenuator PLL is disabled, the the signals/data which are applied to the "RPOS", "RNEG" and "RCLK" input pins will pass through to the "RRPOS", "RRNEG" and "RRCLK" output pins without any jitter attenuation. Setting this input pin "low" enables the Jitter Attenuator" PLL. Whenever the Jitter Attenuator PLL is enabled then the signals/data which are applied to the "RPOS", "RNEG" and "RCLK" output pins will be routed to the "Narrow-band" PLL for jitter reduction. The outputs of the narrow-band PLL will be routed to the "RRPOS", "RRNEG" and "RRCLK" output pins. **Host Mode—Serial Data Output:** This pin will serially output the contents of the specified Command Register, during "Read" Operations. The data, on this pin, will be updated on the falling edge of the SClk input signal. This pin will be tri-stated upon completion of data transfer.
19	$\overline{\text{Reset}}$	I	**Reset Input.** (Active-Low) A high-to-low transition will re-center and clear the contents of the internal FIFO, and will clear the contents of the Command Registers (for Host Mode operation). Resetting this pin may corrupt data within the device. ***NOTE:*** *For normal operation, this pin should be pulled "HIGH".*
20	$\overline{\text{ICT}}$	I	**In Circuit Testing Input.** Active low. With this pin tied to ground, all output pins will be in high impedance mode for in-circuit-testing. ***NOTE:*** *For normal operation this input pin should be pulled "HIGH".*
21	GND	***	Digital Ground:
22	RRClk	O	**Receive Output (De-jittered) Clock.** This pin outputs the "smoothed" (e.g., de-jittered) 34.368MHz, 44.736MHz or 51.84MHz clock signal. Further, this clock signal is also used to clock out the contents of the "Recovered" data (via the "RRPOS" and "RRNEG" output pins). If the "CLKES" pin (or bit-field) is "low", then the XRT71D00 device will output data, via the "RRPOS" and "RRNEG" output pins, upon the falling edge of this clock signal. If the "CLKES" pin (or bit-field) is "high", then the XRT71D00 device will output data, via the "RRPOS" and "RRNEG" output pins, upon the rising edge of this clock signal.
23	RRNEG	O	**Receive Negative Data (De-Jittered) Output.** Data which is input via the "RNEG" input pin will be updated on the rising or falling edge of RRClk, depending upon the state of the ClkES input pin (or bit-field setting).
24	NC	***	**This pin is not connected internally.**
25	NC	***	**This pin is not connected internally.**

PIN DESCRIPTION

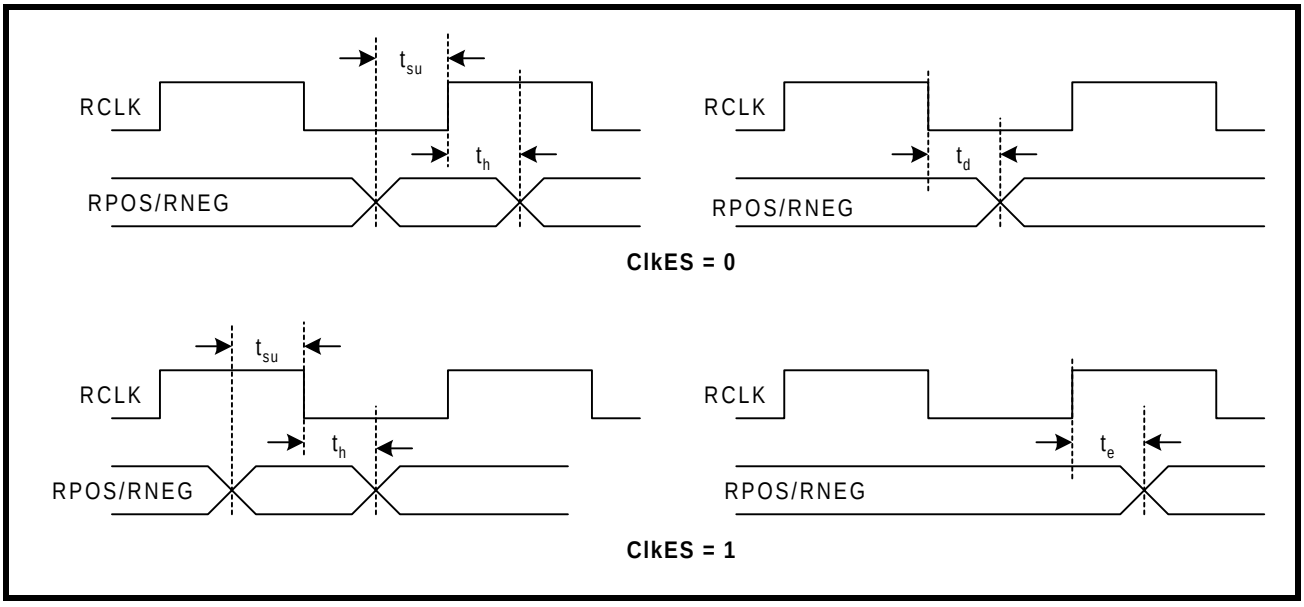
PIN #	NAME	TYPE	DESCRIPTION
26	RRPOS	O	**Receive Positive Data (De-Jittered) Output.** Data which is input via the "RPOS" input pin will be updated on the rising or falling edge of RRClk (see pin 9), depending upon the state of the ClkES input pin (or bit-field setting).
27	VDD	***	**Digital Positive Supply Voltage**: 3.3V or 5.0V ± 5%
28	Ch_Addr_0	I	**Channel Addr_0 Assignment Input.** This input pin, along with pin 15 permits the user to assign a "Channel Address" to the XRT71D00. ***NOTES:*** *1. A detailed discussion on "Channel Assignment" is presented in Section _.* *2. This input pin is only active whenever the XRT71D00 device has been configured to operate in the "Host" Mode.*
29	E3/$\overline{DS3}$ ($\overline{CS}$)	I	**E3/DS3 Select Input/Chip Select Input:** The function of this pin depends on whether the XRT71D00 is configured in Host or Hardware mode. **Hardware Mode—E3/DS3* Select Input**: This pin along with the STS-1 mode select pin (pin 8) selects the operating mode. A table relating the settings of these two input pins to the operatintg mode of the XRT71D00 device is given below.: **STS-1 / E3/DS3* / XRT71D00 Operating Mode** 0 / 0 / DS3 (44.736 MHz) 0 / 1 / E3 (34.368 MHz) 1 / 0 / STS-1 (51.84 MHz) 1 / 1 / E3 (34.368 MHz) ***NOTE:*** *For SONET De-synchronization applications, the user should configure the XRT71D00 device to operate in the DS3 Mode.* **HOST Mode—Chip Select Input:** The local microprocessor must assert this input pin (e.g., set it to "0") in order to enable communication with the XRT71D00 device, via the MIcroprocessor Serial Interface.
30	VDD	***	**Digital Positive Supply Voltage**: 3.3V or 5.0V ± 5%
31	RPOS	I	**Receive Positive Data (Jittery) Input.** Data that is input on this pin is sampled on either the rising or falling edge of RClk depending on the setting of the ClkES pin (pin 10). This data will ultimately be output via the "RRPOS" output pin. If ClkES is "high", then RPOS will be sampled on the falling edge of RClk. If ClkES is "low", then RPOS will be sampled on the rising edge of RClk. ***NOTE:*** *For "Jitter Attenuation" Applications, this pin is typically connected to the "RPOS" output pin of the corresponding LIU IC.*
32	NC	***	**This pin is not connected internally.**

ELECTRICAL CHARACTERISTICS

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS.
MClk	Duty Cycle	30	50	70	%
MClk	Frequency E3		34.368		MHz
MClk	Frequency DS3		44.736		MHz
MClk	Frequency STS-1		51.84		MHz
RClk	Duty Cycle	30	50	70	%
RClk	Frequency (E3,DS3 or STS-1)	-400	0	400	ppm
RClk	Rise/Fall Time E3 DS3 STS-1			 11.6 8.96 7.68	 ns ns ns
tsu	RPOS/RNEG to RClk rise time setup	3	2		ns
th	RPOS/RNEG to RClk rising hold time	3	2		ns
td	RRPOS/RRNEG delay from RRClk rising		3	5	ns
te	RRPOS/RRNEG delay from RRClk falling		3	5	ns

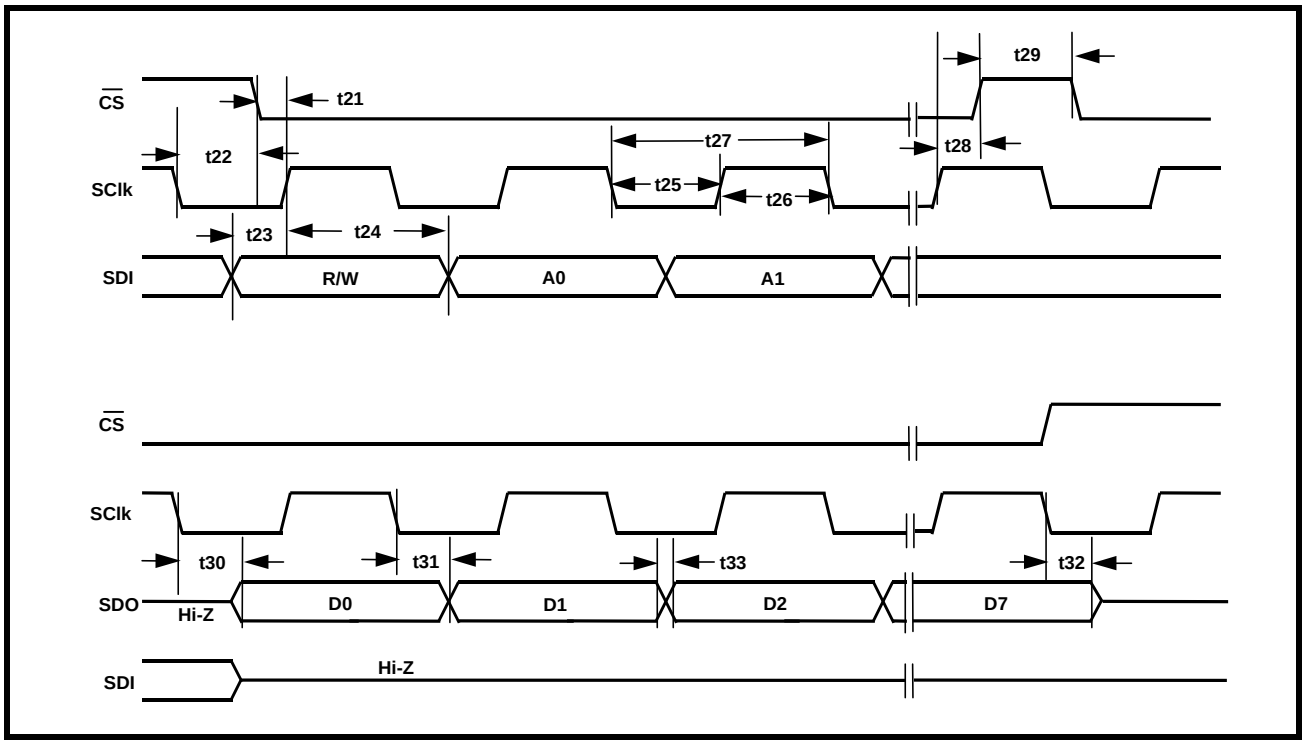
FIGURE 3. INPUT/OUTPUT TIMING



MICROPROCESSOR SERIAL INTERFACE TIMING (SEE FIGURE 4)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS.
t21	$\overline{CS}$ Low to Rising Edge of SClk Setup Time	50			ns
t22	SClk to $\overline{CS}$ Hold Time	20			ns
t23	SDI to Rising Edge of SClk Setup Time	50			ns
t24	SDI to Rising Edge of SClk Hold Time	50			ns
t25	SClk "Low" Time	240			ns
t26	SClk "High" Time	240			ns
t27	SClk Period	500			ns
t28	SClk to $\overline{CS}$ Hold Time	50			ns
t29	$\overline{CS}$ "Inactive" Time	250			ns
t30	Falling Edge of SClk to SDO Valid Time			200	ns
t31	Falling Edge of SClk to SDO Invalid Time			100	ns
t32	Falling Edge of SClk, or rising edge of $\overline{CS}$ to High Z		100		ns

FIGURE 4. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE



DC Electrical Characteristics (TA = 25 0C, VDD = 3.3 V ± 5 % unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	VDD	3.135	3.3	3.465	V
Input High Voltage	VIH	2.0		5.25	V
Input Low Voltage	V_{IL}	-0.5		0.8	V
Output High Voltage @ IOH=-5mA	VOH	2.4			V
Output Low Voltage @ IOL=5mA	VOL			0.4	V
Supply Current (E3)	Icc		25	40	mA
Supply Current (DS3)	Icc		30	45	mA
Supply Current (STS-1)	Icc		35	50	
Input Leakage Current(except Input pins with Pull-up resistor.	IL			± 10	µA
Input Capacitance	CI		5.0		pF
Output Load Capacitance	C_L			25	pF

DC Electrical Characteristics (TA = 25 0C, VDD = 5.0 V ± 5 % unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	VDD	4.75	5.0	5.25	V
Input High Voltage	VIH	2.0		5.25	V
Input Low Voltage	V_{IL}	-0.5		0.8	V
Output High Voltage @ IOH=-5mA	VOH	2.4			V
Output Low Voltage @ IOL=5mA	VOL			0.4	V
Supply Current (E3)	Icc		35	50	mA
Supply Current (DS3)	Icc		45	60	mA
Supply Current (STS-1)	Icc		50	65	
Input Leakage Current(except Input pins with Pull-up resistor.	IL			± 10	µA
Input Capacitance	CI		5.0		pF
Output Load Capacitance	C_L			25	pF

ABSOLUTE MAXIMUM RATINGS:

Supply Range	-0.5 V to + 6.0 V
ESD Rating	> 2000 V on all pins
Operating Temperature	-40^0C to $+85^0$C
Storage Temperature	-65°C to + 150°C

SYSTEM DESCRIPTION

The XRT71D00 is a fully integrated and self-contained DS3, E3 and STS-1 Jitter Attenuator IC which was designed to function as either a "Jitter Attenuator" or as a "Clock Smoother" within SONET De-Synchronizer applications.

More specifically, the XRT71D00 device was designed to do the following.

1. To attenuate the Jitter (of the incoming clock and data) such that the user's system will comply with the following jitter transfer characteristic requirements.
   - ETSI TBR-24 (for E3 applications)
   - ITU-T G.751 (for E3 applications)
   - ITU-T G.752 (for E3 applications)
   - ITU-T G.755 (for E3 applications)
   - Bellcore GR-499-CORE (Category I to Category II Interface Jitter Transfer Characteristic requirements for DS3 applications).
   - Bellcore GR-253-CORE (for SONET STS-1 applications)
2. To receive the gapped 51.84MHz clock and data signals, from an "OC-N to DS3 Mapper/De-Mapper" IC; and to smooth these signals to an "ungapped" 44.736MHz clock and data signals. This particular application is often referred to as a "SONET De-synchronizer" application. In this application, the "smoothed" RRCLK and RRPOS signals could (potentially) be routed to a DS3 LIU IC, for transmission to a remote terminal equipment, over coaxial cable.

In addition, the XRT71D00 also meets both the "mapping" and "pointer adjustment" jitter generation criteria for both Category I and Category II interfaces as specified in Bellcore GR-253.

The XRT71D00 also meets the DS3 wander specification that apply to SONET and asynchronous interfaces as specified in the ANSI T1.105.03b 1997 standard.

Figure 5 presents a simple block diagram of the XRT71D00 device, when it is configured to operate in the "Hardware" Mode. Likewise Figure 6 presents a simple block diagram of the XRT71D00 device, when it is configured to operate in the "Host" Mode.

FIGURE 5. ILLUSTRATION OF THE XRT71D00 (CONFIGURED TO OPERATE IN THE "HARDWARE" MODE)

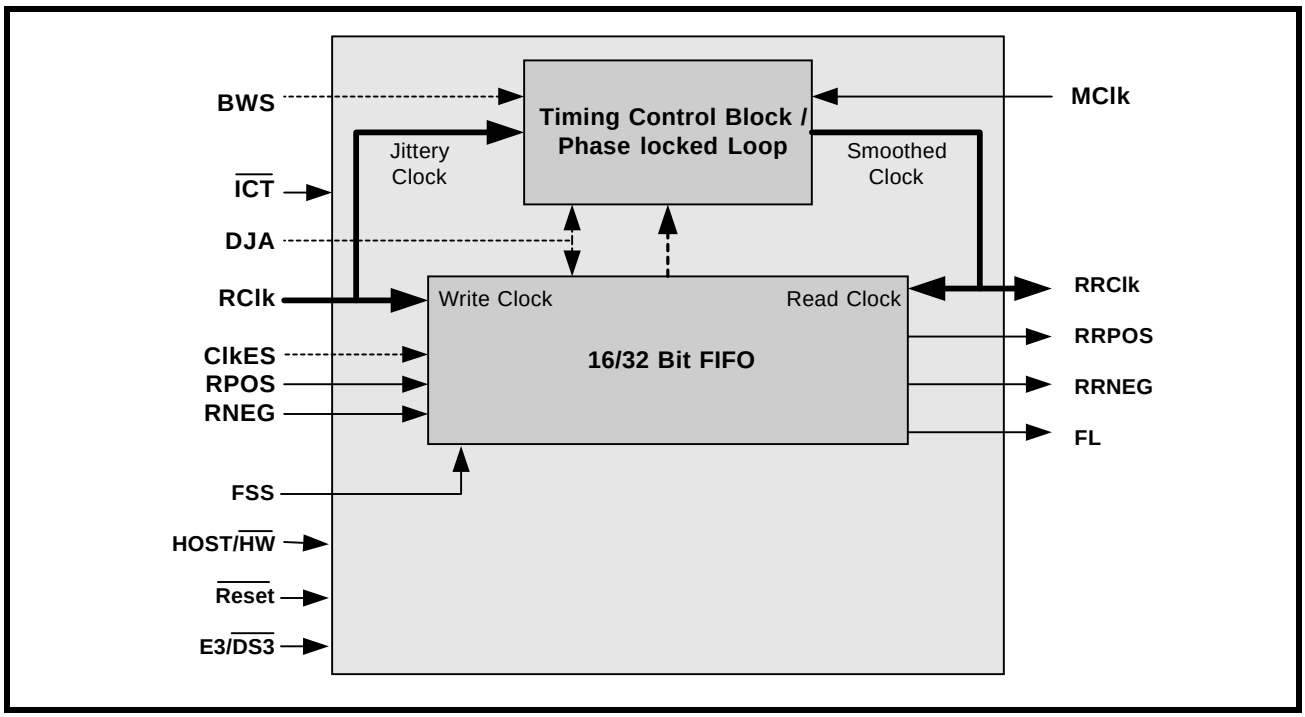
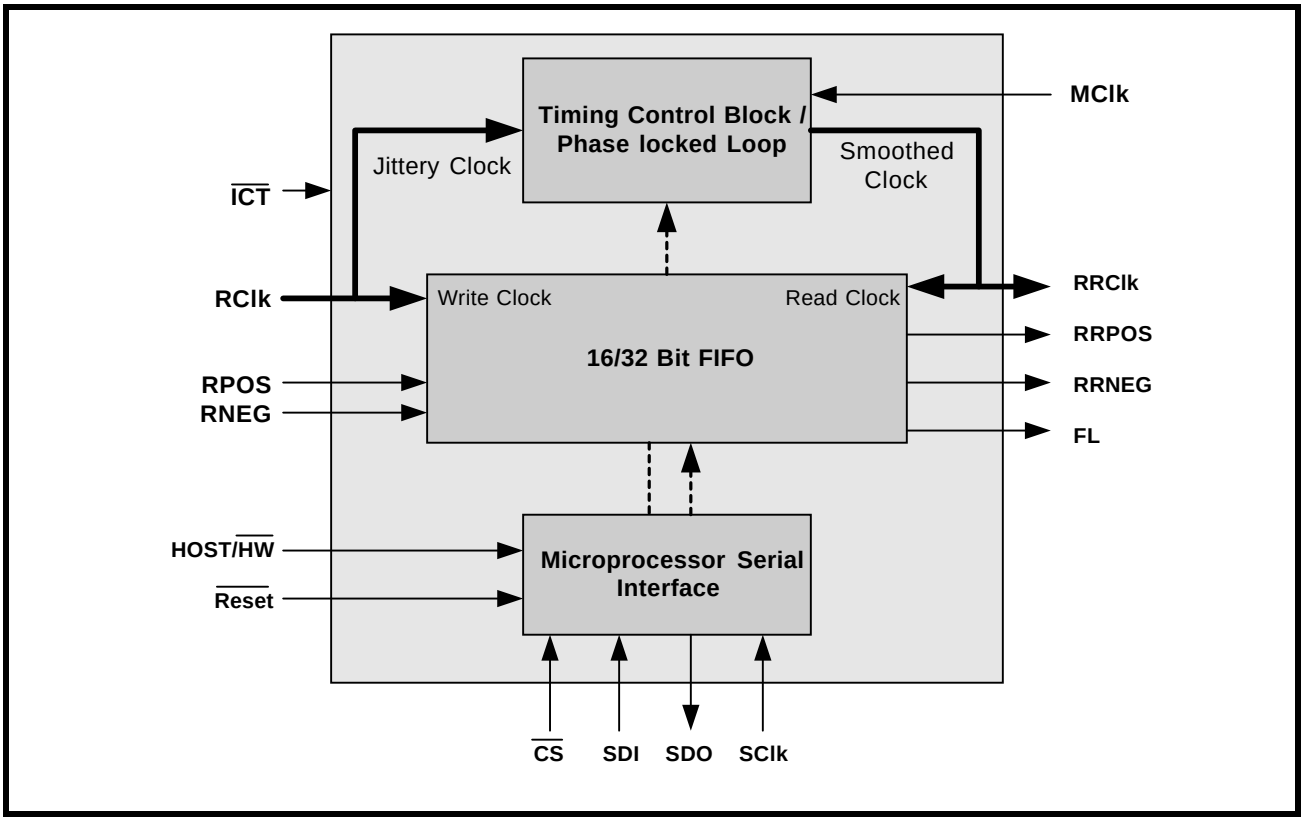


FIGURE 6. ILLUSTRATION OF THE XRT71D00 (CONFIGURED TO OPERATE IN THE "HOST" MODE)



The XRT71D00 DS3/E3/STS-1 Jitter Attenuator IC consists of the following functional blocks:

- Jitter Attenuator Phase Locked Loop(PLL)
- Timing Control
- 2-Channel 16/32 Bit FIFO.
- Microprocessor Serial Interface

1.0 THE JITTER ATTENUATOR PLL

The Jitter Attenuator PLL is a narrow-band PLL that accepts a "jittery" clock signal via the RCLK input pin. The Jitter Attenuator PLL locks onto the RCLK input signal and synthesizes a "same-rate" signal. As the Jitter Attenuator PLL synthesizes this signal, it eliminates much of the jitter that exists within the RCLK input signal. The resulting smoothed clock signal is then output via the "RRCLK" output signal.

1.1 THE JITTER TRANSFER CHARACTERISTICS OF THE JITTER ATTENUATOR PLL

The Jitter Transfer Characteristics of the XRT71D00 device is ultimately dictated by the Jitter Transfer Characteristics of the Jitter Attenuator PLL. The Jitter Transfer Characteristics of the Jitter Attenuator PLL is dictated by the following variables.

1. The operating mode/data rate of the XRT71D00 device.
2. The setting of the BWS (Bandwidth Select) input pin or bit-field.

1.2 DEFINITION OF JITTER

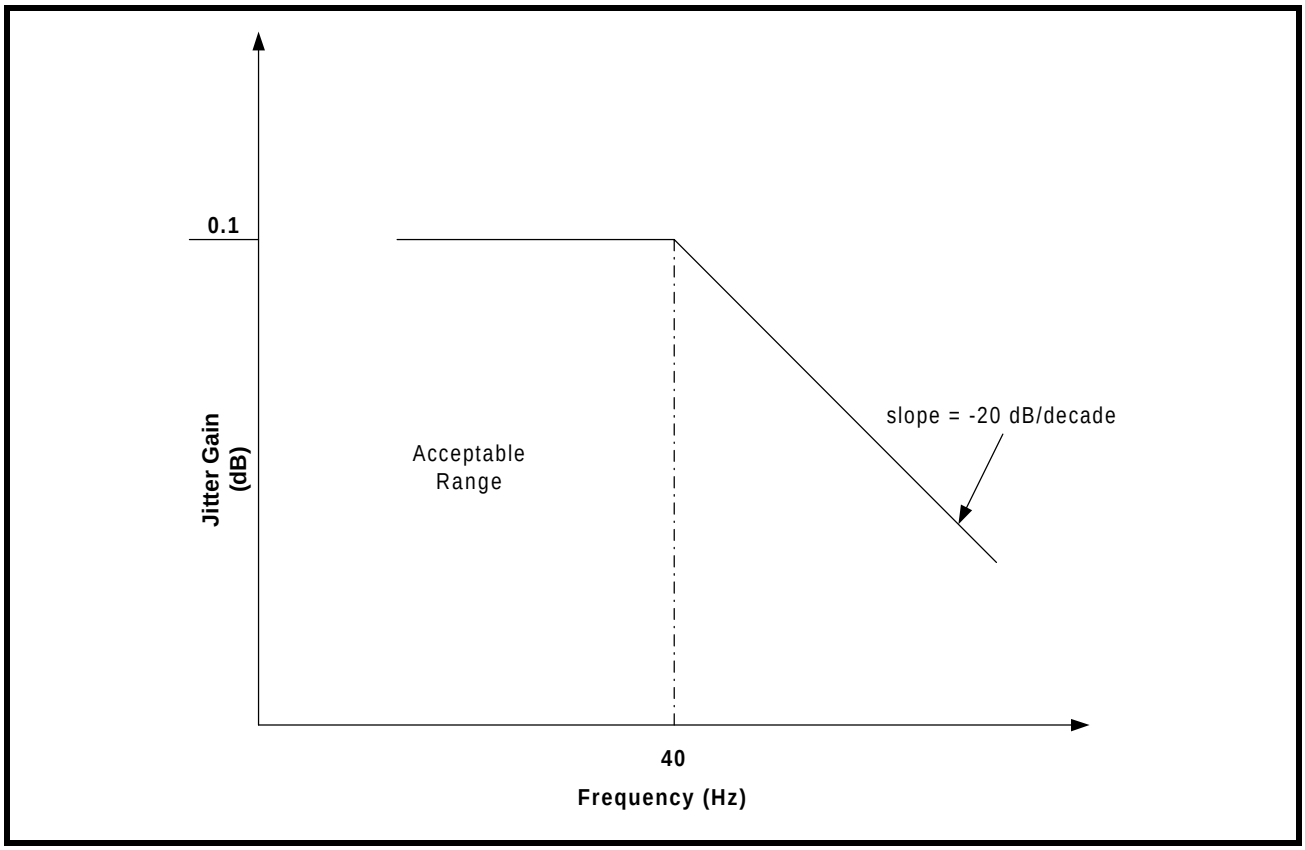
One of the most important and least understood measures of clock performance is jitter. The International Telecommunication Union defines jitter as "short term variations of the significant instants of a digita signal from their ideal positions in time". Jitter can occur due to any of the following:

1) Imperfect timing recovery circuit in the system
2) Cross-talk noise
3) Inter-symbol interference/Signal Distortion

1.3 JITTER TRANSFER CHARACTERISTICS

The primary purpose of jitter transfer requirements is to prevent performance degradations by limiting the accummulation of jitter through the system such that it does not exceed the network interface jitter requirements. Thus, it is more important that a system meet the jitter transfer criteria for relatively high input jitter amplitudes. The jitter transferred through the system must be under the jitter mask for any input jitter amplitude within the range as shown in Figure 7

FIGURE 7. CATEGORY 1 DS3 JITTER TRANSFER MASK



1.3.1 Jitter Tolerance:

The jitter tolerance in the network element is defined as the maximum amount of jitter in the incoming signal that it can receive in an “error-free”manner.

1.3.2 Jitter Generation:

Jitter generation is defined in Section 7.3.3 of GR-499-CORE. Jitter generation criteria exists for both Category I and II interfaces, which consist of “mapping” and “pointer adjustment” jitter generation.

Mapping jitter is the sum of the intrinsic payload mapping jitter and the jitter that is generated as a result of the bit stuffing mechnisms used in all of the asynchronous DSn mapping into STS SPE.

1.3.3 Jitter Attenuation:

A digital Jitter Attenuation loop combined with the FIFO provides Jitter attenuation. The Jitter Attenuator requires no external components except for the reference clock.

Data is clocked into the FIFO with the associated clock signal (TClk or RClk) and clocked out of the FIFO with the dejittered clock and data. When the FIFO is within 2 bits of being completely full, the FIFO Limit (FL) will be set.

In Figure 5 and Figure 6, this “de-jittered” clock is labeled “Smoothed Clock”. This “Smoothed Clock” is now used to “Read Out” the “Recovered Data” from the 16/32 bit FIFO. This “Smoothed Clock” will also be output to the Terminal Equipment via the “RRClk” output pin. Likewise, the “Smoothed Recovered Data” will output to the Terminal Equipment via the RRPOS and RRNEG output pins.

The XRT71D00 device is designed to work as a companion device with XRT73L00 (STS-1/DS3/E3) Line Interface Unit.

ETSI TBR24 specifies the maximum output jitter in loop timing must be no more than 0.4UIpp when measured between 100Hz to 800KHzwith upto 1.5UI input jitter at 100Hz. This means a jitter attenuator with bandwidth less than 100Hz is required to be compliant with the standard. ITU G.751 is another application where low bandwidth jitter attenuator is needed to smooth the gapped clock output in the de-multiplexer system.

1.4 XRT71D00 JITTTER TRANSFER CHARACTERISTICS

Table 1 and Table 2 summarizes the results of jitter transfer characteristics testing, performed on the

XRT71D00. Figure 8, Figure 9 and Figure 10 are graphs of the measure jitter transferr function of the XRT71D00. Table 3 and Table 4 summarize the results of jitter tolerance testing, performed on the XRT71D00.

TABLE 1: XRT71D00 JITTER TRANSFER FUNCTION

APPLICATION	DS3				E3			
BWS	LOW	HIGH	LOW	HIGH	LOW	HIGH	LOW	HIGH
INPUT JITTER	1UIPP		10UIPP		1UIPP		10UIPP	
FREQ. (HZ)	Jitter Gain (dB)				Jitter Gain (dB)			
5	0.02	-0.33	0.36	0.06	0.44	0.37	0.83	0.04
10	-0.10	-0.10	-0.30	-0.01	-0.15	0.20	-0.22	-0.02
20	-2.04	-0.24	-2.24	-0.13	-3.16	0.35	-3.24	-0.32
30	-3.63	-0.35	-4.33	-0.36	-5.51	0.05	-5.93	-0.73
40	-5.98	-0.53	-6.16	-0.72	-7.68	-0.68	-7.99	-1.24
50	-7.55	-1.00	-7.82	-1.12	-10.36	-1.15	-9.61	-1.85
60	-9.57	-1.46	-9.17	-1.66	-12.50	-2.53	-11.27	-2.45
80	-12.54	-2.25	-11.28	-2.64	-15.20	-3.56	-13.59	-3.76
100	-14.67	-3.07	-13.36	-3.52	-16.22	-4.69	-15.51	-5.02
125	-16.67	-3.88	-14.91	-4.76	-17.38	-5.78	-17.07	-6.50
150	-17.32	-5.74	-16.78	-5.89	-19.45	-7.43	-18.75	-7.74
200	-18.77	-7.75	-18.96	-7.90	-20.36	-10.71	-21.11	-9.94
300	-21.43	-12.04	-21.81	-10.89	-22.96	-13.58	-24.46	-13.23
500	-22.22	-16.74	-26.09	-14.98	-23.78	-17.66	-28.84	-17.16
>1000	-25.42	-21.13	-33.44	-20.66	-23.51	-20.96	-35.77	-23.35

TABLE 2: XRT71D00 JITTER TRANSFER FUNCTION

APPLICATION	STS-1			
BWS	LOW	HIGH	LOW	HIGH
INPUT JITTER	1UIPP		10UIPP	
FREQ. (HZ)	Jitter Gain (dB)			
10	-0.92	-0.60	0.71	-0.15
20	-1.71	-0.14	-1.05.	-0.17
30	-4.22	-1.03	-3.06	-0.24
40	-5.66	-1.09	-4.81	-0.61
50	-7.08	-1.23	-6.36	-0.97
60	-8.37	-1.54	-7.86	-1.30
80	-10.69	-2.55	-9.97	-2.02
100	-12.28	-3.44	-11.87	-2.91
125	-14.00	-4.29	-13.62	-4.02
150	-15.27	-5.04	-15.20	-5.01
200	-17.36	-6.77	-17.74	-6.93
300	-19.79	-9.25	-21.22	-9.94
500	-21.75	-13.20	-25.77	-14.06
1000	-24.18	-17.93	-32.92	-19.78
2000	-25.34	-21.29	-41.89	-25.25
5000	-27.14	-24.28	-45.57	-36.25

FIGURE 8. DS3 JITTER TRANSFER CHARACTERISTICS

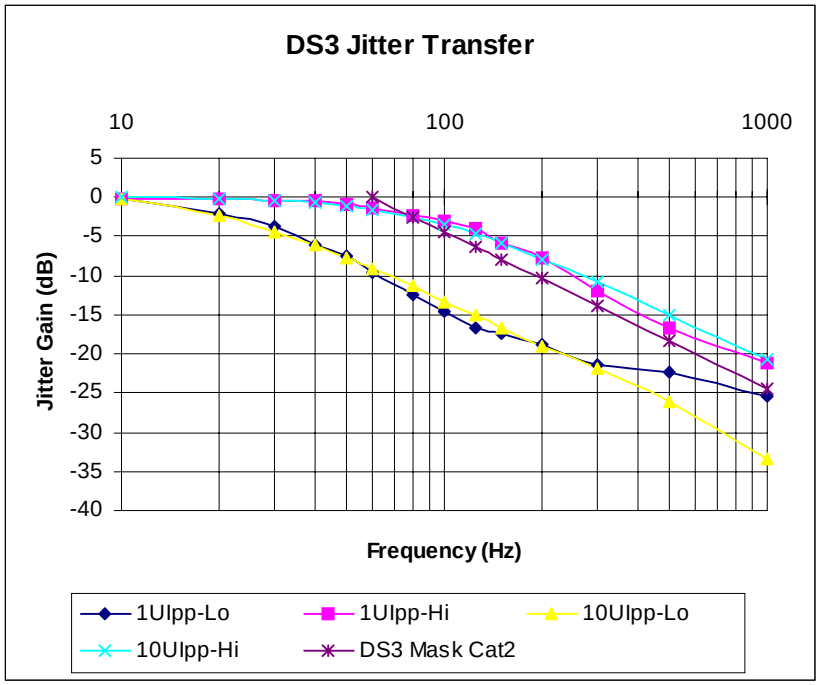


FIGURE 9. E3 JITTER TRANSFER CHARACTERISTICS

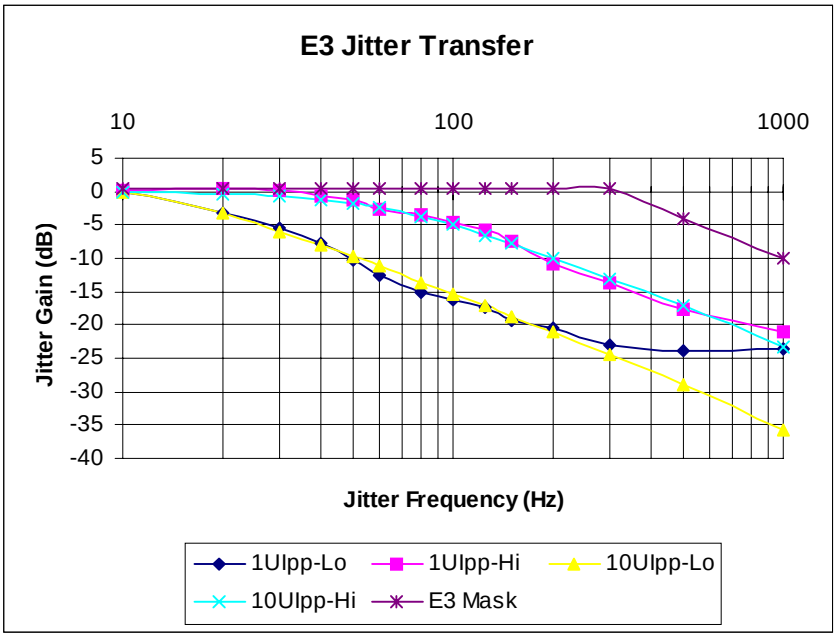


FIGURE 10. STS-1 JITTER TRANSFER CHARACTERISTICS

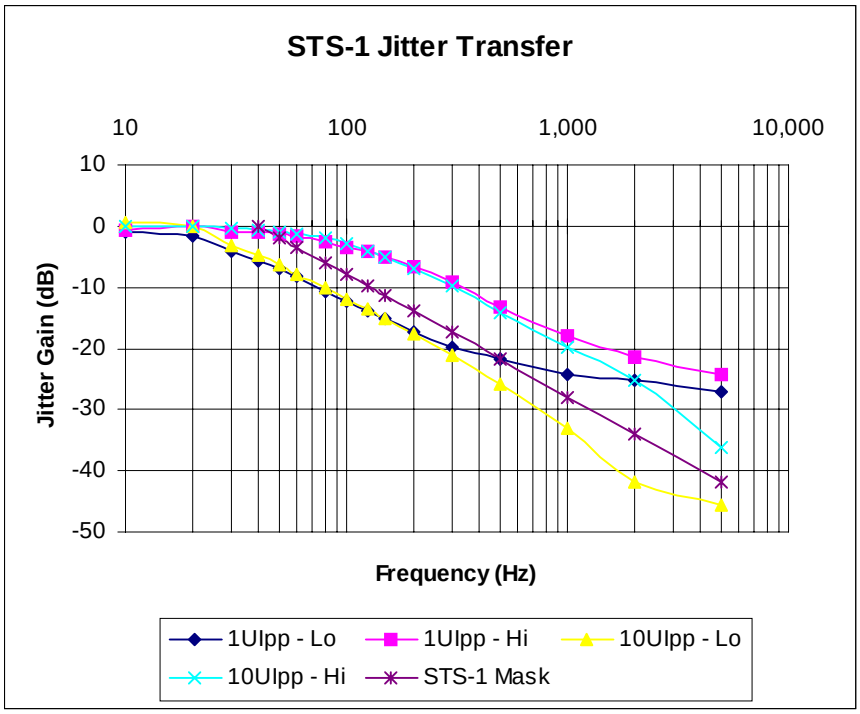


TABLE 3: XRT71D00 MAXIMUM JITTER TOLERANCE

APPLICATION	DS3				E3			
BWS	LOW	HIGH	LOW	HIGH	LOW	HIGH	LOW	HIGH
FIFO SIZE	16		32		16		32	
FREQ. (HZ)	UI (PEAK TO PEAK)				UI (PEAK TO PEAK)			
10	34.313	>64	>64	>64	26.689	>64	53.313	>64
20	21.439	>64	43.188	>64	18.564	52.188	37.438	>64
30	18.314	46.313	36.813	>64	16.689	36.688	33.938	>64
40	16.939	36.188	34.313	>64	16.064	29.314	32.688	58.438
50	16.314	30.314	33.188	60.313	15.689	25.064	32.063	50.438
60	16.064	26.689	32.563	53.188	15.564	22.564	31.689	45.438
80	15.689	22.314	31.814	44.813	15.314	19.689	31.314	39.688
100	15.439	20.064	31.439	40.434	15.314	18.064	31.189	36.813
125	15.439	18.439	31.314	37.313	15.189	17.064	31.064	34.813
150	15.314	17.564	31.189	35.438	15.189	16.564	31.064	33.688
200	15.314	16.464	31.064	33.563	15.189	15.939	30.939	32.438
300	15.189	15.814	30.939	32.063	15.064	15.564	30.939	31.564
500	15.189	15.439	30.939	31.314	15.064	15.314	30.939	31.189
>1000	15.0189	15.189	30.939	30.939	15.189	15.189	30.939	30.939

TABLE 4: XRT71D00 MAXIMUM JITTER TOLERANCE

APPLICATION	STS-1			
BWS	LOW	HIGH	LOW	HIGH
FIFO SIZE	16		32	
FREQ. (HZ)	UI (PEAK TO PEAK)			
10	38.939	>64.00	>64.00	>64.00
20	22.689	>64.00	44.938	>64.00
30	18.939	53.688	37.688	>64.00
40	17.439	41.563	34.938	>64.00
50	16.814	34.438	33.688	>64.00
60	16.314	29.939	32.938	59.063
80	15.939	24.689	32.188	48.938
100	15.814	21.814	31.814	43.438
125	15.689	19.814	31.564	39.438
150	15.564	18.564	31.439	37.063
200	15.564	17.314	31.314	34.688
300	15.439	16.314	31.189	32.813
500	15.439	15.814	31.189	31.689
1000	15.439	15.564	31.189	31.314
2000	15.439	15.439	31.189	31.189
3000	15.439	15.439	26.189	26.189
5000	15.439	15.439	16.189	16.189

2.0 OPERATING MODE

2.1 HARDWARE MODE

The HOST/$\overline{HW}$ pin (pin 12) is used to select the operating mode of the XRT71D00. In Hardware mode (connect this pin to ground), the serial processor interface is disabled and hardwired pins are used to control configuration and report status.

TABLE 5: HARDWARE MODE PIN FUNCTIONS

PIN #	PIN NAME	HARDWARE MODE FUNCTION
10	ClkES/(SDI)	ClkES
11	FSS/(SClk)	FSS
15	BWS/Ch_Addr_1	BWS
18	DJA/(SDO)	DJA
28	Ch_Addr_0	None
29	E3/$\overline{DS3}$/($\overline{CS}$)	E3/$\overline{DS3}$

2.1.1 Host Mode:

In Host mode (connect the HOST/$\overline{HW}$ pin to VDD), the serial port interface pins are used to control configuration and status report. In this mode, serial interface pins : SDI, SDO, SClk and $\overline{CS}$ are used.

A listing of these Command Registers, their Addresses, and their bit-formats are listed below in Table 6.

TABLE 6: ADDRESS AND BIT FORMATS OF THE COMMAND REGISTERS

ADDR	COMMAND REGISTER	CH_ADDR_1	CH_ADDR_0	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
0X06	CR6	0	0	R/W	***	***	STS-1	E3/$\overline{DS3}$	DJA	BWS	ClkES	FSS
0x07	CR7	0	0	RO	***	***	***	***	***	***	***	FL
0x0E	CR14	0	1	R/W	***	***	STS-1	E3/$\overline{DS3}$	DJA	BWS	ClkES	FSS
0x0F	CR15	0	1	RO	***	***	***	***	***	***	***	FL
0x16	CR22	1	0	R/W	***	***	STS-1	E3/$\overline{DS3}$	DJA	BWS	ClkES	FSS
0x17	CR22	1	0	RO	***	***	***	***	***	***	***	FL

3.0 MICROPROCESSOR SERIAL INTERFACE

The serial interface for the XRT71D00 and XRT73L00 E3/DS3/STS-1 LIU are the same, which makes it easy to configure both the XRT71D00 and the LIU with a single $\overline{CS}$, SDI, SDO and SClk input and output pins.

3.1 SERIAL INTERFACE OPERATION.

Serial interface data structure and timings are provided in Figure 11 and Figure 12 respectively.

The clock signal is provided to the SClk and the $\overline{CS}$ is asserted for 50 ns prior to the first rising edge of the SClk.

3.1.1 Bit Descriptions

3.1.1.1 Bit 1—"R/W" (Read/Write) Bit

This bit will be clocked into the SDI input, on the first rising edge of SClk (after $\overline{CS}$ has been asserted).

This bit indicates whether the current operation is a "Read" or "Write" operation. A "1" in this bit specifies a "Read" operation, a "0" in this bit specifies a "Write" operation.

3.1.1.2 Bits 2 through 6

The five (5) bit Address Values (labeled A0, A1, A2 ,A3, and A4)

The next four rising edges of the SClk signal will clock in the 5-bit address value for this particular Read (or Write) operation. The address selects the Command Register for reading data from, or writing data to. The address bits to the SDI input pin is applied in ascending order with the LSB (least significant bit) first.

Bit 7---A5

A5 must be set to "0", as shown in Figure 11.

Bit 8—A6

The value of “A6” is a “don’t care”.

Once these first 8 bits have been written into the Serial Interface, the subsequent action depends upon whether the current operation is a “Read” or “Write” operation.

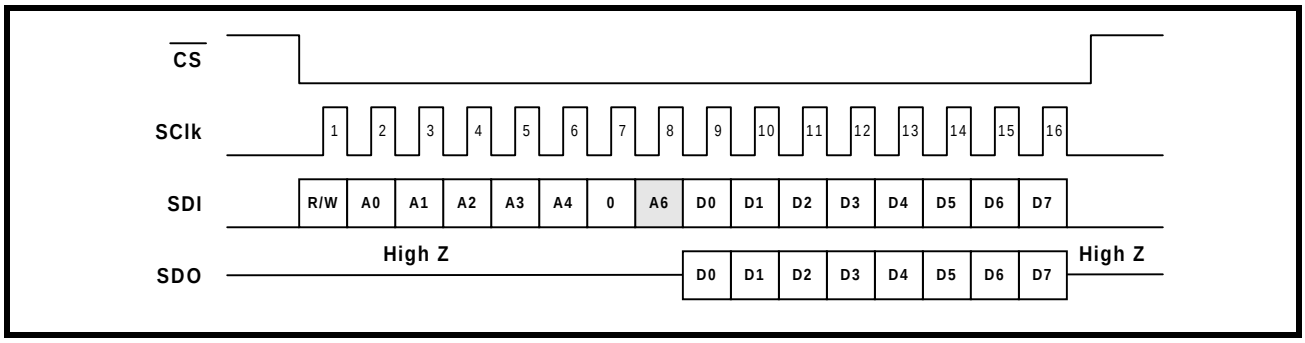
3.2 READ OPERATION

Once the last address bit (A4) has been clocked into the SDI input, the “Read” operation will proceed through an idle period, lasting three SClk periods. On the falling edge of SClk Cycle #8 (see Figure 11) the serial data output signal (SDO) becomes active. At this point the user can begin reading the data contents of the addressed Command Register (at Address [A4, A3, A2, A1, A0]) via the SDO output pin. The Serial Interface will output this eight bit data word (D0 through D7) in ascending order (with the LSB first), on the falling edges of the SClk . The data (on the SDO output pin) is stable for reading on the very next rising edge of the SClk .

3.3 WRITE OPERATION

Once the last address bit (A4) has been clocked into the SDI input, the “Write” operation will proceed through an idle period, lasting three SClk periods. Prior to the rising edge of SClk Cycle #9 , the eight bit data word is applied to SDI input. Data on SDI is latched on the rising edge of SClk.

FIGURE 11. MICROPROCESSOR SERIAL INTERFACE DATA STRUCTURE



NOTES:

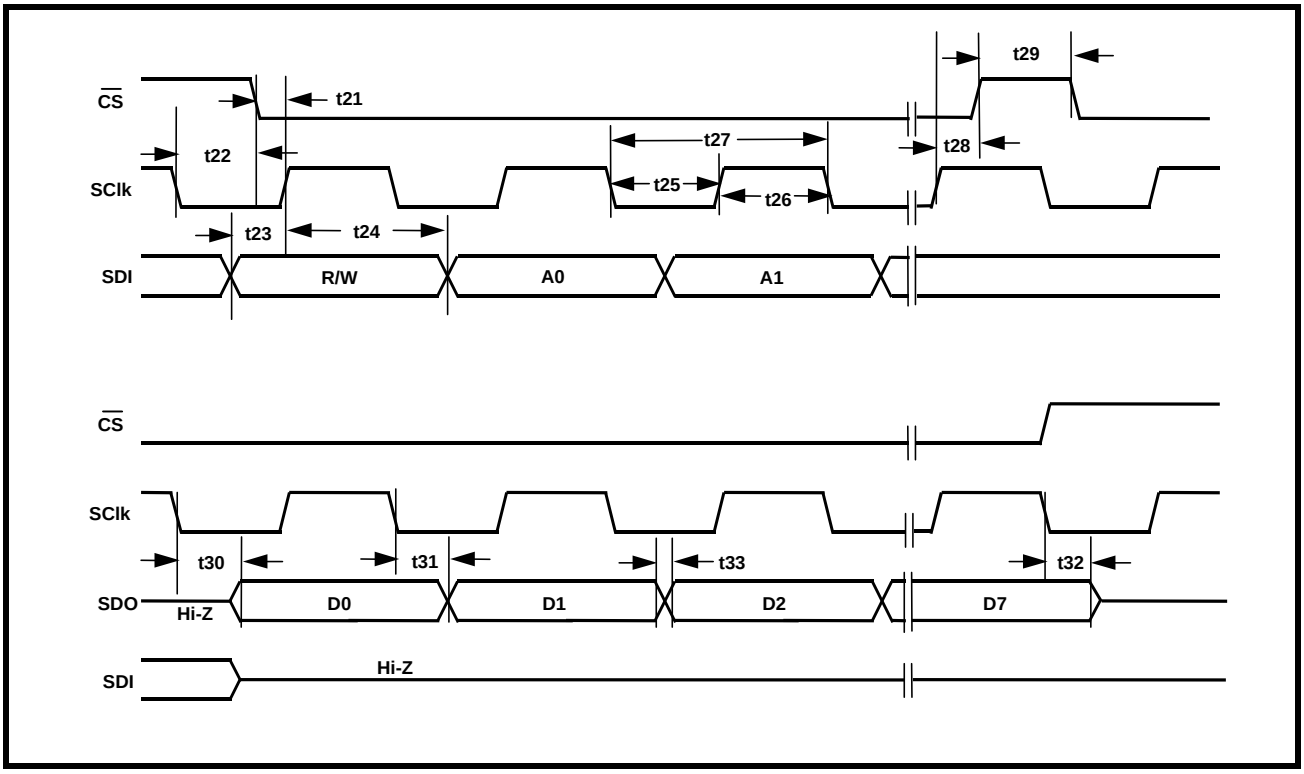
1. *A5 is always “0”.*
2. *R/W = “1” for “Read” Operations*
3. *R/W = “0” for “Write” Operations*
4. *Denotes a “don’t care” value (shaded areas)*

3.4 SIMPLIFIED INTERFACE OPTION

The user can simplify the design of the circuitry connecting to the Microprocessor Serial Interface by tying both the SDO and SDI pins together, and reading data from and/or writing data to this “combined” signal. This simplification is possible because only one

of these signals are active at any given time. The in-active signal will be tri-stated.

FIGURE 12. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE

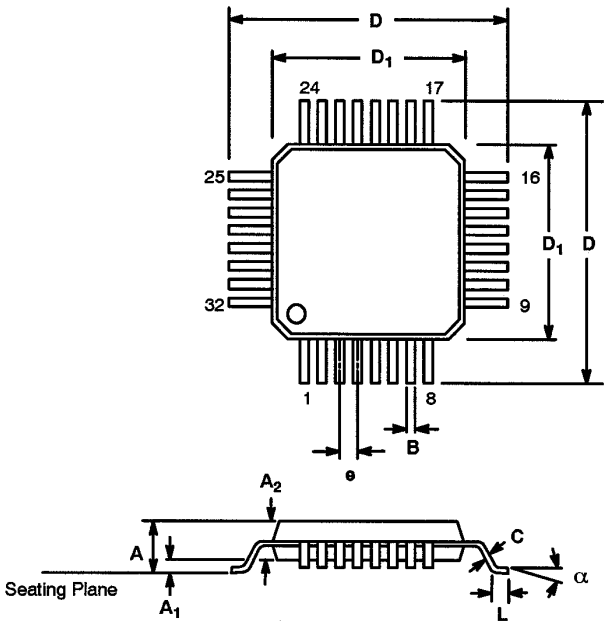


PACKAGE INFORMATION

32 LEAD TQFP PACKAGE DIMENSIONS

32 LEAD THIN QUAD FLAT PACK
(7 x 7 x 1.4 mm TQFP)

Rev. 2.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.012	0.018	0.30	0.45
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D_1	0.272	0.280	6.90	7.10
e	0.0315 BSC		0.80 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT71D00IQ	32 Lead TQFP	-40^0C to $+85^0$C

REVISIONS

Rev. 1.0.1 to 1.1.0 Pin 8 changed from internal **pull-up** resistor to **pull-Down** resistor, removed the preliminary designation. Edited electrical tables.

Rev. 1.2.0 Removed reference to STS-1 to DS3 Desyncronizer. Added Jitter Transfer graphs, Figures 8, 9 and 10.

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