1.25A, 4MHz, Synchronous Step-Down DC/DC Converter

FEATURES

- **High Efficiency: Up to 95%**
- **V_{IN} Range: 2.5V to 5.5V**
- **High Frequency Operation: Up to 4MHz**
- **Selectable Low Ripple (Typical 25mV_{p-p})**
- **Burst Mode® Operation: I_Q = 40µA**
- Stable with Ceramic Capacitors
- Uses Tiny Capacitors and Inductor
- Low $R_{DS(ON)}$ Internal Switches: 0.15Ω
- Current Mode Operation for Excellent Line and Load Transient Response
- Short-Circuit Protected
- Low Dropout Operation: 100% Duty Cycle
- Low Shutdown Current: $I_Q \leq$ 1µA
- Output Voltages from 0.6V to 5V
- Synchronizable to External Clock
- Supports Pre-Biased Outputs
- Small 10-Lead (3mm × 3mm) DFN or MSOP Package

APPLICATIONS

- Notebook Computers
- Digital Cameras
- Cellular Phones
- Handheld Instruments
- Board Mounted Power Supplies

DESCRIPTION

The LTC®3565 is a constant frequency, synchronous step-down DC/DC converter. Intended for medium power applications, it operates from a 2.5V to 5.5V input voltage range and has a user-configurable operating frequency up to 4MHz, allowing the use of tiny, low cost capacitors and inductors 1mm or less in height. The output voltage is adjustable from 0.6V to 5.5V. Internal synchronous power switches provide high efficiency. The LTC3565's current mode architecture and external compensation allow the transient response to be optimized over a wide range of loads and output capacitors.

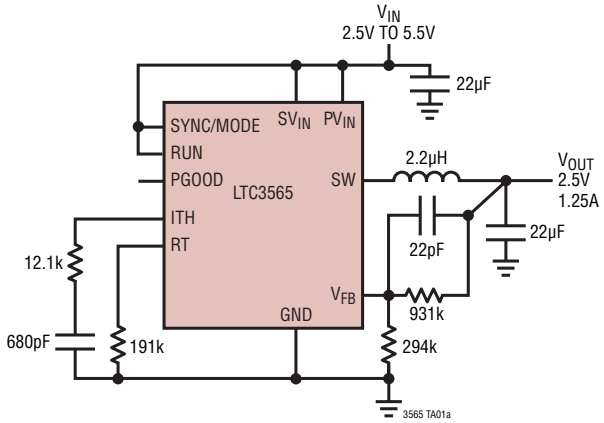
The LTC3565 can be configured for automatic power saving Burst Mode operation (I_Q = 40µA) to reduce gate charge losses when the load current drops below the level required for continuous operation. For reduced noise and RF interference, the SYNC/MODE pin can be configured to skip pulses or provide forced continuous operation.

To further maximize battery life, the P-channel MOSFET is turned on continuously in dropout (100% duty cycle). In shutdown, the device draws <1µA.

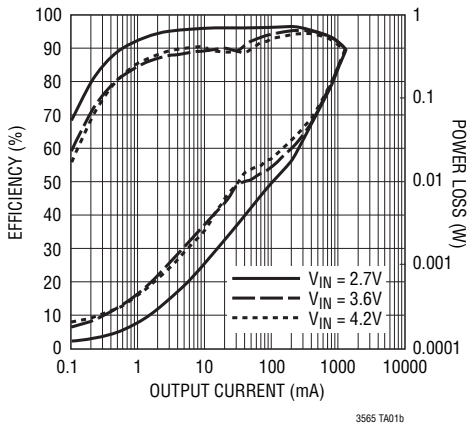
LT, LTC, LTM, Linear Technology the Linear logo, Burst Mode and OPTI-LOOP are registered trademarks of Linear Technology Corporation. Hot Swap and ThinSOT are trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners. Protected by U.S. Patents including 5481178, 6580258, 6498466, 6611131.

TYPICAL APPLICATION

Step-Down 2.5V/1.25A Regulator



Efficiency and Power Loss vs Output Current

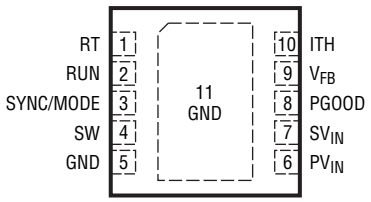


ABSOLUTE MAXIMUM RATINGS (Note 1)

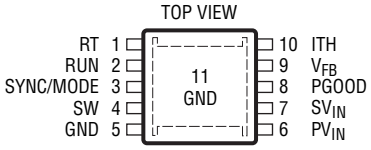
PV_{IN}, SV_{IN} Voltages ..... –0.3V to 6V
V_{FB}, ITH Voltages ..... –0.3V to (V_{IN} + 0.3V)
SYNC/MODE, PGOOD Voltage ..... –0.3V to (V_{IN} + 0.3V)
SW Voltage (DC) ..... –0.3V to (V_{IN} + 0.3V)
RUN Voltage ..... –0.3V to 6V

Operating Junction Temperature Range
(Notes 2, 5, 8) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 7.5°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3565EDD#PBF	LTC3565EDD#TRPBF	LDNR	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3565IDD#PBF	LTC3565IDD#TRPBF	LDNR	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3565EMSE#PBF	LTC3565EMSE#TRPBF	LTDVJ	10-Lead Plastic MSOP	–40°C to 125°C
LTC3565IMSE#PBF	LTC3565IMSE#TRPBF	LTDVJ	10-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 3.6V, R_T = 125k unless otherwise specified. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage Range			2.5		5.5	V
I_{FB}	Feedback Pin Input Current	(Note 3)				50	nA
V_{FB}	Feedback Voltage	(Note 3)	●	0.588	0.6	0.612	V
$\Delta V_{LINEREG}$	Reference Voltage Line Regulation	V_{IN} = 2.5V to 5.5V			0.04	0.2	%/V
$\Delta V_{LOADREG}$	Output Voltage Load Regulation	ITH = 0.55V to 0.9V	●		0.02	0.2	%
$g_{m(EA)}$	Error Amplifier Transconductance	ITH Pin Load = ±5µA (Note 3)			300		µS

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 3.6V, R_T = 125k unless otherwise specified. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_S	Input DC Supply Current (Note 4) Active Mode Sleep Mode Shutdown	 $V_{SYNC/MODE}$ = 3.6V, V_{FB} = 0.55V $V_{SYNC/MODE}$ = 3.6V, V_{FB} = 0.8V V_{RUN} = 0V			 330 40 0.1	 450 60 1	 µA µA µA
f_{OSC}	Oscillator Frequency	RT = 125k (Note 7)		1.3	1.5	1.7 4	MHz MHz
f_{SYNC}	Synchronization Frequency	(Note 7)		0.4		4	MHz
I_{LIM}	Peak Switch Current Limit	V_{IN} = 3V, V_{FB} = 0.5V		1.5	2.1	2.5	A
$R_{DS(ON)}$	Top Switch On-Resistance	MSE Package DD Package (Note 6)			0.15 0.15	0.2	Ω Ω
	Bottom Switch On-Resistance	MSE Package DD Package (Note 6)			0.13 0.13	0.18	Ω Ω
$I_{SW(LKG)}$	Switch Leakage Current	V_{IN} = 5.5V, V_{RUN} = 0V, V_{FB} = 0V			0.01	1	µA
V_{RUN}	RUN Threshold		●	0.3	0.8	1.5	V
I_{RUN}	RUN Leakage Current		●		±0.01	±1	µA
V_{UVLO}	Undervoltage Lockout Threshold	V_{IN} Ramping Down			1.9	2.2	V
PGOOD	Power Good Threshold	V_{FB} Ramping Up from 0.45V to 0.6V V_{FB} Ramping Down from 0.69V to 0.6V			–7 7		% %
R_{PGOOD}	Power Good Pull-Down On-Resistance				15	20	Ω
PGOOD Blanking		V_{FB} Step from 0V to 0.6V V_{FB} Step from 0.6V to 0V			40 105		µs µs
$V_{SYNC-MODE}$	Pulse Skip Force Continuous Burst	V_{IN} = 2.5V to 5.5V V_{IN} = 2.5V to 5.5V V_{IN} = 2.5V to 5.5V		 1.2 V_{IN} – 0.6		0.6 V_{IN} – 1.1	V V V
$t_{SOFT-START}$		10% to 90% of Regulation		0.6	0.9	1.2	ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3565 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3565E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3565I is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: The LTC3565 is tested in a feedback loop which servos V_{FB} to the midpoint for the error amplifier (V_{ITH} = 0.7V).

Note 4: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

Note 5: T_J is calculated from the ambient T_A and power dissipation P_D according to the following formulas:

LTC3565EDD: $T_J = T_A + (P_D \bullet 43°C/W)$

LTC3565EMSE: $T_J = T_A + (P_D \bullet 40°C/W)$

Note 6: Switch on-resistance is guaranteed by correlation to wafer level measurements and assured by design characterization and correlation with statistical process controls.

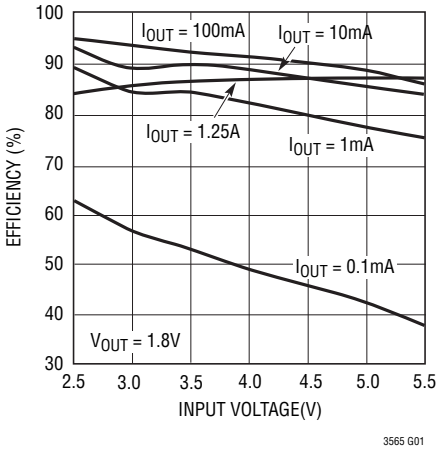
Note 7: 4MHz operation is guaranteed by design but not production tested and is subject to duty cycle limitations (see Applications Information).

Note 8: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

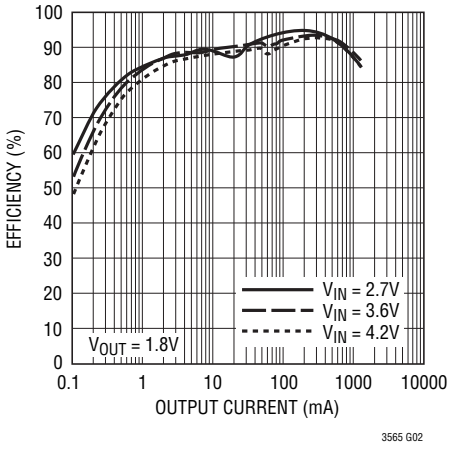
T_J = 25°C, V_{IN} = 3.6V, f_O = 1MHz, unless otherwise noted.

Efficiency vs Input Voltage



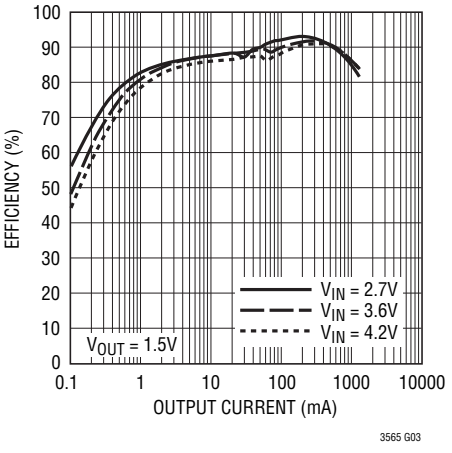
3565 G01

Efficiency vs Output Current



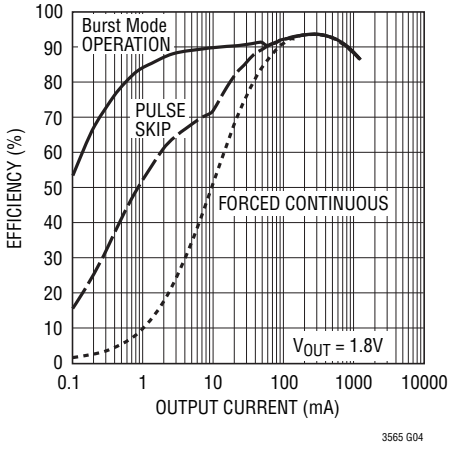
3565 G02

Efficiency vs Output Current



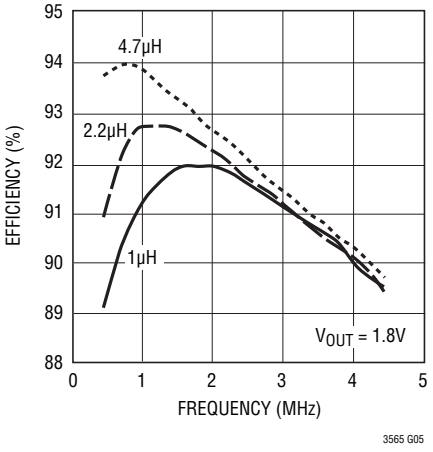
3565 G03

Efficiency vs Output Current



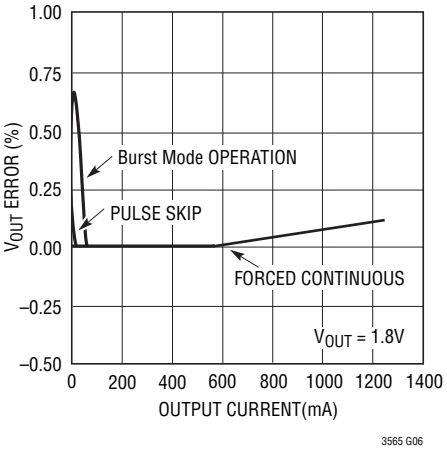
3565 G04

Efficiency vs Frequency



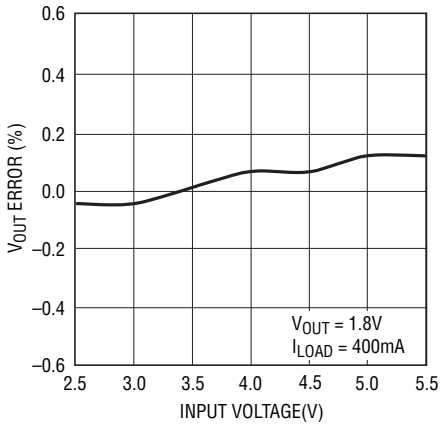
3565 G05

Load Regulation



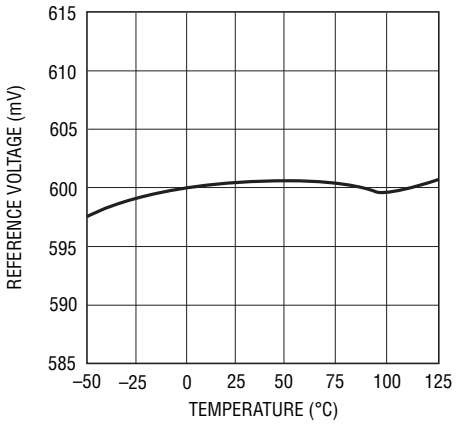
3565 G06

Line Regulation



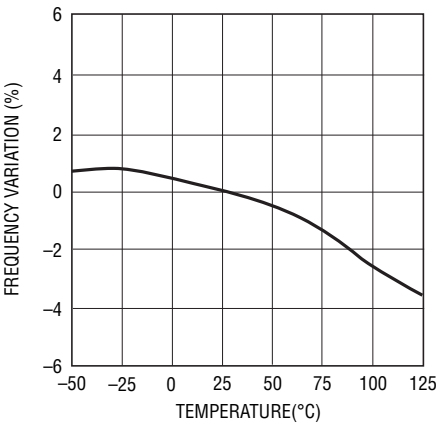
3565 G07

Reference Voltage vs Temperature



3565 G08

Frequency Variation vs Temperature

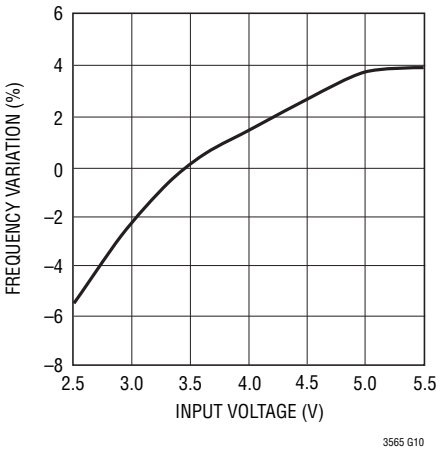


3565 G09

TYPICAL PERFORMANCE CHARACTERISTICS

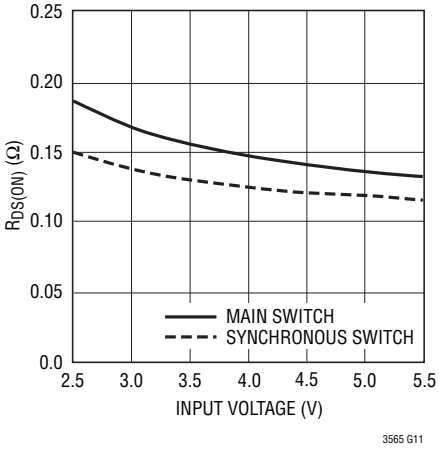
T_J = 25°C, V_{IN} = 3.6V, f_O = 1MHz, unless otherwise noted.

Frequency Variation vs Input Voltage



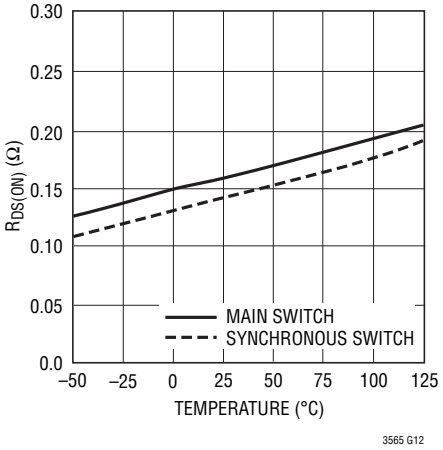
3565 G10

$R_{DS(ON)}$ vs Input Voltage



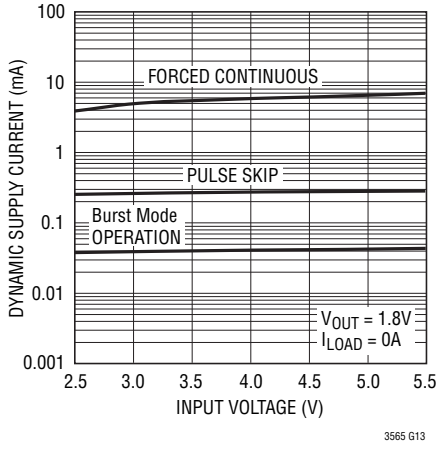
3565 G11

$R_{DS(ON)}$ vs Temperature



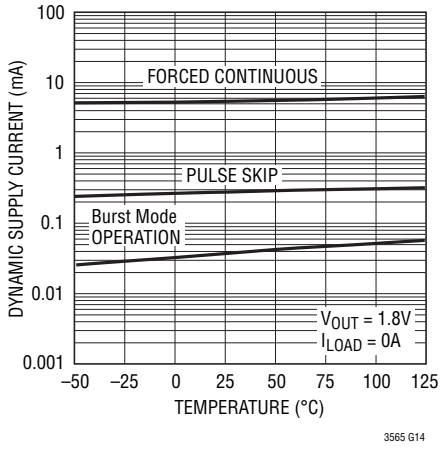
3565 G12

Dynamic Supply Current vs Input Voltage



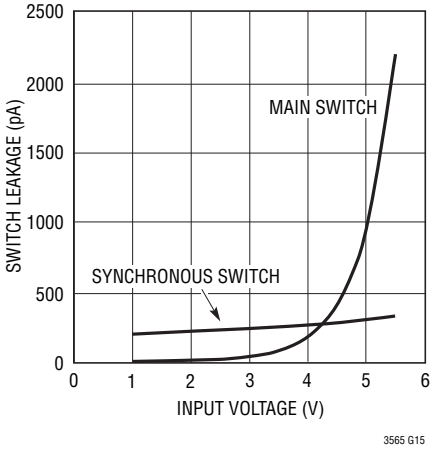
3565 G13

Dynamic Supply Current vs Temperature



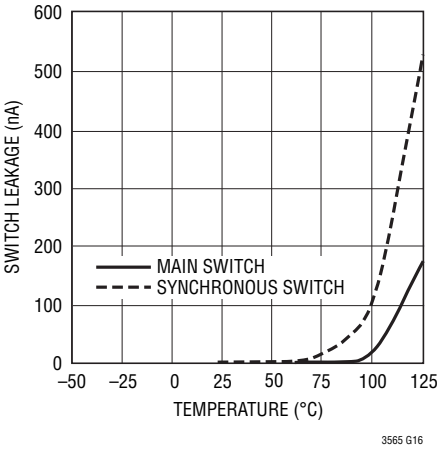
3565 G14

Switch Leakage vs Input Voltage



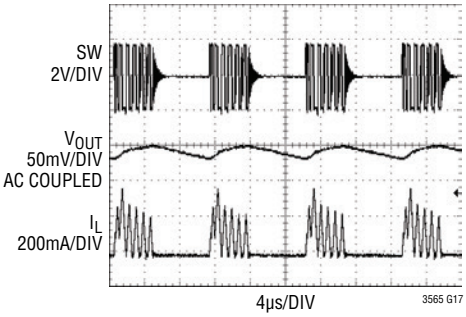
3565 G15

Switch Leakage vs Temperature



3565 G16

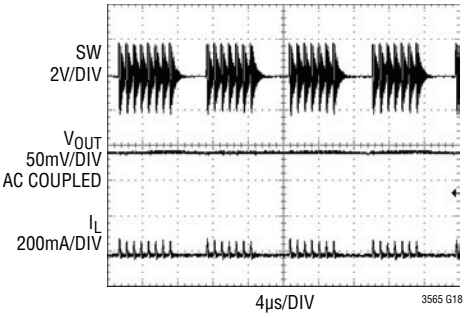
Burst Mode Operation



3565 G17

V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 50mA

Pulse Skipping Mode



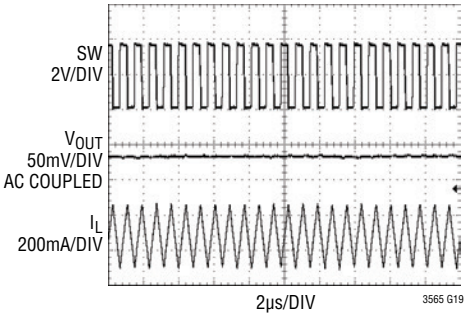
3565 G18

V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 5mA

TYPICAL PERFORMANCE CHARACTERISTICS

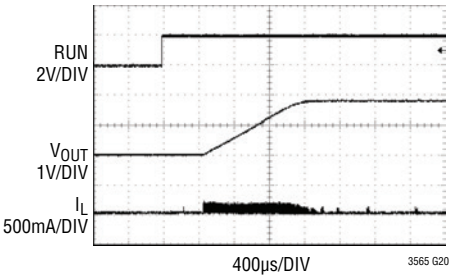
T_J = 25°C, V_{IN} = 3.6V, f_O = 1MHz, unless otherwise noted.

Forced Continuous Mode



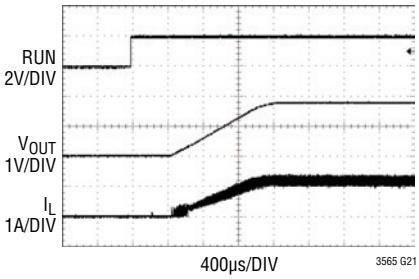
V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 80mA

Start-Up from Shutdown



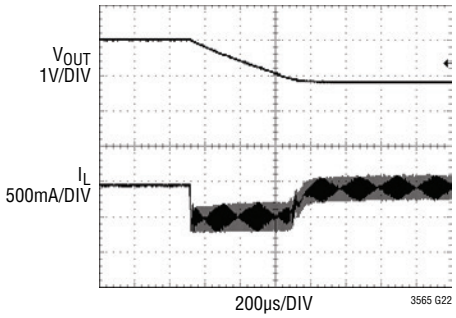
V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 0A
Burst Mode OPERATION

Start-Up from Shutdown



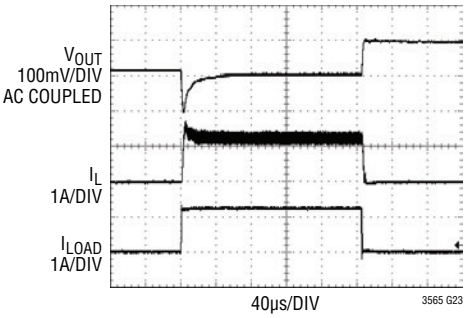
V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 1.25A
Burst Mode OPERATION

Start-Up from Shutdown with a Prebiased Output (Forced Continuous Mode)



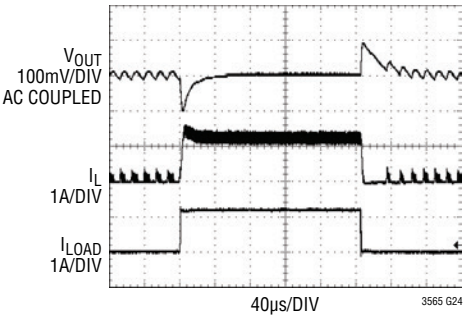
V_{IN} = 3.6V
PREBIASED V_{OUT} = 3V, V_{OUT} = 1.8V
I_{LOAD} = 0A

Load Step



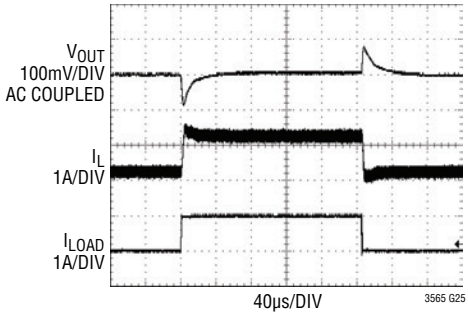
V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 0A to 1.25A
Burst Mode OPERATION

Load Step



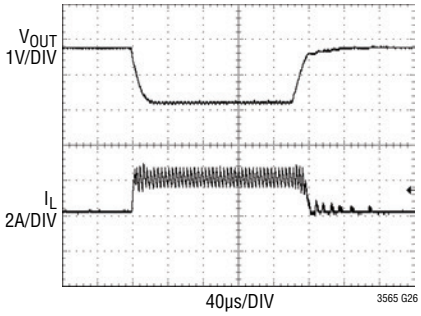
V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 50mA to 1.25A
Burst Mode OPERATION

Load Step



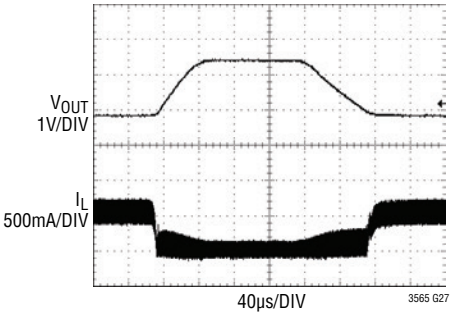
V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 250mA to 1.25A
Burst Mode OPERATION

V_{OUT} Short to Ground



V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 0A

V_{OUT} Short to V_{IN} (Forced Continuous Mode)



V_{IN} = 3.6V
V_{OUT} = 1.8V
I_{LOAD} = 0A

PIN FUNCTIONS

RT (Pin 1): Timing Resistor Pin. The oscillator frequency is programmed by connecting a resistor from this pin to ground.

RUN (Pin 2): Converter Enable Pin. Forcing this pin above 1.5V enables this part, while forcing it below 0.3V causes the device to shut down. In shutdown, the device draws <1µA supply current. This pin must be driven; do not float.

SYNC/MODE (Pin 3): Combination Mode Selection and Oscillator Synchronization Pin. This pin controls the operation of the device. When tied to SV_{IN} or GND, Burst Mode operation or pulse skipping mode is selected, respectively. If this pin is held at half of SV_{IN}, the forced continuous mode is selected. The oscillation frequency can be synchronized to an external oscillator applied to this pin. When synchronized to an external clock, pulse skip mode is selected.

SW (Pin 4): The Switch Node Connection to the Inductor. This pin swings from PV_{IN} to GND.

GND (Pin 5, Exposed Pad Pin 11): Main Power Ground Pin. Connect to the (–) terminal of C_{OUT}, and (–) terminal of C_{IN}. The exposed pad must be soldered to electrical ground on the PCB.

PV_{IN} (Pin 6): Main Supply Pin. Must be closely decoupled to GND.

SV_{IN} (Pin 7): The Signal Power Pin. All active circuitry is powered from this pin. Must be closely decoupled to GND. SV_{IN} must be greater than or equal to PV_{IN}.

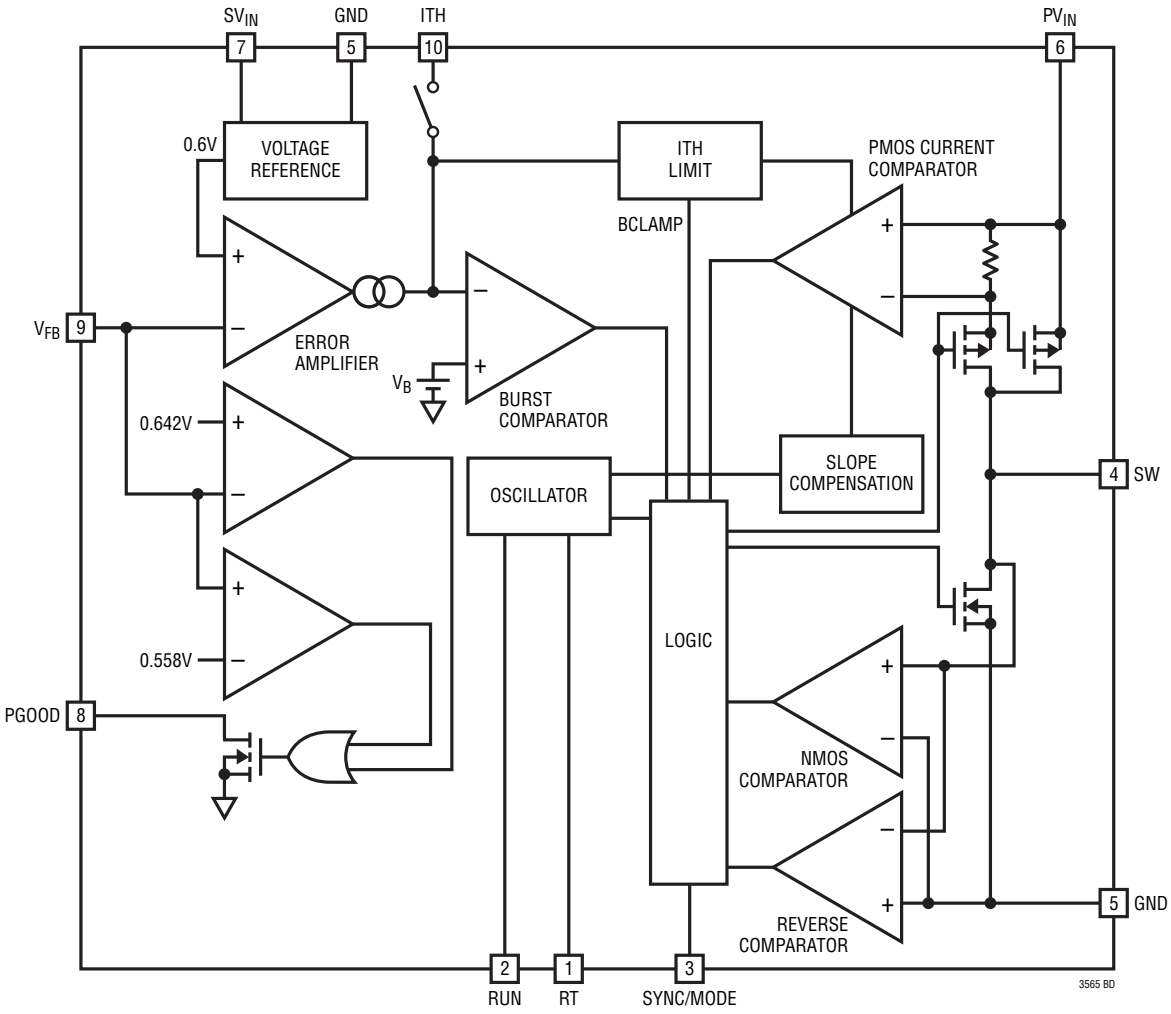
PGOOD (Pin 8): The Power Good Pin. This common drain logic output is pulled to GND when the output voltage is not within ±7% of regulation.

V_{FB} (Pin 9): Receives the feedback voltage from the external resistive divider across the output. Nominal voltage for this pin is 0.6V.

ITH (Pin 10): Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0.4V to 1.4V.

PIN	NAME	DESCRIPTION	NOMINAL (V)			ABSOLUTE MAX (V)	
			MIN	TYP	MAX	MIN	MAX
1	RT	Timing Resistor	–0.3	0.4	SV_{IN}	–0.3	SV_{IN} + 0.3
2	RUN	Enable Pin	–0.3		SV_{IN}	–0.3	SV_{IN}
3	SYNC/MODE	Mode Select/Synchronization Pin	0		SV_{IN}	–0.3	SV_{IN} + 0.3
4	SW	Switch Node	0		PV_{IN}	–0.3	PV_{IN} + 0.3
5	GND	Main Power Ground		0			
6	PV_{IN}	Main Power Supply	–0.3		5.5	–0.3	6
7	SV_{IN}	Signal Power Supply	2.5		5.5	–0.3	6
8	PGOOD	Power Good Pin	0		SV_{IN}	–0.3	SV_{IN} + 0.3
9	V_{FB}	Output Feedback Pin	0	0.8	1.0	–0.3	SV_{IN} + 0.3
10	ITH	Error Amplifier Compensation	0		1.5	–0.3	SV_{IN} + 0.3

BLOCK DIAGRAM



OPERATION

The LTC3565 uses a constant frequency, current mode architecture. The operating frequency is determined by the value of the R_T resistor or can be synchronized to an external oscillator. To suit a variety of applications, the selectable MODE pin allows the user to trade-off noise for efficiency.

The output voltage is set by an external divider returned to the V_{FB} pin. An error amplifier compares the divided output voltage with the reference voltage of 0.6V and adjusts the peak inductor current accordingly. Overvoltage and undervoltage comparators will pull the PGOOD output low if the output voltage is not within ±7% of its regulated value. A tripping delay of 40µs and untripping delay of 105µs ensures PGOOD will not glitch due to transient spikes on V_{OUT}.

Main Control Loop

During normal operation, the top power switch (P-channel MOSFET) is turned on at the beginning of a clock cycle. Current flows through this switch into the inductor and the load, increasing until the peak inductor current reaches the limit set by the voltage on the ITH pin. Then, the top switch is turned off, the bottom switch is turned on, and the energy stored in the inductor forces the current to flow through the bottom switch and the inductor out into the load until the next clock cycle.

The peak inductor current is controlled by the voltage on the ITH pin, which is the output of the error amplifier. The output is developed by the error amplifier comparing the feedback voltage, V_{FB}, to the 0.6V reference voltage. When the load current increases, the output voltage and V_{FB} decrease slightly. This decrease in V_{FB} causes the error amplifier to increase the ITH voltage until the average inductor current matches the new load current.

The main control loop is shut down by grounding the RUN pin, resetting the internal soft-start. Re-enabling the main control loop by pulling RUN high activates the internal soft-start, which slowly ramps the output voltage over approximately 0.9ms until it reaches regulation.

Low Current Operation

Three modes are available to control the operation of the LTC3565 at low currents. All three modes automatically switch from continuous operation to the selected mode when the load current is low.

To optimize efficiency, the Burst Mode operation can be selected. When the load is relatively light, the LTC3565 automatically switches into Burst Mode operation in which the PMOS switch operates intermittently based on load demand. By running cycles periodically, the switching losses which are dominated by the gate charge losses of the power MOSFETs are minimized. The main control loop is interrupted when the output voltage reaches the desired regulated value. The burst comparator trips when ITH is below approximately 0.5V, shutting off the switch and reducing the power. The output capacitor and the inductor supply the power to the load until ITH rises above approximately 0.5V, turning on the switch and the main control loop which starts another cycle.

For lower output voltage ripple at low currents, pulse skipping mode can be used. In this mode, the LTC3565 continues to switch at a constant frequency down to very low currents, where it will eventually begin skipping pulses.

Finally, in forced continuous mode, the inductor current is constantly cycled which creates a fixed output voltage ripple at all output current levels. This feature is desirable in telecommunications since the noise is at a constant frequency and is thus easy to filter out. Another advantage of this mode is that the regulator is capable of both sourcing current into a load and sinking current from the output.

Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases to 100% which is the dropout condition. In dropout, the PMOS switch is turned on continuously with the output voltage being equal to the input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor.

Low Supply Operation

The LTC3565 incorporates an undervoltage lockout circuit which shuts down the part when the input voltage drops below about 1.9V to prevent unstable operation.

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A general LTC3565 application circuit is shown in Figure 4. External component selection is driven by the load requirement, and begins with the selection of the inductor L1. Once L1 is chosen, C_{IN} and C_{OUT} can be selected.

Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

The operating frequency, f_O, of the LTC3565 is determined by an external resistor that is connected between the RT pin and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator and can be calculated by using the following equation:

$$R_T = 1.21 \times 10^6 \, (f_O)^{-1.2674} \ (k\Omega)$$

where R_T is in kΩ and f_O is in kHz or can be selected using Figure 1.

The maximum usable operating frequency is limited by the minimum on-time and the duty cycle. This can be calculated as:

$$f_{O(MAX)} \approx 6.67 \bullet \frac{V_{OUT}}{V_{IN(MAX)}} \ (MHz)$$

The minimum frequency is limited by leakage and noise coupling due to the large resistance of R_T.

Inductor Selection

The operating frequency, f_O, has a direct effect on the inductor value, which in turn influences the inductor ripple current, ΔI_L:

$$\Delta I_L = \frac{V_{OUT}}{f_O \bullet L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The inductor ripple current decreases with larger inductance or frequency, and increases with higher V_{IN} or V_{OUT}. Accepting larger values of ΔI_L allows the use of lower inductances, but results in higher output ripple voltage, greater core loss and lower output capability.

A reasonable starting point for setting ripple current is $\Delta I_L = 0.4 \bullet I_{OUT(MAX)}$, where $I_{OUT(MAX)}$ is 1.25A. The largest ripple current ΔI_L occurs at the maximum input voltage. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \frac{V_{OUT}}{f_O \bullet \Delta I_L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

The inductor value will also have an effect on Burst Mode operation. The transition from low current operation begins when the peak inductor current falls below a level set by the burst clamp. Lower inductor values result in higher ripple current which causes this to occur at lower load currents. This causes a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

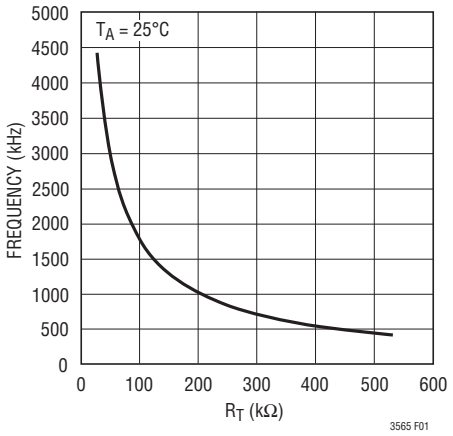


Figure 1. Frequency vs R_T

Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs size requirements and any radiated field/EMI requirements than on what the LTC3565 requires to operate. Table 1

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shows some typical surface mount inductors that work well in LTC3565 applications.

Table 1. Representative Surface Mount Inductors

MANUFACTURER	PART NUMBER	VALUE	MAX DC CURRENT	DCR	HEIGHT
Toko	A914BYW-1R2M=P3: D52LC	1.2µH	2.15A	44mΩ	2mm
	A960AW-1R2M=P3: D518LC	1.2µH	1.8A	46mΩ	1.8mm
	DB3015C-1068AS-1R0N	1.0µH	2.1A	43mΩ	1.5mm
	DB3018C-1069AS-1R0N	1.0µH	2.1A	45mΩ	1.8mm
	DB3020C-1070AS-1R0N	1.0µH	2.1A	47mΩ	2mm
	A914BYW-2R2M-D52LC	2.2µH	2.05A	49mΩ	2mm
	A915AY-2ROM-D53LC	2.0µH	3.3A	22mΩ	3mm
Coilcraft	LPO1704-122ML	1.2µH	2.1A	80mΩ	1mm
	D01608C-222	2.2µH	2.3A	70mΩ	3mm
	LP01704-222M	2.2µH	2.4A	120mΩ	1mm
Sumida	CR32-1R0	1.0µH	2.1A	72mΩ	3mm
	CR5D11-1R0	1.0µH	2.2A	40mΩ	1.2mm
	CDRH3D14-1R2	1.2µH	2.2A	36mΩ	1.5mm
	CDRH4D18C/LD-1R1	1.1µH	2.1A	24mΩ	2mm
	CDRH4D28C/LD-1R0	1.0µH	3.0A	17.5mΩ	3mm
	CDRH4D28C-1R1	1.1µH	3.8A	22mΩ	3mm
	CDRH4D28-1R2	1.2µH	2.56A	23.6mΩ	3mm
	CDRH6D12-1R0	1.0µH	2.80A	37.5mΩ	1.5mm
	CDRH4D282R2	2.2µH	2.04A	23mΩ	3mm
	CDC5D232R2	2.2µH	2.16A	30mΩ	2.5mm
Taiyo Yuden	NPO3SB1ROM	1.0µH	2.6A	27mΩ	1.8mm
	N06DB2R2M	2.2µH	3.2A	29mΩ	3.2mm
	N05DB2R2M	2.2µH	2.9A	32mΩ	2.8mm
Murata	LQN6C2R2M04	2.2µH	3.2A	24mΩ	5mm
FDK	MIPW3226DORGM	0.9µH	1.4A	80mΩ	1mm

Catch Diode Selection

Although unnecessary in most applications, a small improvement in efficiency can be obtained in a few applications by including the optional diode D1 shown in Figure 2, which conducts when the synchronous switch is off. When using Burst Mode operation or pulse skip mode, the synchronous switch is turned off at a low current and the remaining current will be carried by the optional diode. It is important to adequately specify the diode peak current and average power dissipation so as not to exceed the diode ratings. The main problem with Schottky diodes is that their parasitic capacitance reduces the efficiency, usually negating the possible benefits for LTC3565 circuits. Another problem that a Schottky diode can introduce is higher leakage current at high temperatures, which could reduce the low current efficiency.

Remember to keep lead lengths short and observe proper grounding (see Board Layout Considerations) to avoid ringing and increased dissipation when using a catch diode.

Input Capacitor (C_{IN}) Selection

In continuous mode, the input current of the converter is a square wave with a duty cycle of approximately V_{OUT}/V_{IN}. To prevent large voltage transients, a low equivalent series resistance (ESR) input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \approx I_{MAX} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

where the maximum average output current I_{MAX} equals the peak current minus half the peak-to-peak ripple current, $I_{MAX} \cong I_{LIM} - \Delta I_L/2$.

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case is commonly used to design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours lifetime. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the design. An additional 0.1µF to 1µF ceramic capacitor is also recommended on V_{IN} for high frequency decoupling, when not using an all ceramic capacitor solution.

Output Capacitor (C_{OUT}) Selection

The selection of C_{OUT} is driven by the required ESR to minimize voltage ripple and load step transients. Typically, once the ESR requirement is satisfied, the capacitance

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is adequate for filtering. The output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8 f_O C_{OUT}} \right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. With $\Delta I_L = 0.4 \bullet I_{OUT(MAX)}$, the output ripple will be less than 100mV at maximum V_{IN}, a minimum C_{OUT} of 10µF and f_O = 1MHz with:

$$ESRC_{OUT} < 150m\Omega$$

Once the ESR requirements for C_{OUT} have been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement, except for an all ceramic solution.

In surface mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirement of the application. Aluminum electrolytic, special polymer, ceramic and dry tantalum capacitors are all available in surface mount packages. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR(size) product of any aluminum electrolytic at a somewhat higher price. Special polymer capacitors, such as Sanyo POSCAP, offer very low ESR, but have a lower capacitance density than other types. Tantalum capacitors have the highest capacitance density, but it has a larger ESR and it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Aluminum electrolytic capacitors have a significantly larger ESR, and is often used in extremely cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have the lowest ESR and cost but also have the lowest capacitance density, a high voltage and temperature coefficient and exhibit audible piezoelectric effects. In addition, the high Q of ceramic capacitors along with trace inductance can lead to significant ringing. Other capacitor types include the Panasonic specialty polymer (SP) capacitors.

In most cases, 0.1µF to 1µF of ceramic capacitors should also be placed close to the LTC3565 in parallel with the main capacitors for high frequency decoupling.

Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the LTC3565's control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used freely to achieve very low output ripple and small circuit size.

However, care must be taken when ceramic capacitors are used at the input. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part. Refer to Linear Technology Application Note 88 for a detailed discussion of this potential issue.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation components and the output capacitor value. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is usually about 2 to 3 times the linear

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drop of the first cycle. Thus, a good place to start is with the output capacitor value of approximately:

$$C_{OUT} \approx 2.5 \frac{\Delta I_{OUT}}{f_O \bullet V_{DROOP}}$$

More capacitance may be required depending on the duty cycle and load step requirements.

In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 10µF ceramic capacitor is usually enough for these conditions.

Setting the Output Voltage

The LTC3565 develops a 0.6V reference voltage between the feedback pin, V_{FB}, and the signal ground as shown in Figure 4. The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} \approx 0.6V\left(1+\frac{R2}{R1}\right)$$

Keeping the current small (<5µA) in these resistors maximizes efficiency, but making them too small may allow stray capacitance to cause noise problems and reduce the phase margin of the error amp loop.

To improve the frequency response, a feed-forward capacitor C_F may also be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

Shutdown and Soft-Start

Pulling the RUN pin high allows an internal soft-start circuit to slowly ramp the output voltage up until regulation. Soft-start prevents surge currents from V_{IN} by gradually ramping the output voltage up during start-up. The output will ramp from zero to full scale over a time period of approximately 0.9ms. This prevents the LTC3565 from having to quickly charge the output capacitor and thus supplying an excessive amount of instantaneous current.

The LTC3565 can start into a back-biased output in force continuous operation. When the output is pre-biased at either a higher or lower value than the regulated output voltage, the LTC3565 will sink or source current as needed to bring the output back into regulation. However, during soft-start the regulator will always start in pulse skip mode ignoring the mode selected with the SYNC/MODE pin. This prevents the output from discharging to below the regulation point when soft-starting.

Mode Selection and Frequency Synchronization

The SYNC/MODE pin is a multipurpose pin which provides mode selection and frequency synchronization. Connecting this pin to V_{IN} enables Burst Mode operation, which provides the best low current efficiency at the cost of a higher output voltage ripple. When this pin is connected to ground, pulse skipping operation is selected which provides the lowest output voltage and current ripple at the cost of low current efficiency. Applying a voltage that is half the value of the input voltage results in forced continuous mode, which creates a fixed output ripple and is capable of sinking up to 0.4A. Since the switching noise is constant in this mode, it is also the easiest to filter out.

The LTC3565 can also be synchronized to an external clock signal by the SYNC/MODE pin. The internal oscillator frequency should be set to ±20% of the external clock frequency to ensure adequate slope compensation, since slope compensation is derived from the internal oscillator. During synchronization, the mode is set to pulse skipping and the top switch turn on is synchronized to the falling edge of the external clock.

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Checking Transient Response

The OPTI-LOOP® compensation allows the transient response to be optimized for a wide range of loads and output capacitors. The availability of the ITH pin not only allows optimization of the control loop behavior but also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time and settling time at this test point truly reflects the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin.

The ITH external components shown in the circuit on page 1 of this data sheet will provide an adequate starting point for most applications. The series R-C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} • ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The gain of the loop increases with R and the bandwidth of the loop increases with decreasing C. If R is increased by the same factor that C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. In addition, a feedforward capacitor C_F can be added to improve the high frequency response, as shown in Figure 2. Capacitor C_F provides phase lead by creating a high frequency zero with R2 which improves the phase margin.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Linear Technology Application Note 76.

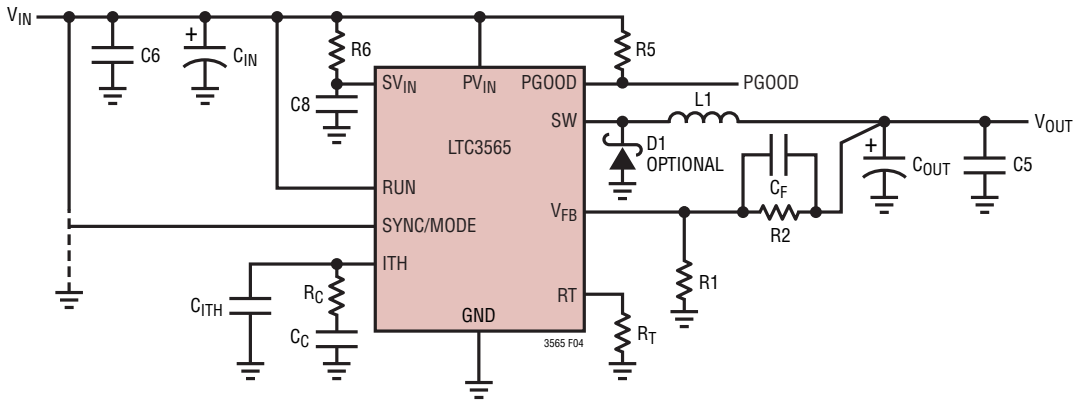


Figure 2. LTC3565 General Schematic

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Although a buck regulator is capable of providing the full output current in dropout, it should be noted that as the input voltage V_{IN} drops toward V_{OUT}, the load step capability does decrease due to the decreasing voltage across the inductor. Applications that require large load step capability near dropout should use a different topology such as SEPIC, Zeta or single inductor, positive buck/boost.

In some applications, a more severe transient can be caused by switching in loads with large (>1µF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft-starting.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

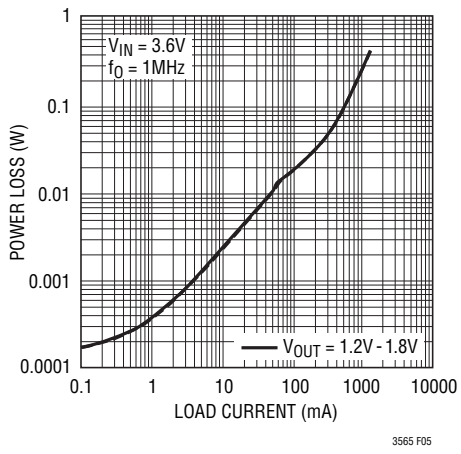


Figure 3. Power Loss vs Load Currrent

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3565 circuits: 1) LTC3565 V_{IN} current, 2) switching losses, 3) I^2R losses, 4) other losses.

1) The V_{IN} current is the DC supply current given in the electrical characteristics which excludes MOSFET driver and control currents. V_{IN} current results in a small (<0.1%) loss that increases with V_{IN}, even at no load.

2) The switching current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} that is typically much larger than the DC bias current. In continuous mode, $I_{GATECHG} = f_O(QT + QB)$, where QT and QB are the gate charges of the internal top and bottom MOSFET switches. The gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

3) I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flowing through inductor L is "chopped" between the internal top and bottom switches. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)}TOP)(DC) + (R_{DS(ON)}BOT)(1 – DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses:

$$I^2R \text{ losses} = I_{OUT}2(R_{SW} + R_L)$$

4) Other "hidden" losses such as copper trace and internal battery resistances can account for additional efficiency degradations in portable systems. It is very important to include these "system" level losses in the design of a system. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. Other

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losses including diode conduction losses during dead-time and inductor core losses, which generally account for less than 2% total additional loss.

Thermal Considerations

In a majority of applications, the LTC3565 does not dissipate much heat due to its high efficiency. However, in applications where the LTC3565 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

To avoid the LTC3565 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$$T_J = T_{RISE} + T_{AMBIENT}$$

As an example, consider the case when the LTC3565 is in dropout at an input voltage of 3.3V with a load current of 1A. From the Typical Performance Characteristics graph of Switch Resistance, the $R_{DS(ON)}$ resistance of the P-channel switch is 0.160Ω. Therefore, power dissipated by the part is:

$$P_D = I_{OUT}^2 \bullet R_{DS(ON)} = 160mW$$

The MSE package junction-to-ambient thermal resistance, θ_{JA}, will be in the range of about 40°C/W. Therefore, the junction temperature of the regulator operating in a 70°C ambient temperature is approximately:

$$T_J = 0.16 \bullet 40 + 70 = 76.4°C$$

Remembering that the above junction temperature is obtained from an $R_{DS(ON)}$ at 25°C, we might recalculate the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. However, we can safely assume that the actual junction temperature will not exceed the absolute maximum junction temperature of 125°C.

Design Example

As a design example, consider using the LTC3565 in a portable application with a Li-Ion battery. The battery provides a V_{IN} = 2.5V to 4.2V. The load requires a maximum of 1.25A in active mode and 10mA in standby mode. The output voltage is V_{OUT} = 2.5V. Since the load still needs power in standby, Burst Mode operation is selected for good low load efficiency.

First, calculate the timing resistor for 1MHz operation:

$$R_T = 1.21 \bullet 10^6 \ \ (10^3)^{-1.2674} = 190.8k$$

Use a standard value of 191k. Next, calculate the inductor value for about 40% ripple current at maximum V_{IN}:

$$L = \frac{2.5V}{1MHz \bullet 500mA} \bullet \left(1 - \frac{2.5V}{4.2V}\right) = 2\mu H$$

Choosing the closest inductor from a vendor of 2.2µH, results in a maximum ripple current of:

$$\Delta I_L = \frac{2.5V}{1MHz \bullet 2.2\mu H} \bullet \left(1 - \frac{2.5V}{4.2V}\right) = 460mA$$

For cost reasons, a ceramic capacitor will be used. C_{OUT} selection is then based on load step droop instead of ESR requirements. For a 5% output droop:

$$C_{OUT} \approx 2.5 \frac{1.25A}{1MHz \bullet (5\% \bullet 2.5V)} = 25\mu F$$

The closest standard value is 22µF. Since the output impedance of a Li-Ion battery is very low, C_{IN} is typically 22µF. In noisy environments, decoupling SV_{IN} from PV_{IN} with an R6/C8 filter of 1Ω/0.1µF may help, but is typically not needed.

APPLICATIONS INFORMATION

The output voltage can now be programmed by choosing the values of R1 and R2. To maintain high efficiency, the current in these resistors should be kept small. Choosing 2µA with the 0.6V feedback voltage makes R1~300k. A close standard 1% resistor value is 294k then R2 is 931k.

The compensation should be optimized for these components by examining the load step response but a good place to start for the LTC3565 is with a 12.1kΩ and 680pF filter. The output capacitor may need to be increased depending on the actual undershoot during a load step.

The PGOOD pin is a common drain output and requires a pull-up resistor. A 100k resistor is used for adequate speed.

The circuit on page 1 of this data sheet shows the complete schematic for this design example.

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3565. These items are also illustrated graphically in the layout diagram of Figure 4. Check the following in your layout:

1. Does the capacitor C_{IN} connect to the power V_{IN} (Pin 6) and power GND (Pin 5) as close as possible? This capacitor provides the AC current to the internal power MOSFETs and their drivers.

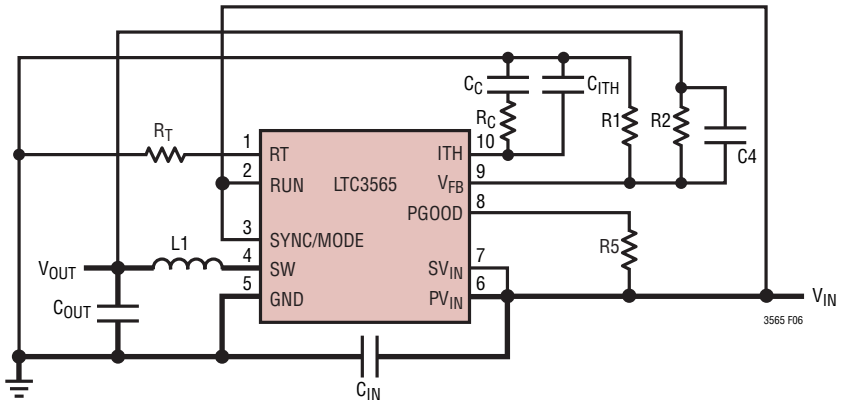
2. Are the C_{OUT} and L1 closely connected? The (–) plate of C_{OUT} returns current to PGND and the (–) plate of C_{IN}.

3. The resistor divider, R1 and R2, must be connected between the (+) plate of C_{OUT} and a ground line. The feedback signal V_{FB} should be routed away from noisy components and traces, such as the SW line (Pin 4), and its trace should be minimized.

4. Keep sensitive components away from the SW pin. The input capacitor C_{IN}, the compensation capacitor C_C and C_{ITH} and all the resistors R1, R2, R_T, and R_C should be routed away from the SW trace and the inductor L1. The SW pin pad should be kept as small as possible.

5. A ground plane is preferred, but if not available, keep the signal and power grounds segregated with small signal components returning to the GND pin at one point.

6. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to one of the input supply rails: PV_{IN}, SV_{IN} or GND.

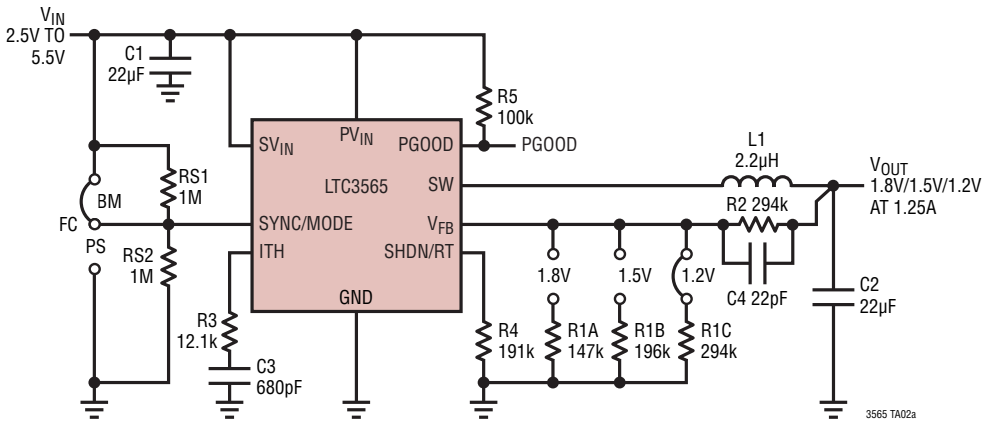


BOLD LINES INDICATE HIGH CURRENT PATHS

Figure 4. LTC3565 Layout Diagram (See Board Layout Checklist)

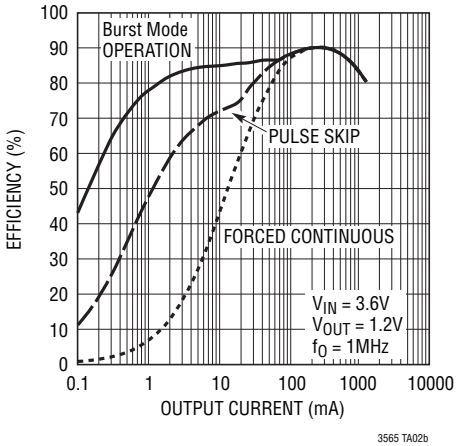
TYPICAL APPLICATION

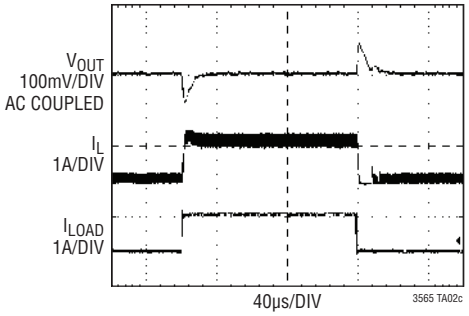
General Purpose Buck Regulator Using Ceramic Capacitors



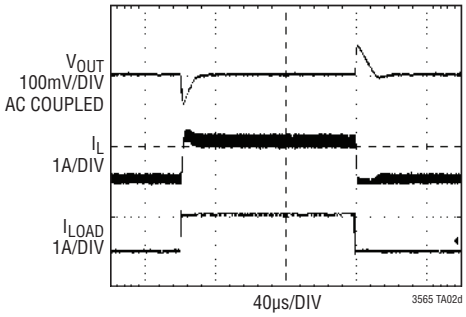
NOTE: IN DROPOUT, THE OUTPUT TRACKS THE INPUT VOLTAGE
C1, C2: TAIYO YUDEN JMK325BJ226MM
L1: TOKO A914BYW-2R2M (D52LC SERIES)

Efficiency vs Output Current





VIN = 3.6V
VOUT = 1.2V
ILOAD = 100mA TO 1.25A
Burst Mode OPERATION

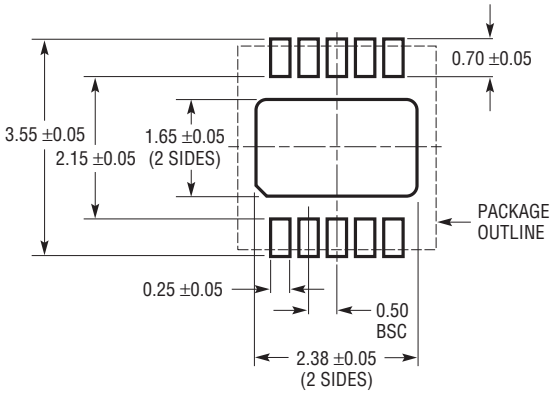


VIN = 3.6V
VOUT = 1.8V
ILOAD = 100mA TO 1.25A
PULSE SKIPPING MODE

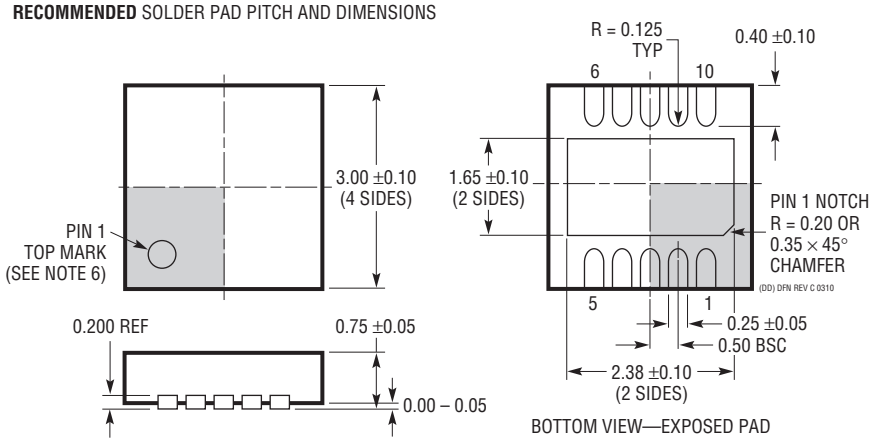
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



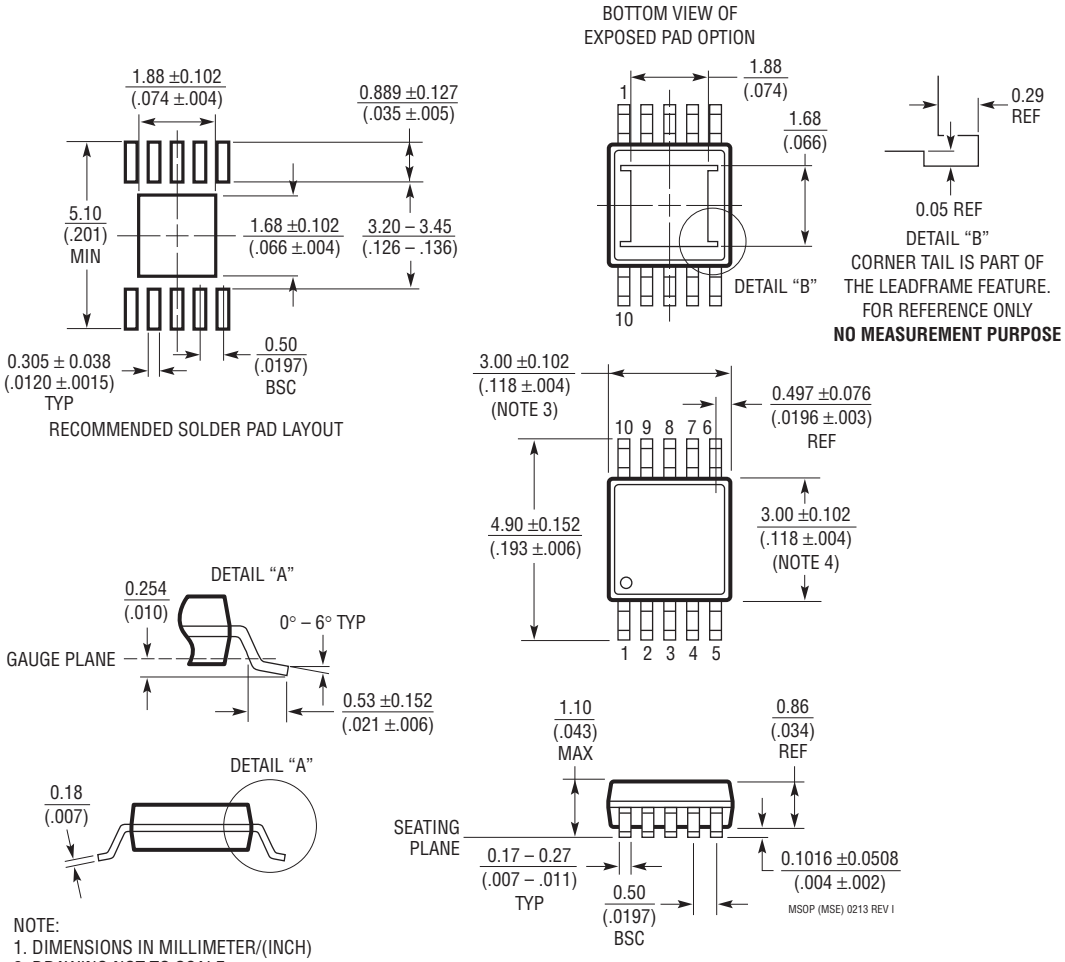
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev I)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

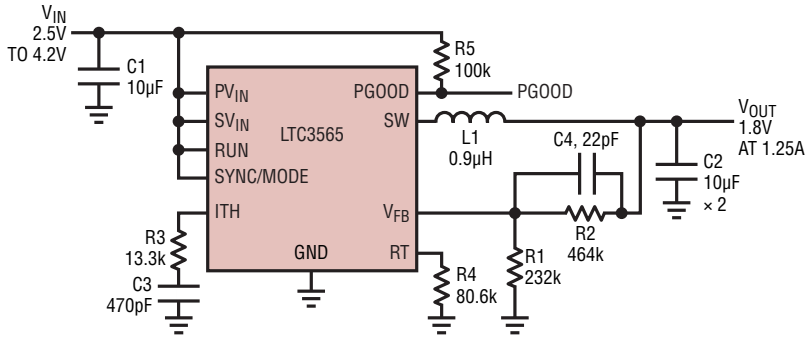
REV	DATE	DESCRIPTION	PAGE NUMBER
A	2/10	Changes to Electrical Characteristics	2, 3
		Change T_A = 25°C to T_J = 25°C	2, 3, 4, 5, 6
		Changes to Pin Functions (GND Pin 5)	8
		Changes to Block Diagram	9
		Updated Related Parts Table	20
B	03/12	Changed Top Marking for DFN Package	2
		Clarified Temperature Grade Test Conditions	3
		Added note for website referral for most recent package drawings	20
C	10/13	Changed parameters and limits on $V_{SYNC-MODE}$ test	3

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

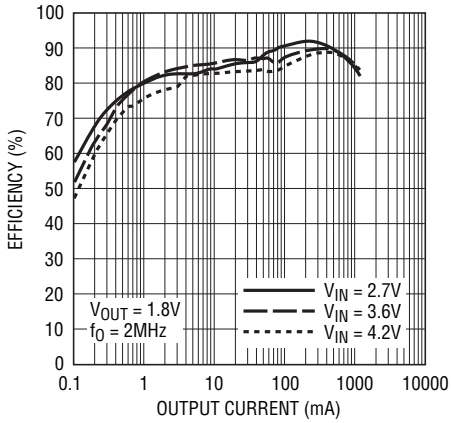
1mm Height, 2MHz, Li-Ion to 1.8V Converter



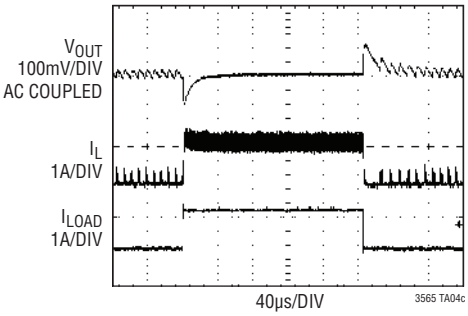
C1, C2: TAIYO YUDEN JMK107BJ106MA
L1: FDK MIPW3226DORGM

3565 TA04a

Efficiency vs Output Current

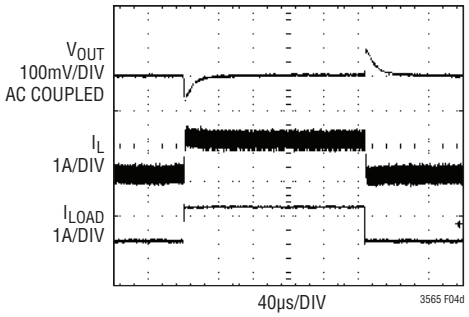


3565 TA04b



3565 TA04c

VIN = 3.6V
VOUT = 1.8V
ILOAD = 50mA TO 1.25A



3565 F04d

VIN = 3.6V
VOUT = 1.8V
ILOAD = 250mA TO 1.25A

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3406/LTC3406B	600mA (I_{OUT}), 1.5MHz Synchronous Step-Down DC/DC Converters	96% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT™
LTC3407A/LTC3407A-2	Dual 600mA/800mA (I_{OUT}), 1.5MHz/2.25MHz Synchronous Step-Down DC/DC Converters	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, MS10E, DFN
LTC3410/LTC3410B	300mA (I_{OUT}), 2.25MHz Synchronous Step-Down DC/DC Converters	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 26µA, I_{SD} < 1µA, SC70
LTC3411A	1.25A (I_{OUT}), 4MHz Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, MS10, 3mm × 3mm DFN
LTC3412A	3A (I_{OUT}), 4MHz Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 62µA, I_{SD} < 1µA, TSSOP16E, 4mm × 4mm QFN
LTC3560	800mA (I_{OUT}), 2.25MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 16µA, I_{SD} < 1µA, ThinSOT
LTC3564	1.25A, 2.25MHz Synchronous Step-Down Regulator	96% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT, 2mm × 3mm DFN-10

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