具有 16-V 过压保护功能的TS5USBC400双路 2:1 USB 2.0 多路复用器/多路信号分离器

1 特性

- 电源范围：2.3V 至 5.5V
- 差分 2:1 或 1:2 开关/多路复用器
- 公共引脚上具有 0V 至 16V 过压保护 (OVP)
- V_{CC} = 0V 时具有断电保护
- 较低的 R_{ON}（最大值为 9Ω）
- 典型带宽为 1.1GHz
- 典型的 C_{ON} 为 4.5pF
- 低功耗禁用模式
- 1.8V 兼容型逻辑输入
- ESD 保护性能超出 JESD 22 标准
  - 2000V 人体模型 (HBM)
- TS5USBC400：标准温度范围为 0°C 至 70°C
- TS5USBC400I：工业温度范围为 -40°C 至 85°C
- 小型 DSBGA 封装

2 应用

- 移动设备
- 台式机/笔记本电脑
- 平板电脑
- 使用 USB Type-C™ 或 Micro-B 连接器的任何场合

3 说明

TS5USBC400 是一种双向低功耗双端口高速 USB 2.0 模拟开关，具有针对 USB Type-C™系统的集成保护功能。该器件配置为双路 2:1 或 1:2 开关，并经过了优化，能够应对 USB Type-C™ 系统中的 USB 2.0 D+/- 线路。

TS5USBC400 在 I/O 引脚上的保护功能可承受高达 16V 的电压，并配备自动关闭电路来保护开关后面的系统组件。

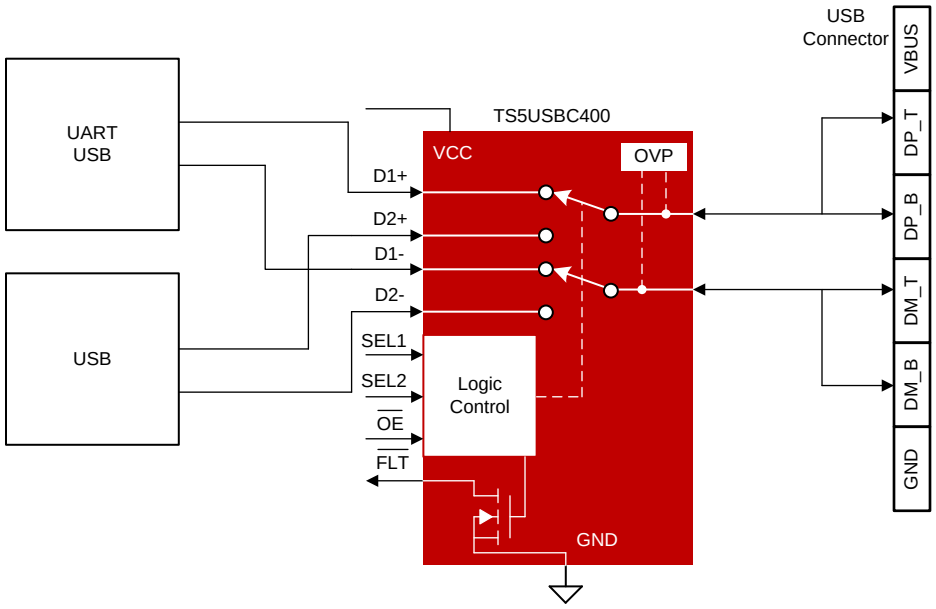
TS5USBC400 采用小型 12 引脚 DSBGA 封装，使其成为移动应用和空间受限型 应用中的杂音问题。中对于高效率、高电源密度和稳健性的需求。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TS5USBC400 TS5USBC400I	DSBGA (12)	1.582mm × 1.182mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化电路原理图



目录

4 修订历史记录

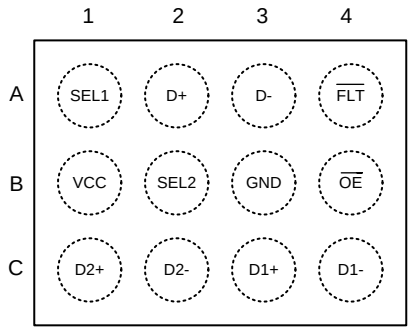
注：之前版本的页码可能与当前版本有所不同。

Changes from Original (September 2017) to Revision A **Page**

- Added I_{CC} Active supply current and Supply current during OVP condition to the E*lectrical Specification* table 4

5 Pin Configuration and Functions

YFP Package
12-Pin DSBGA
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SEL1	A1	I	Switch select1 (Active high)
D+	A2	I/O	Data switch input (Differential +)
D–	A3	I/O	Data switch input (Differential –)
$\overline{FLT}$	A4	O	Fault indicator output pin (Active low) - open drain
VCC	B1	PWR	Supply Voltage
SEL2	B2	I	Switch select2 (Active high)
GND	B3	GND	Ground
$\overline{OE}$	B4	I	Output enable (Active low)
D2+	C1	I/O	Data switch output 2 (Differential +)
D2–	C2	I/O	Data switch output 2 (Differential -)
D1+	C3	I/O	Data switch output 1 (Differential +)
D1–	C4	I/O	Data switch output 1 (Differential -)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(3)		–0.5	6	V
$V_{I/O}$	Input/Output DC voltage (D+, D-)(3)		–0.5	18	V
$V_{I/O}$	Input/Output DC voltage (D1+/D1-, D2+/D2-) (3)		–0.5	6	V
V_I	Digital input voltage (SEL1, SEL2, $\overline{OE}$)		–0.5	6	V
V_O	Digital output voltage ($\overline{FLT}$)		–0.5	6	V
I_K	Input-output port diode current (D+, D-, D1+, D1-, D2+, D2-)	$V_{IN} < 0$	–50		mA
I_{IK}	Digital logic input clamp current (SEL1, SEL2, $\overline{OE}$) (3)	$V_I < 0$	–50		mA
I_{CC}	Continuous current through VCC			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	5.5	V
$V_{I/O\ (D+,\ D-)}$	Analog input/output voltage	0	18	V
$V_{I/O\ (D1,\ D1-,\ D2+,\ D2-)}$		0	3.6	V
V_I	Digital input voltage (SEL1, SEL2, $\overline{OE}$)	0	5.5	V
V_O	Digital output voltage ($\overline{FLT}$)	0	5.5	V
$I_{I/O\ (D+,\ D-,\ D1+,\ D1-,\ D2+,\ D2-)}$	Analog input/output port continuous current	-50	50	mA
I_{OL}	Digital output current		3	mA
T_A	Operating free-air temperature (TS5USBC400) Standard	0	70	ºC
T_A	Operating free-air temperature (TS5USBC400I) Industrial	–40	85	ºC
T_J	Junction temperature	–40	125	ºC

6.4 Thermal Information

THERMAL METRIC (1)		TS5USBC400 YFP 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	91.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = –40°C to +85°C (Industrial), TA = 0℃ to 70℃ (Standard), V_{CC} = 2.3 V to 5.5 V, GND = 0V, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{CC}	Power supply voltage		2.3		5.5	V
I_{CC}	Active supply current	$\overline{OE}$ = 0 V SEL1, SEL2 = 0 V, 1.8 V or V_{CC} 0 V < $V_{I/O}$ < 3.6 V		72	100	µA
	Supply current during OVP condition	$\overline{OE}$ = 0 V SEL1, SEL2 = 0 V, 1.8 V or V_{CC} $V_{I/O}$ > V_{POS_THLD}		80	120	µA
I_{CC_PD}	Standby powered down supply current	$\overline{OE}$ = 1.8 V or V_{CC} SEL1 = 0 V, 1.8 V, or VCC SEL2 = 0 V, 1.8 V, or VCC		2.2	10	µA
DC Characteristics						
R_{ON}	ON-state resistance	$V_{I/O}$ = 0.4 V I_{SINK} = 8 mA Refer to ON-State Resistance Figure		5.6	9	Ω
ΔR_{ON}	ON-state resistance match between channels	$V_{I/O}$ = 0.4 V I_{SINK} = 8 mA Refer to ON-State Resistance Figure		0.07	0.3	Ω
$R_{ON\ (FLAT)}$	ON-state resistance flatness	$V_{I/O}$ = 0 V to 0.4 V I_{SINK} = 8 mA Refer to ON-State Resistance Figure		0.07	0.4	Ω
I_{OFF}	I/O pin OFF leakage current	$V_{D\pm}$ = 0 V or 3.6 V V_{CC} = 2.3 V to 5.5 V $V_{D1\pm}$or $V_{D2+/-}$ = 3.6 V or 0 V Refer to Off Leakage Figure	-1	1.2	6	µA
		$V_{D\pm}$ = 0 V or 16 V V_{CC} = 2.3 V to 5.5 V $V_{D1\pm}$ or $V_{D2+/-}$ = 0 V Refer to Off Leakage Figure	-1	165	200	µA
I_{ON}	ON leakage current	$V_{D\pm}$ = 0 V or 3.6 V $V_{D1\pm}$ and $V_{D2+/-}$ = high-Z Refer to On Leakage Figure	-1	1.2	6	µA
Digital Characteristics						
V_{IH}	Input logic high	SEL1, SEL2, $\overline{OE}$	1.4			V
V_{IL}	Input logic low	SEL1, SEL2, $\overline{OE}$			0.5	V
V_{OL}	Output logic low	$\overline{FLT}$ I_{OL} = 3 mA			0.4	V
I_{IH}	Input high leakage current	SEL1, SEL2, $\overline{OE}$ = 1.8 V, V_{CC}	-1	1	5	µA
I_{IL}	Input low leakage current	SEL1, SEL2, $\overline{OE}$ = 0 V	-1	±0.2	5	µA

Electrical Characteristics (continued)

T_A = –40°C to +85°C (Industrial), TA = 0℃ to 70℃ (Standard), V_{CC} = 2.3 V to 5.5 V, GND = 0V, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PD}	Internal pull-down resistor on digital input pins			6		MΩ
C_I	Digital input capacitance	SEL1, SEL2 = 0 V, 1.8 V or VCC f = 1 MHz		3.4		pF
Protection						
V_{OVP_TH}	OVP positive threshold		4.5	4.8	5.2	V
V_{OVP_HYST}	OVP threshold hysteresis		75	230	425	mV
V_{CLAMP_V}	Maximum voltage to appear on D1± and D2± pins during OVP scenario	$V_{D±}$ = 0 to 18 V t_{RISE} and t_{FALL}(10% to 90 %) = 100 ns R_L = Open Switch on or off $\overline{OE}$ = 0 V	0		9.6	V
		$V_{D±}$ = 0 to 18 V t_{RISE} and t_{FALL}(10% to 90 %) = 100 ns R_L = 50Ω Switch on or off $\overline{OE}$ = 0 V	0		9.0	V
t_{EN_OVP}	OVP enable time	R_{PU} = 10 kΩ to VCC ($\overline{FLT}$) C_L = 35 pF Refer to OVP Timing Diagram Figure		0.6	3	µs
t_{REC_OVP}	OVP recovery time	R_{PU} = 10 kΩ to VCC ($\overline{FLT}$) C_L = 35 pF Refer to OVP Timing Diagram Figure		1.5	5	µs

6.6 Dynamic Characteristics

T_A = –40°C to +85°C (Industrial), TA = 0℃ to 70℃ (Standard), V_{CC} = 2.3 V to 5.5V, GND = 0V, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

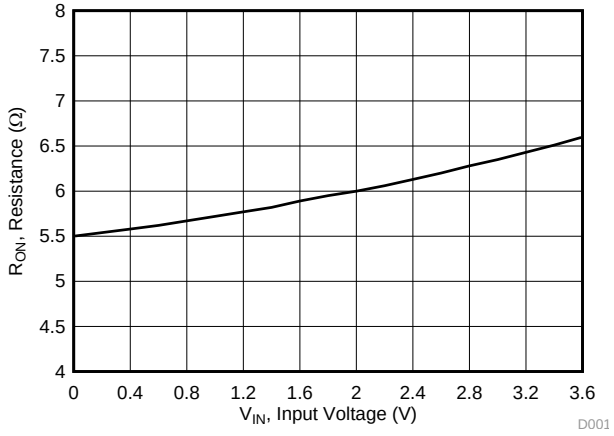
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{OFF}	D+, D- off capacitance	$\overline{V_{D+/-}}$ = 0 or 3.3 V, $\overline{OE}$ = V_{CC} f = 240 MHz	Switch OFF	1.2	3.5	6.2	pF
	D1+, D1-, D2+, D2- off capacitance	$\overline{V_{D+/-}}$ = 0 or 3.3 V, $\overline{OE}$ = V_{CC} or $\overline{OE}$ = 0V with SEL1, SEL2 (switch not selected) f = 240 MHz	Switch OFF or not selected	1.2	3.5	6.2	pF
C_{ON}	IO pins ON capacitance	$V_{D+/-}$ = 0 or 3.3 V, f = 240 MHz	Switch ON	1.4	4.5	6.2	pF
O_{ISO}	Differential off isolation	RL = 50 Ω CL = 5 pF f = 100 kHz Refer to Off Isolation Figure	Switch OFF		-90		dB
		RL = 50 Ω CL = 5 pF f = 240 MHz Refer to Off Isolation Figure	Switch OFF		-22		dB
X_{TALK}	Channel to Channel crosstalk	RL = 50 Ω CL = 5 pF f = 100 kHz Refer to Crosstalk Figure	Switch ON		-90		dB
BW	Bandwidth	RL = 50 Ω; Refer to BW and Insertion Loss Figure	Switch ON		1.1		GHz
I_{LOSS}	Insertion loss	RL = 50 Ω f = 240 MHz; Refer to BW and Insertion Loss Figure	Switch ON		-0.7		dB

6.7 Timing Requirements

T_A = –40°C to +85°C (Industrial), TA = 0℃ to 70℃ (Standard), V_{CC} = 2.3 V to 5.5V, GND = 0V, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
t_{switch}	Switching time between channels (SEL1, SEL2 to output)	$V_{D+/-}$ = 0.8 V Refer to Tswitch Timing Figure	R_L = 50 Ω, C_L = 5 pF, V_{CC} = 2.3 V to 5.5 V		0.45	1.2	µs
t_{on}	Device turn on time ($\overline{OE}$ to output)	$V_{D+/-}$ = 0.8 V Refer to Ton and Toff Figure			100	250	µs
t_{off}	Device turn off time ($\overline{OE}$ to output)	$V_{D+/-}$ = 0.8 V Refer to Ton and Toff Figure			0.35	1	µs
$t_{SK(P)}$	Skew of opposite transitions of same output (between D+ and D-)	$V_{D+/-}$ = 0.4 V Refer to Tsk Figure	R_L = 50 Ω, C_L = 1 pF, V_{CC} = 2.3 V to 5.5 V		9	50	ps
t_{pd}	Propagation delay	$V_{D+/-}$ = 0.4 V Refer to Tpd Figure	R_L = 50 Ω, C_L = 5 pF, V_{CC} = 2.3 V to 5.5 V		130	180	ps

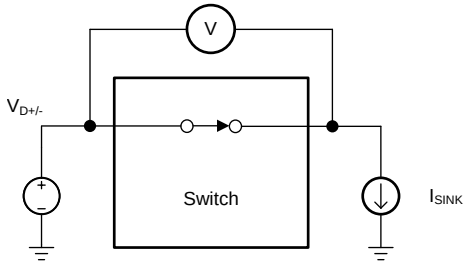
6.8 Typical Characteristics



V_{CC} = 3.3 V T_A = 25°C

图 1. ON-Resistance vs Input Voltage

7 Parameter Measurement Information



Channel ON, $R_{ON} = V/I_{SINK}$

图 2. ON-State Resistance (R_{ON})

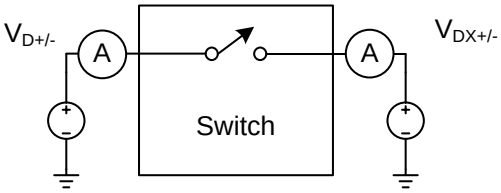


图 3. Off Leakage

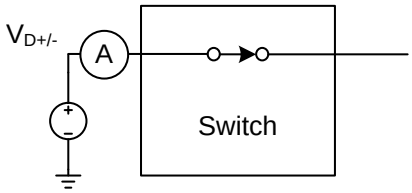
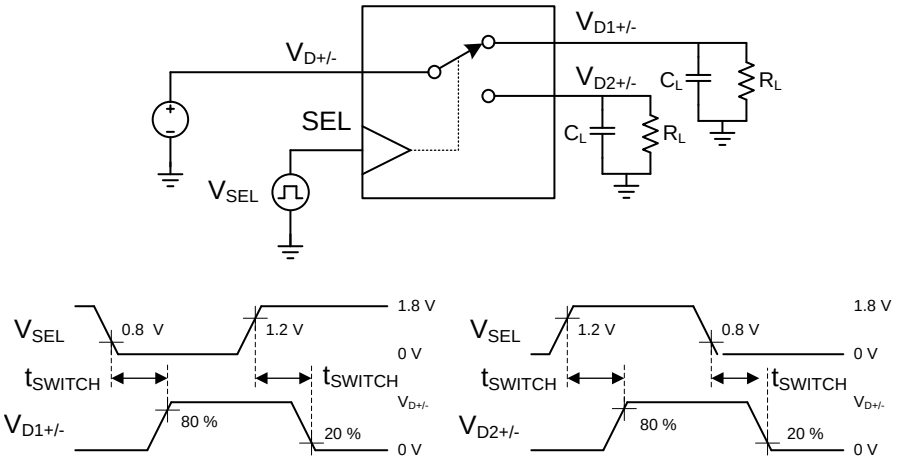


图 4. On Leakage

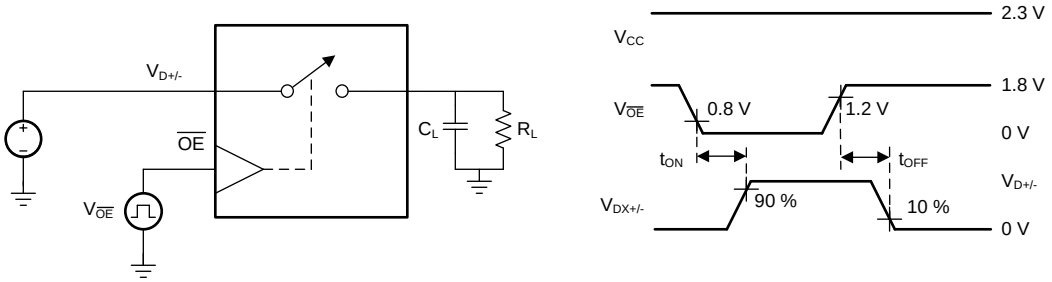


(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 500 ps, t_f < 500 ps.

(2) C_L includes probe and jig capacitance.

图 5. t_{SWITCH} Timing

Parameter Measurement Information (接下页)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 500 ps, t_f < 500 ps.

(2) C_L includes probe and jig capacitance.

图 6. t_{ON}, t_{OFF} for $\overline{OE}$

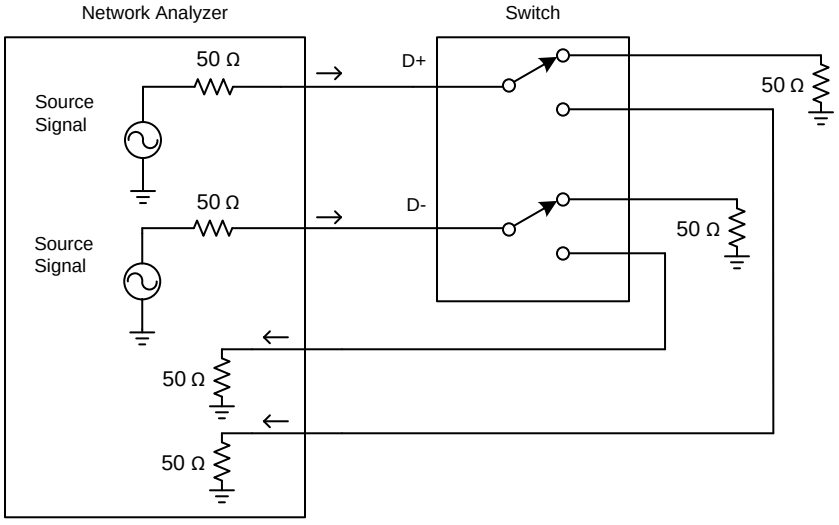


图 7. Off Isolation

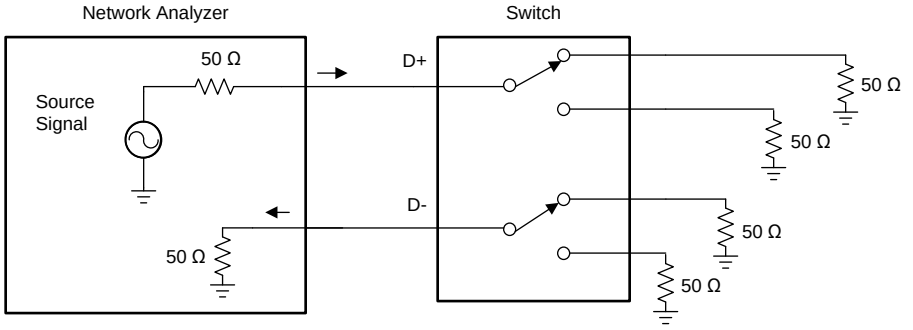


图 8. Cross Talk

Parameter Measurement Information (接下页)

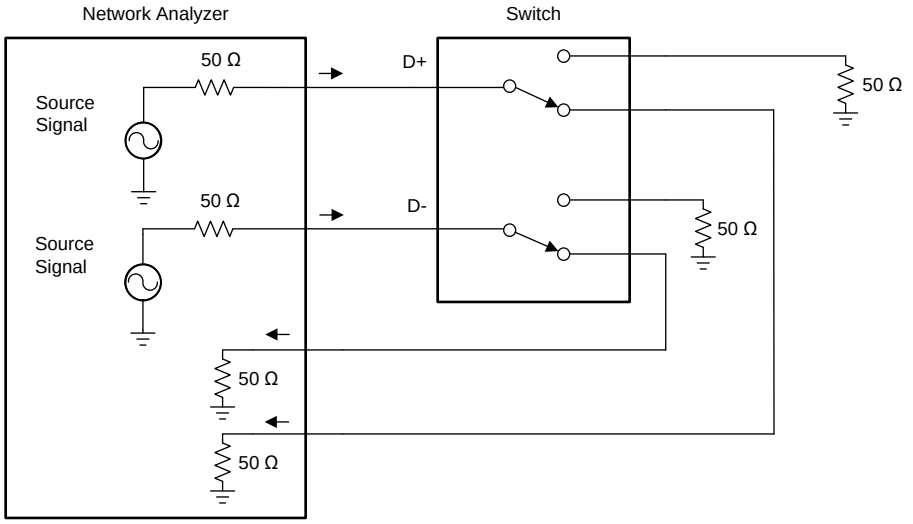


图 9. BW and Insertion Loss

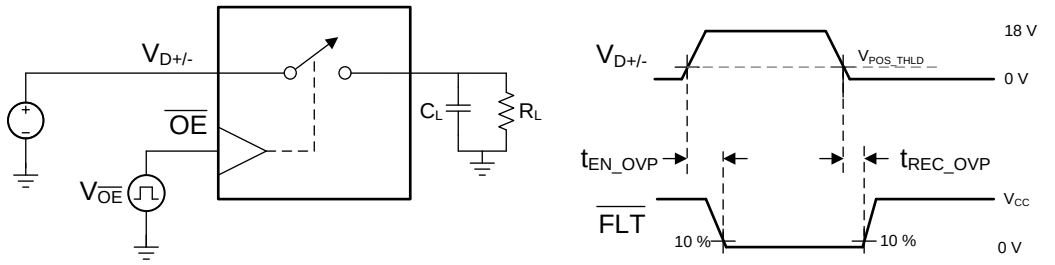
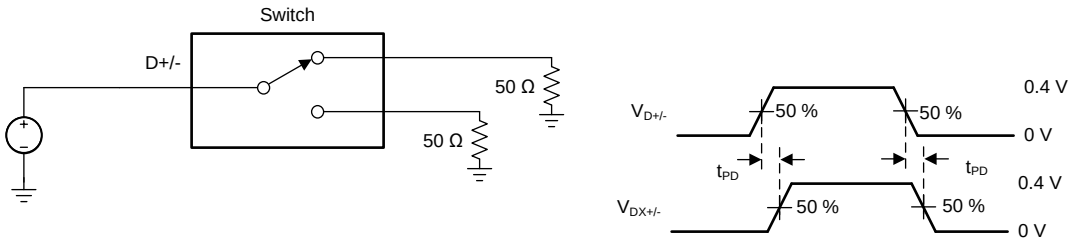


图 10. t_{EN_OVP} and t_{DIS_OVP} Timing Diagram

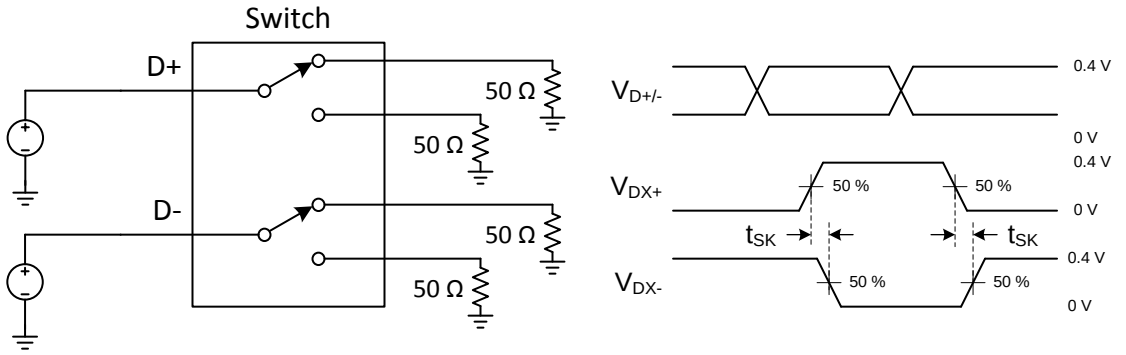


(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 500 ps, t_f < 500 ps.

(2) C_L includes probe and jig capacitance.

图 11. t_{PD}

Parameter Measurement Information (接下页)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 500 ps, t_f < 500 ps.

(2) C_L includes probe and jig capacitance.

图 12. t_{SK}

8 Detailed Description

8.1 Overview

The TS5USBC400 is a bidirectional low-power dual port, high-speed, USB 2.0 analog switch with integrated protection for USB Type-C systems. The device is configured as a dual 2:1 or 1:2 switch and is optimized for handling the USB 2.0 D+/- lines in a USB Type-C system as shown in 图 13.

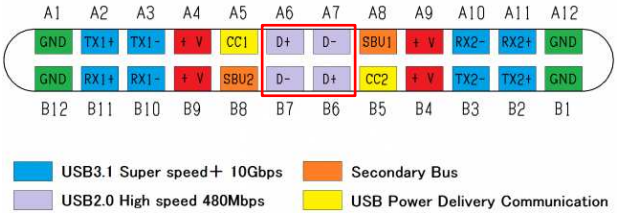
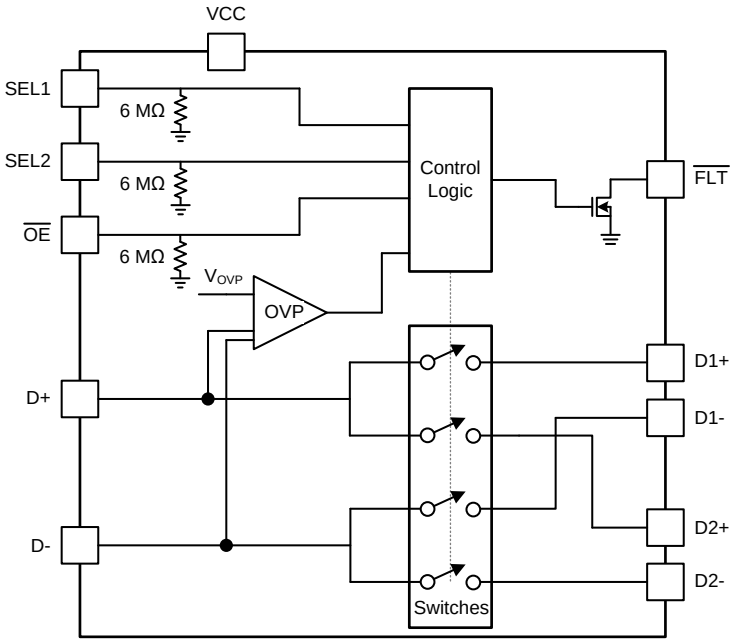


图 13. USB Type-C Connector Pinout

The TS5USBC400 also works in traditional USB systems that need protection from fault conditions such as automotive and applications that require higher voltage charging. The device maintains excellent signal integrity through the optimization of both R_{ON} and BW while protecting the system with 0 V to 16 V OVP protection. The OVP implementation is designed to protect sensitive system components behind the switch that cannot survive a fault condition where VBUS is shorted the D+ and D- pins on the connector.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Powered-off Protection

When the TS5USBC400 is powered off the I/Os of the device remain in a high-Z state. The crosstalk, off-isolation, and leakage remain within the *Electrical Specifications*.

This prevents errant voltages from reaching the rest of the system and maintains isolation when the system is powering up.

8.3.2 Overvoltage Protection

The OVP of the TS5USBC400 is designed to protect the system from D+/- shorts to VBUS at the USB and USB Type-C connector. 图 14 depicts a moisture short that would cause 16 V to appear on an existing USB solution that could pass through the device and damage components behind the device.

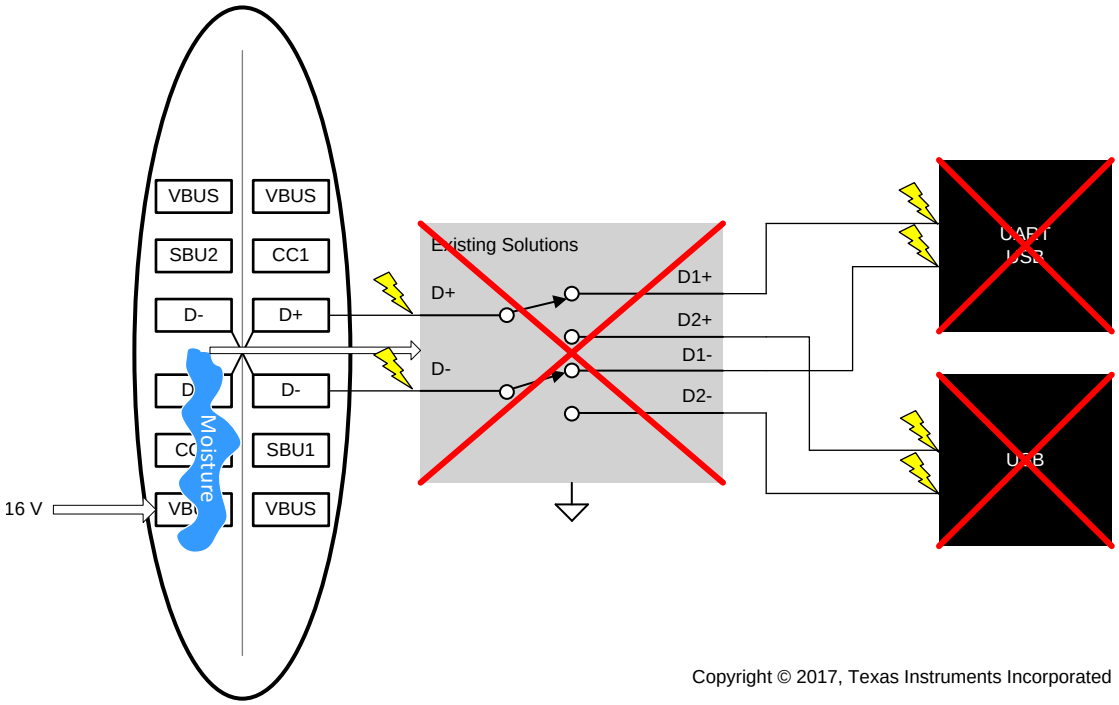


图 14. Existing Solution Being Damaged by a Short, 16 V

The TS5USBC400 will open the switches and protect the rest of the system by blocking the 16 V as depicted in .

Feature Description (接下页)

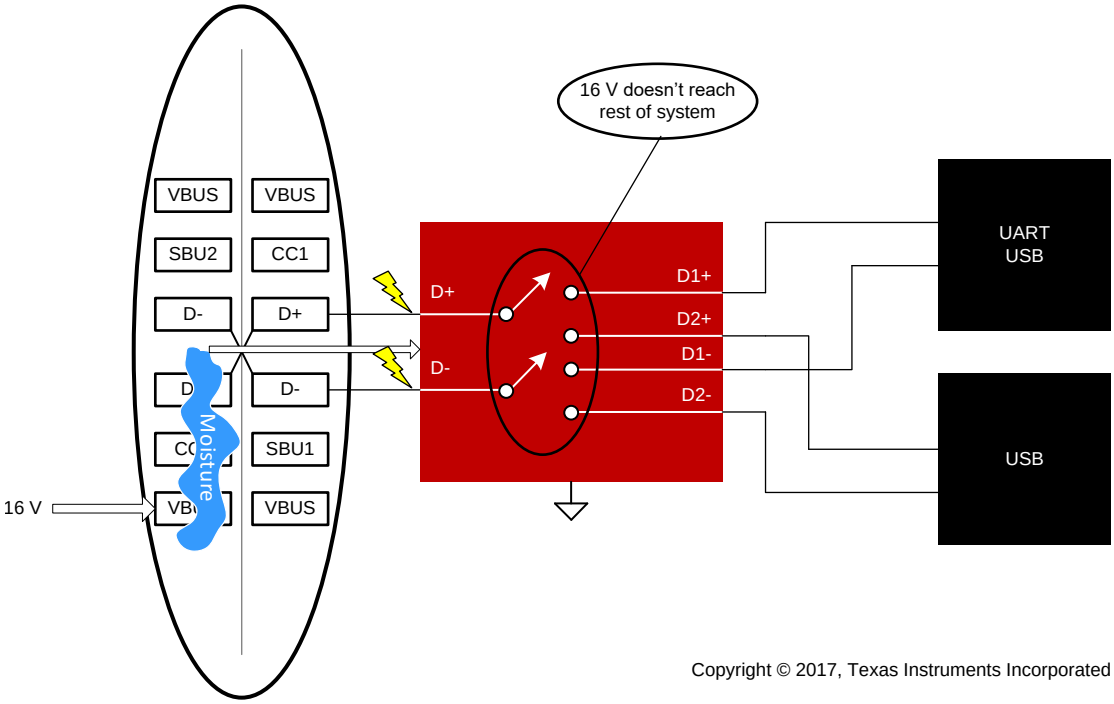


图 15. Protecting During a 16-V Short

图 16 is a waveform showing the voltage on the pins during an over-voltage scenario.

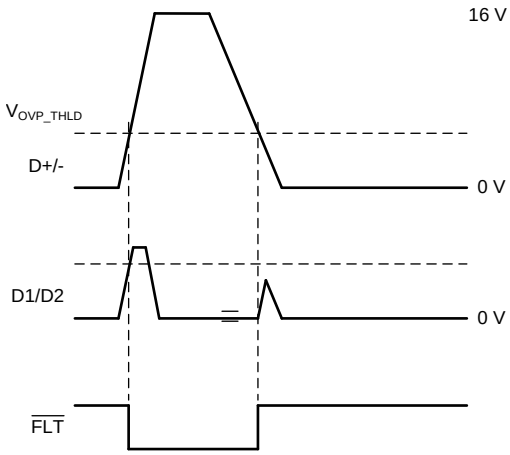


图 16. Overvoltage Protection Waveform, 16 V

8.4 Device Functional Modes

8.4.1 Pin Functions

表 1. Function Table

$\overline{OE}$	SEL1	SEL2	D- Connection	D+ Connection
H	X	X	High-Z	High-Z
L	L	L	D- to D1-	D+ to D1+
L	L	H	D- to D1-	D+ to D2+
L	H	L	D- to D2-	D+ to D1+
L	H	H	D- to D2-	D+ to D2+

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

There are many USB applications in which the USB hubs or controllers have a limited number of USB I/Os or need to route signals from a single USB connector. The TS5USBC400 solution can effectively expand the limited USB I/Os by switching between multiple USB buses to interface them to a single USB hub or controller or route signals from on connector to two different locations. With independent control of the two switches using SEL1 and SEL2, TS5USBC400 can be used to cross switch single ended signals.

9.2 Typical Application

TS5USBC400 USB/UART switch. The TS5USBC400 is used to switch signals between the USB path, which goes to the baseband or application processor, or the UART path, which goes to debug port. The TS5USBC400 has internal 6-MΩ pull-down resistors on SEL1, SEL2, and $\overline{OE}$. The pull-down on SEL1 and SEL2 pins ensure the D1+/D1- channel is selected by default. The pull-down on $\overline{OE}$ enables the switch when power is applied.

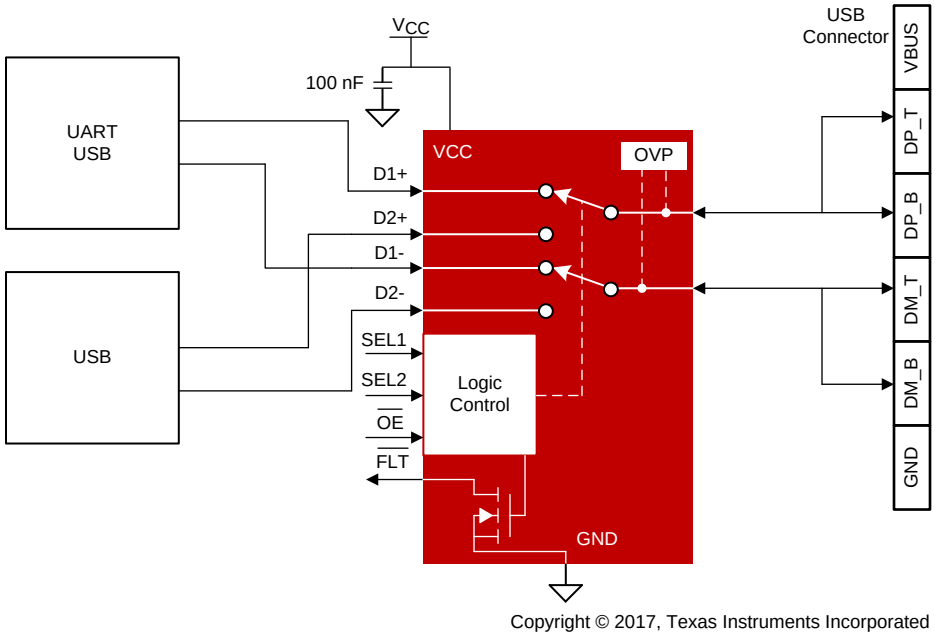


图 17. Typical TS5USBC400 Application

9.2.1 Design Requirements

Design requirements of USB 1.0,1.1, and 2.0 standards must be followed. The TS5USBC400 has internal 6-MΩ pulldown resistors on SEL1, SEL2, and $\overline{OE}$, so no external resistors are required on the logic pins. The internal pull-down resistor on SEL1 and SEL2 pins ensures the D1+ and D1- channels are selected by default. The internal pull-down resistor on $\overline{OE}$ enables the switch when power is applied to VCC.

9.2.2 Detailed Design Procedure

The TS5USBC400can be properly operated without any external components. However, TI recommends that unused pins must be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device. TI does recommend a 100nF bypass capacitor placed close to TS5USBC400 VCC pin.

Typical Application (接下页)

9.2.3 Application Curves

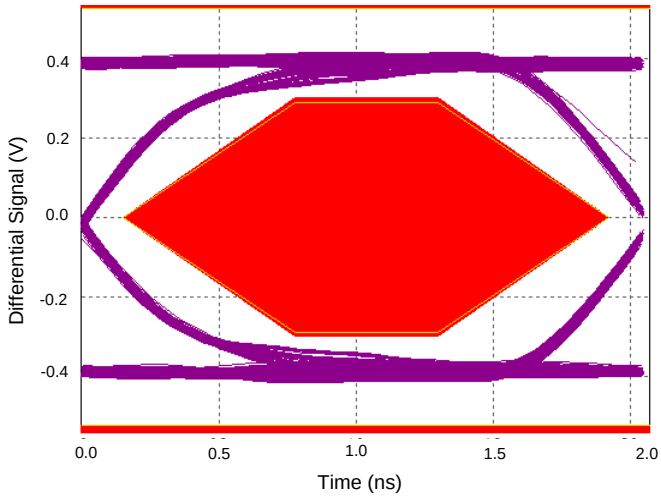


图 18. High Speed Eye Diagram With TS5USBC400

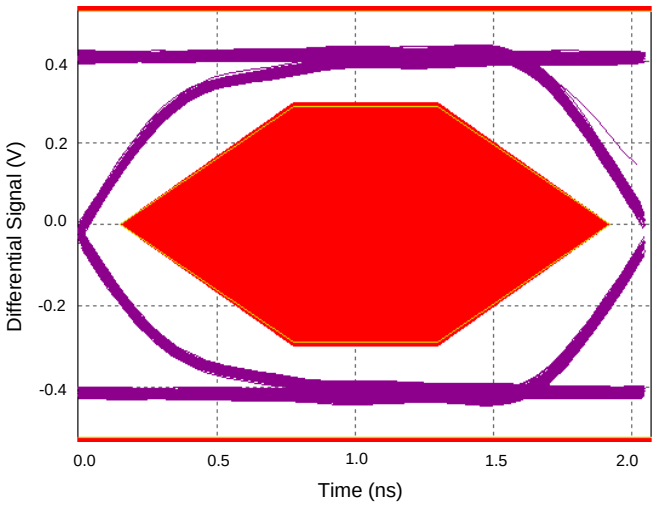


图 19. High Speed Eye Diagram Without TS5USBC400

10 Power Supply Recommendations

Power to the device is supplied through the VCC pin and must follow the USB 1.0, 1.1, and 2.0 standards. TI recommends placing a 100nF bypass capacitor as close to the supply pin VCC as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

11 Layout

11.1 Layout Guidelines

1. Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass caps near the D± traces.
2. The high-speed D± must match and be no more than 4 inches long; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D– traces must match the cable characteristic differential impedance for optimal performance.
3. Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
4. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
5. Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
6. Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub must be less than 200 mm.
7. Route all high-speed USB signal traces over continuous GND planes, with no interruptions.
8. Avoid crossing over anti-etch, commonly found with plane splits.
9. Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in 图 20.

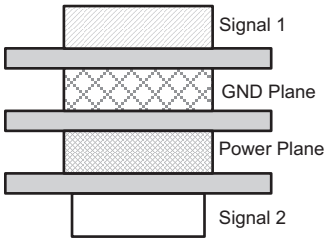


图 20. Four-Layer Board Stack-Up

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

11.2 Layout Example

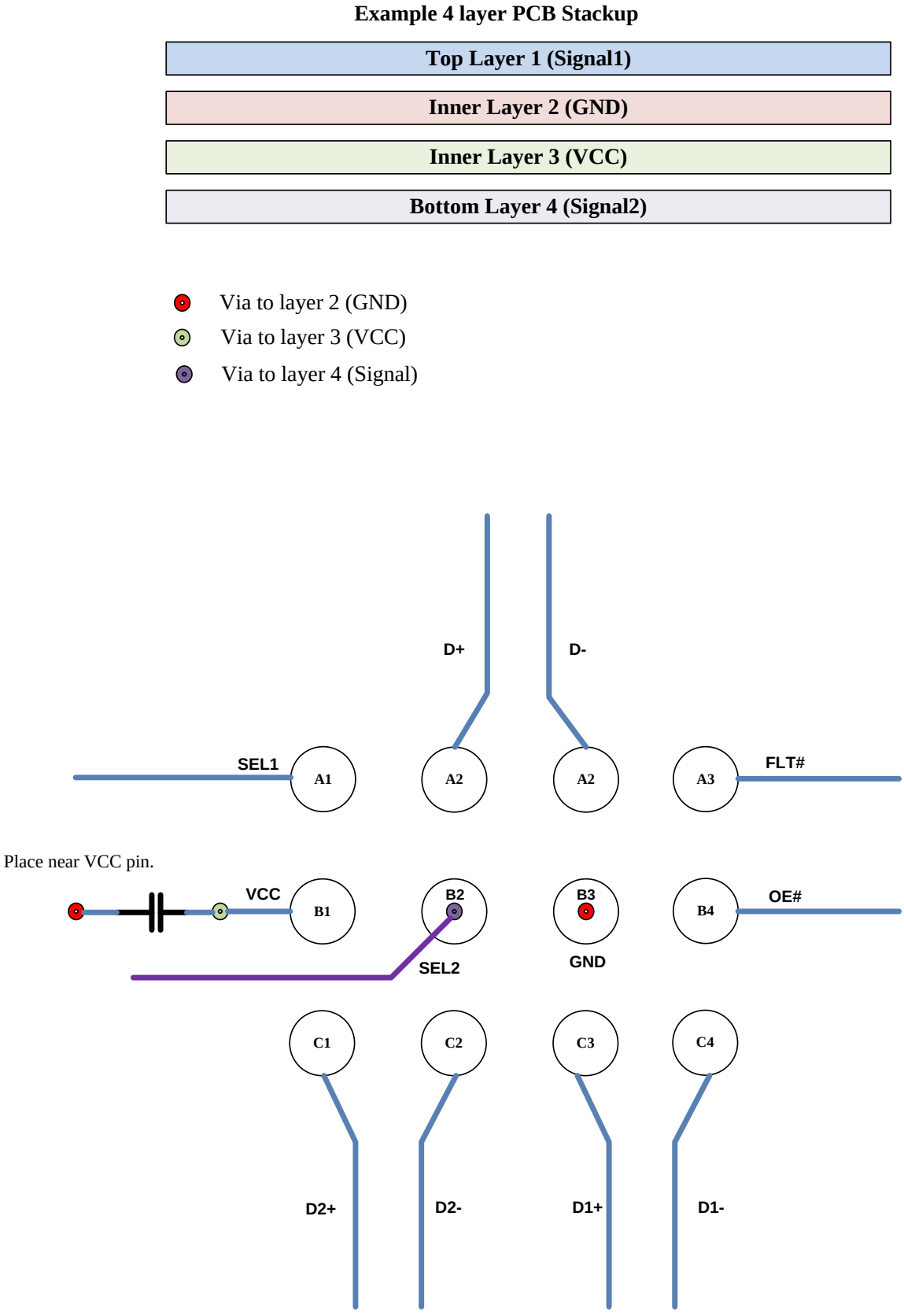


图 21. Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- *USB 2.0 电路板设计及布线指南*
- *应用报告《高速布局指南》*
- *《高速接口布局指南》*

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.3 商标

E2E is a trademark of Texas Instruments.
USB Type-C is a trademark of USB Implementers Forum.
All other trademarks are the property of their respective owners.

12.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 Glossary

SLYZ022 — *TI Glossary*.

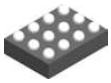
This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

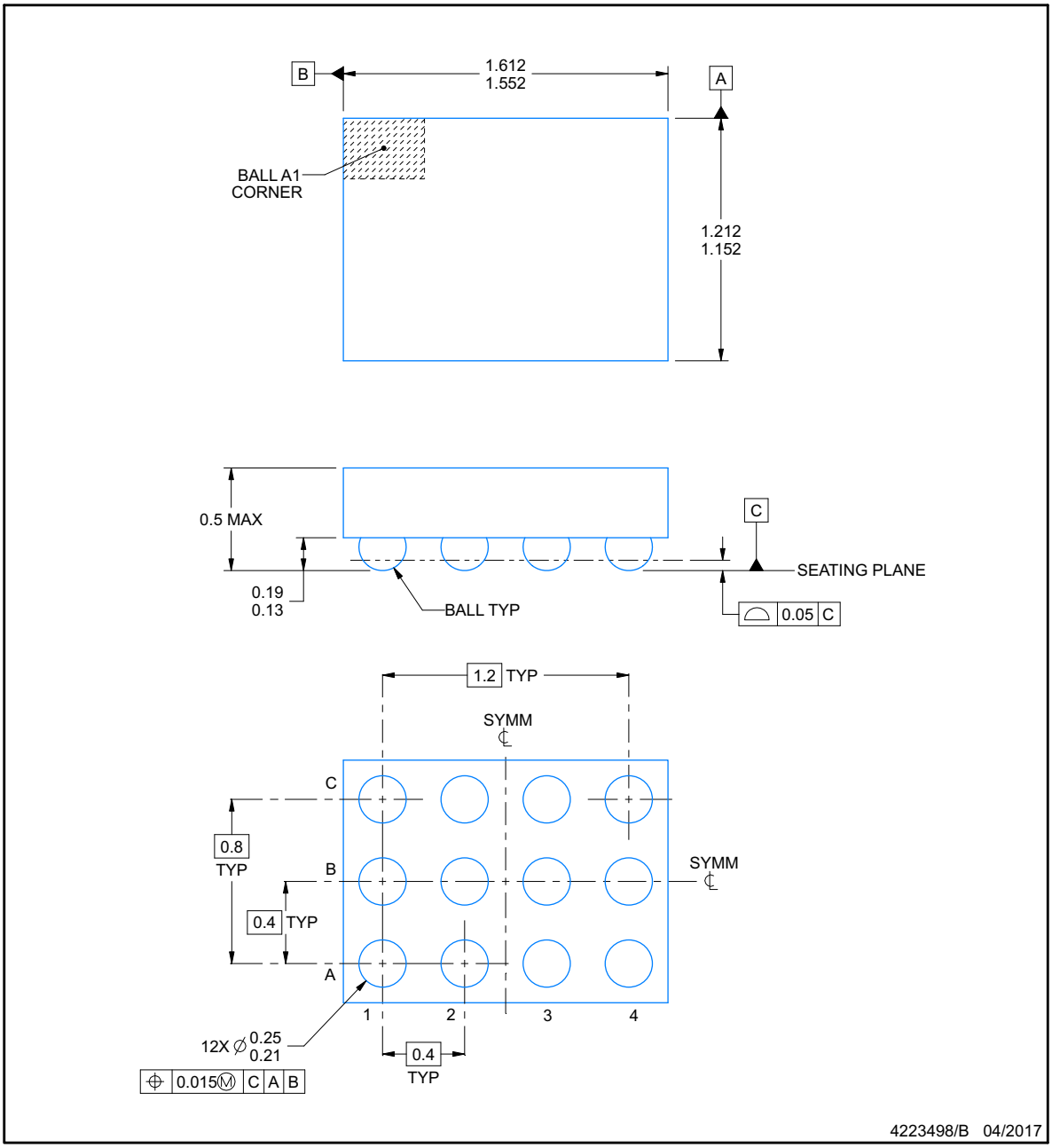
PACKAGE OUTLINE

YFP0012-C01



DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

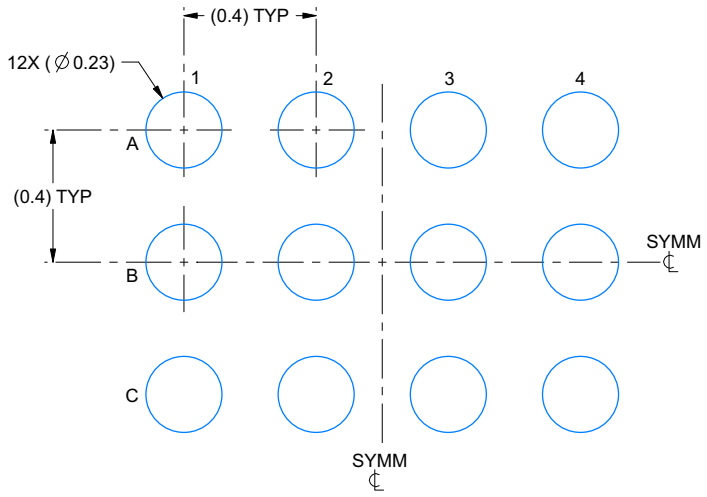
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

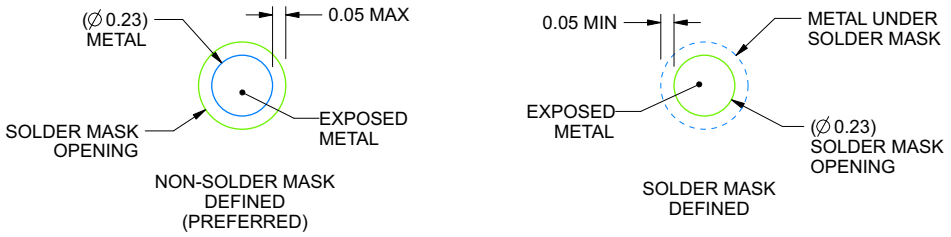
YFP0012-C01

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4223498/B 04/2017

NOTES: (continued)

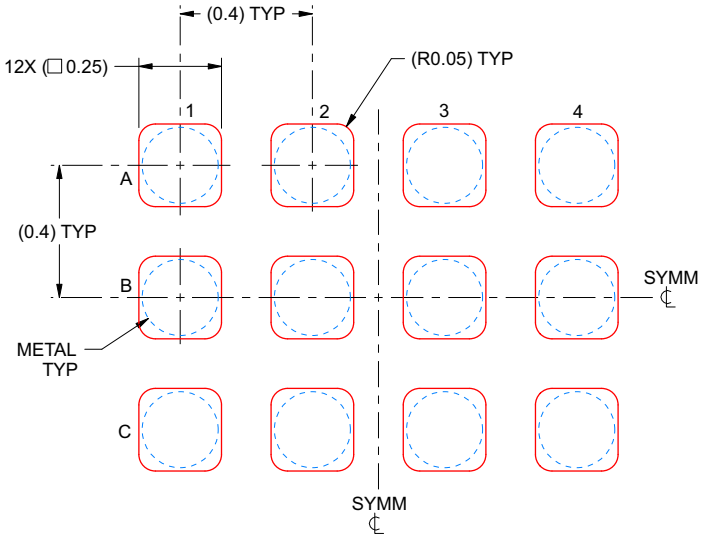
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0012-C01

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223498/B 04/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5USBC400IYFPR	ACTIVE	DSBGA	YFP	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	USB4	Samples
TS5USBC400IYFPT	ACTIVE	DSBGA	YFP	12	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	USB4	Samples
TS5USBC400YFPR	ACTIVE	DSBGA	YFP	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	0 to 70	USB4	Samples
TS5USBC400YFPT	ACTIVE	DSBGA	YFP	12	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	0 to 70	USB4	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

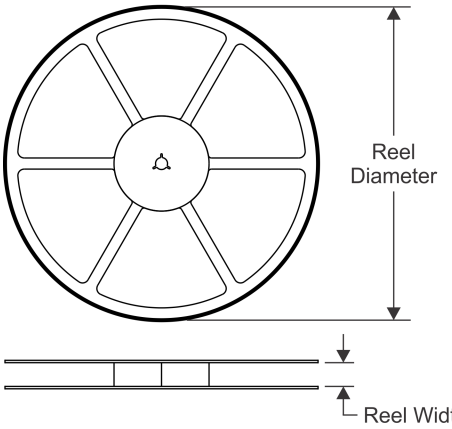
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

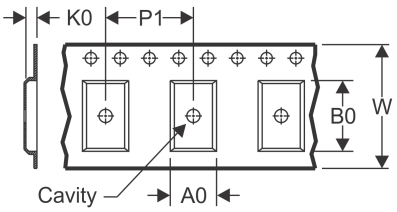
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

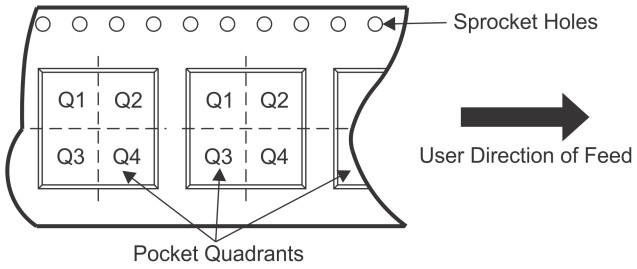


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

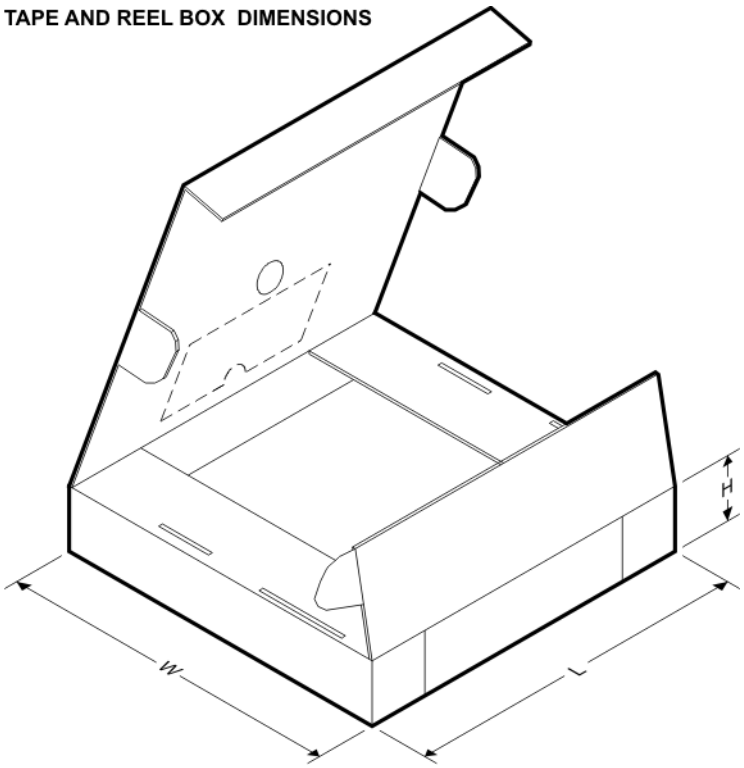
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5USBC400IYFPR	DSBGA	YFP	12	3000	180.0	8.4	1.32	1.72	0.62	4.0	8.0	Q2
TS5USBC400IYFPT	DSBGA	YFP	12	250	180.0	8.4	1.32	1.72	0.62	4.0	8.0	Q2
TS5USBC400YFPR	DSBGA	YFP	12	3000	180.0	8.4	1.32	1.72	0.62	4.0	8.0	Q2
TS5USBC400YFPT	DSBGA	YFP	12	250	180.0	8.4	1.32	1.72	0.62	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5USBC400IYFPR	DSBGA	YFP	12	3000	182.0	182.0	20.0
TS5USBC400IYFPT	DSBGA	YFP	12	250	182.0	182.0	20.0
TS5USBC400YFPR	DSBGA	YFP	12	3000	182.0	182.0	20.0
TS5USBC400YFPT	DSBGA	YFP	12	250	182.0	182.0	20.0

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122