Rev 0; 11/07

100MHz HCSL Clock Generator

DS4100H

General Description

The DS4100H is a low-jitter 100MHz clock generator with a high-speed current steering logic (HCSL) output. It combines an AT-cut crystal, an oscillator, and a low-noise phase-locked loop (PLL) in a 5mm by 3.2mm ceramic package. Typical phase jitter is 0.9ps$_{RMS}$ from 12kHz to 20MHz. The device operates from a single +3.3V supply.

Applications

PCI Express®

Features

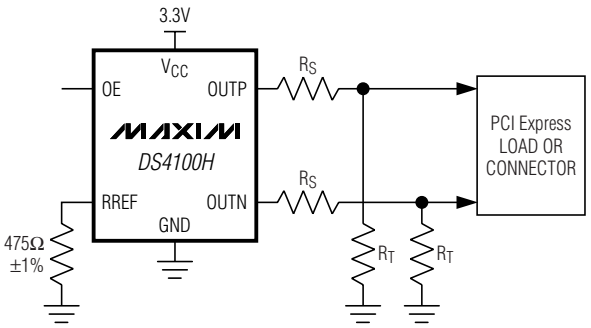
- **100MHz Output Frequency**
- **3.3V ±5% Operating Voltage**
- **HCSL Output**
- **Phase Jitter (RMS): 0.9ps Typical**
- **±39ppm Frequency Stability Over Voltage, Temperature, 10 Years of Aging**
- **Output-Enable (OE) Control Input**
- **5mm x 3.2mm x 1.49mm Ceramic Package (LCCC)**
- **Pb Free/RoHS Compliant**

Ordering Information

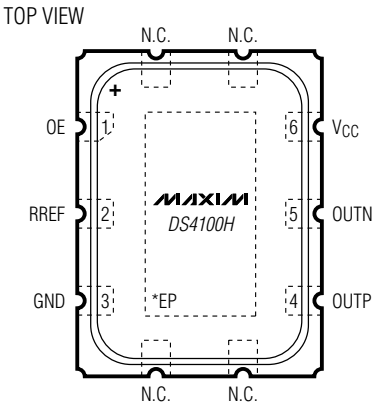
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
DS4100H+	-40°C to +85°C	10 LCCC	10H

+Denotes a lead-free package. The lead finish is JESD97 category e4 (Au over Ni) and is compatible with both lead-based and lead-free soldering processes.

Typical Operating Circuit



Pin Configuration



LCCC
(5.00mm × 3.20mm × 1.49mm)

*EXPOSED PAD

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For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

100MHz HCSL Clock Generator

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC}) .....-0.3V, +4V
Continuous Power Dissipation (T_A = +70°C) 280mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-40°C to +85°C
Soldering Temperature Profile
(3 passes max) .....Refer to the IPC/JEDEC J-STD-020 specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.135V to 3.465V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	3.135	3.300	3.465	V
Supply Current	I_{CC}	OE = V_{IH}, Figure 2			85	mA
Input High Voltage (OE)	V_{IH}	(Note 1)	2.0		V_{CC}	V
Input Low Voltage (OE)	V_{IL}	(Note 1)	0		0.8	V
Input Leakage Current (OE)	I_{IN}	GND ≤ OE ≤ V_{CC}	-55		+10	µA
HCSL OUTPUTS (OUTP, OUTN)						
Output High Current	I_{OH}	475Ω resistor connected between RREF and GND, V_{OUTN} or V_{OUTP} = 1.2V, V_{CC} = 3.3V ±5%	12.25	13.92	15.59	mA
Output High Voltage	V_{OH}	R_S = 0Ω, R_T = 50Ω (Notes 1, 2)	612.5	696.0	779.5	mV
Output Low Voltage	V_{OL}	R_S = 0Ω, R_T = 50Ω (Notes 1, 2)		0	50	mV
Output Leakage High Current	$I_{_LEAKH}$	V_{OE} = 0; V_{OUTN}, V_{OUTP} = V_{CC}	-10		+10	µA
Output Leakage Low Current	$I_{_LEAKL}$	V_{OE} = 0; V_{OUTN}, V_{OUTP} = 0	-10		+10	µA
Output Resistance	R_O	Measure current out of OUTN pin at V_{OUTN} = 0.5V and 1.0V; R_O = 0.5 / $I_{0.5}$ - $I_{1.0}$	3000			Ω
Crossover Voltage	V_{CROSS}	Measure crossing voltage at OUTP and OUTN (Notes 1, 2, and 3)	(50% x V_{OH}) ±5%			mV
Output Rise Time	t_R	20% to 80%, CL = 2pF	175		700	ps
Output Fall Time	t_F	80% to 20%, CL = 2pF	175		700	ps
Overshoot	V_{OVER}	Measure overshoot voltage at OUTP and OUTN (Notes 1, 2, and 3)	V_{OH} + 0.2V			V
Undershoot	V_{UNDER}	Measure undershoot voltage at OUTP and OUTN (Notes 1, 2, and 3)	-0.2			V
Output-Enable Time to Low Level	t_{PZL}	Figure 3 (Note 4)			200	ns
Output-Enable Time to High Level	t_{PZH}	Figure 3 (Note 5)			200	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.135V to 3.465V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Disable Time	t_{PZ}	Figure 3 (Note 6)			10	ns
CLOCK OUTPUT AS MEASURED AT OUTP WITH RESPECT TO OUTN						
Clock Output	f_{OUT}			100		MHz
Frequency Stability Total	$\Delta f / f_O$	Over temperature range, aging, load, and supply (Note 7)	-39		+39	ppm
Initial Frequency Tolerance	f_TOL	V_{CC} = 3.3V, T_A = +25°C		±15		ppm
Frequency Stability vs. Temperature	$\Delta f / f_O \mid T_A$	V_{CC} = 3.3V	-30		+30	ppm
Frequency Stability vs. V_{CC}	$\Delta f / f_O \mid V$	V_{CC} = 3.3V ±5%	-3		+3	ppm/V
Frequency Stability vs. Load	$\Delta f / f_O \mid LOAD$	±10% variation in termination resistance		±1		ppm
Aging (10 Years)	f_{AGING}		-7		+7	ppm
Phase Jitter (RMS)	PJ_{RMS}	12kHz to 20MHz		0.9		ps
Accumulated Deterministic Jitter Due to Power-Supply Noise (Note 8)	$DJ_{PN,P-P}$	10kHz		3.0		ps
		100kHz		27		
		200kHz		15		
		1MHz		7.0		
Rise and Fall Time Mismatching		20% to 80%; CL = 2pF; Figure 2; $2 \times (t_R - t_F) / (t_R + t_F)$		±20		%
Duty Cycle	t_{DC}	Measure at OUTP and OUTN, Figure 2	45		55	%
Oscillation Startup Time		(Note 9)		3		ms
Clock Output SSB Phase Noise		100Hz		-90.0		ps
		1kHz		-112		
		10kHz		-115		
		100kHz		-123		
		1MHz		-142		
		10MHz		-147		

Note 1: All voltages are referenced to ground.

Note 2: With 50Ω load to ground on each output pin.

Note 3: Guaranteed by design and not production tested.

Note 4: t_{PZL} is defined as the time at which VOE = 1.0V on the rising edge of OE to the time at which V_{OUTP} or V_{OUTN} = $0.1V_{OH}$ on the falling edge of OUTP or OUTN.

Note 5: t_{PZH} is defined as the time at which the voltage on the rising edge of OE is equal to 1.0V to the time at which V_{OUTP} or V_{OUTN} = $0.9V_{OH}$ on the rising edge of V_{OUTP} or V_{OUTN}.

Note 6: t_{PZ} is defined as the time at which VOE = 1.0V on the falling edge of OE to the time at which both V_{OUTP} and V_{OUTN} are less than $0.1V_{OH}$.

Note 7: Frequency stability is calculated as: $\Delta f_{TOTAL} = \Delta f_{TEMP} + \Delta f_{VCC} \times 0.165 + \Delta f_{LOAD} + \Delta f_{AGING}$.

Note 8: Measured with $50mV_{P-P}$ sinusoidal signal on the supply from 10kHz to 1MHz.

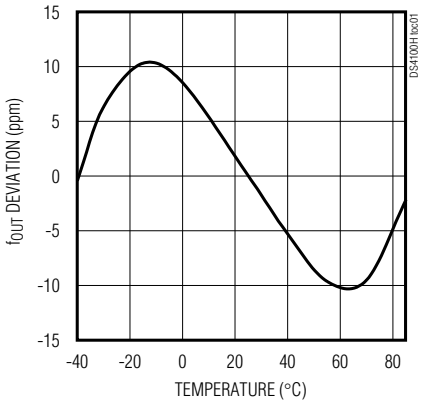
Note 9: Including oscillator startup time and PLL acquisition time measured after V_{CC} reaches 3.0V from power-on.

100MHz HCSL Clock Generator

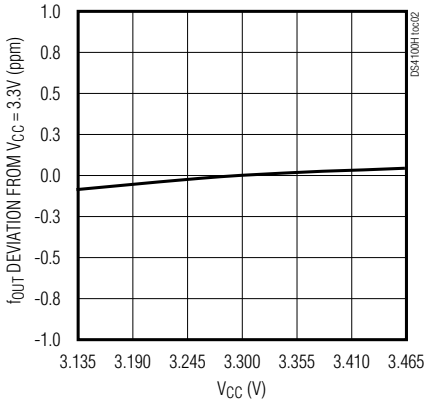
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

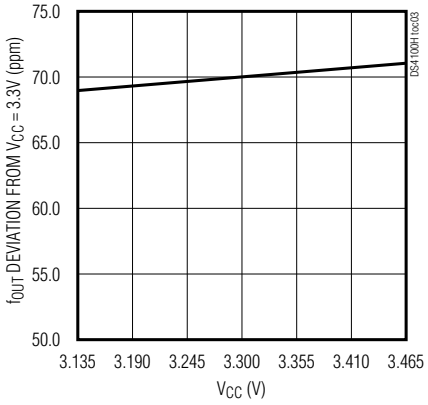
FREQUENCY vs. TEMPERATURE



CLOCK OUTPUT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



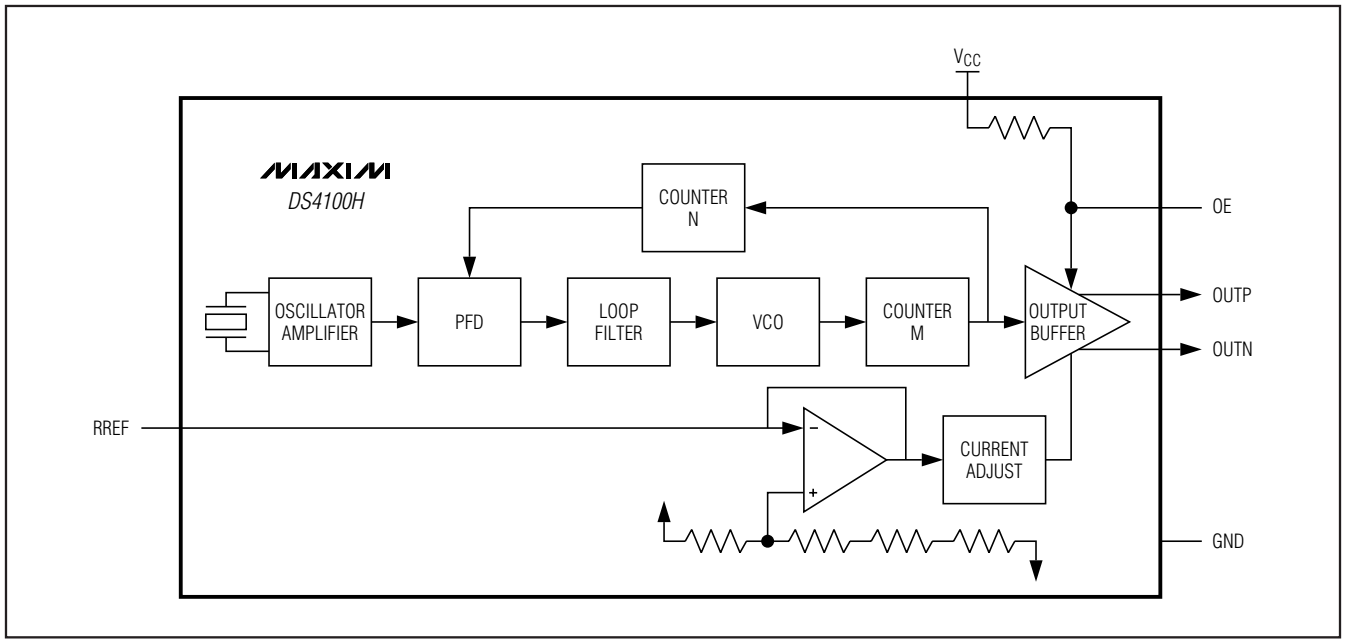


Figure 1. Functional Diagram

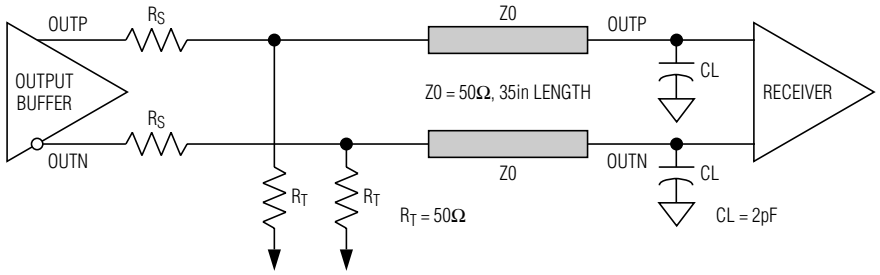


Figure 2. Typical Termination for HCSL Driver and Test Conditions

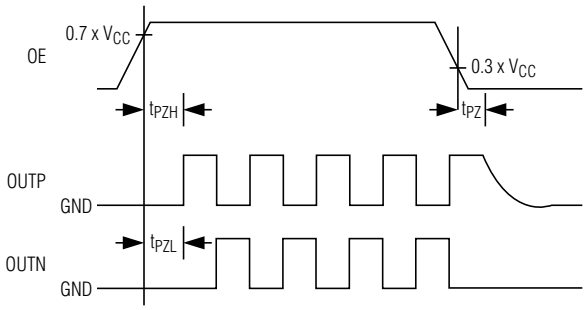


Figure 3. HCSL Output Timing Diagram When OE is Enabled and Disabled

Pin Description

PIN	NAME	FUNCTION
1	OE	Output Enable. On-chip pullup resistor. If connected to logic-high or left open, the clock output is enabled. If connected to logic-low, the output is three-stated.
2	RREF	Connect a 475Ω ±1% resistor from RREF to ground.
3	GND	Ground
4	OUTP	Positive Clock Output. Requires a series resistor and a pulldown resistor.
5	OUTN	Negative Clock Output. Requires a series resistor and a pulldown resister.
6	V_{CC}	+3.3V Supply Input. Device power can range from 3.135V to 3.465V.
7–10	N.C.	No Connection
—	EP	Exposed Paddle. The exposed pad must be used for thermal relief. This pad can be connected to ground.

100MHz HCSL Clock Generator

Detailed Description

The DS4100H is a low-jitter HCSL 100MHz clock generator. It combines an AT-cut crystal, an oscillator, and a low-noise PLL in a 5mm by 3.2mm ceramic package. The typical phase jitter is $0.9ps_{RMS}$ from 12kHz to 20MHz. The device operates from a single +3.3V supply.

PLL

The PLL generates a 1.6GHz high-speed clock signal based on the 25MHz crystal oscillator output. Clock-divider circuit M generates the output clock by scaling the VCO output frequency. Clock-divider circuit N applies a scaled version of the output clock signal to the phase/frequency detector (PFD) circuit.

Output Drivers

The DS4100H is available with HCSL output buffers. When not needed, the output buffers can be disabled by driving the OE input to a logic-low. OE has an internal pullup resistor so that, if OE is left open, the outputs are enabled by default. When disabled, the output buffer goes to a high-impedance state.

Chip Information

TRANSISTOR COUNT: 2850

SUBSTRATE CONNECTED TO GROUND

PROCESS: Bipolar SiGe

Thermal Information

THETA-JA (°C/W)
90

Package Information

(For the latest package outline information go to **www.maxim-ic.com/DallasPackInfo**.)

PACKAGE TYPE	DOCUMENT NO.
10 LCCC	56-G5032-002

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