FEATURES

- Internal LDO allows single 21V operation
- Output Voltage Range: 0.5V to 0.875*PVin
- 0.5% accurate Reference Voltage
- Programmable Switching Frequency up to 1.5MHz using Rt/Sync pin or PMBus
- Internal Soft-Start with Pre-Bias Start-up
- Enable input with Voltage Monitoring Capability
- Remote Sense Amplifier with True Differential Voltage Sensing
- Fast mode I2C and 400 kHz PMBus interface
- Sequencing and tracking capable
- Selectable analog mode or digital mode
- 66 PMBus commands for configuration, control, fault protection and telemetry.
- Thermally compensated current limit with configurable overcurrent responses
- Optional light load efficiency mode
- External synchronization with Smooth Clocking
- Dedicated output voltage sensing protection which remains active even when Enable is low.
- Integrated MOSFETs and Bootstrap diode
- Operating junction temp: -40°C<Tj<125°C
- Small Size 5mmx7mm PQFN
- Pb-Free (RoHS Compliant)

DESCRIPTION

The IR38062 PMBus SupIRBuck™ is an easy-to-use, fully integrated and highly efficient DC/DC regulator with I2C/PMBus interface. The onboard PWM controller and MOSFETs make IR38062 a space-efficient solution, providing accurate power delivery for low output voltage and high current applications.

The IR38062 can be comprehensively configured via PMBus and the configuration stored in internal memory. In addition, PMBus commands allow run-time control, fault status and telemetry.

The IR38062 can also operate as a standard analog regulator without any programming and can provide current and temperature telemetry in an analog format.

APPLICATIONS

Server Applications

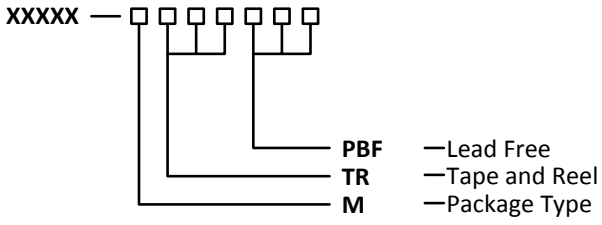
Netcomm applications

Embedded telecom Systems

Distributed Point Of Load Architectures

ORDERING INFORMATION

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IR38062	QFN 5 mm x 7 mm	Tape and Reel	4000	IR38062MTRPBF



BASIC APPLICATION

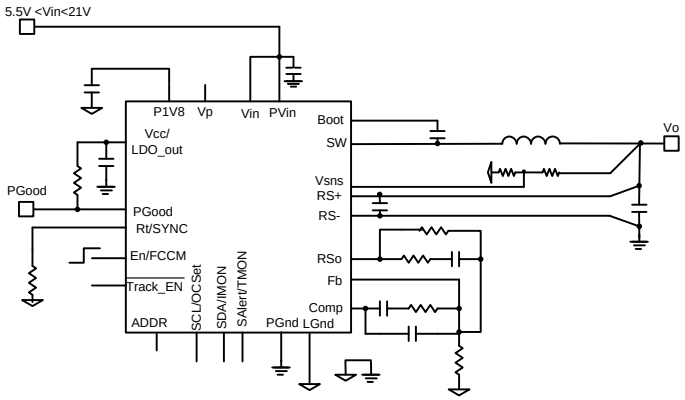


Figure 1: Typical Application Circuit

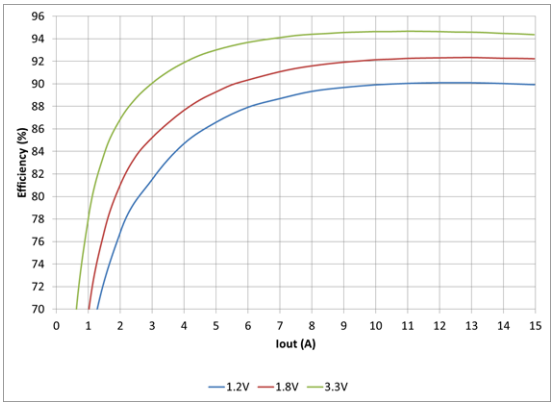
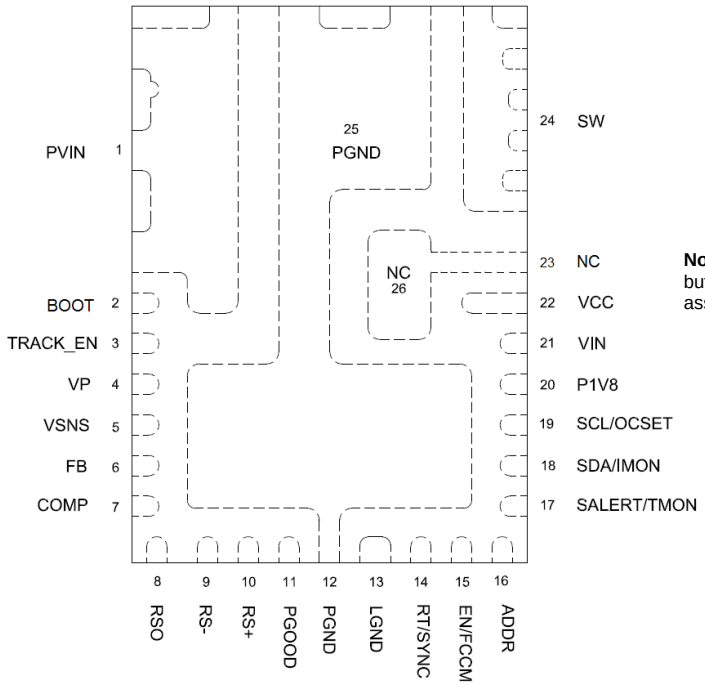


Figure 2: Performance Curve

PINOUT DIAGRAM



Note: Pins 23 and 26 are connected internally but appear separated externally (refer to assembly drawing)

Figure 3: IR38062 package (Top View) 5mm x 7mm PQFN

BLOCK DIAGRAM

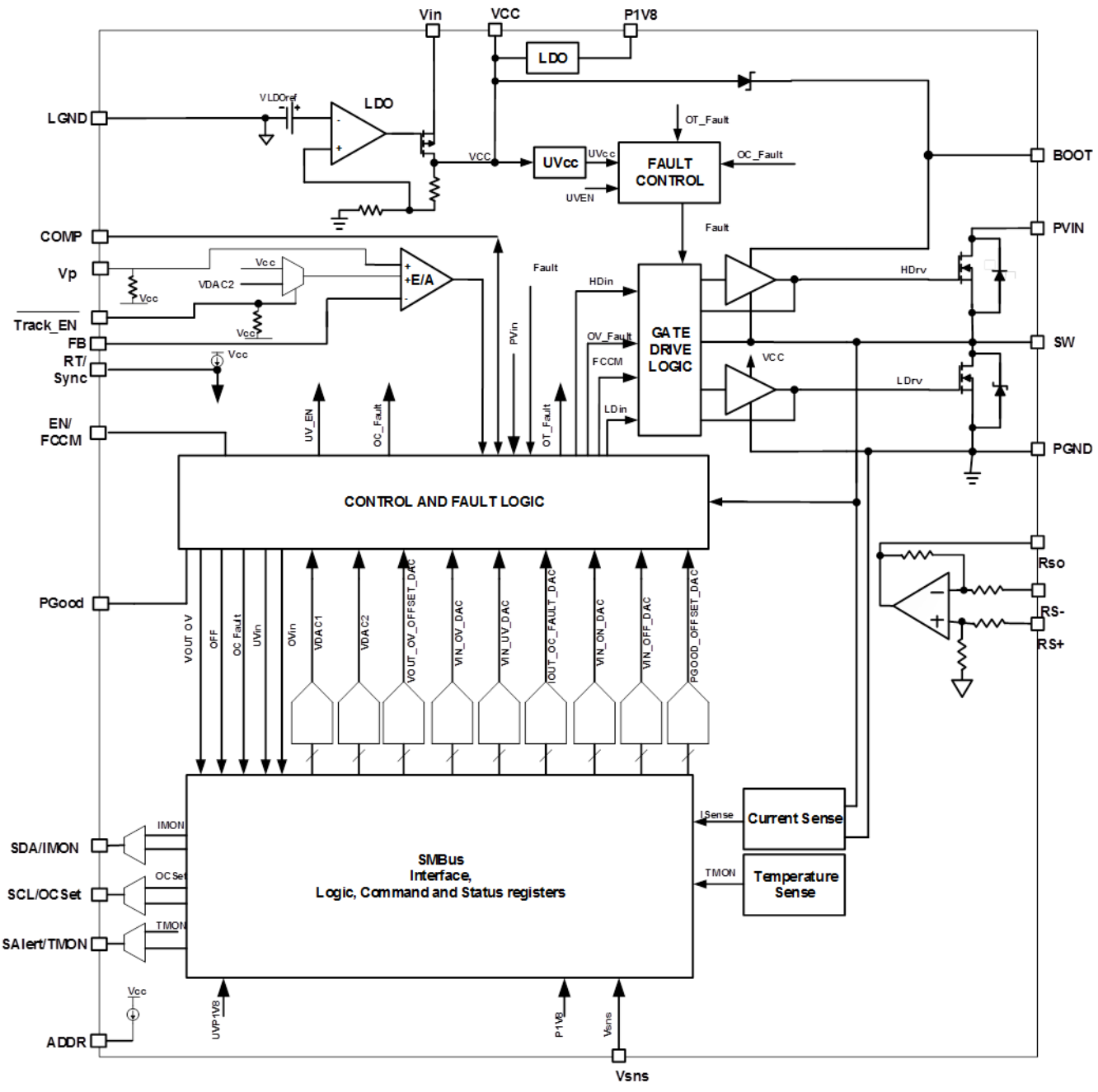


Figure 4: IR38062 Simplified Block Diagram

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	PVIN	Input voltage for power stage. Bypass capacitors between PVin and PGND should be connected very close to this pin and PGND.
2	Boot	Supply voltage for high side driver
3	$\overline{\text{Track_En}}$	Pull low to enable tracking function. Leave floating to disable tracking function.
4	Vp	Used for sequencing and tracking applications. Leave open if not used.
5	Vsns	Sense pin for OVP and Pgood
6	FB	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator or to the output of the remote sense amplifier, via resistor divider to set the output voltage and provide feedback to the error amplifier.
7	COMP	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to FB to provide loop compensation.
8	RSo	Remote Sense Amplifier Output
9	RS-	Remote Sense Amplifier input. Connect to ground at the load.
10	RS+	Remote Sense Amplifier input. Connect to output at the load.
11	PGood	Power Good status pin. Output is open drain. Connect a pull up resistor from this pin to VCC.
12,25	PGND	Power ground. This pin should be connected to the system's power ground plane. Bypass capacitors between PVin and PGND should be connected very close to the PVIN pin (pin 1) and this pin.
13	LGND	Signal ground for internal reference and control circuitry.
14	RT/Sync	In analog mode, use an external resistor from this pin to GND to set the switching frequency. The resistor should be placed very close to the pin. This pin can also be used for external synchronization. No resistor is used in digital mode.
15	EN/FCCM	Enable pin to turn on and off the IC. In analog mode, also serves as a mode pin, forcing the converter to operate in CCM when pulled to<3.1V.
16	ADDR	Sets PMBus address for the device; should be floated if digital communication is not needed.
17	$\overline{\text{SALERT}}$ /TMON	SMBus $\overline{\text{Alert}}$ line; pin provides a voltage proportional to the junction temperature if digital communication is not needed.
18	SDA/IMON	SMBus data serial input/output line; pin provides a voltage proportional to the output current if digital communication is not needed.
19	SCL/OCSet	SMBus clock line; used to set OC thresholds if digital communication is not needed.
20	P1V8	This is the supply for the digital circuits; bypass with a 2.2uF capacitor to LGnd or PGnd
21	Vin	Input Voltage for LDO.
22	VCC	Bias Voltage for IC and driver section, output of LDO. Add 10 uF bypass cap from this pin to PGnd.
23,26	NC	NC
24	SW	Switch node. This pin is connected to the output inductor.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond these listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PVin, Vin	-0.3V to 25V
VCC	-0.3V to 6V
P1V8	-0.3V to 2 V
SW	-0.3V to 25V (DC), -4V to 25V (AC, 100ns)
BOOT	-0.3V to 31V
PGD, other Input/output pins	-0.3V to 6V (Note 1)
BOOT to SW	-0.3V to 6V (DC), -0.3V to 6.5V (AC, 100ns)
PGND to GND, RS- to GND	-0.3V to + 0.3V
THERMAL INFORMATION	
Junction to Case Thermal Resistance $\Theta_{JC\text{-}TOP}$	30°C/W
Junction to Ambient Thermal Resistance Θ_{JA}	13.8°C/W
Junction to PCB Thermal Resistance $\Theta_{J\text{-}PCB}$	2.05°C/W
Storage Temperature Range	-55°C to 150°C
Junction Temperature Range	-40°C to 150°C

(Voltages referenced to GND unless otherwise specified)

Note 1: Must not exceed 6V.

ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

SYMBOL	DEFINITION	MIN	MAX	UNITS
PVin	Input Bus Voltage	1.2	21*	V
Vin	LDO supply voltage	5.5	21	
VCC	LDO output/Bias supply voltage	4.5	5.5	
Boot to SW	High Side driver gate voltage	4.5	5.5	
V_O	Output Voltage	0.5	0.875*PV_{in}	
I_O	Output Current	0	15	A
Fs	Switching Frequency	225	1650	kHz
T_J	Junction Temperature	-40	125	°C

* SW Node must not exceed 25V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, these specification apply over, 1.5V < PVin < 21V, 4.5V < Vcc < 5.5, 0°C < T_J < 125°C.

Typical values are specified at T_A = 25°C.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
MOSFET $R_{ds(on)}$						
Top Switch	Rds(on)_Top	V_{Boot} – V_{SW} = 5V, I_D = 15A, Tj = 25°C	2.7	4	5.6	mΩ
Bottom Switch	Rds(on)_Bot	Vcc =5V, I_D = 15A, Tj = 25°C	1.11	1.58	2.05	
Reference Voltage						
Accuracy $0^0C<Tj<85^0C$		1.25V<V_{FB}<2.555V VOUT_SCALE_LOOP=1;	-1		+1	%
		0.75V<V_{FB}<1.25V VOUT_SCALE_LOOP=1;	-0.75		+0.75	
		0.45V<V_{FB}<0.75V VOUT_SCALE_LOOP=1;	-0.5		+0.5	%
Accuracy $-40^0C<Tj<125^0C$		1.25V<V_{FB}<2.555V VOUT_SCALE_LOOP=1;	-1.6		+1.6	%
		0.75V<V_{FB}<1.25V	-1.0		+1.0	%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		VOUT_SCALE_LOOP=1;				
		0.45V<V_{FB}<0.75V VOUT_SCALE_LOOP=1;	-2.0		+2.0	%
Supply Current						
PVin range (using external Vcc=5.1V)				1.2-21		V
Vin range (using internal LDO)		Fsw=600kHz		5.3-21		V
		Fsw=1.5MHz		5.5-21		
Vin range (when Vin=Vcc)			4.5	5.1	5.5	V
V_{in} Supply Current (Standby) (internal Vcc)	$I_{in(Standby)}$	Enable low, No Switching, Vin=21V, low power mode enabled		2.7	4	mA
V_{in} Supply Current (Dyn)(internal Vcc)	$I_{in(Dyn)}$	Enable high, Fs = 600kHz, Vin=21V		39	50	mA
VCC Supply Current (Standby)(external Vcc)	$I_{cc(Standby)}$	Enable low, No Switching, Vcc=5.5V, low power mode enabled		2.7	5	mA
VCC Supply Current (Dyn)(external Vcc)	$I_{cc(Dyn)}$	Enable high, Fs = 600kHz, Vcc=5.5V		39	50	mA
Under Voltage Lockout						
VCC – Start – Threshold	VCC_UVLO_Start	VCC Rising Trip Level	4.0	4.2	4.4	V
VCC – Stop – Threshold	VCC_UVLO_Stop	VCC Falling Trip Level	3.7	3.9	4.1	
PVin-Start-Threshold	PVin_UVLO_Start	PVin Rising Trip Level	0.85	0.95	1.05	V
PVin-Stop-Threshold	PVin_UVLO_Stop	PVin Falling Trip Level	0.35	0.45	0.55	
Enable – Start – Threshold	Enable_UVLO_Start	Supply ramping up	1.14	1.2	1.36	V
Enable – Stop – Threshold	Enable_UVLO_Stop	Supply ramping down	0.9	1.0	1.06	
Enable leakage current	Ien	Enable=5.5V			1	uA
Oscillator						
Rt current (analog mode only)		Rt pin voltage < 1.1V	98	100	102	uA
Frequency Range	F_S	Rt=1.54K	360	400	440	kHz
		Rt=3.83K	540	600	660	
		Rt=11.8K	1350	1500	1650	
Ramp Amplitude	Vramp	PVin=5V, D=Dmax, Note 2		0.71		Vp-p
		PVin=12V, D=Dmax, Note 2		1.84		

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		PVin=16V,D=Dmax, Note 2		2.46		
Ramp Offset	Ramp (os)	Note 2		0.22		V
Min Pulse Width	Dmin (ctrl)	Note 2		35	50	ns
Fixed Off Time		Note 2 Fs=1.5MHz		100	150	ns
Max Duty Cycle	Dmax	Fs=400kHz	86.5	87.5	88.5	%
Sync Frequency Range		Note 2	225		1650	kHz
Sync Pulse Duration			100	200		ns
Sync Level Threshold	High		2.1			V
	Low				1	
Error Amplifier						
Input Offset Voltage	Vos_Vp	VFb – Vp, Vp = 0.5V	-1.5		+1.5	%
Input Bias Current	IFb(E/A)		-0.5		+0.5	µA
Input Bias Current	IVp(E/A)		0		4	µA
Sink Current	Isink(E/A)		0.6	1.1	1.8	mA
Source Current	Isource(E/A)		8	13	25	mA
Slew Rate	SR	Note 2	7	12	20	V/µs
Gain-Bandwidth Product	GBWP	Note 2	20	30	40	MHz
DC Gain	Gain	Note 2	100	110	120	dB
Maximum Voltage	Vmax(E/A)		2.8	3.9	4.3	V
Minimum Voltage	Vmin(E/A)				100	mV
Common Mode Voltage	Vcm_Vp	Note 2	0		2.555	V
Remote Sense Differential Amplifier						
Unity Gain Bandwidth	BW_RS	Note 2	3	6.4		MHz
DC Gain	Gain_RS	Note 2		110		dB
Offset Voltage	Offset_RS	0.5V<RS+<2.555V, 4kOhm load $27^0C<Tj<85^0C$	-1.6	0	1.6	mV
		0.5V<RS+<2.555V, 4kOhm load $-40^0C<Tj<125^0C$	-3		3	
Source Current	Isource_RS	V_RSO=1.5V, V_RSP=4V	11		16	mA
Sink Current	Isink_RS		0.4	1	2	mA
Slew Rate	Slew_RS	Note 2, Cload = 100pF	2	4	8	V/µs
RS+ input impedance	Rin_RS+		36	55	74	Kohm
RS- input impedance	Rin_RS-	Note 2	36	55	74	Kohm
Maximum Voltage	Vmax_RS	V(VCC) – V(RS+)	0.5	1	1.5	V
Minimum Voltage	Min_RS			4	20	mV

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Bootstrap Diode						
Forward Voltage		I(Boot) = 40mA	150	300	450	mV
Switch Node						
SW Leakage Current	Isw	SW = 0V, Enable = 0V			1	µA
	Isw_En	SW=0; Enable= 2V		18		
Internal Regulator (VCC/LDO)						
Output Voltage	VCC	Vin(min) = 5.5V, Io=0mA, Cload = 10uF	4.8	5.15	5.4	V
		Vin(min) = 5.5V, Io=70mA, Cload = 10uF	4.5	4.99	5.2	
VCC dropout	VCC_drop	Io=0-100mA, Cload = 10uF, Vin=5.1V			0.7	V
Short Circuit Current	Ishort			110		mA
Internal Regulator (P1V8)						
Output Voltage	P1V8	Vin(min) = 4.5V, Io = 0-10mA, Cload = 2.2uF	1.795	1.83	1.905	V
1.8V Short Circuit Current	Ishort_P1V8		12	20	35	mA
1.8V UVLO Start	P1V8_UVLO_Start	1.8V Rising Trip Level	1.66	1.72	1.78	V
1.8V UVLO Stop	P1V8_UVLO_Stop	1.8V Falling Trip Level	1.59	1.63	1.68	V
Adaptive On time Mode						
AOT Threshold	High	En/Fccm	3.8	3.9	4.1	V
	Low		3.1	3.6	3.8	
Zero-crossing comparator threshold	ZC_Vth		-4	-1	2	mV
Zero-crossing comparator delay	ZC_Tdly			8/Fs		s
FAULTS						
Power Good						
Power Good High threshold	Power_Good_High	Vsns rising, VOUT_SCALE_LOOP=1, Track_EN floating, VDAC1=0.5V		91		%VDAC1
		Vsns rising, VOUT_SCALE_LOOP=1, Track_EN low, Vp=0.5V		90		%Vp
Power Good Low Threshold	Power_Good_Low	Vsns falling, VOUT_SCALE_LOOP=1, Track_EN floating, VDAC1=0.5V		86		%VDAC1
		Vsns falling, VOUT_SCALE_LOOP=1, Track_EN low, Vp=0.5V		84.5		%Vp
Power Good High	TPDLY	Vsns rising, Vsns >		0		ms

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Threshold Rising Delay		Power_Good_High				
Power Good Low Threshold Falling delay	VPG_low_Dly	Vsns falling, Vsns < Power_Good_Low	150	175	200	us
Tracker Comparator Upper Threshold	VPG(tracker_ upper)	Vp Rising, VOUT_SCALE_LOOP=1, Track_EN low, Vsns=Vp	0.38	0.4	0.42	V
Tracker Comparator Lower Threshold	VPG(tracker_ lower)	Vp Falling, VOUT_SCALE_LOOP=1, Track_EN low, Vsns=Vp	0.28	0.3	0.32	V
PGood Voltage Low	PG (voltage)	I_{PGood} = -5mA			0.5	V
Over Voltage Protection (OVP)						
OVP Trip Threshold	OVP (trip)	Vsns rising, VOUT_SCALE_LOOP=1, Track_EN floating, VDAC1=0.5V	115	121	125	%VDAC1
		Vsns rising, VOUT_SCALE_LOOP=1, Track_EN low, Vp=0.5V	115	120	125	%Vp
OVP comparator Hysteresis	OVP (hyst)	Vsns falling, VOUT_SCALE_LOOP=1, Track_EN floating, VDAC1=0.5V	2.5	4.5	5.8	%OVP (trip)
		Vsns falling, VOUT_SCALE_LOOP=1, Track_EN low, Vp=0.5V	2.5	4.5	5.8	%OVP (trip)
OVP Fault Prop Delay	OVP (delay)	Vsns rising, Vsns-OVP(trip)>200 mV		200		ns
Over-Current Protection						
OC Trip Current	I_{TRIP}	OC limit=20A, VCC = 5.05V, T_j=25^{0}C	17	20	23	A
		OC limit=15A, VCC = 5.05V, T_j=25^{0}C	13.5	15	17.5	A
		OC limit=12A, VCC = 5.05V, T_j=25^{0}C	10.25	12	13.75	A
OCset Current Temperature coefficient	OCSET(temp)	-40^{0}C to 125^{0}C, VCC=5.05V, Note 2		5900		ppm/°C
Hiccup blanking time	Tblk_Hiccup	Note 2		20		ms
Thermal Shutdown						
Thermal Shutdown		Note 2		145		°C
Hysteresis		Note 2		25		°C
Input Over-Voltage Protection						
PVin overvoltage threshold	$PVin_{OV}$		22	23.7	25	V
PVin overvoltage	$PVin_{ov\ hyst}$			2.4		V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Hysteresis						
MONITORING AND REPORTING						
Bus Speed[1]				100	400	kHz
Iout & Vout filter				78		Hz
Iout & Vout Update rate				31.25		kHz
Vin & Temperature filter				78		Hz
Vin & Temperature update rate				31.25		kHz
Output Voltage Reporting						
Resolution	N_{Vout}	Note 2		1/256		V
Lowest reported Vout	Vomon_low	Vsns=0V		0		V
Highest reported Vout	Vomon_high	VOUT_SCALE_LOOP=1, Vsns=3.3V		3.3		V
		VOUT_SCALE_LOOP=0.5, Vsns=3.3V		6.6		V
		VOUT_SCALE_LOOP=0.25, Vsns=3.3V		13.2		V
		VOUT_SCALE_LOOP=0.125, Vsns=3.3V		26.4		V
Vout reporting accuracy		0^0C to 85^0C, 4.5V<Vcc<5.5V, 1V<Vsns≤ 1.5V VOUT_SCALE_LOOP=1		+/- 0.6		%
		0^0C to 85^0C, 4.5V<Vcc<5.5V, Vsns> 1.5V VOUT_SCALE_LOOP=1		+/-1		
		0^0C to 125^0C, 4.5V<Vcc<5.5V, Vsns>0.9V VOUT_SCALE_LOOP=1		+/- 1.5		
		0^0C to 125^0C, 4.5V<Vcc<5.5V, 0.5V<Vsns<0.9V VOUT_SCALE_LOOP=1		+/-3		
Iout Reporting						
Resolution	N_{Iout}	Note 2		62.5		mA
Iout (digital) monitoring Range	Iout_dig		0		22.5	A
Iout_dig Accuracy		0^0C to 125^0C, 4.5V<Vcc<5.5V, **5A < Iout <1 5A**		+/-5		%
Imon (analog) voltage	Imon		0.3		1.1	V
Imon (analog) accuracy		0^0C to 125^0C, 4.5V<Vcc<5.5V, 5A < Iout <1		+/- 1.5		A

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		5A, -30uA< I_IMON<30uA				
Temperature Reporting						
Resolution	N_{Tmon}	Note 2		1		°C
Temperature Monitoring (digital) Range	Tmon_dig		-40		150	°C
Temperature Monitoring (digital) accuracy		-40^{0}C to 125^{0}C, 4.5V<Vcc<5.5V, -30uA< I_TMON<30uA; Guaranteed by char	-5		5	°C
Analog monitoring range	Tmon	-40^{0}C to 150^{0}C	500		1100	mV
Analog Monitoring Accuracy		-40^{0}C to 125^{0}C, 4.5V<Vcc<5.5V, -30uA< I_TMON<30uA, Note 2	-9		9	°C
Temperature coefficient				2.27		mV/°C
Thermal shutdown hysteresis		Note 2		25		°C
Input Voltage Reporting						
Resolution	N_{PVin}	Note 2		1/32		V
Monitoring Range	PMBVinmon		0		21	V
Monitoring accuracy		0^{0}C to 85^{0}C, 4.5V<Vcc<5.5V, PVin>10V	-1.5		1.5	%
		-40^{0}C to 125^{0}C, 4.5V<Vcc<5.5V, PVin>14V	-1.5		1.5	
		-40^{0}C to 125^{0}C, 4.5V<Vcc<5.5V, 6V<PVin<14V	-3		3	
PMBus Interface Timing Specifications						
SMBus Operating frequency	F_{SMB}				400	kHz
Bus Free time between Start and Stop condition	T_{BUF}		1.3			us
Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	$T_{HD:STA}$		0.6			us
Repeated start condition setup time	$T_{SU:STA}$		0.6			us
Stop condition setup time	$T_{SU:STO}$		0.6			us
Data Rising Threshold			1.339		1.766	V
Data Falling Threshold			1.048		1.495	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Clock Rising Threshold			1.339		1.766	V
Clock Falling Threshold			1.048		1.499	V
Data Hold Time	$T_{HD:DAT}$		300		900	ns
Data Setup Time	$T_{SU:DAT}$		100			ns
Clock low time out	$T_{TIMEOUT}$		25		35	ms
Clock low period	T_{LOW}		1.3			us
Clock High Period	T_{HIGH}		0.6		50	us

Notes

2. Guaranteed by design but not tested in production
3. Guaranteed by statistical correlation, but not tested in production

TYPICAL APPLICATION DIAGRAMS

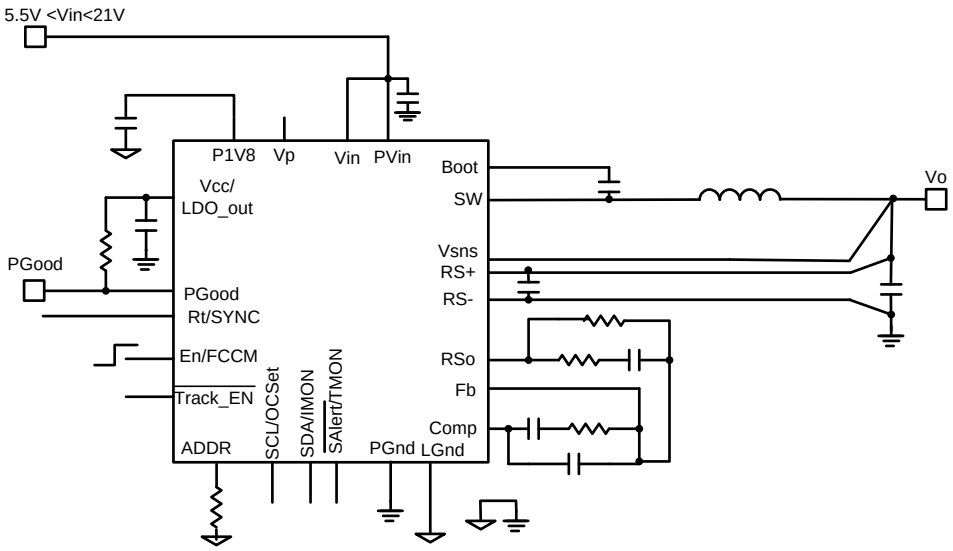


Figure 5: Using the internal LDO, digital mode, Vo < 2.555V

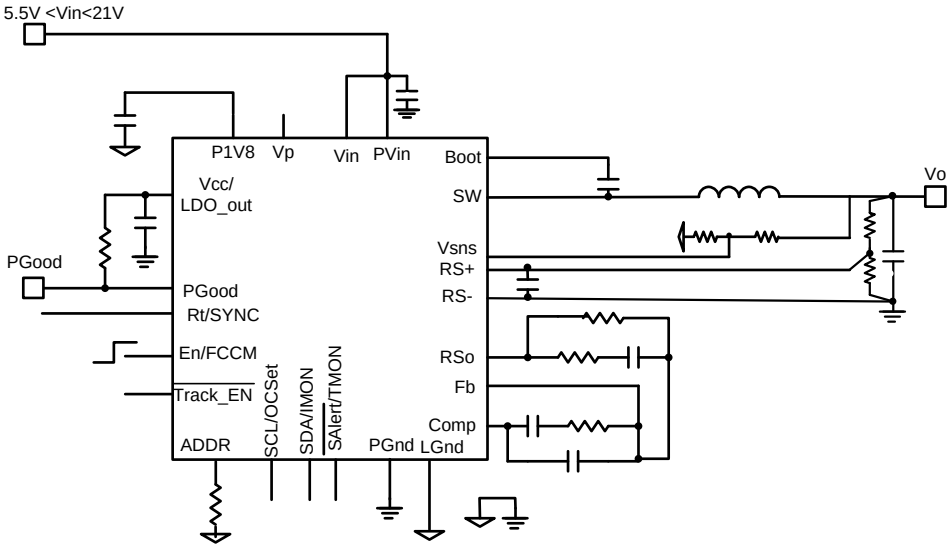


Figure 6: Using the internal LDO, digital mode, Vo > 2.555V

TYPICAL APPLICATION DIAGRAMS

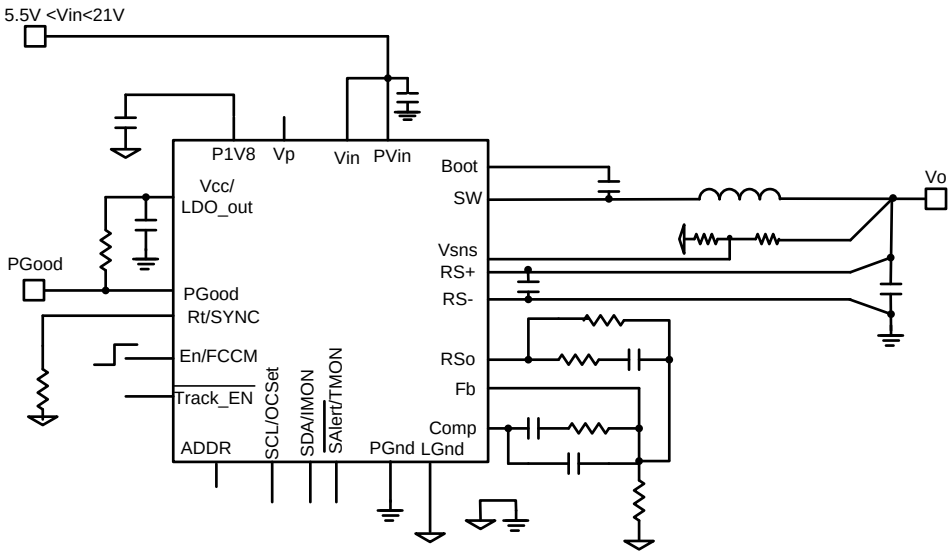


Figure 7: Using the internal LDO, analog mode

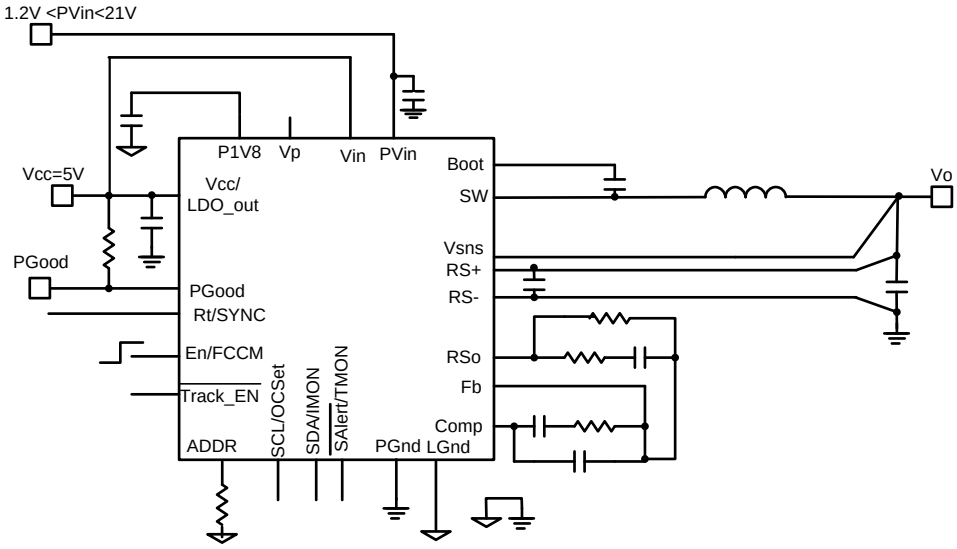


Figure 8: Using external Vcc, digital mode, Vo<2.555V

TYPICAL APPLICATION DIAGRAMS

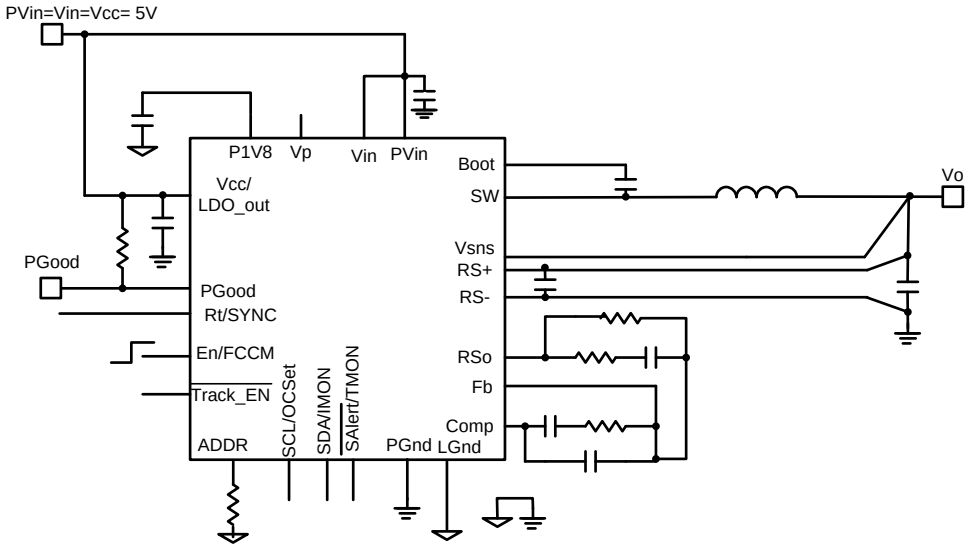


Figure 9: Single 5V application, digital mode, Vo<2.555V

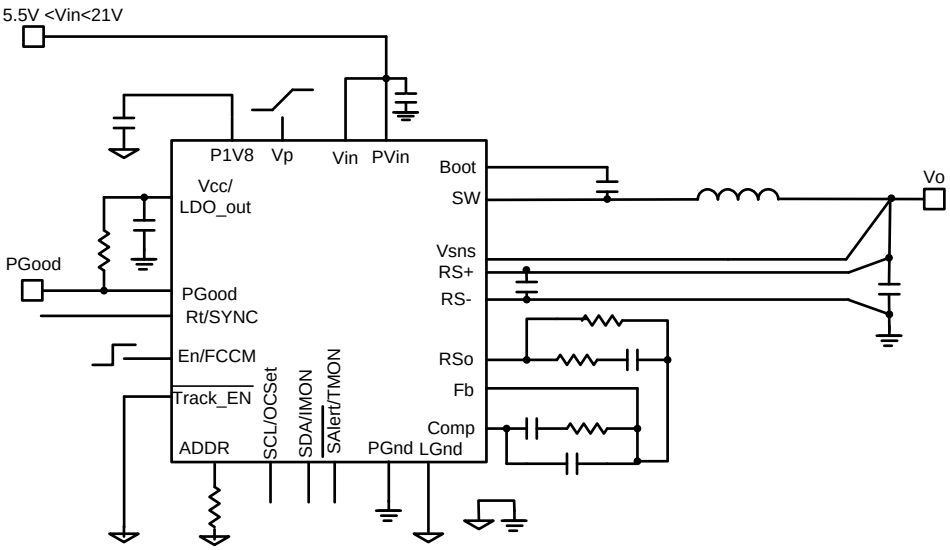
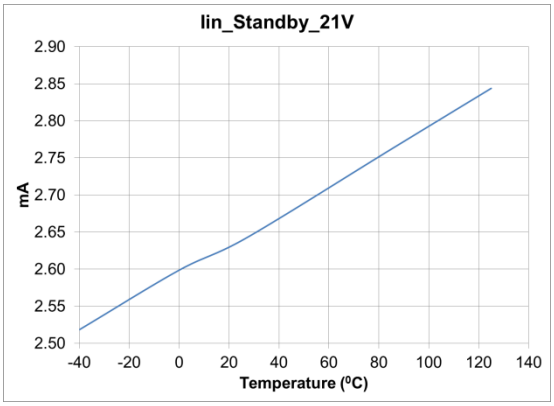
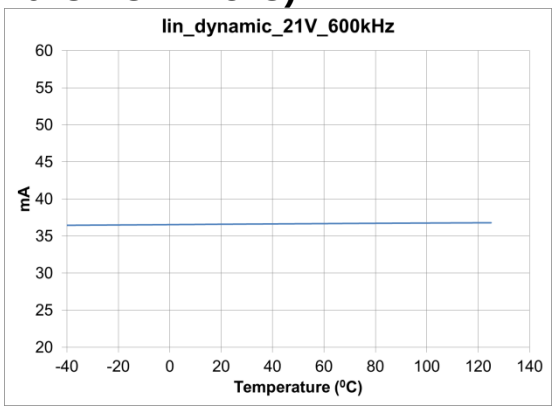
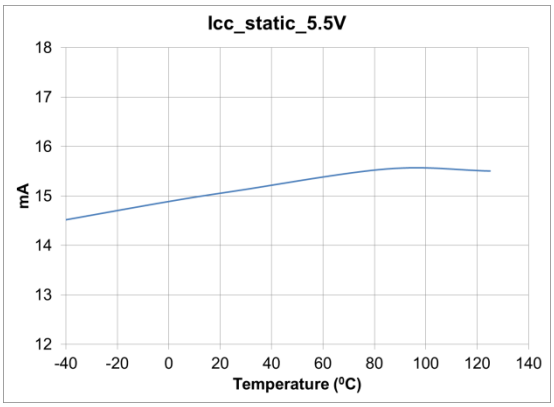


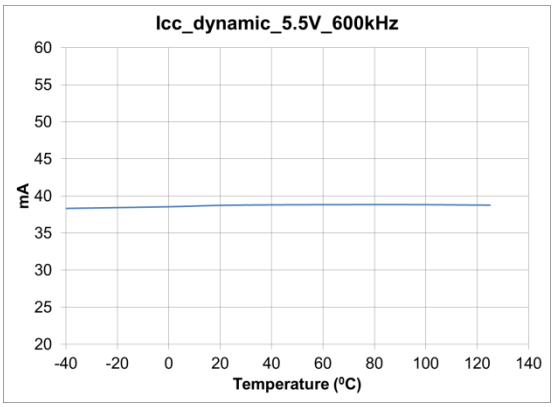
Figure 10: Using the internal LDO, digital mode, tracking mode

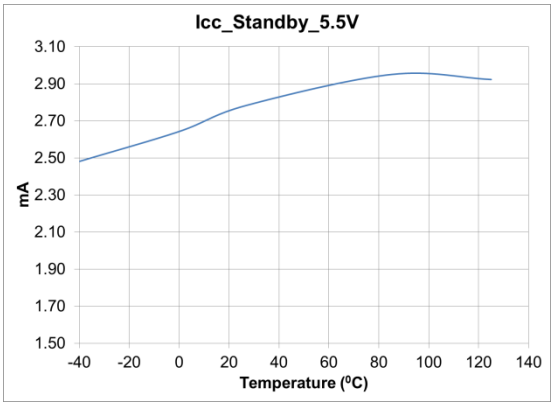
TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)

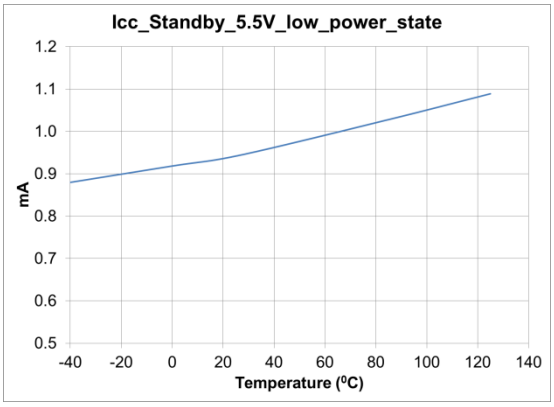




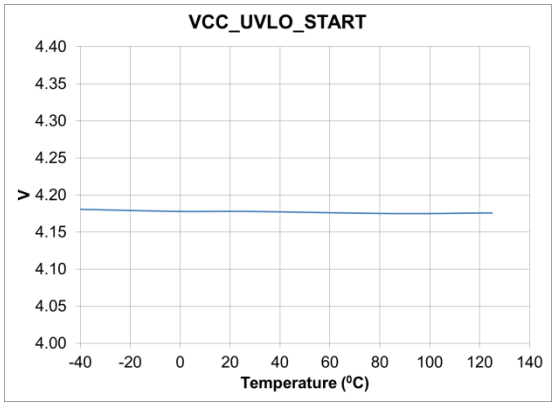


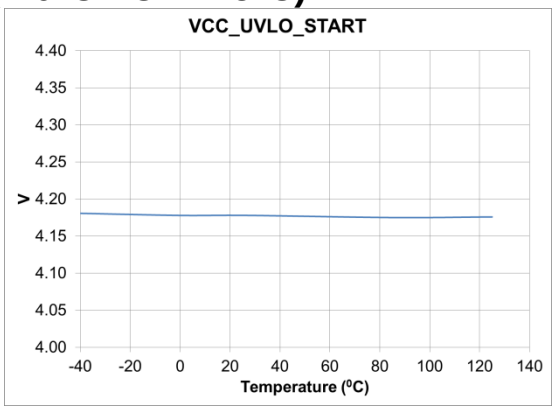


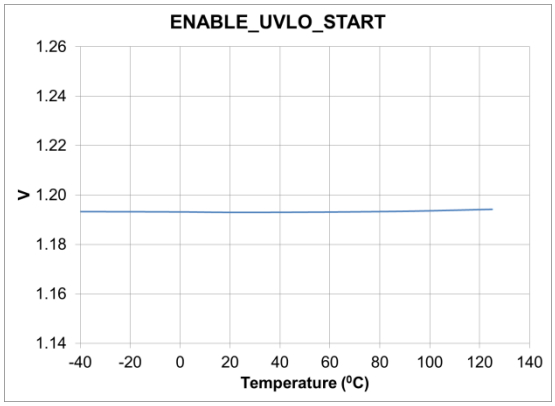


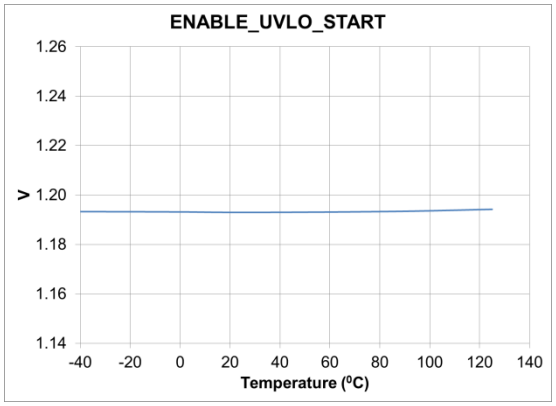


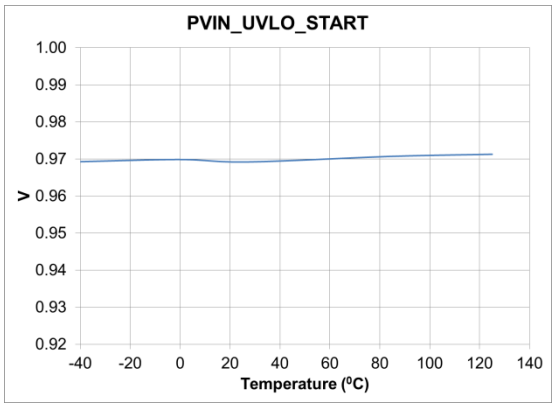
TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)

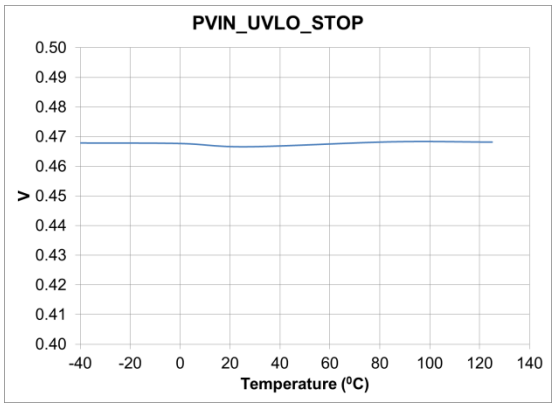




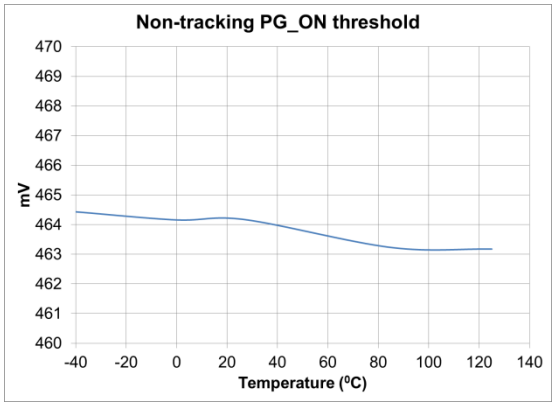


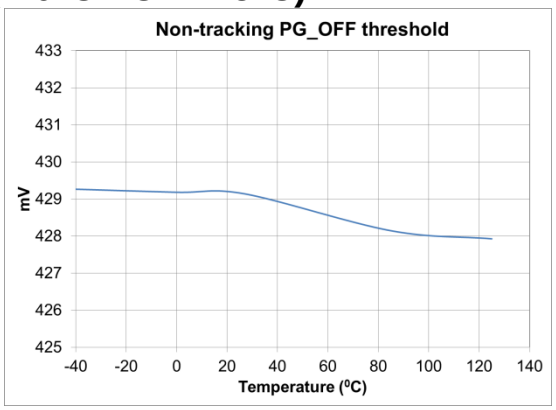


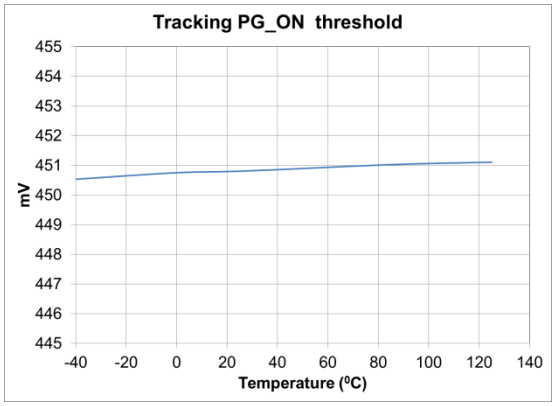


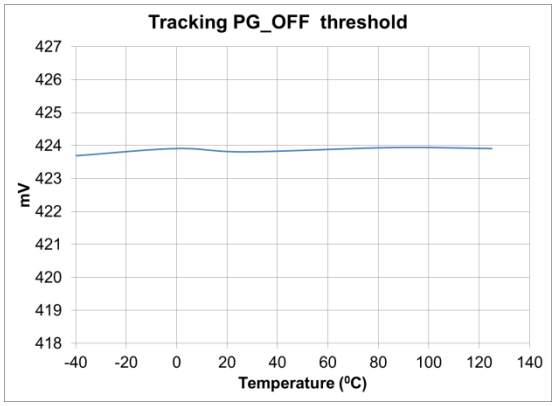


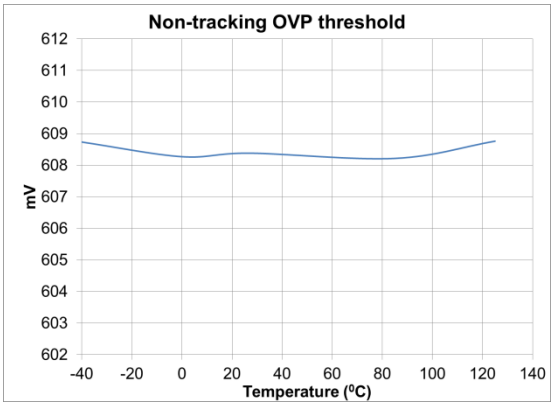
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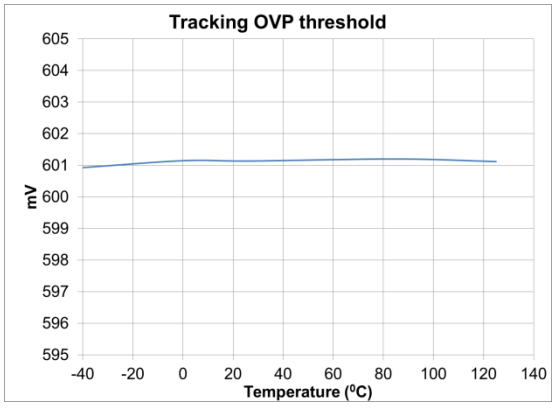




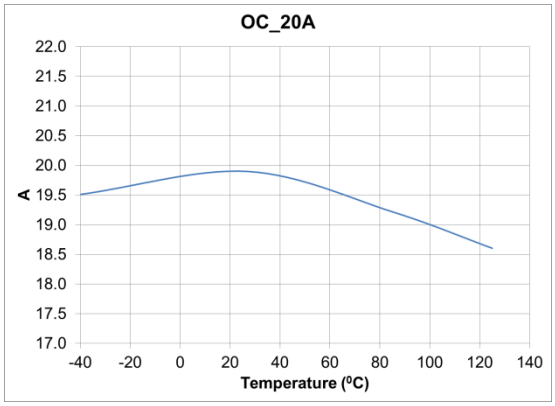


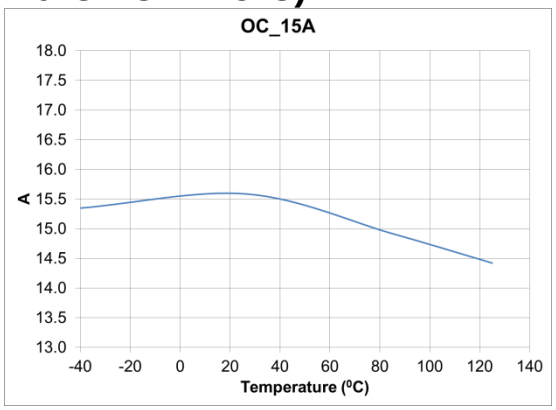


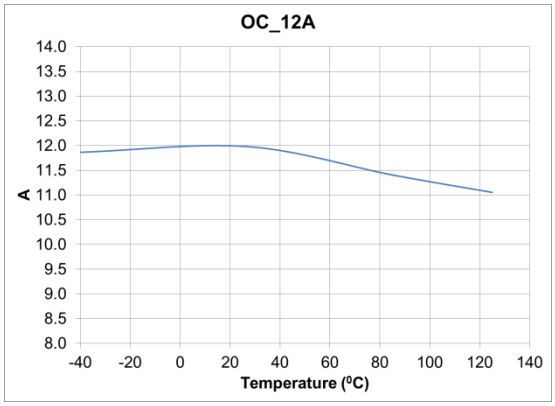


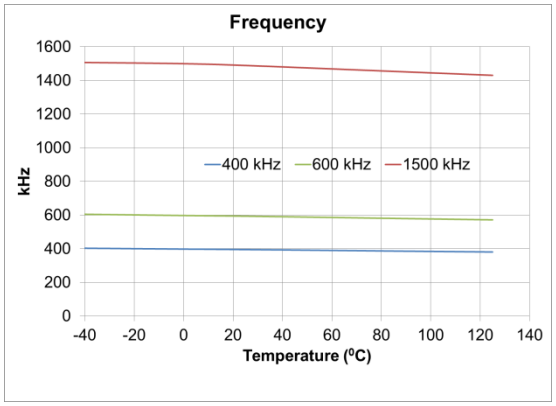


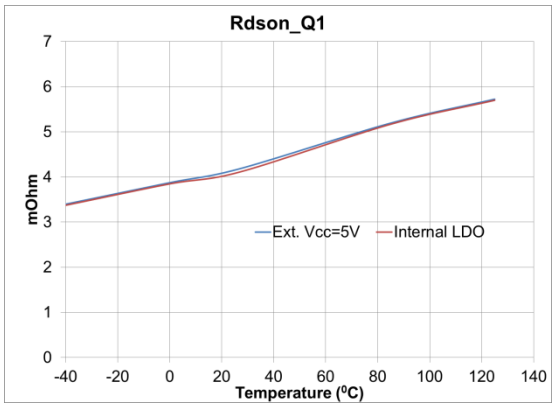
TYPICAL OPERATING CHARACTERISTICS (-40°C TO +125°C)

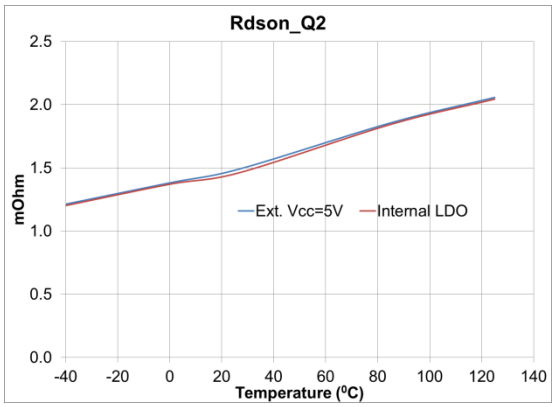








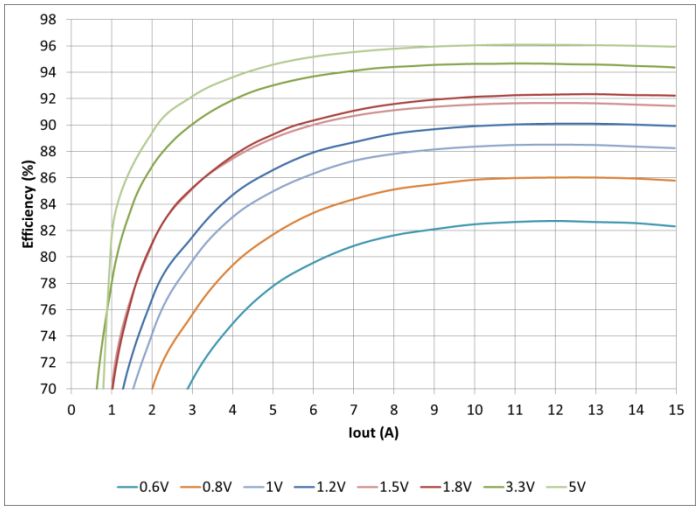


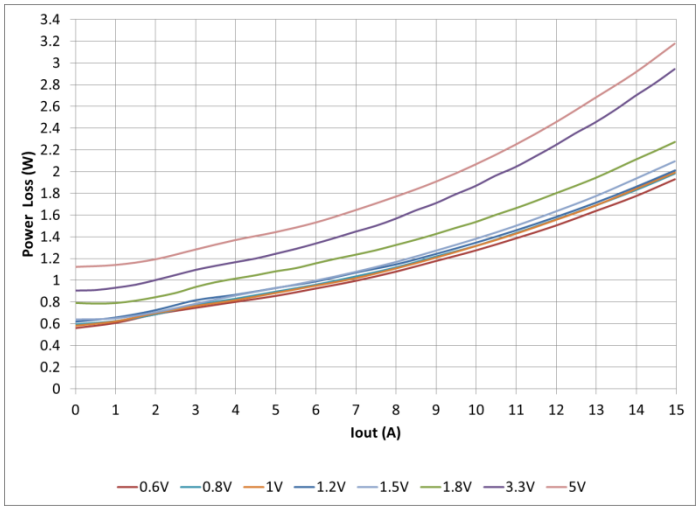


TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = Vin = 12V, VCC = Internal LDO, Io=0-15A, Fs= 600kHz, Room Temperature, No Air Flow. Note that the losses of the inductor, input and output capacitors are also considered in the efficiency and power loss curves. The table below shows the indicator used for each of the output voltages in the efficiency measurement.

VOUT (V)	LOUT (uH)	P/N	DCR (mΩ)
0.6	0.215	PCDC1008-R215EMO (Cyntec)	0.29
0.8	0.215	PCDC1008-R215EMO (Cyntec)	0.29
1	0.3	59PR9874N (Vitec)	0.29
1.2	0.3	59PR9874N (Vitec)	0.29
1.5	0.3	59PR9874N (Vitec)	0.29
1.8	0.4	FP1107-R1-R40-R (Coiltronics)	0.29
3.3	0.65	XAL7070651 (Coilcraft)	1.75
5	0.65	XAL7070651 (Coilcraft)	1.75

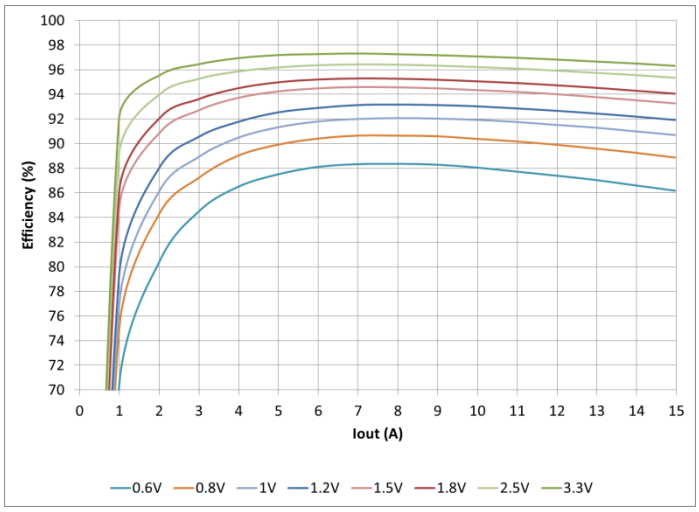


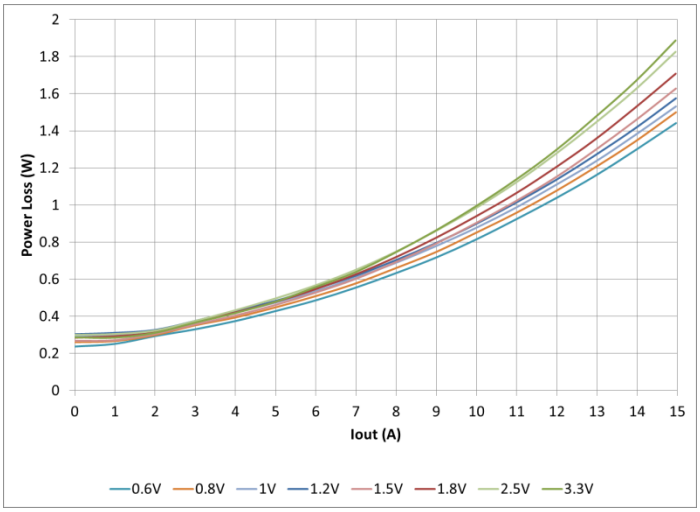


TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = Vin = VCC = 5V, Io=0-15A, Fs= 600kHz, Room Temperature, No Air Flow. Note that the losses of the inductor, input and output capacitors are also considered in the efficiency and power loss curves. The table below shows the indicator used for each of the output voltages in the efficiency measurement.

VOUT (V)	LOUT (uH)	P/N	DCR (mΩ)
0.6	0.215	PCDC1008-R215EMO (Cyntec)	0.29
0.8	0.215	PCDC1008-R215EMO (Cyntec)	0.29
1	0.215	PCDC1008-R215EMO (Cyntec)	0.29
1.2	0.215	PCDC1008-R215EMO (Cyntec)	0.29
1.5	0.3	59PR9874N (Vitec)	0.29
1.8	0.3	59PR9874N (Vitec)	0.29
2.5	0.3	59PR9874N (Vitec)	0.29
3.3	0.3	59PR9874N (Vitec)	0.29





THEORY OF OPERATION

DESCRIPTION

The IR38062 is a 15A synchronous buck regulator with a selectable digital interface and an externally compensated fast, analog, PWM voltage mode control scheme to provide good noise immunity as well as fast dynamic response in a wide variety of applications. At the same time, enabling the digital PMBus interface allows complete configurability of output setting and fault functions, as well as telemetry.

The switching frequency is programmable from 166 kHz to 1.5MHz and provides the capability of optimizing the design in terms of size and performance.

IR38062 provides precisely regulated output voltage from 0.5V to 0.875*PVin programmed via two external resistors or digitally through PMBus commands. The IR38062 operates with an internal bias supply (LDO), typically 5.2V. This allows operation with a single supply. The output of this LDO is brought out at the Vcc pin and may be bypassed to the system power ground with a 10 uF decoupling capacitor. The Vcc pin may also be connected to the Vin pin, and an external Vcc supply between 4.5V and 5.5V may be used, allowing an extended operating bus voltage (PVin) range from 1.2V to 21V.

The device utilizes the on-resistance of the low side MOSFET (synchronous MOSFET) as current sense element. This method enhances the converter's efficiency and reduces cost by eliminating the need for external current sense resistor.

IR38062 includes two low $R_{ds(on)}$ MOSFETs using IR's HEXFET technology. These are specifically designed for high efficiency applications.

DEVICE POWER-UP AND INITIALIZATION

During the power-up sequence, when Vin is brought up, the internal LDO converts it to a regulated 5.2V at Vcc. There is another LDO which further converts this down to 1.8V to supply the internal digital circuitry. An under-voltage lockout circuit monitors the voltage of VCC pin and the P1V8 pin, and holds the Power-on-reset (POR) low until these voltages exceed their thresholds and the internal 48 MHz oscillator is stable. When the device comes out of reset, it initializes a multiple times programmable memory (MTP) load cycle, where the contents of the MTP are loaded into the working registers. Once the registers are loaded from MTP, the designer can use PMBus commands to re-configure the various parameters to suit the specific VR design requirements if desired, irrespective of the status of Enable.

In the default configuration, power conversion is enabled only when the En/FCCM pin voltage exceeds its undervoltage threshold, the PVin bus voltage exceeds its undervoltage threshold, the contents of the MTP have been fully loaded into the working registers and the device address has been read. The initialization sequence is shown in Figure Figure 11.

IR38062 provides additional options to enable the device power conversion through software and these options may be configured to override the default by using the I2C interface or PMBus, if used in digital mode. For further details see the UN0060 IR3806x PMBus commandset user note.

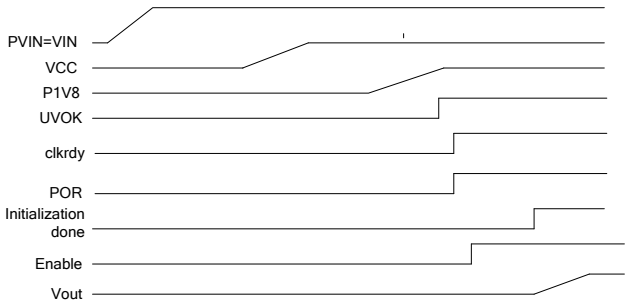


Figure 11: IR38062 Initialization sequence

ANALOG AND DIGITAL MODE OPERATION

The IR38062 has 2 7-bit registers that are used to set the base I2C address and base PMBus address of the device, as shown below in Table 1.

Table 1: Registers used to set device base address

Register	Description
I2c_address[6:0]	The chip I2C address. An address of 0 will disable communication
Pmbus_address[6:0]	The chip PMBus address. An address of 0 will disable communication.

In addition, a resistor may be connected between the ADDR and LGND pins to set an offset from the default preconfigured I2C address (0x10) /PMBus address (0x40) in the MTP. Up to 16 different offsets can be set, allowing 16 IR38062 devices with unique addresses in a single system. This offset, and hence, the device address, is read by the internal 10 bit ADC during the initialization sequence.

Table below provides the resistor values needed to set the 16 offsets from the base address.

Table 2 : Address offset vs. External Resistor(R_{ADDR})

ADDR Resistor (Ohm)	Address Offset
0	+0
1050	+1
1540	+2
2050	+3
2610	+4
3240	+5
3830	+6
4530	+7
5230	+8
6040	+9
6980	+10
7870	+11
8870	+12
9760	+13
10700	+14
11800	+15

The device will then respond to I2C/PMbus commands sent to this address. This mode in which digital communication to and from the device is allowed following the MTP load sequence is referred to as the digital mode of operation. However, if the ADDR pin is left floating, the IR38062 disables digital communication and will not respond to commands sent over the bus. In fact, the 3 pins used for digital communication are dual purpose pins which get reconfigured for analog applications if ADDR is left floating. Hence, in the analog mode, the default configuration parameters loaded in to the working registers from the MTP during the initialization sequence cannot be modified on the fly, and the device can be operated similar to an analog only SupIRBuck such as IR3847.

BUS VOLTAGE UVLO

In the analog mode of operation or with the default configuration, if the input to the Enable pin is derived from the bus voltage by a suitably programmed resistive divider, it can be ensured that the IR38062 does not turn on until the bus voltage reaches the desired level as shown in Figure 12. Only after the bus voltage reaches or exceeds this level and voltage at the Enable pin exceeds its threshold (typically 1.2V) IR38062 will be enabled. Therefore, in addition to being a logic input pin to enable the IR38062, the Enable feature, with its precise threshold, also allows the user to override the default 1 V Under-Voltage Lockout for the bus voltage (PVin). This is desirable particularly for high output voltage applications, where we might want the IR38062 to be disabled at least until PVin exceeds the desired output voltage level. Alternatively, the default 1 V PVin UVLO threshold may be reconfigured/overridden using the VIN_ON and VIN_OFF PMBus commands. It should be noted that while the input voltage is also fed to an ADC through a 21:1 internal resistive divider, the digitized input voltage is used only for the purposes of reporting the input voltage through the READ_VIN PMBUs command and has no impact on the bus voltage UVLO, input overvoltage faults and input undervoltage warnings, all of which are implemented by using analog comparators to compare the input voltage to the corresponding thresholds

programmed by the PMBus commands VIN_ON, VIN_OFF, VIN_OV_FAULT_LIMIT and VIN_UV_WARN_LIMIT respectively. The bus voltage reading as reported by READ_VIN has no effect on the input feedforward function either.

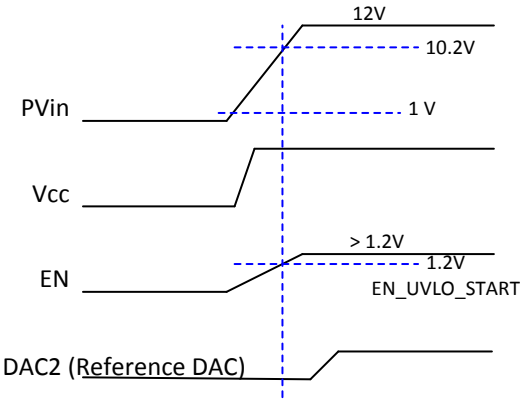


Figure 12: Normal Start up, device turns on when the bus voltage reaches 10.2V

A resistor divider is used at EN pin from PVin to turn on the device at 10.2V.

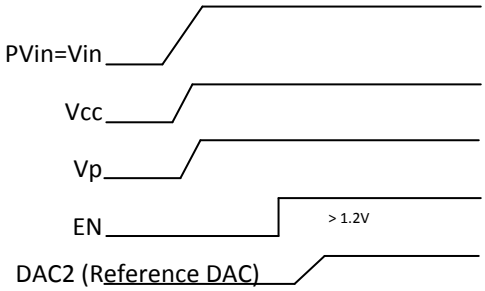


Figure 13: Recommended startup for Normal operation

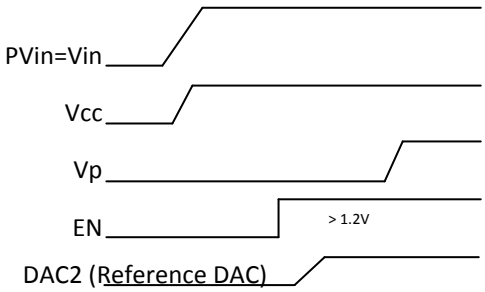


Figure 14: Recommended startup for sequencing operation (ratiometric or simultaneous)

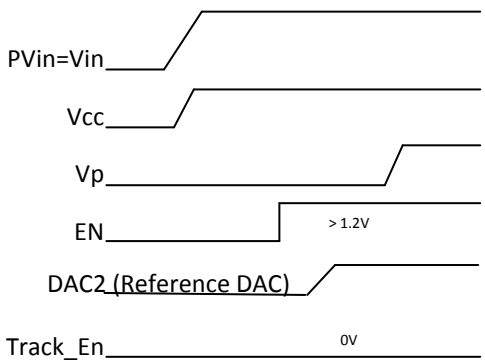


Figure 15: Recommended startup for memory tracking operation (DDR-VTT)

Figure 13 shows the recommended startup sequence for the normal (non-tracking, non-sequencing) operation of IR38062, when Enable is used as logic input. In this operating mode $\overline{\text{Track_En}}$ is left floating. Figure 14 shows the recommended startup sequence for sequenced operation of IR38062 with Enable used as logic input. For this mode of operation, $\overline{\text{Track_En}}$ is left floating. Figure 15 shows the recommended startup sequence for tracking operation of IR38062 with Enable used as logic input. For this mode of operation, $\overline{\text{Track_En}}$ should be connected to LGND.

PRE-BIAS STARTUP

IR38062 is able to start up into pre-charged output, which prevents oscillation and disturbances of the output voltage.

The output starts in asynchronous fashion and keeps the synchronous MOSFET (Sync FET) off until the first gate signal for control MOSFET (Ctrl FET) is generated. Figure 16 shows a typical Pre-Bias condition at start up. The sync FET always starts with a narrow pulse width (12.5% of a switching period) and gradually increases its duty cycle with a step of 12.5%, with 16 cycles at each step, until it reaches the steady state value. Figure 17 shows the series of 16x8 startup pulses.

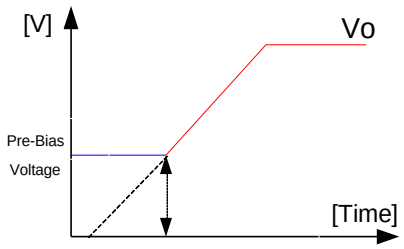


Figure 16: Pre-Bias startup

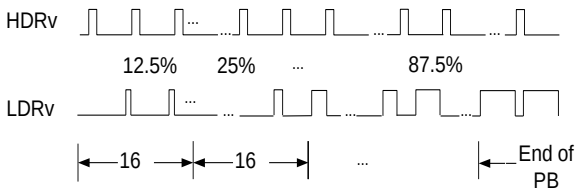


Figure 17: Pre-Bias startup pulses

SOFT-START (REFERENCE DAC RAMP)

IR38062 has an internal soft starting DAC to control the output voltage rise and to limit the current surge at the start-up. In the default configuration and in analog mode, to ensure correct start-up, the DAC sequence initiates only after power conversion is enabled when the En/FCCM pin voltage exceeds its undervoltage threshold, the PVin bus voltage exceeds its undervoltage threshold and the contents of the MTP have been fully loaded into the working registers. In analog mode and in the default configuration, the reference DAC signal linearly rises to 0.5V in 2 ms. Figure 18 shows the waveforms during soft start In digital mode, the reference DAC soft-start may be delayed from time power conversion is enabled. The range for this programmable delay is 0ms to 127 ms, and the resolution is 1 ms. Further, the soft start time may be configured from 1ms to 127 ms with 1 ms resolution.

For more details on the PMBus commands TON_DELAY and TON_RISE used to program the startup sequence, please see UN0060 IR3806x PMBus commandset user note.

Note however, that a shorter Ton_Rise can lead to a slight overshoot on the output voltage during startup and it is recommended that the system designer should verify in the actual design that the selected rise time keeps the overshoot within limits acceptable to the system.

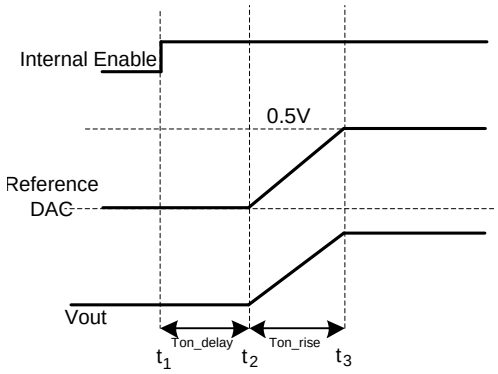


Figure 18: DAC2 (VREF) Soft start

During the startup sequence the over-current protection (OCP) and over-voltage protection (OVP) are active to protect the device for any short circuit or over voltage condition.

OPERATING FREQUENCY

In the analog mode, the switching frequency can be programmed between 306kHz – 1500kHz by connecting an external resistor from R_t pin to LGnd. This frequency is set during the initialization sequence, when the 10 bit ADC reads the voltage at the RT pin. It should be noted that after the initialization sequence is complete, the ADC no longer reads the voltage at the ADC pin, so changing the resistor on the fly after initialization will not affect the switching frequency. Table 3 tabulates the oscillator frequency versus R_t.

Table 3: Switching Frequency (F_s) vs. External Resistor(R_t)

R_t Resistor (Ohm)	F_s(kHz)
0	306
1050	356
1540	400

2050	444
2610	500
3240	550
3830	600
4530	706
5230	750
6040	800
6980	923
7870	1000
8870	1091
9760	1200
10700	1333
11800	1500

In the digital mode, the default switching frequency is configured to be 607 kHz, with a recommended programmable range from 250 kHz to 1500 kHz. The user can override this using the FREQUENCY_SWITCH PMBus command. In the digital mode of operation no resistor is used or needed on the R_t/Sync pin.

EXTERNAL SYNCHRONIZATION

IR38062 incorporates an internal phase lock loop (PLL) circuit which enables synchronization of the internal oscillator to an external clock. This function is important to avoid sub-harmonic oscillations due to beat frequency for embedded systems when multiple point-of-load (POL) regulators are used. A multi-function pin, Rt/Sync, is used to connect the external clock. In the analog mode, if the external clock is applied before the initialization sequence is done, the internal ADC cannot read the value of the RT resistor and hence, for proper operation, it is mandatory that the external clock remains applied. If the synchronization clock is then lost after initialization, the IR38062 will treat this as a symptom of a failure in the system and disable power conversion. Therefore, for such applications, where the switching frequency is always determined by an external synchronization clock, the Rt/Sync pin can be connected to the external clock signal solely and no other resistor is needed. If the external clock is applied after the initialization sequence, the IR38062 treats this as an application where the converter switching frequency needs to toggle between the external clock frequency and the internal free-running frequency, and in the analog mode, an external resistor from Rt/Sync pin to LGnd is required to set the free-running frequency. In the digital mode, the resistor is not needed because the free running frequency is set in an internal register.

When an external clock is applied to Rt/Sync pin after the converter runs in steady state with its free-running frequency, a transition from the free-running frequency to the external clock frequency will happen. This transition is to gradually make the actual switching frequency equal to the external clock frequency, no matter which one is higher. When the external clock signal is removed from Rt/Sync pin, the switching frequency is also changed to free-running gradually.

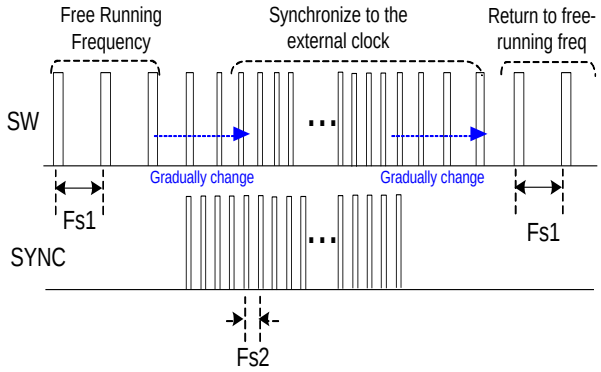


Figure 19: Timing Diagram for Synchronization to the external clock (Fs1>Fs2 or Fs1<Fs2)

An internal circuit is used to change the PWM ramp slope according to the clock frequency applied on Rt/Sync pin. Even though the frequency of the external synchronization clock can vary in a wide range, the PLL circuit will make sure that the ramp amplitude is kept constant, requiring no adjustment of the loop compensation. PVin variation also affects the ramp amplitude, which will be discussed separately in Feed-Forward section.

It must be noted here that in analog mode, since the voltage at the Rt/Sync pin is read by the ADC at startup special care must be taken if a low impedance system clock is used for synchronization and is applied before the initialization sequence is

done. The circuit shown in **Figure** 20 below shows how this may be done using a diode-capacitor combination. This couples the clock edges to the Rt/Sync pin while not loading the Rt/SYNC pin with the impedance of the synchronization clock, and thus not affecting the Rt voltage read by the ADC at startup.

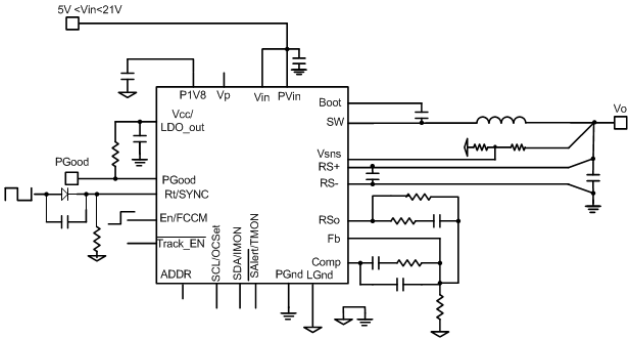


Figure 20: Synchronizing a low impedance clock in analog mode

It must be re-iterated that this is not a concern in digital mode and the clock may be directly applied to the Rt/Sync pin.

SHUTDOWN

In the default configuration, IR38062 can be shutdown by pulling the Enable pin below its 1.0V threshold. During shutdown the high side and the low side drivers are turned off. By default, the device exhibits an immediate shutdown with no delay and no soft stop.

Alternatively, in digital mode, the part may be configured to allow shutdown using the OPERATION PMBus command as well.

CURRENT SENSING, TELEMETRY AND OVER CURRENT PROTECTION

Current sensing for both, telemetry as well as overcurrent protection is done by sensing the voltage across the sync FET RDson. This method enhances the converter's efficiency, reduces cost by eliminating a current sense resistor and any minimizes sensitivity to layout related noise issues. A novel, patented scheme allows reconstruction of the average inductor current from the voltage sensed across the Sync FET Rdson. It should be noted here that it is this reconstructed average inductor current that is digitized by the ADC and used for output current reporting as well as for overcurrent warning, the threshold for which may be set using the IOUT_OC_WARN_LIMIT command. The current is reported in 1/16A resolution using the READ_IOUT PMBus command.

The Over current (OC) fault protection circuit also uses the voltage sensed across the $R_{DS(on)}$ of the Synchronous MOSFET; however, the protection mechanism relies on a fast comparator to compare the sensed signal to the overcurrent threshold and does not depend on the ADC or reported current. In the analog mode of operation, the current limit can be set to one of three possible settings by floating the OCSelect pin, or pulling it up to Vcc or pulling it down to PGnd. The current limit scheme in the IR38062 uses an internal temperature compensated current source that has the same temperature coefficient as the $R_{DS(on)}$ of the Synchronous MOSFET. As a result, the over-current trip threshold remains almost constant over temperature. .

For the IR38062, the Sync FET is turned OFF on the falling edge of a PWMSet or Clock signal that has duration of 12.5% of the switching period.

For operation at the maximum duty cycle, the OCP circuit is enabled for 60 ns, latching the OCP comparator output 45 ns after the low drive signal for the Sync FET > 70% of PVcc. For operating duty cycles less than the maximum duty cycle, the OCP circuit is still enabled for typically 60ns, but latches the OCP comparator output 45 ns after the rising edge of PWMSet.

Thus, for low duty cycle operation, the inductor current is sensed close to the valley. This allows a longer delay after the falling edge of the switch node, than the corresponding delay for an over-current sensing scheme which samples the current at the peak of the inductor current. This longer delay serves to filter out any noise on the switch node, making this method more immune to false tripping. Because the IR38062 uses valley current sensing, the actual DC output current limit point will be greater than the valley point by an amount equal to approximately half of peak to peak inductor ripple current. The current limit point will be a function of

the inductor value, input voltage, output voltage and the frequency of operation.

$$I_{OCP} = I_{LIMIT} + \frac{\Delta i}{2} \quad (1)$$

I_{OCP} = DC current limit hiccup point
I_{LIMIT} = Current Limit Valley Point
Δi = Inductor ripple current

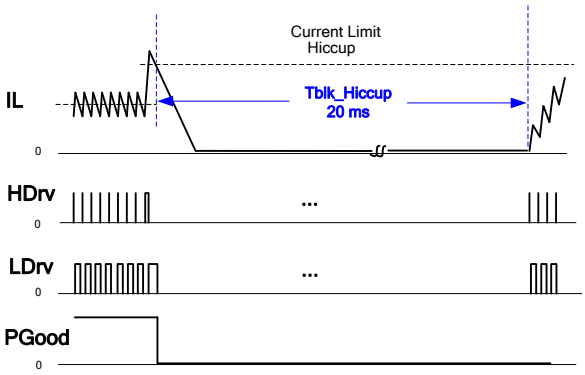


Figure 21: Timing Diagram for Current Limit Hiccup

In the default configuration and in analog mode, if the overcurrent detection trips the OCP comparator, the IR38062 goes into a hiccup mode. The hiccup is performed by de-asserting the internal Enable signal to the analog and power conversion circuitry and holding it low for 20 ms.

Following this, the OCP signal resets and the converter recovers. After every hiccup cycle, the converter stays in this mode until the overload or short circuit is removed. This behavior is shown in Figure 21.

Note that the IR38062 allows the user to override the default overcurrent threshold using the PMBus command IOUT_OC_FAULT_LIMIT.

Also, using the PMBus command IOUT_OC_FAULT_RESPONSE, the part may be configured to respond to an overcurrent fault in one of five ways

1) Constant current operation through pulse by pulse current limiting

2) Pulse by pulse current limiting for a programmed number of switching cycles (8 to 64 cycles, in 8 cycle resolution) followed by a latched shutdown.

3) Pulse by pulse current limiting for a programmed number (8 to 64 cycles, in 8 cycle resolution) of switching cycles followed by hiccup.

4) Immediate latched shutdown

5) Immediate hiccup.

The pulse-by-pulse or constant current limiting mechanism is briefly explained below.

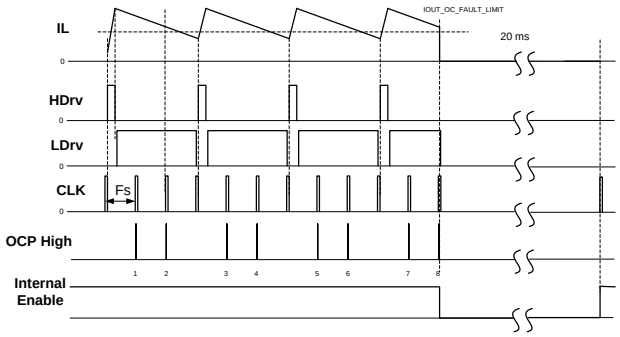
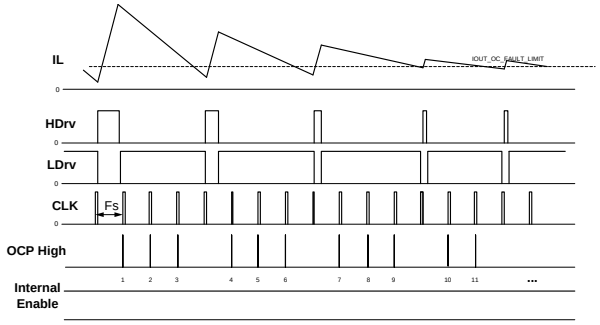


Figure 22: Pulse by pulse current limiting for 8 cycles, followed by hiccup.

In Figure 22 above, with the overcurrent response set to pulse-by-pulse current limiting for 8 cycles followed by hiccup, the converter is operating at D<0.125 when the overcurrent condition occurs. In



such a case, no duty cycle limiting is applied.

Figure 23: Constant current limiting.

Figure **23** depicts a case where the overcurrent condition happens when the converter is

operating at D>0.5 and the overcurrent response has been set to Constant current operation through pulse by pulse current limiting. In such a case, after 3 consecutive overcurrent cycles are recognized, the pulse width is dropped such that D=0.5 and then after 3 more consecutive OCP cycles, to 0.25 and then finally to 0.125 at which it keeps running until the total OCP count reaches the programmed maximum following which the part enters hiccup mode. Conversely, when the overcurrent condition disappears, the pulse width is restored to its nominal value gradually, by a similar mechanism in reverse; every sequence of 4 consecutive cycles in which the current is below the overcurrent threshold doubles the duty cycle, so that D goes from 0.125 to 0.25, then to 0.5 and finally to its nominal value.

DIE TEMPERATURE SENSING, TELEMETRY AND THERMAL SHUTDOWN

IR38062 uses on die temperature sensing for accurate temperature reporting and over temperature detection. The READ_TEMEPRATURE PMBus command reports this temperature in 1^0C resolution. The trip threshold is set by default to 145^oC. The default over temperature response of the IR38062 (also the response in analog mode) is to inhibit power conversion while the fault is present, followed by automatic restart after the fault condition is cleared. Hence, in the default configuration, when trip threshold is exceeded, the internal Enable signal to the power conversion circuitry is de-asserted, turning off both MOSFETs.

Automatic restart is initiated when the sensed temperature drops within the operating range. There is a 25^oC hysteresis in the thermal shutdown threshold.

The default overtemperature threshold as well as overtemperature response may be re-configured or overridden using the OT_FAULT_LIMIT and OT_FAULT_RESPONSE PMBus commands respectively. The devices support three types of responses to an over-temperature fault:

1) Ignore

2) Inhibit when over temperature condition exists and auto-restart when over temperature condition disappears

3) Latched shutdown.

REMOTE VOLTAGE SENSING

True differential remote sensing in the feedback loop is critical to high current applications where the output voltage across the load may differ from the output voltage measured locally across an output capacitor at the output inductor, and to applications that require die voltage sensing.

The RS+ and RS- pins of the IR38062 form the inputs to a remote sense differential amplifier with high speed, low input offset and low input bias current which ensure accurate voltage sensing and fast transient response in such applications.

The input range for the differential amplifier is limited to 1.5V below the VCC rail. Therefore, for applications in which the output voltage is more than 3V, it is recommended to use local sensing, or if remote sensing is a must, then the output voltage between the RS+ and RS-pins must be divided down to less than 3V using a resistive voltage divider. Practically, since designs for output voltage greater than 2.555V require the use of a resistive divider anyway, it is recommended that this divider be placed at the input of the remote sense amplifier. Please note, however, that this modifies the open loop transfer function and requires a change in the compensation network to optimally stabilize the loop.

FEED-FORWARD

Feed-Forward (F.F.) is an important feature, because it can keep the converter stable and preserve its load transient performance when PVin varies over a wide range. The PWM ramp amplitude (Vramp) is proportionally changed with PVin to maintain PVin/Vramp almost constant throughout PVin variation range (as shown in Figure 24). Thus, the control loop bandwidth and phase margin can be maintained constant. Feed-forward function can also minimize impact on output voltage from fast PVin change. The feedforward is disabled for PVin<4.7V. Hence, for PVin<4.7V, a re-calculation of control loop parameters is needed for re-compensation.

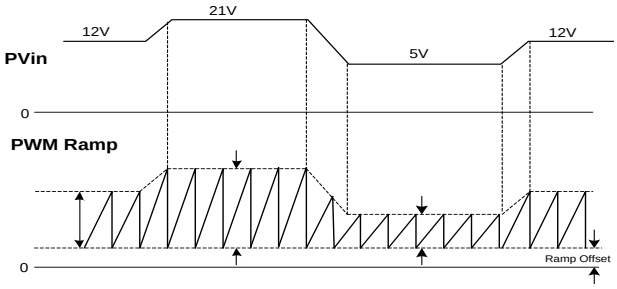


Figure 24: Timing Diagram for Feed-Forward (F.F.) Function

LIGHT LOAD EFFICIENCY ENHANCEMENT (AOT)

The IR38062 implements an Adaptive On Time control or AOT scheme to improve light load efficiency. It is based on a COT (Constant On Time) control scheme with some novel advancements that make the on-time during diode emulation adaptive and dependent upon the pulse width in constant frequency operation. This allows the scheme to be combined with a PWM scheme, while providing relatively smooth transition between the two modes of operation. In other words, the switching regulator can operate in AOT mode at light loads and automatically switch to PWM at medium and heavy loads and vice versa. Therefore, the regulator will benefit from the high efficiency of the AOT mode at light loads, and from the constant frequency and fast transient response of the PWM at medium to heavy loads.

In order to enable this light load efficiency enhancement mode in analog operation, the voltage at the En/FCCM pin needs to be kept above 4V. In digital mode, a MFR_SPECIFIC PMBus command (MFR_FCCM) can be used to enable AOT operation at light load.

Shortly after the reference voltage has finished ramping up, an internal circuit which is called the “calibration circuit” starts operation. It samples the Comp voltage (output of the error amplifier), digitizes it and stores it in a register. There is a DAC which converts the value of this register to an analog voltage which is equal to the sampled Comp voltage. At this time, the regulator is ready to enter AOT mode if the load condition is appropriate. If the load is so low that the inductor current becomes negative before the next SW pulse, the operation can be switched to AOT mode. The condition to enter AOT is the occurrence of 8 consecutive inductor current zero crossings in eight consecutive switching cycles. If this happens, operation is switched to AOT mode as shown in Figure 25. The inductor current is sensed using the RDS_ON of the Sync-FET and no direct inductor current measuring is required. In AOT mode, just like COT operation, pulses with constant width are generated and diode emulation is utilized. This means that a pulse is generated and LDrv is held on until the inductor current becomes zero. Then both HDrv and LDrv remain off until the voltage of the sense pin comes down and reaches the reference voltage. At this moment the next pulse is generated. The sense pin is connected to the output voltage by a resistor divider which has the same ratio as the voltage divider which is connected to the feedback pin (Fb).

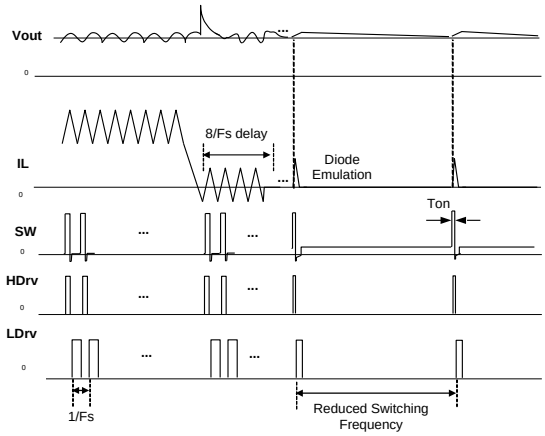


Figure 25: Timing Diagram for Reduced Switching Frequency and Diode Emulation in Light Load Condition (AOT mode)

When the load increases beyond a certain value, the control is switched back to PWM through either of the following two mechanisms:

- If due to the increase in load, the output voltage drops to 95% of the reference voltage.

-If Vsense remains below the reference voltage for 3 consecutive inductor current zero-cross events

It is worth mentioning that in AOT mode, when Vsense comes down to reference voltage level, a new pulse in generated only if the inductor current is already zero. If at this time the inductor current (sensed on the Sync-FET) is still positive, the new pulse generation is postponed till the current decays to zero. The second condition mentioned above usually happens when the load is gradually increased.

It should be noted that in tracking mode, AOT operation is disabled and the IR38062 can only operate in continuous conduction mode even at light loads.

In digital mode, if the output voltage and hence the reference voltage is commanded to a different voltage, AOT is disabled during the transition. It is enabled only after reference voltage finishes its ramp (up or down) and the calibration circuit has sampled and held the new Comp voltage.

OUTPUT VOLTAGE TRACKING AND SEQUENCING

IR38062 can accommodate user programmable tracking and/or sequencing options using Vp, Track_En , Enable, and Power Good pins. The error-amplifier (E/A) has two non-inverting inputs. Ideally, the input with the lowest voltage is used for regulating the output voltage and the other input is ignored. In practice the voltage of the other input should be about 200mV greater than the low-voltage input so that its effects can completely be ignored. Vp and Track_Enable are internally biased to 5V via a high impedance path. For normal operation, Vp and Track_Enable are left floating. Therefore, in normal operating condition, after Enable goes high, DAC2 ramps up the output voltage until Vfb (voltage of feedback/Fb pin) reaches about 0.5V.

Tracking-mode operation is achieved by connecting Track_En to LGND. In tracking mode, Vfb always follows Vp which means Vout is always proportional to Vp voltage (typical for DDR/Vtt rail applications). The effective Vp variation range is 0V~2.555V.

In sequencing mode of operation (simultaneous or ratiometric), Track_En is left floating and Vp is kept to ground level until DAC2 signal reaches the final value. Then Vp is ramped up and Vfb follows Vp. When Vp>DAC2 (0.5V in analog mode or default configuration) the error-amplifier switches to DAC2 and the output voltage is regulated with DAC2. The final Vp voltage after sequencing startup should between 0.7V ~ 5V.

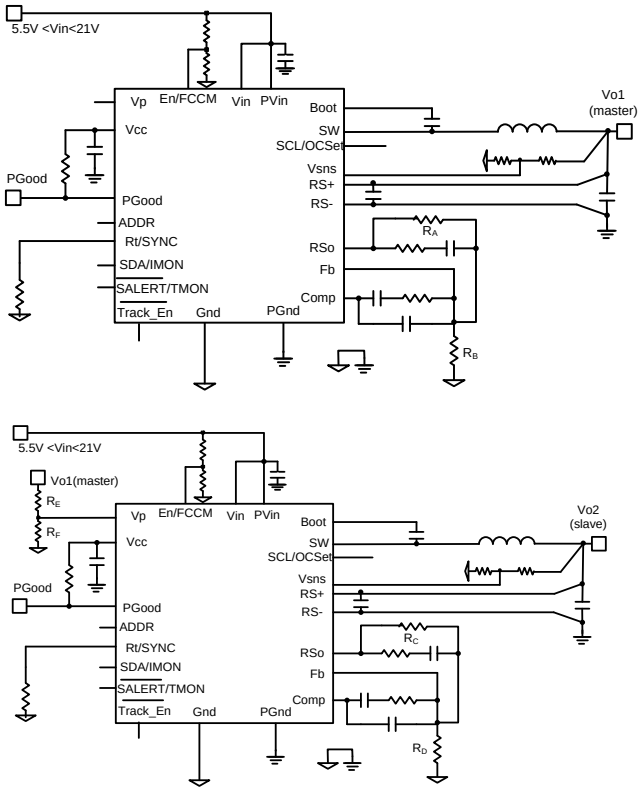


Figure 26: Application Circuit for Simultaneous and Ratiometric Sequencing

Tracking and sequencing operations can be implemented to be simultaneous or ratiometric (refer to Figure 27 and Figure 28). Figure 26 shows typical circuit configuration for sequencing operation. With this power-up configuration, the voltage at the Vp pin of the slave reaches 0.5V before the Fb pin of the master. If $R_E/R_F = R_C/R_D$, simultaneous startup is achieved. That is, the output voltage of the slave follows that of the master until the voltage at the Vp pin of the slave reaches 0.5 V. After the voltage at the Vp pin of the slave exceeds 0.5V, the internal 0.5V reference of the slave dictates its output voltage. In reality the regulation gradually shifts from

Vp to internal DAC2. The circuit shown in Figure 26 can also be used for simultaneous or ratiometric tracking operation if the $\overline{\text{Track_En}}$ pin of the slave is connected to LGND. Table 4 summarizes the required conditions to achieve simultaneous / ratiometric tracking or sequencing operations.

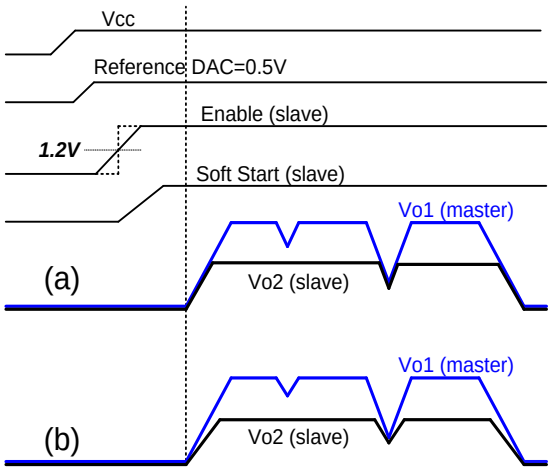


Figure 27: Typical waveforms for sequencing mode of operation: (a) simultaneous, (b) ratiometric

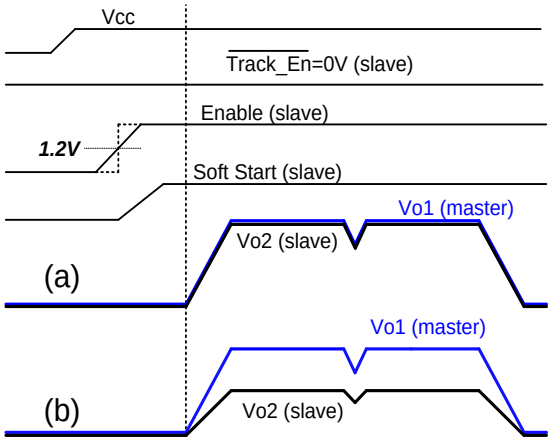


Figure 28: Typical waveforms in tracking mode of operation: (a) simultaneous, (b) ratiometric

Table 4: Required Conditions for Simultaneous / Ratiometric Tracking and Sequencing (Figure 26)

Operating Mode	Track_Enable (Slave)	Vp	Required Condition
Normal (Non-sequencing, Non-tracking)	Floating	Floating	—
Simultaneous Sequencing	Floating	Ramp up from 0V	$R_A/R_B>R_E/R_F=R_C/R_D$
Ratiometric Sequencing	Floating	Ramp up from 0V	$R_A/R_B>R_E/R_F>R_C/R_D$
Simultaneous Tracking	0V	Ramp up from 0V	$R_E/R_F=R_C/R_D$
Ratiometric Tracking	0V	Ramp up from 0V	$R_E/R_F>R_C/R_D$

$\overline{\text{TRACK_EN}}$

This pin is used to choose between tracking or non-tracking mode of operation. To enable operation in tracking mode, this pin must be tied to LGnd. If left floating, this pin internally pulls up to Vcc and selects non-tracking or sequencing mode of operation.

OUTPUT VOLTAGE SENSING, TELEMETRY AND FAULTS

In the IR38062, the voltage sense and regulation circuits are decoupled, enabling ease of testing as well as redundancy. In order to do this, IR38062 uses the sense voltage at the dedicated Vsns pin for output voltage reporting (in 1/256 V resolution, using the READ_VOUT PMBus command) as well as for power good detection and output overvoltage protection.

Power good detection and output overvoltage detection rely on fast analog comparator circuits, whereas overvoltage warnings as well as undervoltage faults and warnings rely on comparing the digitized Vsns to the corresponding thresholds programmed using PMBus commands VOUT_OV_WARN_LIMIT,VOUT_UV_FAULT_LIMIT and VOUT_UV_WARN_LIMIT respectively.

Power Good Output

The Vsns voltage is an input to the window comparator with default upper and lower thresholds of 0.45V and 0.42V respectively. PGood signal is high whenever Vsns voltage is within the PGood

comparator window thresholds. The PGood pin is open drain and it needs to be externally pulled high. High state indicates that output is in regulation. It should be noted, that in digital mode, the Power Good thresholds may be changed through the POWER_GOOD_ON and POWER_GOOD_OFF commands, which set the rising and falling PGood thresholds respectively. However, when no resistive divider is used, such as for output voltages lower than 2.555V, the Power Good thresholds must be programmed to within 630 mV of the output voltage, otherwise, the effective power good threshold changes from an absolute threshold to one that tracks the output voltage with a 630 mV offset.

The threshold is set differently in different operating modes and the result of the comparison sets the PGood signal. Figure 29, Figure 30 and Figure 31 show the timing diagram of the PGood signal in different operating modes. The Vsns signal is also used by OVP comparator to detect an output over voltage condition. By default, the PGood signal will assert as soon as the Vsns signal enters the regulation window. In digital mode, this delay is programmable from 0 to 10ms with a 1 ms resolution, using the MFR_TPGDLY command.

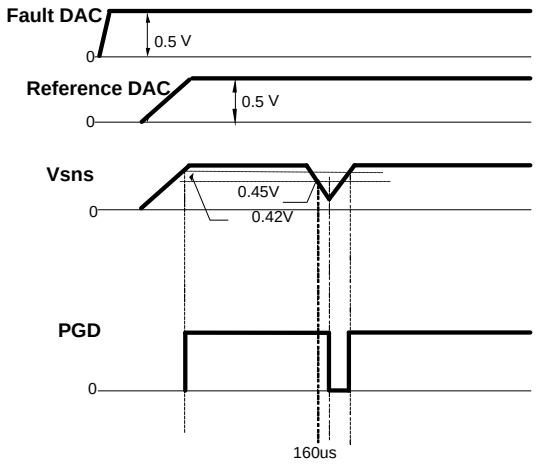


Figure 29: Non-sequenced, Non-tracking Startup

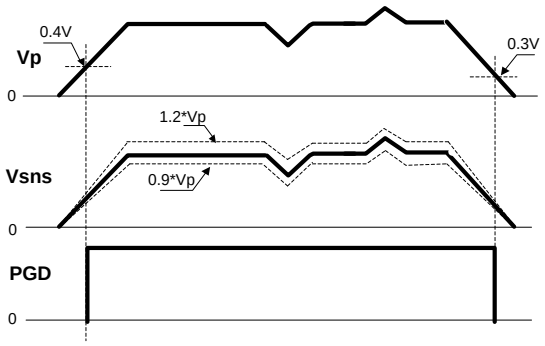


Figure 30: Vp Tracking ($\overline{\text{Track_En}}$ = 0V)

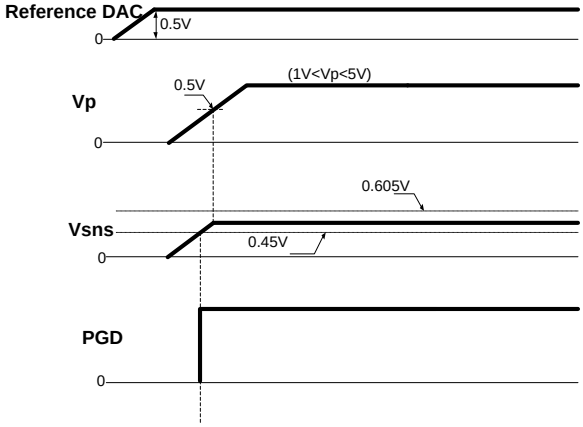


Figure 31: Vp Sequencing ($\overline{\text{Track_En}}$ =Float)

Over-Voltage Protection (OVP)

Over-voltage protection in IR38062 is achieved by comparing sense pin voltage Vsns to a configurable overvoltage threshold.

For non-tracking operation, in analog mode, or in digital mode using the default configuration, the OVP threshold is set to 0.605V; for tracking operation, it is set at 1.2*Vp.

For non-tracking operation, in digital mode, the OVP threshold may be reprogrammed to within 655 mV of the output voltage (for output voltages lower than 2.555V, without any resistive divider on the Fb pin), using the VOUT_OV_FAULT_LIMIT PMBus command. For an OVP threshold programmed to be more than 655 mV greater than the output voltage,

the effective OV threshold ceases to be an absolute value and instead tracks the output voltage with a 655 mV offset.

When Vsns exceeds the over voltage threshold, an over voltage trip signal asserts after 200ns (typ.) delay. The default response is that the high side drive signal HDrv is latched off immediately and PGood flags are set low. The low side drive signal is kept on until the Vsns voltage drops below the threshold. HDrv remains latched off until a reset is performed by cycling either Vcc or Enable, or in the digital mode, using the OPERATION command. IR38062 allows the user to reconfigure this response by the use of the VOUT_OV_FAULT_RESPONSE PMBus command. In addition to the default response described above, this command can be used to configure the device such that Vout overvoltage faults are ignored and the converter remains enabled. (however, they will still be flagged in the STATUS_REGISTERS and by $\overline{\text{SAlert}}$). For further details on the corresponding PMBus commands related to OVP, please refer to the UN0060 IR3806x PMBus commandset user note.

Vsns voltage is set by an external resistive voltage divider connected to the output.

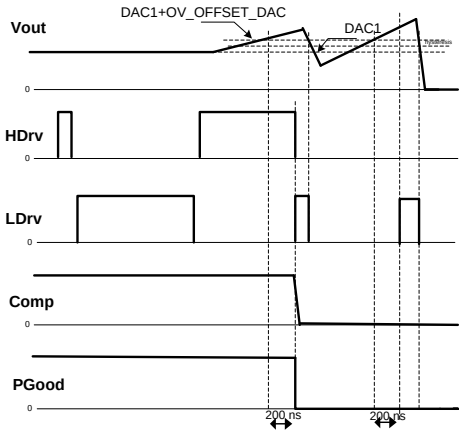


Figure 32: Timing Diagram for OVP in non-tracking mode

MINIMUM ON TIME CONSIDERATIONS

The minimum ON time is the shortest amount of time for Ctrl FET to be reliably turned on. This is a very critical parameter for low duty cycle, high frequency applications. In the conventional approach, when the error amplifier output is near the bottom of the ramp waveform with which it is compared to generate the PWM output, propagation delays can be high enough to cause pulse skipping, and hence limit the minimum pulse width that can be realized. Moreover, in the conventional approach, the bottom of the ramp often presents a high gain region to the error amplifier output, making the modulator more susceptible to noise and requiring the use of lower control loop bandwidth to prevent noise, jitter and pulse skipping.

IR has developed a proprietary scheme to improve and enhance the minimum pulse width which minimizes these delays and hence, allows stable operation with pulse-widths as small as 35ns. At the same time, this scheme also has greater noise immunity, thus allowing stable, jitter free operation down to very low pulse widths even with a high control loop bandwidth, thus reducing the required output capacitance.

Any design or application using IR38062 must ensure operation with a pulse width that is higher than the minimum on-time and at least 50 ns of on-time is recommended in the application. This is necessary for the circuit to operate without jitter and pulse-skipping, which can cause high inductor current ripple and high output voltage ripple.

$$t_{on} = \frac{D}{F_s} = \frac{V_{out}}{Vin \times F_s} \quad (2)$$

In any application that uses IR38062, the following condition must be satisfied:

$$t_{on(\min)} \le t_{on} \quad (3)$$

$$t_{on(\min)} \le \frac{V_{out}}{V_{in} \times F_s} \quad (4)$$

$$\therefore V_{in} \times F_s \le \frac{V_{out}}{t_{on(\min)}} \quad (5)$$

The minimum output voltage is limited by the reference voltage and hence $V_{out(min)}$ = 0.5V. Therefore, for $V_{out(min)}$ = 0.5V,

$$\therefore V_{in} \times F_s \le \frac{V_{out}}{t_{on(\min)}} \quad (6)$$

$$\therefore V_{in} \times F_s \le \frac{0.5V}{50nS} = 10V / \mu S$$

Therefore, at the maximum recommended input voltage 21V and minimum output voltage, the converter should be designed at a switching frequency that does not exceed 476 kHz. Conversely, for operation at the maximum recommended operating frequency (1.5 MHz) and minimum output voltage (0.5V), the input voltage (PVin) should not exceed 6.7V, otherwise pulse skipping may happen.

MAXIMUM DUTY RATIO

A certain off-time is specified for IR38062. This provides an upper limit on the operating duty ratio at any given switching frequency. The off-time remains at a relatively fixed ratio to switching period in the low and mid frequency range, while at higher frequencies, the maximum duty ratio at which IR38062 can operate shows a corresponding decrease. Figure 33 shows a plot of the maximum duty ratio vs. the switching frequency with built in input voltage feed forward mechanism.

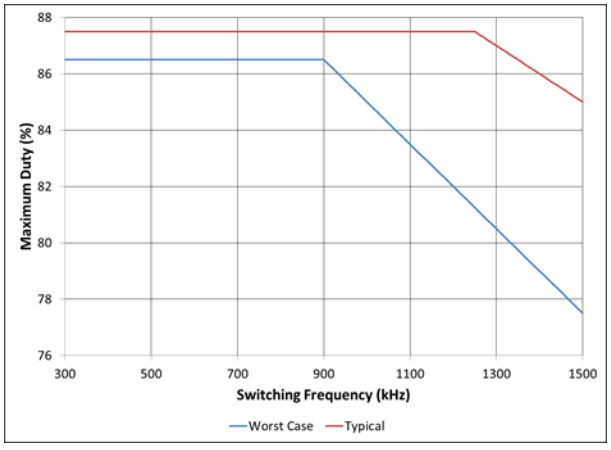


Figure 33: Maximum duty cycle vs. switching frequency

DESIGN EXAMPLE

The following example is a typical application for the IR38062.

PV_{in} = V_{in}=12V
F_s = 607 kHz
V_o = 1.2V
I_o = 15A
Ripple Voltage = ± 1% * V_o
ΔV_o = ± 5% * Vo (for 30% load transient)
Digital mode operation

Enabling the IR38062

As explained earlier, in analog mode, the precise threshold of the Enable lends itself well to implementation of a UVLO for the Bus Voltage as shown in Figure 34.

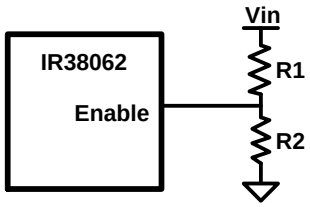


Figure 34: Using Enable pin for UVLO implementation

For a typical Enable threshold of V_{EN} = 1.2 V

$$PV_{in(\min)} \times \frac{R_2}{R_1 + R_2} = V_{EN} = 1.2 \quad (7)$$

$$R_2 = R_1 \frac{V_{EN}}{PV_{in(\min)} - V_{EN}} \quad (8)$$

For $PV_{in\ (min)}$=9.2V, R_1=49.9K and R_2=7.5K ohm is a good choice.

Alternatively, if used in digital mode, the PVin UVLO thresholds may be programmed to suitable values such as 9V and 8V, through the VIN_ON and VIN_OFF PMBus commands or through the appropriate configuration registers respectively.

Programming the frequency

The device is programmed with a default switching frequency=607 kHz. This value may be read using the FREQUENCY_SWITCH PMBus command.

If operating in analog mode, the timing resistor Rt should be chosen to be 3.83K

Output Voltage Programming

The IR38062 offers flexibility for programming the output voltage. Two distinct methods of programming the Output voltage are available and the appropriate one should be chosen depending upon if the mode of operation is analog or digital.

In the analog mode of operation, the output voltage is programmed by the reference voltage and an external resistive divider. The FB pin is the inverting input of the error amplifier, which is internally referenced to VREF.
The divider ratio is set such that the voltage at the VREF pin equals that at the FB pin when the output is at its desired value. When an external resistor divider is connected to the output as shown in Figure 35, the output voltage is defined by using the following equation:

$$V_o = V_{ref} \times \left(1 + \frac{R_5}{R_6}\right) \quad (9)$$

$$R_6 = R_5 \times \left(\frac{V_{ref}}{V_o - V_{ref}}\right) \quad (10)$$

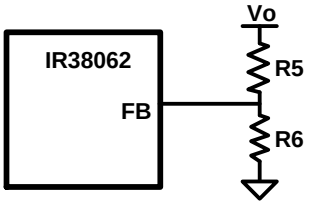


Figure 35: Typical application of the IR38062 for programming the output voltage

However, in the digital mode of operation, the Vout related PMBus commands and the Vout related registers allow the user to program the output voltage directly, by changing the reference voltage (up to a maximum of 2.555V) in response to the commanded

voltage. Therefore, no resistive divider is necessary for this design since Vo=1.2V.

Bootstrap Capacitor Selection

To drive the Control FET, it is necessary to supply a gate voltage at least 4V greater than the voltage at the SW pin, which is connected to the source of the Control FET. This is achieved by using a bootstrap configuration, which comprises the internal bootstrap diode and an external bootstrap capacitor (C1). The operation of the circuit is as follows: When the sync FET is turned on, the capacitor node connected to SW is pulled down to ground. The capacitor charges towards V_{cc} through the internal bootstrap diode (Figure 36), which has a forward voltage drop V_D. The voltage V_c across the bootstrap capacitor C1 is approximately given as:

$$V_c \cong V_{cc} - V_D \tag{11}$$

When the control FET turns on in the next cycle, the capacitor node connected to SW rises to the bus voltage PV_{in}. However, if the value of C1 is appropriately chosen, the voltage V_c across C1 remains approximately unchanged and the voltage at the Boot pin becomes:

$$V_{Boot} \cong PV_{in} + V_{cc} - V_D \tag{12}$$

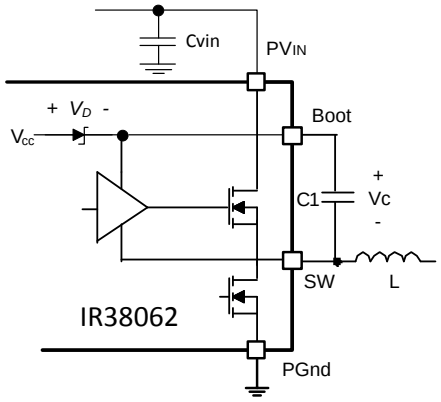


Figure 36: Bootstrap circuit to generate Vc voltage

A bootstrap capacitor of value 0.1uF is suitable for most applications.

Input Capacitor Selection

The ripple currents generated during the on time of the control FETs should be provided by the input capacitor. The RMS value of this ripple for each channel is expressed by:

$$I_{RMS} = I_o \times \sqrt{D \times (1 - D)} \tag{13}$$

$$D = \frac{V_o}{PV_{in}} \tag{14}$$

Where:

D is the Duty Cycle

I_{RMS} is the RMS value of the input capacitor current.

Io is the output current.

I_o=15A and *D* = 0.1, the I_{RMS} = 4.5A.

Ceramic capacitors are recommended due to their peak current capabilities. They also feature low ESR and ESL at higher frequency which enables better efficiency. For this application, it is advisable to have 3x22uF, 25V ceramic capacitors, C3216X5R1E226M160AB from TDK. In addition to these, although not mandatory, a 1x330uF, 25V SMD capacitor EEV-FK1E331P from Panasonic may also be used as a bulk capacitor and is recommended if the input power supply is not located close to the converter.

Inductor Selection

Inductors are selected based on output power, operating frequency and efficiency requirements. A low inductor value causes large ripple current, resulting in the smaller size, faster response to a load transient but poor efficiency and high output noise. Generally, the selection of the inductor value can be reduced to the desired maximum ripple current in the inductor (Δi). The optimum point is usually found between 20% and 50% ripple of the output current. For the buck converter, the inductor value for the desired operating ripple current can be determined using the following relation:

$$PV_{in} - V_o = L \times \frac{\Delta i}{\Delta t}; \Delta t = D \times \frac{1}{F_s}$$

$$L = (PV_{in} - V_o) \times \frac{V_o}{PV_{in} \times \Delta i \times F_s} \tag{15}$$

Where:

PV_{in} = Maximum input voltage

V_0 = Output Voltage
Δi = Inductor Ripple Current
F_s = Switching Frequency
Δ_t = On time for Control FET
D = Duty Cycle

If $\Delta i \approx 40\% * I_o$, then the inductor is calculated to be 0.3µH. Select L=0.3µH, 59PR9874N, from Cyntec which provides a compact, low DCR inductor suitable for this application. The selected inductor value give a peak-to-peak inductor ripple current=6A.

Output Capacitor Selection

The voltage ripple and transient requirements determine the output capacitors type and values. The criterion is normally based on the value of the Effective Series Resistance (ESR). However the actual capacitance value and the Equivalent Series Inductance (ESL) are other contributing components. These components can be described as:

$$\Delta V_o = \Delta V_{o(ESR)} + \Delta V_{o(ESL)} + \Delta V_{o(C)}$$

$$\Delta V_{0(ESR)} = \Delta I_L \times ESR$$

$$\Delta V_{0(ESL)} = \left(\frac{PV_{in} - V_o}{L} \right) \times ESL$$

$$\Delta V_{0(C)} = \frac{\Delta I_L}{8 \times C_o \times F_s} \quad \textbf{(16)}$$

Where:
ΔV_0 = Output Voltage Ripple
ΔI_L = Inductor Ripple Current

Since the output capacitor has a major role in the overall performance of the converter and determines the transient response, selection of the capacitor is critical. The IR38062 can perform well with all types of capacitors.

As a rule, the capacitor must have low enough ESR to meet output ripple and load transient requirements.

The goal for this design is to meet the voltage ripple requirement in the smallest possible capacitor size. Therefore it is advisable to select ceramic capacitors due to their low ESR and ESL and small size. Five of TDK C2012X5R0J476M (47uF/0805/X5R/6.3V) capacitors is a good choice.

It is also recommended to use a 0.1µF ceramic capacitor at the output for high frequency filtering.

Feedback Compensation

The IR38062, while allowing flexibility and configurability through the digital wrapper of the PMBus interface, still employs a high performance voltage mode control engine. The control loop is a single voltage feedback path including error amplifier and a PWM comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed-loop transfer function with the highest 0 dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, -40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180°. The resonant frequency of the LC filter is expressed as follows:

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{L_o \times C_o}} \quad (17)$$

Figure 37 shows gain and phase of the LC filter. Since we already have 180° phase shift from the output filter alone,
the system runs the risk of being unstable.

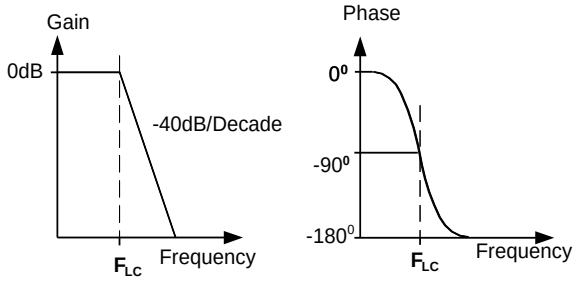


Figure 37: Gain and Phase of LC filter

The IR38062 uses a voltage-type error amplifier with high-gain (90dB) and high-bandwidth (30MHz). The

output of the amplifier is available for DC gain control and AC phase compensation.

The error amplifier can be compensated either in type II or type III compensation.

Local feedback with Type II compensation is shown in Figure 38.

This method requires that the output capacitor have enough ESR to satisfy stability requirements. If the output capacitor's ESR generates a zero at 5kHz to 50kHz, the zero generates acceptable phase margin and the Type II compensator can be used.

The ESR zero of the output capacitor is expressed as follows:

$$F_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_o} \quad (18)$$

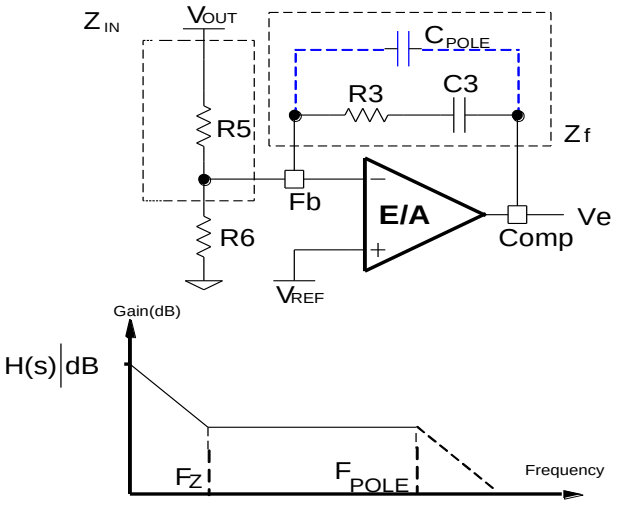


Figure 38: Type II compensation network and its asymptotic gain plot

The transfer function (V_e/V_{out}) is given by:

$$\frac{V_e}{V_{out}} = H(s) = -\frac{Z_f}{Z_{IN}} = -\frac{1 + sR_3C_3}{sR_5C_3} \quad (19)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s)| = \frac{R_3}{R_5} \quad (20)$$

$$F_z = \frac{1}{2 \times \pi \times R_3 \times C_3} \quad (21)$$

First select the desired zero-crossover frequency (F_o):

$$F_o > F_{ESR} \text{ and } F_o \le (1/5 \sim 1/10) \times F_s \quad (22)$$

Use the following equation to calculate R3:

$$R_3 = \frac{V_{osc} \times F_o \times F_{ESR} \times R_5}{PV_{in} \times F_{LC}^2} \quad (23)$$

Where:

PV_{in} = Maximum Input Voltage
V_{osc} =Effective amplitude of the oscillator ramp
F_o = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
R_5 = Feedback Resistor

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_Z = 75\% \times F_{LC}$$

$$F_Z = 0.75 \times \frac{1}{2 \times \pi \sqrt{L_o \times C_o}} \quad (24)$$

Use equation (22), (23) and (24) to calculate C3.

One more capacitor is sometimes added in parallel with C3 and R3. This introduces one more pole which is mainly used to suppress the switching noise.

The additional pole is given by:

$$F_p = \frac{1}{2 \times \pi \times \frac{C_3 \times C_{POLE}}{C_3 + C_{POLE}}} \quad (25)$$

The pole sets to one half of the switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi \times R_3 \times F_S - \frac{1}{C_3}} \cong \frac{1}{\pi \times R_3 \times F_S} \quad (26)$$

For a general unconditional stable solution for any type of output capacitors with a wide range of ESR

values, we use a local feedback with a type III compensation network. The typically used compensation network for voltage-mode controller is shown in Figure 39.

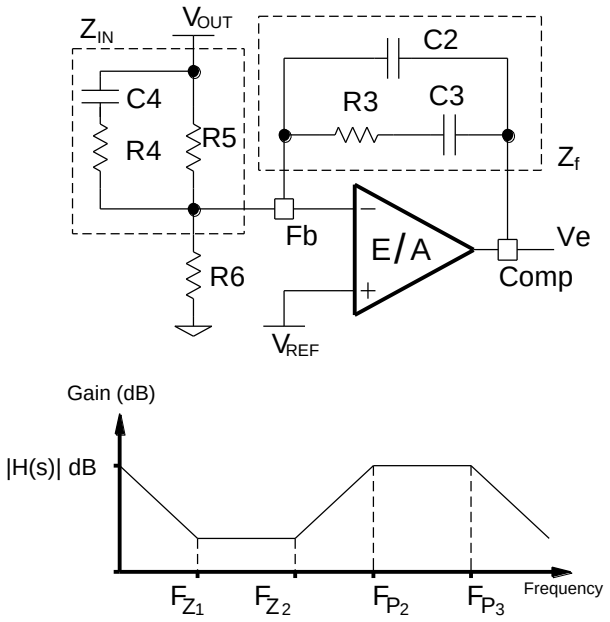


Figure 39: Type III Compensation network and its asymptotic gain plot

Again, the transfer function is given by:

$$\frac{V_e}{V_{out}} = H(s) = -\frac{Z_f}{Z_{IN}}$$

By replacing Z_{in} and Z_f, according to Figure 39, the transfer function can be expressed as:

$$H(s) = -\frac{(1+sR_3C_3)[1+sC_4(R_4+R_5)]}{sR_5(C_2+C_3)\left[1+sR_3\left(\frac{C_2\times C_3}{C_2+C_3}\right)\right](1+sR_4C_4)} \quad (27)$$

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0 \quad (28)$$

$$F_{P2} = \frac{1}{2\pi\times R_4\times C_4} \quad (29)$$

$$F_{P3} = \frac{1}{2\pi\times R_3\left(\frac{C_2\times C_3}{C_2+C_3}\right)} \cong \frac{1}{2\pi\times R_3\times C_2} \quad (30)$$

$$F_{Z1} = \frac{1}{2\pi\times R_3\times C_3} \quad (31)$$

$$F_{Z2} = \frac{1}{2\pi\times C_4\times(R_3\times R_5)} \cong \frac{1}{2\pi\times C_4\times R_5} \quad (32)$$

Cross over frequency is expressed as:

$$F_o = R_3\times C_4\times\frac{PV_{in}}{V_{osc}}\times\frac{1}{2\pi\times L_o\times C_o} \quad (33)$$

Based on the frequency of the zero generated by the output capacitor and its ESR, relative to the crossover frequency, the compensation type can be different. Table 5 shows the compensation types for relative locations of the crossover frequency.

Table 5: Different types of compensators

Compensator Type	F_{ESR} vs F_O	Typical Output Capacitor
Type II	$F_{LC} < F_{ESR} < F_O < F_S/2$	Electrolytic
Type III	$F_{LC} < F_O < F_{ESR}$	SP Cap, Ceramic

The higher the crossover frequency is, the potentially faster the load transient response will be. However, the crossover frequency should be low enough to allow attenuation of switching noise. Typically, the control loop bandwidth or crossover frequency (F_o) is selected such that:

$$F_o \le (1/5 \sim 1/10)^* F_s$$

The DC gain should be large enough to provide high DC-regulation accuracy. The phase margin should be greater than 45° for overall stability.

In this design, we target F_o= 75 kHz.

The specifications

PV_{in} = 12V

V_o = 1.2V

V_{osc} = 1.357 (This is a function of PVin, duty cycle and switching frequency. Infineon's SupIRBuck online design tool can help the user in accounting for this operating point dependency of the effective oscillator ramp amplitude)
V_{ref} = 1.2V
L_o = 0.3 µH
C_o = 5 x 47µF, ESR≈3mΩ each

It must be noted here that the value of the capacitance used in the compensator design must be the small signal value. For instance, the small signal capacitance of the 47µF capacitor used in this design is 34µF at 1.2 V DC bias and 607 kHz frequency. It is this value that must be used for all computations related to the compensation. The small signal value may be obtained from the manufacturer's datasheets, design tools or SPICE models. Alternatively, they may also be inferred from measuring the power stage transfer function of the converter and measuring the double pole frequency F_{LC} and using equation **(22)** to compute the small signal C_o.

These result to:
F_{LC} = 22.3 kHz
F_{ESR} = 1220 kHz
$F_s/2$ = 300 kHz
Select crossover frequency F_0=75 kHz

Since $F_{LC}<F_0<Fs/2<F_{ESR}$, Type III is selected to place the pole and zeros.

Detailed calculation of compensation Type III:

Desired Phase Margin Θ = 70°

$$F_{Z2} = F_o\sqrt{\frac{1-\sin\Theta}{1+\sin\Theta}} = 13.22 \text{ kHz}$$

$$F_{P2} = F_o\sqrt{\frac{1+\sin\Theta}{1-\sin\Theta}} = 425.35 \text{ kHz}$$

Select:

$$F_{Z1} = 0.5\times F_{Z2} = 6.61 \text{ kHz and}$$

$$F_{P3} = 0.5\times F_s = 300 \text{ kHz}$$

Select C_4 = 2.2nF.

Calculate R_3, C_3 and C_2:

$$R_3 = \frac{2\times\pi\times F_o\times L_o\times C_o\times V_{osc}}{C_4\times PV_{in}}$$; R_3 = 1.18 kΩ,

Select: R_3 = 1.21 kΩ

$$C_3 = \frac{1}{2\times\pi\times F_{Z1}\times R_3}$$; C_3 = 19.3 nF, Select: C_3 = 22 nF

$$C_2 = \frac{1}{2\times\pi\times F_{P3}\times R_3}$$; C_2 = 450 pF, Select: C_2 = 390 pF

Calculate R_4, R_5 and R_6:

$$R_4 = \frac{1}{2\times\pi\times C_4\times F_{P2}}$$; R_4 = 170 Ω, Select R_4 = 182 Ω

$$R_5 = \frac{1}{2\times\pi\times C_4\times F_{Z2}}$$; R_5 = 5.29kΩ, Select R_5 = 5.62 kΩ

In digital mode, R6 is not necessary.

Setting the Power Good Threshold

In digital mode, the PMBus commands POWER_GOOD_ON and POWER_GOOD_OFF, or the corresponding registers may be used to adjust the power good thresholds to within 630 mV of the output voltage (for output voltages <2.555V). In this design, the power good thresholds have been set such that the Power Good is asserted when the output voltage rises above 1.074V, and is de-asserted when the output voltage falls below 1V, giving 74mV of hysteresis.

In this design, a power good assertion delay of 0 ms was programmed. Therefore, the PGood signal asserts as soon as the output voltage rises above the

power good assertion threshold, and remains asserted until the output voltage drops below the power good de-assertion threshold. There is a fixed 160us delay for power good de-assertion. It should be noted, however, that an overvoltage condition or any fault condition that causes a shutdown will lead to PGood de-assertion without any delay.

Selecting Power Good Pull-Up Resistor

The PGood is an open drain output and require pull up resistors to VCC. The value of the pull-up resistors should limit the current flowing into the PGood pin to less than 5mA. A typical value used is 4.99kΩ.

Setting the Overvoltage Threshold

In digital mode, the overvoltage protection threshold may be programmed using the PMBus command VOUT_OV_FAULT_LIMIT, or the corresponding configuration registers, to within 655 mV of the output voltage (for output voltages <2.555V). In this design, the threshold has been set to 1.5V. The fault response has been set to shutdown, so that an overvoltage condition will cause the part to shutdown with the sync FET remaining on until the voltage drops 5% below the overvoltage threshold. In analog

Setting the Overcurrent Threshold

For this 15A design, the overcurrent protection threshold has been programmed such that the part goes into a hiccup current limiting mode when the inductor valley current exceeds 20A, or when the load current exceeds ~23A.

Communicating on the I2C/PMBus

In order to enable digital mode, as explained earlier, a resistor needs to be connected from the ADDR pin to LGnd. In this design, R_{ADDR} was chosen to be 0 ohm, to have no offset from the base i2c/PMBus address.

Further, Infineon's PowIRCenter USB-to-I2C dongles have their SCL and SDA lines internally pulled up to 3.3V. Therefore, although this design provides placeholders for the bus pullups, they may be left unpopulated if the PowIRCenter dongle is used. The $\overline{\text{SAlert}}$ line is pulled up to Vcc with a 4.99K resistor.

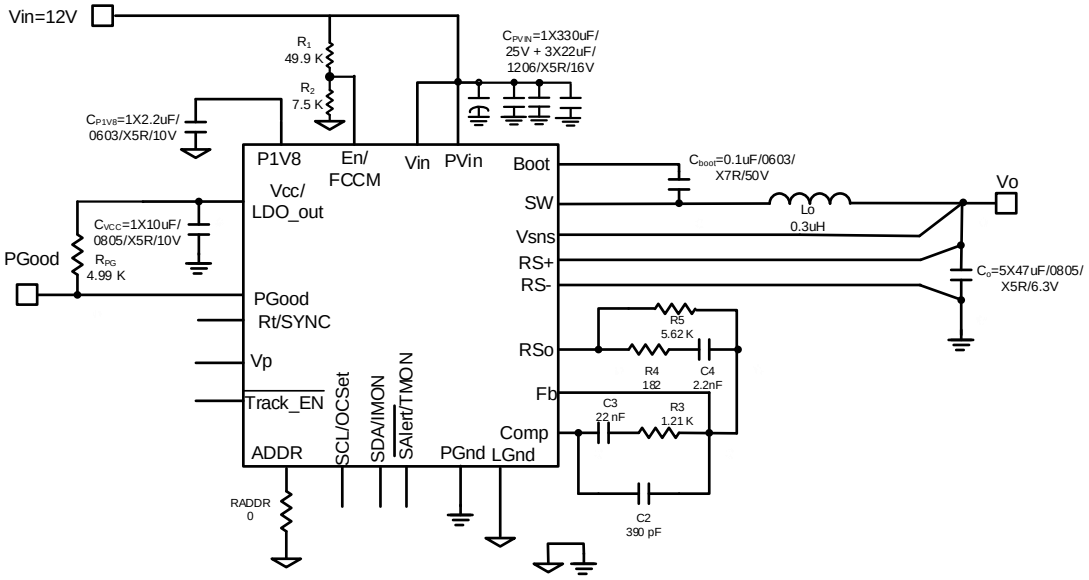


Figure 40: Application circuit for a single supply, 12V to 1.2V, 15A Point of Load Converter

TYPICAL OPERATING WAVEFORMS

Vin = PVin = 12V, Vout = 1.2V, Iout = 0-15A, Room Temperature, No Air Flow

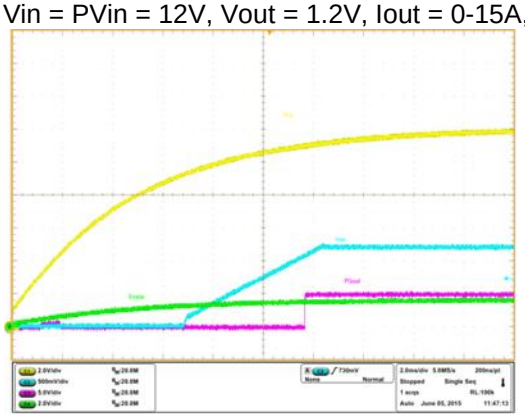


Figure 41: PV_{in} Start up at 15A Load
Ch_1:P_{Vin}, Ch_2:V_{out}, Ch_3:P_{Good}, Ch_4:Enable

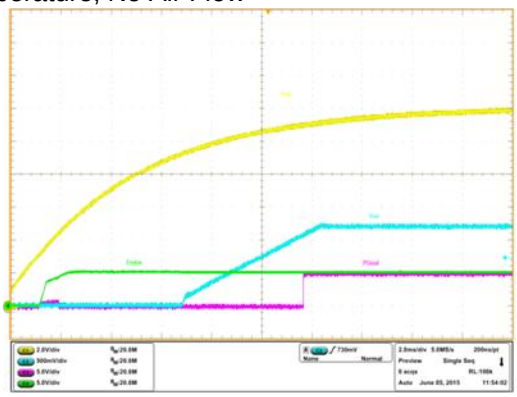


Figure 42:PV_{in} Start up at 15A Load
Ch_1:P_{Vin}, Ch_2:V_{out}, Ch_3:P_{Good},Ch_4:V_{cc}

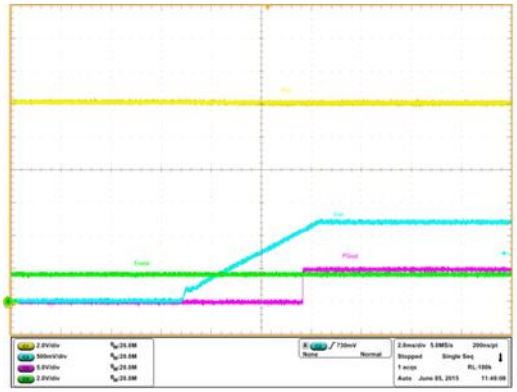


Figure 43:Operation 80,Turn ON without margining, 15A load
Ch_1:P_{Vin}, Ch_2:V_{out}, Ch_3:P_{Good}, Ch_4:Enable

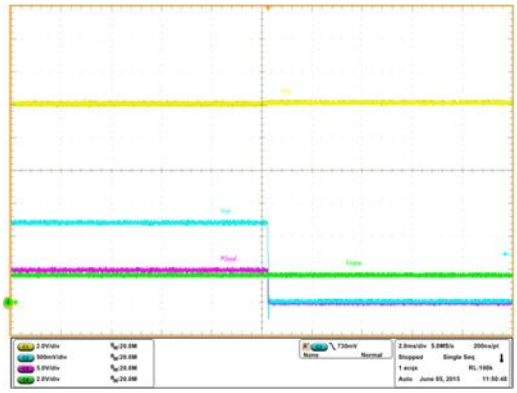


Figure 44: Operation 00, Immediate OFF, 15A load
Ch_1:P_{Vin}, Ch_2:V_{out}, Ch_3:P_{Good}, Ch_4:Enable

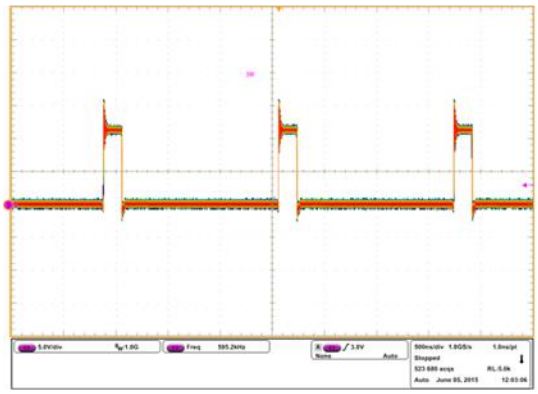


Figure 45: Inductor node at 15A load
Ch_3:SW node

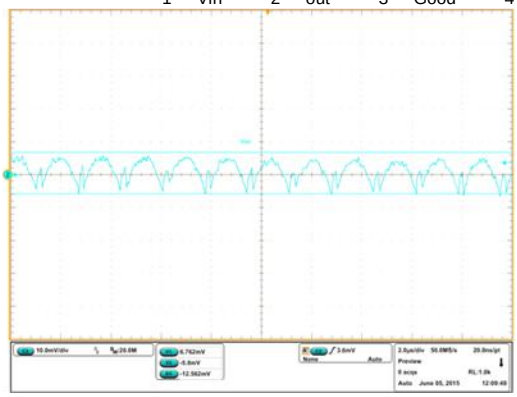


Figure 46: Output voltage ripple at 15A load
Ch_2:V_{out}

TYPICAL OPERATING WAVEFORMS

Vin = PVin = 12V, Vout = 1.2V, Iout = 0-15A, Room Temperature, No Air Flow

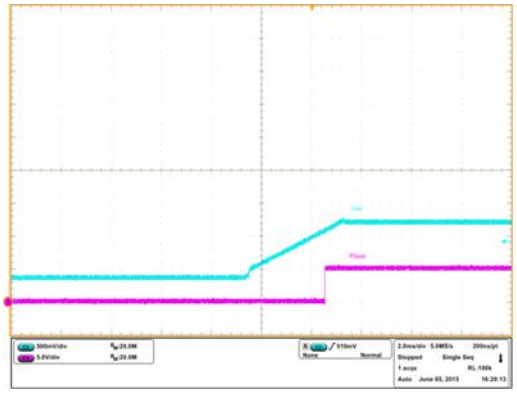


Figure 47: 0.35V Prebias voltage startup at 0A load
Ch_2:V_{out}, Ch_3:P_{Good}

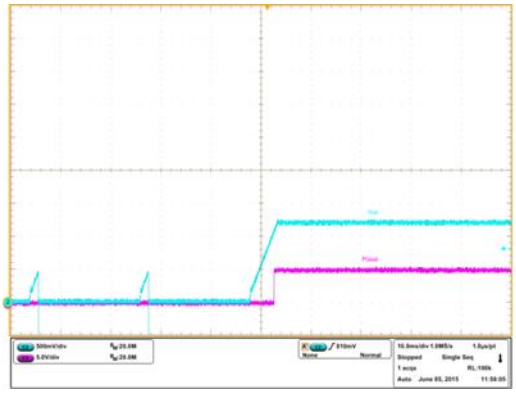


Figure 48: Short-circuit recovery (Hiccup) at 15A load
Ch2:V_{out}, Ch3:P_{Good}

TYPICAL OPERATING WAVEFORMS

Vin = PVin = 12V, Vout = 1.2V, Iout = 0-15A, Room Temperature, No Air Flow

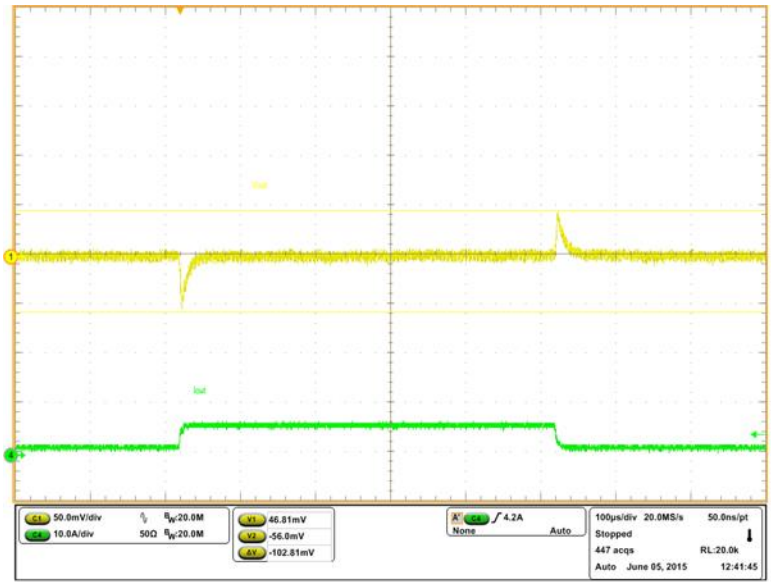


Figure 49: Transient Response, 1.5A to 6A step (2.5A/us)
Ch_1:V_{out}, Ch_4:I_{out}

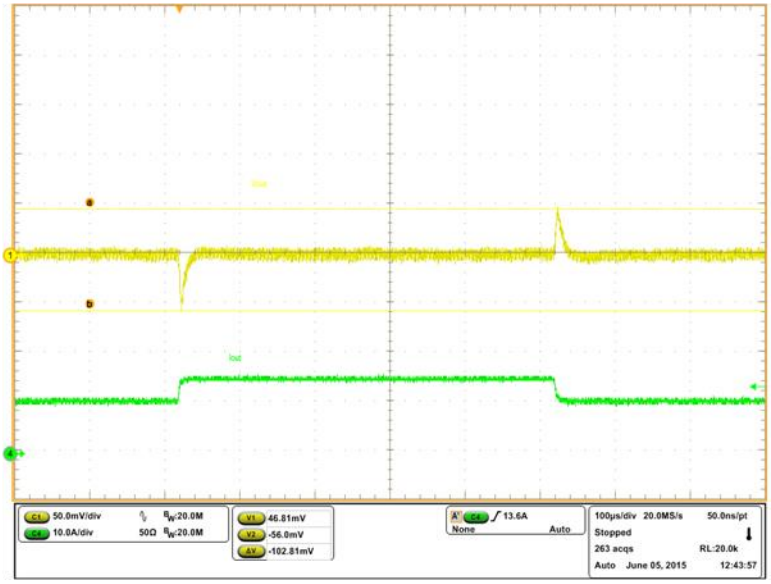


Figure 50: Transient Response, 10.5A to 15A step (2.5A/us)
Ch_1:V_{out}, Ch_4:I_{out}

TYPICAL OPERATING WAVEFORMS

Vin = PVin = 12V, Vout = 1.2V, Iout = 0-15A, Room Temperature, No Air Flow

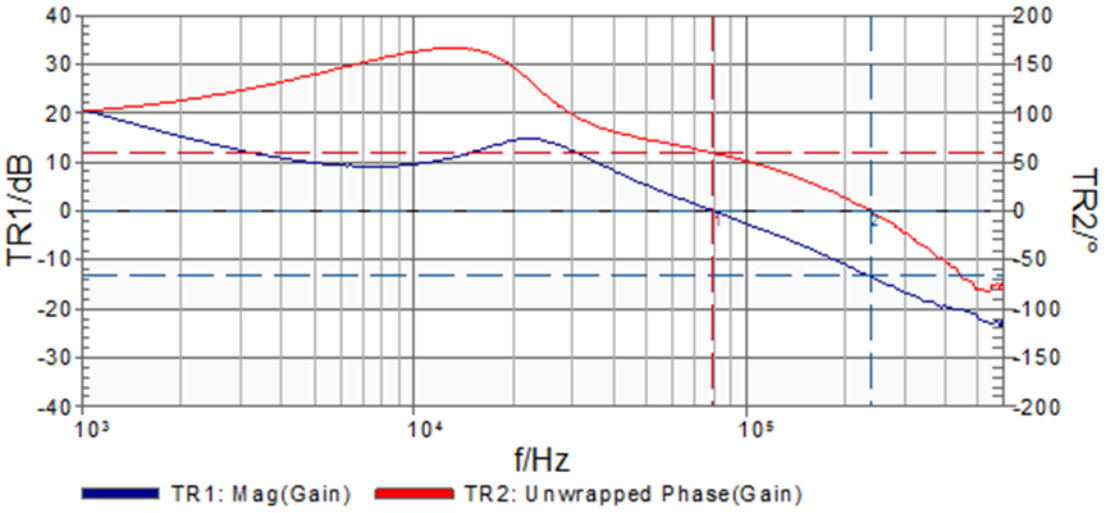


Figure 51: Bode Plot at 0A load
Bandwidth = 79.6kHz, Phase Margin = 59.5° , Gain Margin = 13.4dB

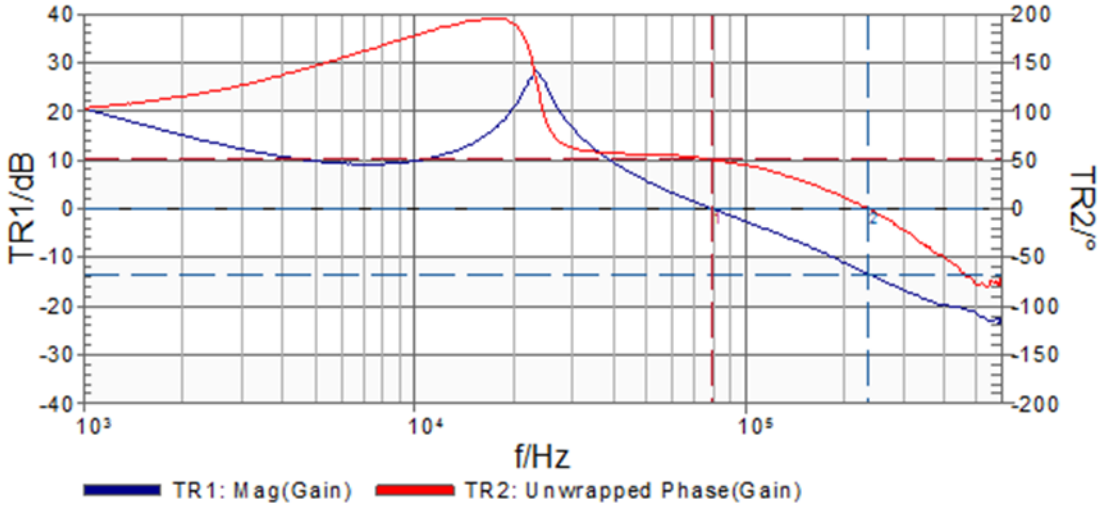


Figure 52: Bode Plot at 15A load
Bandwidth = 79.6kHz, Phase Margin = 50.3° , Gain Margin = 13.4dB

TYPICAL OPERATING WAVEFORMS

Vin = PVin = 12V, Vout = 1.2V, Iout = 0-15A, Room Temperature, No Air Flow

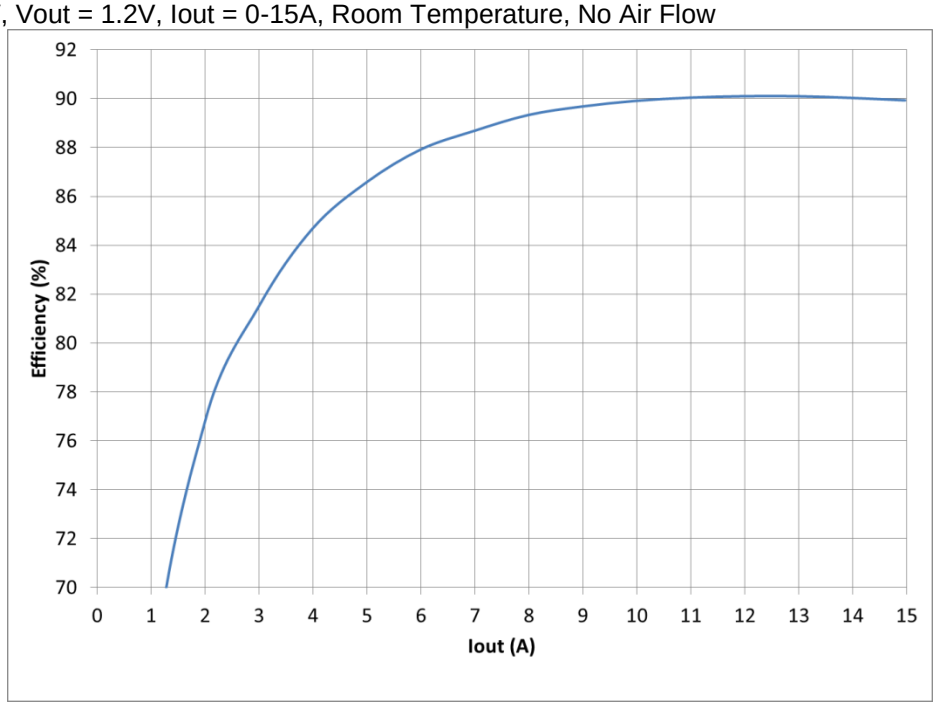


Figure 53: Efficiency versus load current

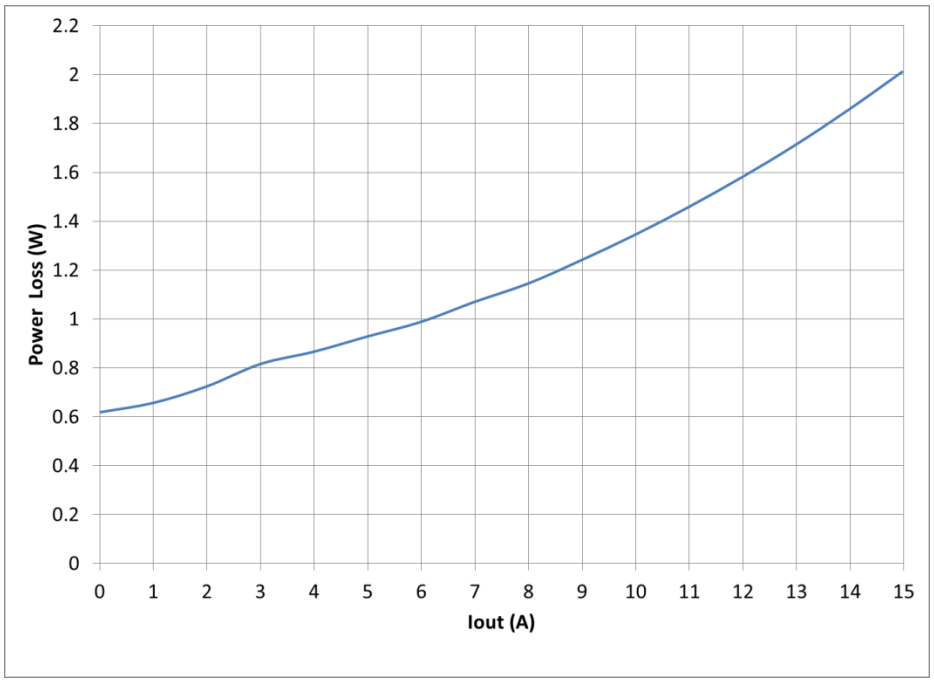


Figure 54: Power loss versus load current

TYPICAL OPERATING WAVEFORMS

Vin = PVin = 12V, Vout = 1.2V, Iout = 0-15A, Room Temperature, No Air Flow

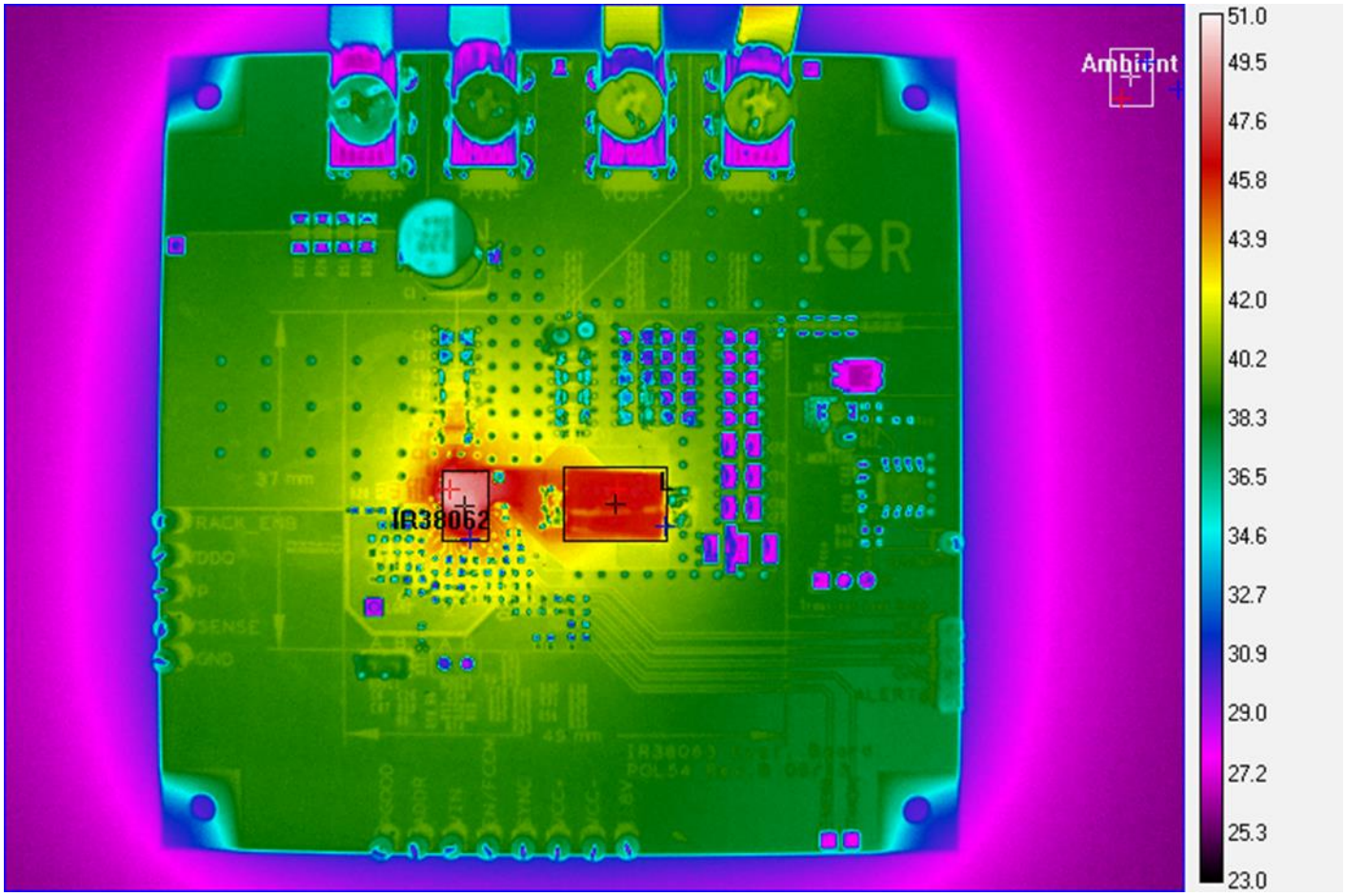


Figure 55: Thermal Image of the board at 15A load
IR38062: 50.0°C, inductor: 46.8°C, Ambient:25.8°C

Code	Command	Value
01	OPERATION	On
02	ON_OFF_CONFIG	0x1F
10	WRITE_PROTECT	0x00
19	CAPABILITY	0xB0
1B	SMBALERT_MASK	
	STATUS_VOUT	00
	STATUS_IOUT	00
	STATUS_INPUT	00
	STATUS_TEMPERATURE	00
	STATUS_CML	00
21	VOUT_COMMAND	1.203 V
22	VOUT_TRIM	0.000 V
24	VOUT_MAX	6.000 V
25	VOUT_MARGIN_HIGH	1.258 V
26	VOUT_MARGIN_LOW	1.137 V
27	VOUT_TRANSITION_RATE	0.125 mV/us
29	VOUT_SCALE_LOOP	1.000
33	FREQUENCY_SWITCH	600 KHz
35	VIN_ON	1.000 V
36	VIN_OFF	0.500 V
39	IOUT_CAL_OFFSET	0.000 A
40	VOUT_OV_FAULT_LIMIT	1.500 V
41	VOUT_OV_FAULT_RESPONSE	Shutdown
42	VOUT_OV_WARN_LIMIT	1.379 V
43	VOUT_UV_WARN_LIMIT	1.020 V
44	VOUT_UV_FAULT_LIMIT	0.961 V
45	VOUT_UV_FAULT_RESPONSE	Ignore

Code	Command	Value
46	IOUT_OC_FAULT_LIMIT	20.000 A
47	IOUT_OC_FAULT_RESPONSE	Immediate off, retry after 20ms
4A	IOUT_OC_WARN_LIMIT	17.500 A
4F	OT_FAULT_LIMIT	145 °C
50	OT_FAULT_RESPONSE	Inhibit
51	OT_WARN_LIMIT	125 °C
55	VIN_OV_FAULT_LIMIT	24.000 V
56	VIN_OV_FAULT_RESPONSE	Ignore
58	VIN_UV_WARN_LIMIT	0.50 V
5E	POWER_GOOD_ON	1.074 V
5F	POWER_GOOD_OFF	1.000 V
60	TON_DELAY	0.0 ms
61	TON_RISE	6.0 ms
62	TON_MAX_FAULT_LIMIT	0.000 ms
63	TON_MAX_FAULT_RESPONSE	Ignore
64	TOFF_DELAY	0.0 ms
65	TOFF_FALL	6.0 ms
78	STATUS_BYTE	0x00
79	STATUS_WORD	0x0000
7A	STATUS_VOUT	0x00
7B	STATUS_IOUT	0x00
7C	STATUS_INPUT	0x00
7D	STATUS_TEMPERATURE	0x00
7E	STATUS_CML	0x00
88	READ_VIN	11.969 V
8B	READ_VOUT	1.199 V
8C	READ_IOUT	0.000 A

Code	Command	Value
64	TOFF_DELAY	0.0 ms
65	TOFF_FALL	6.0 ms
78	STATUS_BYTE	0x00
79	STATUS_WORD	0x0000
7A	STATUS_VOUT	0x00
7B	STATUS_IOUT	0x00
7C	STATUS_INPUT	0x00
7D	STATUS_TEMPERATURE	0x00
7E	STATUS_CML	0x00
88	READ_VIN	11.969 V
8B	READ_VOUT	1.199 V
8C	READ_IOUT	0.000 A
8D	READ_TEMPERATURE_1	29 °C
96	READ_POUT	0.000 W
98	PMBUS_REVISION	0x22
99	MFR_ID	IR
9A	MFR_MODEL	0x32
9B	MFR_REVISION	0x04
AD	IC_DEVICE_ID	0x32
AE	IC_DEVICE_REV	0x04
D6	MFR_I2C_ADDRESS	0x10
D8	MFR_TPGDLY	0 ms
D9	MFR_FCCM	Forced Cont. Conduction M...
DB	MFR_VOUT_PEAK	1.199 V
DC	MFR_IOUT_PEAK	0.0 A
DD	MFR_TEMP_PEAK	29 °C

Figure 56: PMBus Command Summary for the 1.2V design

I2C PROTOCOLS

All registers may be accessed using either I2C or PMBus protocols. I2C allows the use of a simple format whereas PMBus provides error checking capability. Figure 57 shows the I2C format employed by Manhattan

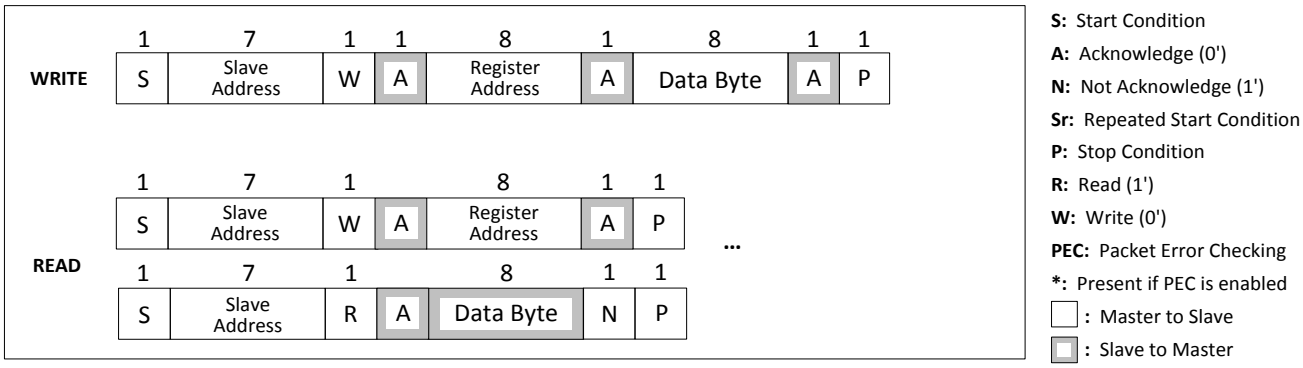


Figure 57: I2C Format

SMBUS/PMBUS PROTOCOLS

To access IR's configuration and monitoring registers, 4 different protocols are required:

the SMBus Read/Write Byte/Word protocol with/without PEC (for status and monitoring)

the SMBus Send Byte protocol with/without PEC (for CLEAR_FAULTS only)

the SMBus Block Read protocol for accessing Model and Revision information

the SMBus Process call (for accessing Configuration Registers)

In addition, Manhattan supports:

Alert Response Address (ARA)

Bus timeout (10ms)

Group Command for writing to many VRs within one command

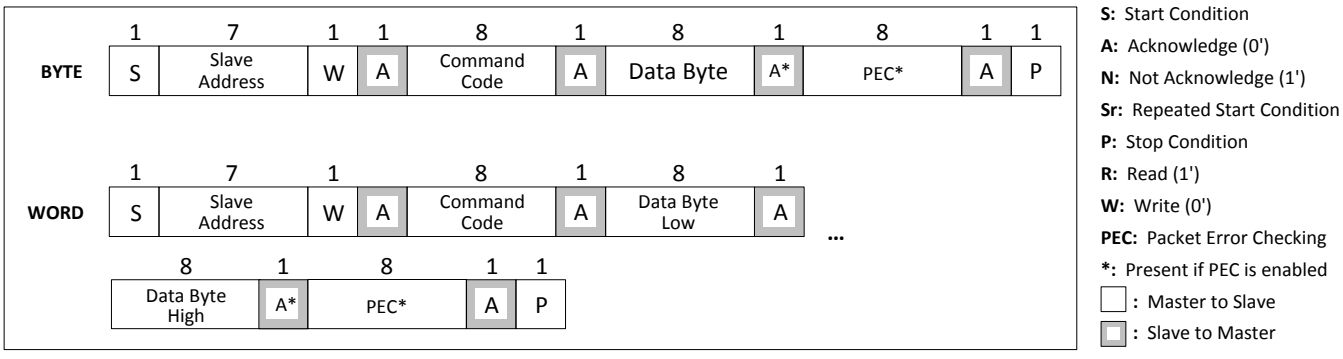


Figure 58: SMBus Write Byte/Word

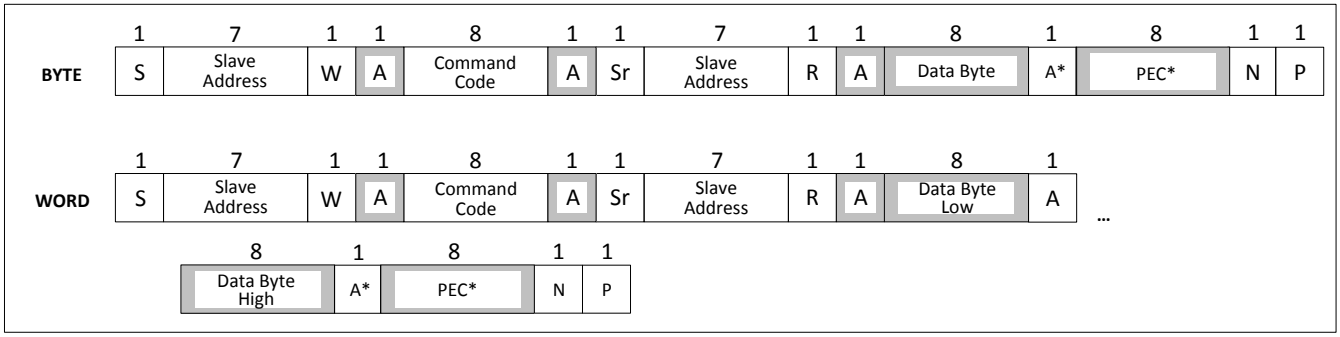


Figure 59: SMBus Read Byte/Word

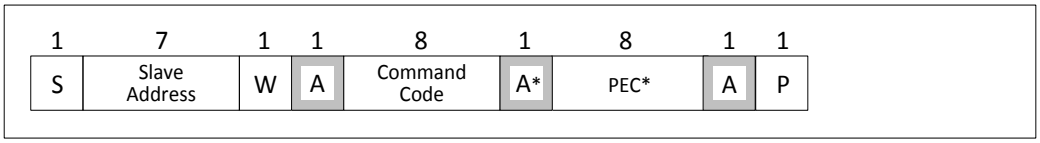


Figure 60: SMBus Send Byte

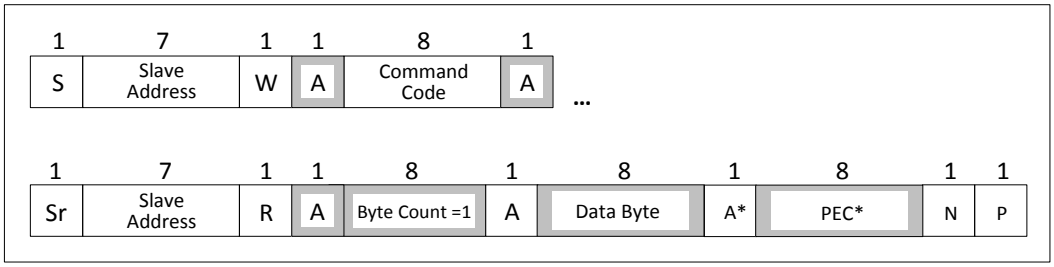


Figure 61: SMBus Block Read with Byte Count=1



Figure 62: MFR specific command to Write an IR Register

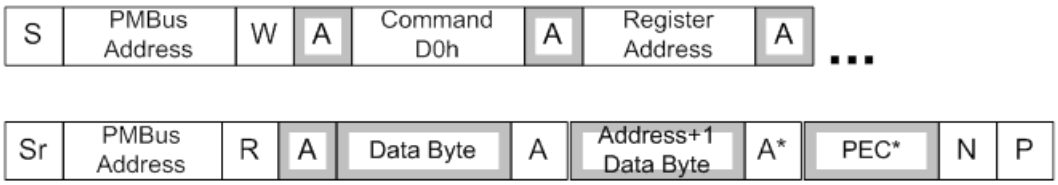


Figure 63: SMBus Custom Process Call to Read an IR Register

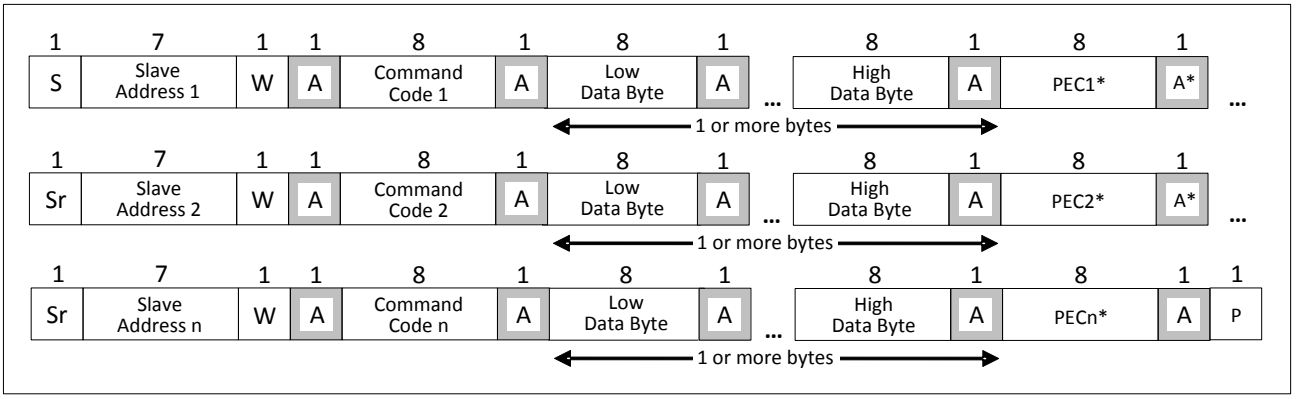


Figure 64: Group Command

LAYOUT RECOMMENDATIONS

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Make the connections for the power components in the top layer with wide, copper filled areas or polygons. In general, it is desirable to make proper use of power planes and polygons for power distribution and heat dissipation.

The input capacitors, inductor, output capacitors and the IR38062 should be as close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place the input capacitor directly at the PVin pin of IR38062.

The feedback part of the system should be kept away from the inductor and other noise sources.

The critical bypass components such as capacitors for Vin, VCC and 1.8V should be close to their respective pins. It is important to place the feedback components including feedback resistors and compensation components close to Fb and Comp pins.

In a multilayer PCB use one layer as a power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point. It is recommended to place all the compensation parts over the analog ground plane in top layer.

The Power QFN is a thermally enhanced package. Based on thermal performance it is recommended to use at least a 6-layers PCB. To effectively remove heat from the device the exposed pad should be connected to the ground plane using vias.

IR38062 has 3 pins, SCL, SDA and $\overline{\text{SALERT}}$ that are used for I2C/PMBus communication. It is recommended that the traces used for these communication lines be at least 10 mils wide with a spacing between the SCL and SDA traces that is at least 2-3 times the trace width. Also, it is important that these traces be routed away from any noise sources (such as Sw node)

SUPPORTED PMBUS COMMANDS

Command Code	Command Name	SMBus transaction	No. of bytes	Range	Resolution	Default Value	Description
01h	OPERATION	R/W Byte	1				Enables or disables the device and controls margining
02h	ON_OFF_CONFIG	R/W Byte	1				Configures the combination of Enable pin input and serial bus commands needed to turn the unit on and off.
03h	CLEAR_FAULTS	Send Byte	0				Clear contents of Fault registers
10h	WRITE_PROTECT	R/W Byte	1				Used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes.
15h	STORE_USER_ALL	Send Byte	0				Burns the User section registers into OTP memory
16h	RESTORE_USER_ALL	Send Byte	0				Copies the OTP registers into User memory
19h	CAPABILITY	Read Byte	1				Returns 1011xxxx to indicate Packet Error Checking is supported, maximum bus speed is 400kHz and SMBAlert# is supported.
1Bh	SMBALERT_MASK	Write word/Block read Process call	2				May be used to prevent a warning or fault condition from asserting the SMBALERT# signal.
21h	VOUT_COMMAND[16]	R/W Word	2	0-2.555V/V_S	5mV/V_S	0.5V	Causes the device to set its output voltage to the commanded value. V_S= VOUT_SCALE_LOOP
22h	VOUT_TRIM[16]	R/W Word	2	-128-+128V		0V	Available to the device user to trim the output voltage
24h	VOUT_MAX[16]	R/W Word	2			6V	Sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations.
25h	VOUT_MARGIN_HIGH[16]	R/W Word	2	0-2.555V/V_S	5mV/V_S	0.55V	Sets the MARGIN high voltage when commanded by OPERATION V_S= VOUT_SCALE_LOOP
26h	VOUT_MARGIN_LOW[16]	R/W Word	2	0-2.555V/V_S	5mV/V_S	0.45V	Sets the MARGIN low voltage when commanded by OPERATION V_L= VOUT_SCALE_LOOP
27h	VOUT_TRANSITION_RATE[11]	R/W Word	2	0-127ms/us		0.125mV/us	Sets the rate in mV/µs at which the output should change voltage. Exponent 0 to -4 allowed.
29h	VOUT_SCALE_LOOP[11]	R/W Word	2	0.125-1		1	Compensates for external resistor divider in feedback path and in the sense path. Values 1, 0.5, 0.25, 0.125 allowed. Exponent -3 allowed.
33h	FREQUENCY_SWITCH[11]	R/W Word	2	166-1500kHz		607kHz	Sets the switching frequency, in kHz. Exponent 0 to 1 allowed.
35h	VIN_ON[11]	R/W Word	2	0-16.5V	0.5V	1V	Sets the value of the input voltage, in volts, at which the unit should start power conversion. Exponent -1 allowed.
36h	VIN_OFF[11]	R/W Word	2	0-16V	0.5V	0.5V	Sets the value of the input voltage, in volts, at which the unit, once operation has started, should stop power conversion. Exponent -1 allowed.
39h	IOUT_CAL_OFFSET[11]	R/W Word	2	-128A-+127.5A	0.5A	0A	Used to null out any offsets in the output current sensing circuit. Exponent -1 allowed.
40h	VOUT_OV_FAULT_LIMIT[16]	R/W Word	2	(25-655mV)/V_S	10mV/V_S	0.605V	Sets the value of the output voltage measured at the sense pin that causes an output overvoltage fault. V_S= VOUT_SCALE_LOOP
41h	VOUT_OV_FAULT_RESPONSE	R/W Byte	1	Ignore/Shutdown		Shutdown	Instructs the device on what action to take in response to an output overvoltage fault.
42h	VOUT_OV_WARN_LIMIT[16]	R/W Word	2		3.9mV	0.56V	Sets the value of the output voltage at the sense pin that causes an output voltage high warning.
43h	VOUT_UV_WARN_LIMIT[16]	R/W Word	2		3.9mV	0.44V	Sets the value of the output voltage at the Sense pin that causes an output voltage low warning.

44h	VOUT_UV_FAULT_LIMIT[16]	R/W Word	2		3.9mV	0.395V	Sets the value of the output voltage at the sense pin that causes an output undervoltage fault.
45h	VOUT_UV_FAULT_RESPONSE	R/W Byte	1	Ignore/Shutdown		Ignore	Instructs the device on what action to take in response to an output undervoltage fault.
46h	IOUT_OC_FAULT_LIMIT[11]	R/W Word	2	3-22.5A	0.5A	20A	Sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an overcurrent fault. Exponent -1 allowed.
47h	IOUT_OC_FAULT_RESPONSE	R/W Byte	1			Hiccup forever	Instructs the device on what action to take in response to an output overcurrent fault.
4Ah	IOUT_OC_WARN_LIMIT[11]	R/W Word	2	0-63.5A	0.5A	17.5A	Sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an overcurrent warning. Exponent -1 allowed.
4Fh	OT_FAULT_LIMIT[11]	R/W Word	2	0-150°C	1°C	145°C	Set the temperature, in degrees Celsius, of the unit at which it should indicate an Overtemperature Fault. Exponent 0 allowed.
50h	OT_FAULT_RESPONSE	R/W Byte	1	Ignore/Shutdown/Inhibit		Inhibit	Instructs the device on what action to take in response to an overtemperature fault.
51h	OT_WARN_LIMIT[11]	R/W Word	2	0-150°C	1°C	125°C	Set the temperature, in degrees Celsius, of the unit at which it should indicate an Overtemperature Warning alarm. Exponent 0 allowed.
55h	VIN_OV_FAULT_LIMIT[11]	R/W Word	2	6.25V-24V	0.25V	24V	Sets the value of the input voltage that causes an input overvoltage fault. Exponent -2 allowed.
56h	VIN_OV_FAULT_RESPONSE	R/W Byte	1	Ignore/Shutdown		Shutdown	Instructs the device on what action to take in response to an input overvoltage fault.
58h	VIN_UV_WARN_LIMIT[11]	R/W Word	2	0-16V	0.5V	0.5V	Sets the value of the input voltage PVin, in volts, that causes an input overvoltage fault. Exponent -1 allowed.
5Eh	POWER_GOOD_ON[16]	R/W Word	2	(0-0.63V)/V_S	10mV/V_S	0.45V	Sets the output voltage at which an optional POWER_GOOD signal should be asserted. V_S=VOUT_SCALE_LOOP
5Fh	POWER_GOOD_OFF[16]	R/W Word	2	(0-0.63V)/V_S	10mV/V_S	0.42V	Sets the output voltage at which an optional POWER_GOOD signal should be negated. V_S=VOUT_SCALE_LOOP
60h	TON_DELAY[11]	R/W Word	2	0-127ms	1ms	0ms	Sets the time, in milliseconds, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise. Exponent 0 allowed.
61h	TON_RISE[11]	R/W Word	2	0-127ms	1ms	2ms	Sets the time, in milliseconds, from when the output starts to rise until the voltage has entered the regulation band. Exponent 0 allowed.
62h	TON_MAX_FAULT_LIMIT[11]	R/W Word	2	0-127ms	1ms	0 (No limit)	Sets an upper limit, in milliseconds, on how long the unit can attempt to power up the output without reaching the output undervoltage fault limit. Exponent 0 allowed.
63h	TON_MAX_FAULT_RESPONSE	R/W Byte	1	Ignore/Shutdown		Ignore	Instructs the device on what action to take in response to a TON_MAX fault.
64h	TOFF_DELAY	R/W Word	2	0-127ms	1ms	0ms	Sets the time, in milliseconds, from a stop condition is received (as programmed by the ON_OFF_CONFIG command) until the unit stops transferring energy to the output. Exponent 0 allowed.
65h	TOFF_FALL	R/W Word	2	0-127ms	1ms	1ms	Device will acknowledge this command but ignore it.
78h	STATUS BYTE	Read Byte	1				Returns 1 byte where the bit meanings are: Bit <7> device busy fault Bit <6> output off (due to fault or enable) Bit <5> Output over-voltage fault Bit <4> Output over-current fault Bit <3> Input Under-voltage fault Bit <2> Temperature fault

							Bit <1> Communication/Memory/Logic fault Bit <0>: None of the above
79h	STATUS WORD	Read Word	2				Returns 2 bytes where the Low byte is the same as the STATUS_BYTE data. The High byte has bit meanings are: Bit <7> Output high or low fault Bit <6> Output over-current fault Bit <5> Input under-voltage fault Bit <4> Reserved; hardcoded to 0 Bit <3> Output power not good Bit <2:0> Hardcoded to 0
7Ah	STATUS_VOUT	Read Byte	1				Reports types of VOUT related faults.
7Bh	STATUS_IOUT	Read Byte	1				Reports types of IOUT related faults.
7Ch	STATUS_INPUT	Read Byte	1				Reports types of INPUT related faults.
7Dh	STATUS_TEMPERATURE	Read Byte	1				Returns Over Temperature warning and Over Temperature fault (OTP level). Does not report under temperature warning/fault. The bit meanings are: Bit <7> Over Temperature Fault Bit <6> Over Temperature Warning Bit <5> Under Temperature Warning Bit <4> Under Temperature Fault Bit <3:0> Reserved
7Eh	STATUS_CML	Read Byte	1				Returns 1 byte where the bit meanings are: Bit <7> Command not Supported Bit <6> Invalid data Bit <5> PEC fault Bit <4> OTP fault Bit <3:2> Reserved Bit<1> Other communication fault Bit<0> Other memory or logic fault; hardcoded to 0
88h	READ_VIN[11]	Read Word	2				Returns the input voltage in Volts
8Bh	READ_VOUT[16]	Read Word	2				Returns the output voltage in Volts
8Ch	READ_IOUT[11]	Read Word	2				Returns the output current in Amperes
8Dh	READ_TEMPERATURE[11]	Read Word	2				Returns the device temperature in degrees Celcius
96h	READ_POUT[11]	Read Word	2				Returns the output power in Watts
98h	PMBUS_REVISION	Read Byte	1				Reports PMBus Part I rev 1.1 & PMBus Part II rev 1.2(draft)
99h	MFR_ID	Block Read/Write	3			IR	Returns 2 bytes used to read the manufacturer's ID. User can overwrite with any value.
9Ah	MFR_MODEL	Block Read/Write	2			Set 00	If set to 00h, returns a 1 byte code corresponding to IC_DEVICE_ID. Alternatively, user can set to any non-zero value
9Bh	MFR_REVISION	Block Read/Write	2			Set 00	If set to 00h, returns a 1 byte code corresponding to IC_DEVICE_REV. Alternatively, user can set to any non-zero value
ADh	IC_DEVICE_ID	Block Read	2				Used to read the type or part number of an IC. IR38060: 30h IR38061:31h IR38060: 32h IR38060: 33h IR38064:34h IR38065:35h

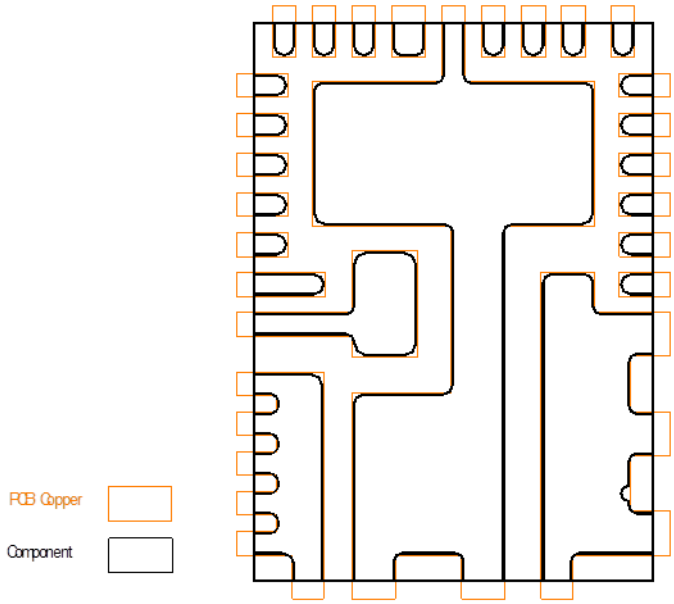
AEh	IC_DEVICE_REV	Block Read	2				Used to read the revision of the IC
D0h	MFR_READ_REG	Custom	2				Manufacturer Specific: Read from configuration registers
D1h	MFR_WRITE_REG	Custom	2				Manufacturer Specific: Write to configuration & status registers
D8h	MFR_TPGDLY	R/W Word	2	0-10ms	1ms	0ms	Sets the delay in ms, between the output voltage entering the regulation window and the assertion of the PGood signal. Exponent 0 allowed.
D9h	MFR_FCCM	R/W Byte	1	0-1		1 (CCM)	Allows the user to choose between forced continuous conduction mode and adaptive on-time operation at light load.
D6h	MFR_I2C_address	R/W Word	1	0-7Fh		10h	Sets and returns the device I2C base address
DBh	MFR_VOUT_PEAK[16]	Read Word	2				Continuously records and reports the highest value of Read Vout.
DCh	MFR_IOUT_PEAK[11]	Read Word	2				Continuously records and reports the highest value of Read Iout.
DDh	MFR_TEMPERATURE_PEAK[11]	Read Word	2				Continuously records and reports the highest value of Read_Temperature

Notes

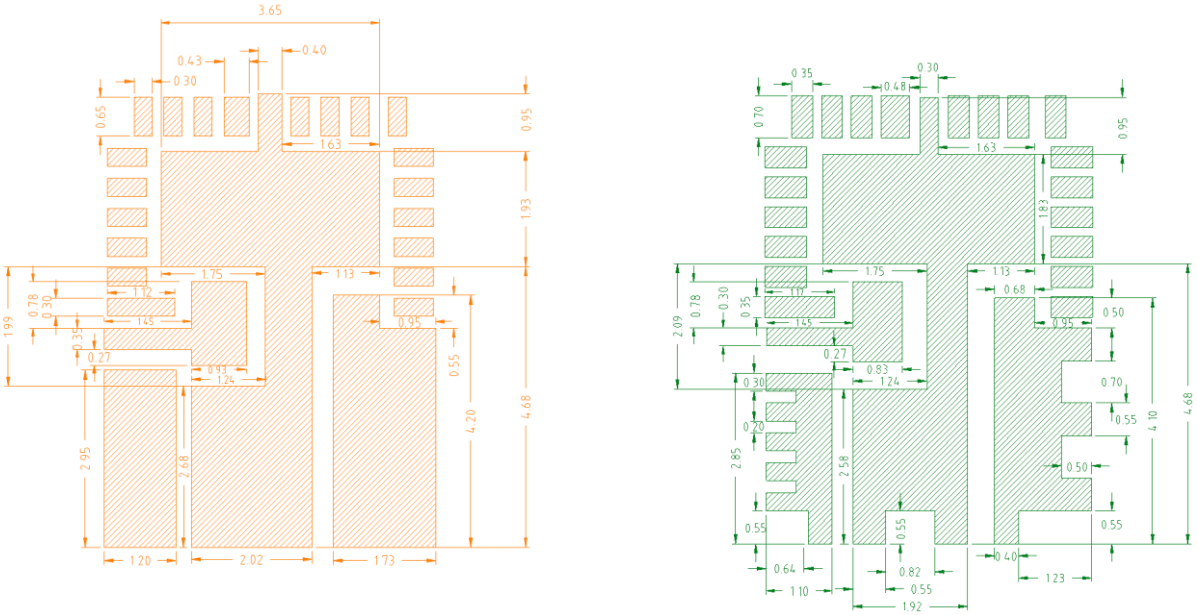
[11] Uses LINEAR11 format

[16] Uses LINEAR16 format with exponent set to -8

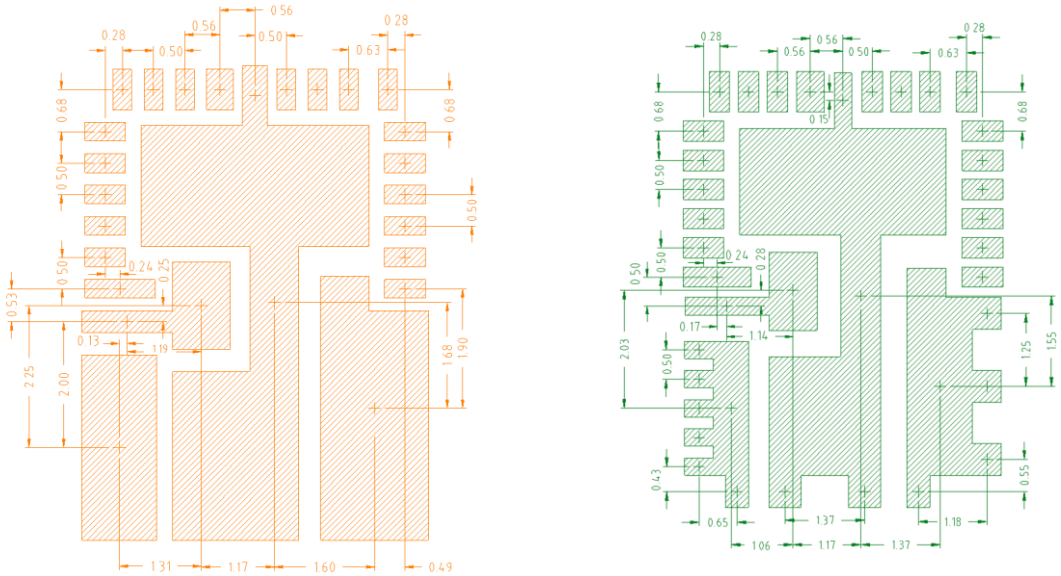
PCB PADS AND COMPONENT



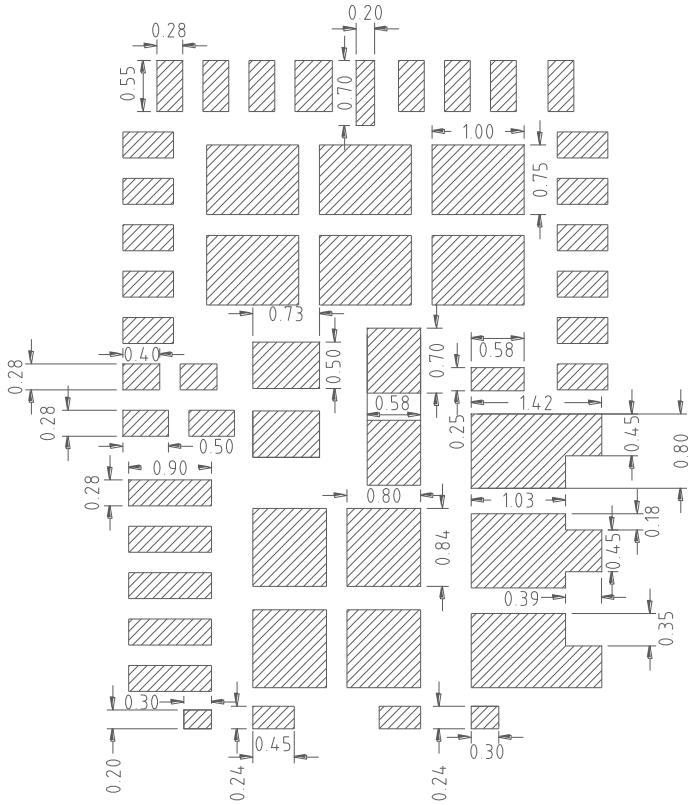
PCB COPPER AND SOLDER RESIST (PAD SIZES)



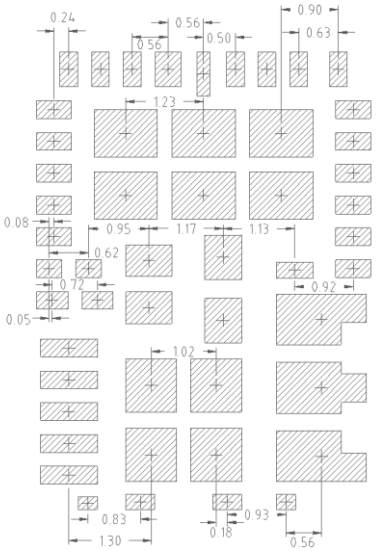
PCB COPPER AND SOLDER RESIST (PAD SPACING)

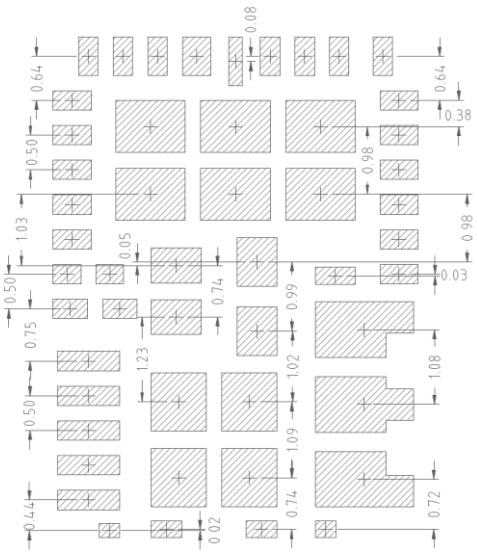


SOLDER PASTE STENCIL (PAD SIZES)

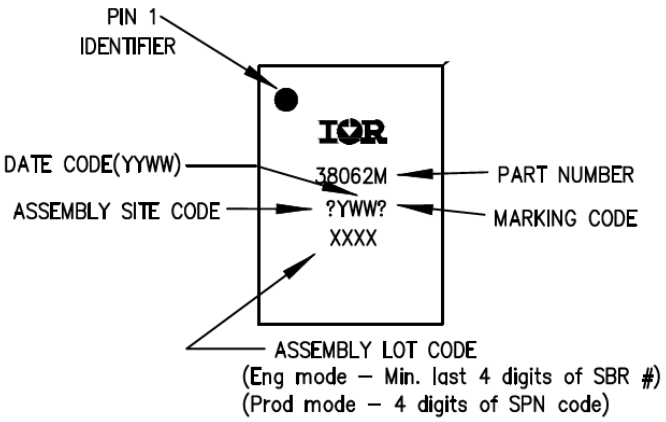


SOLDER PASTE STENCIL (PAD SPACING)



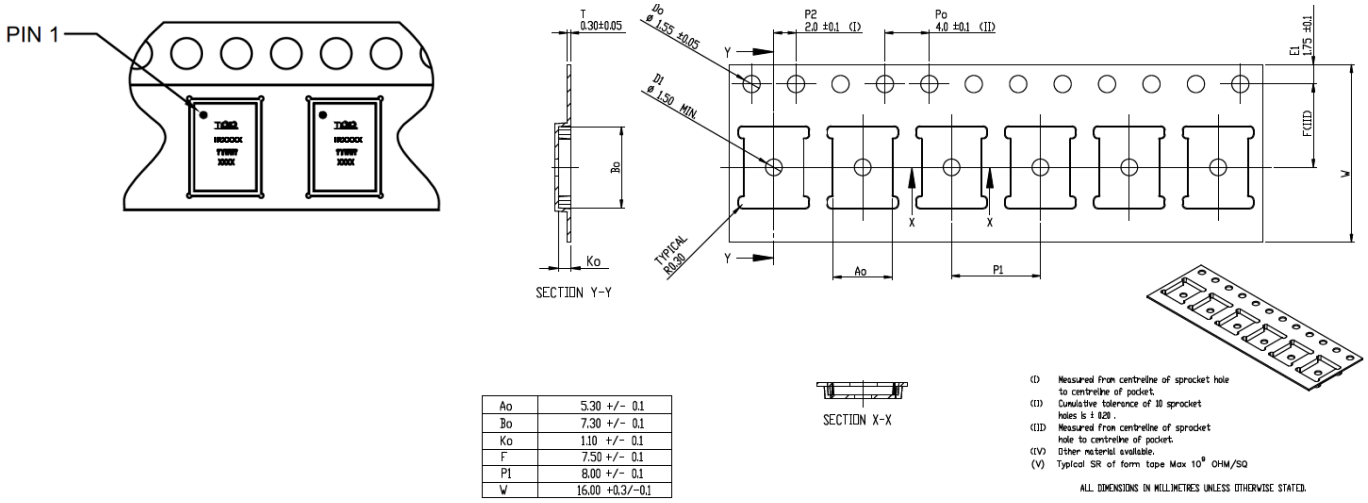


MARKING INFORMATION



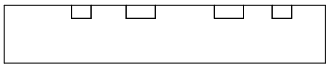
TAPE AND REEL INFORMATION

Refer to Application Note AN-1132 for more information.

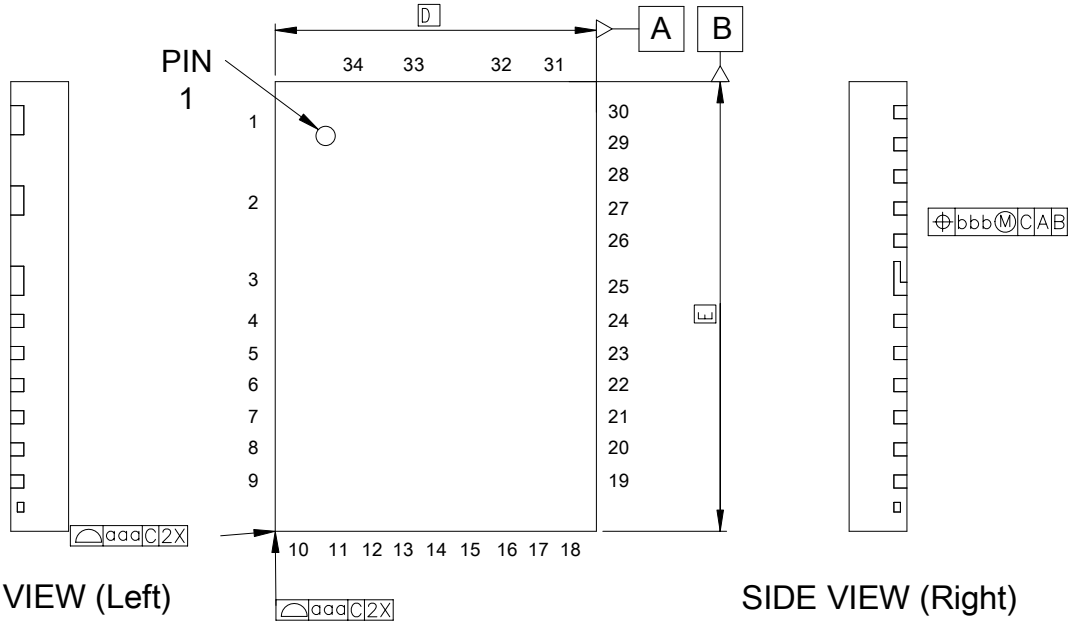


Ao	5.30 +/- 0.1
Bo	7.30 +/- 0.1
Ko	1.10 +/- 0.1
F	7.50 +/- 0.1
P1	8.00 +/- 0.1
W	16.00 +0.3/-0.1

PACKAGE INFORMATION



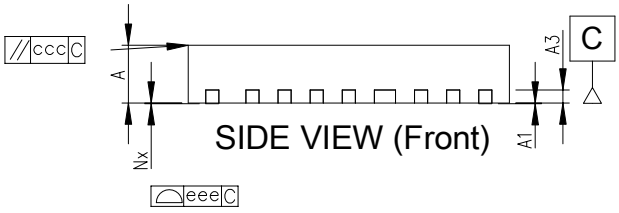
SIDE VIEW (Back)



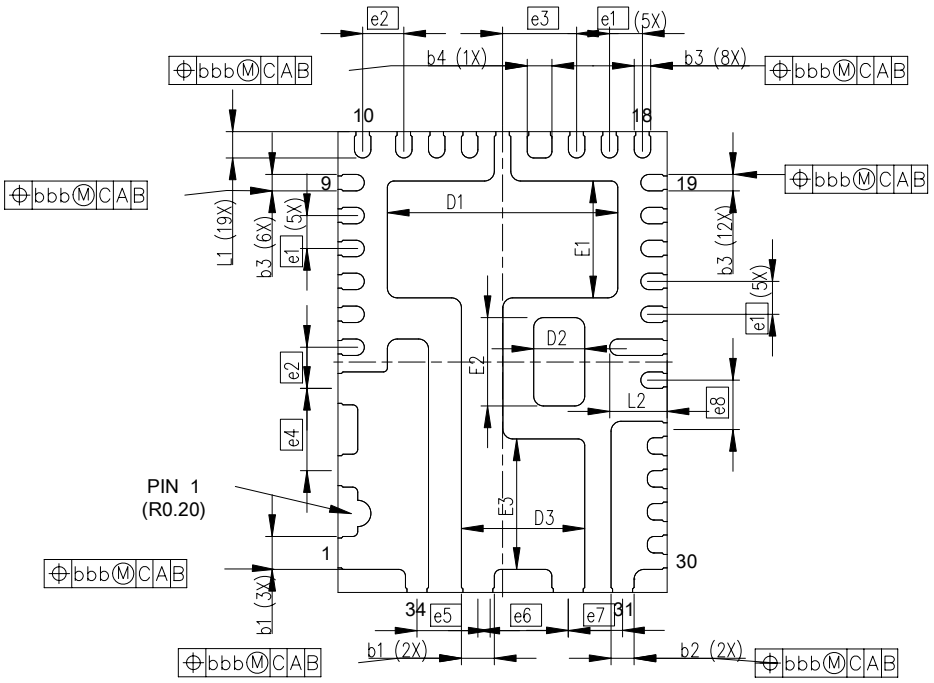
SIDE VIEW (Left)

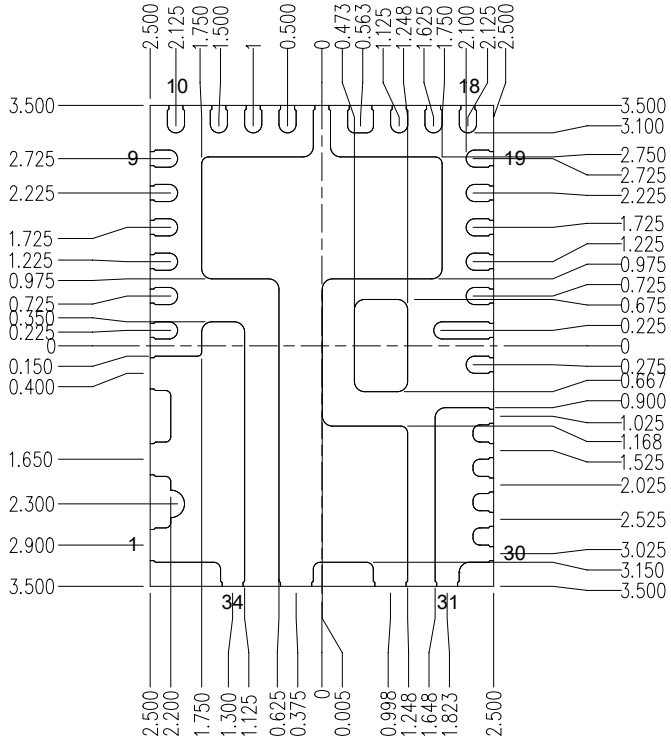
TOP VIEW

SIDE VIEW (Right)



SIDE VIEW (Front)





BOTTOM VIEW

DIMENSION TABLE			
SYMBOL	MINIMUM	NOMINAL	MAXIMUM
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.203 Ref	
b1	0.45	0.50	0.55
b2	0.30	0.35	0.40
b3	0.20	0.25	0.30
b4	0.325	0.375	0.425
D		5.00 BSC	
E		7.00 BSC	
D1	3.450	3.500	3.550
E1	1.725	1.775	1.825
D2	0.725	0.775	0.825
E2	1.292	1.342	1.392
D3	1.823	1.873	1.923
E3	1.932	1.982	2.032
L1	0.35	0.40	0.45
L2	0.822	0.872	0.922
e1		0.500 BSC	
e2		0.625 BSC	
e3		1.125 BSC	
e4		1.250 BSC	
e5		0.925 BSC	
e6		1.373 BSC	
e7		0.825 BSC	
e8		0.750 BSC	
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
N		34	

ENVIRONMENTAL QUALIFICATIONS

Qualification Level		Industrial	
Moisture Sensitivity Level		5mm x 7mm PQFN	MSL2
ESD	Machine Model (JESD22-A115A)	JEDEC Class B	
	Human Body Model (JESD22-A114F)	JEDEC Class 2 (2KV)	
	Charged Device Model (JESD22-C101D)	JEDEC Class 3	
RoHS Compliant		Yes (with Exemption 7a)	

† Qualification standards can be found at International Rectifier web site: http://www.irf.com

REVSION HISTORY

Rev.	Date	Description
3.0	9/9/2015	Initial Release
3.1	10/5/2015	Corrected OC test condition
3.2	10/17/2015	Added Recommended Vcc range 4.9V-5.3V Updated Frequency_Switch default to 607kHz (was 600kHz)
3.3	10/21/2015	Added reference to UN0060 PMBus commandset Corrected default Ton_Rise to 2ms (was 1ms)
3.4	11/06/2015	Added Reference accuracy over -40C→125C Updated package drawing to include L-shaped pin
3.5	1/15/2016	Improved assembly drawing quality Removed unnecessary info from Marking diagram Added Linear telemetry formats to PMBus command table Corrected Mfr_ID/Model/Rev and other descriptions in PMBus command table Clearly specified Vin/Vcc operating ranges Added Tape & Reel information Converted to Infineon format
3.6	2/4/2016	Added AC specification for Boot to SW, explicitly stated that no Rt resistor needed in digital mode, added ESD specifications, corrected a typo in Vin operating range to PVin operating range
3.7	3/4/2016	Corrected IOUT_OC_FAULT_LIMIT, IOUT_OC_FAULT_RESPONSE and IOUT_OC_WARN_LIMIT range and defaults in PMBus commandset table
3.8	5/26/2016	Changed recommended Vcc operating range, Corrected typo in caption for transient waveforms, changed Iout reporting resolution display format from 0.0625A to 62.5 mA

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