Discontinued Product

OKI Semiconductor

Version1.20, Jun.16, 1999

MSM9844

VOICE SYNTHESIS LSI with on-chip FIFO Memory

■ General Description

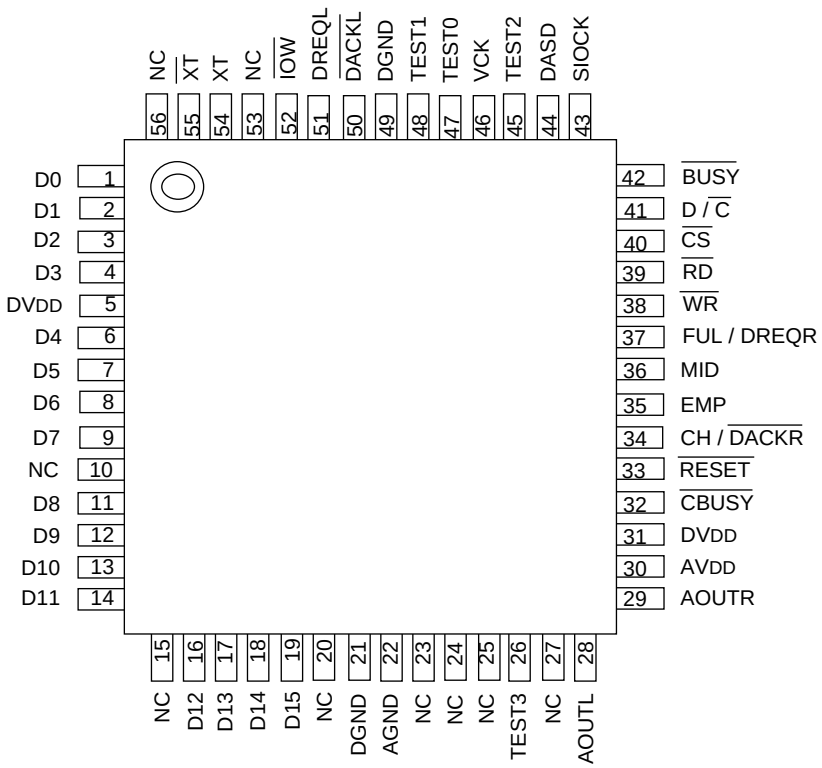
MSM9844 is a Voice Synthesizer LSI with on-chip FIFO memory.
A newly developed synthesis algorithm, OKI ADPCM2, promises superb sound quality. The LSI is fully controllable from an external CPU via 16/8-bit bus interface.
MSM9844 is an ideal choice for application systems where such non-microchip data storage as CD ROM is used..

■ Features

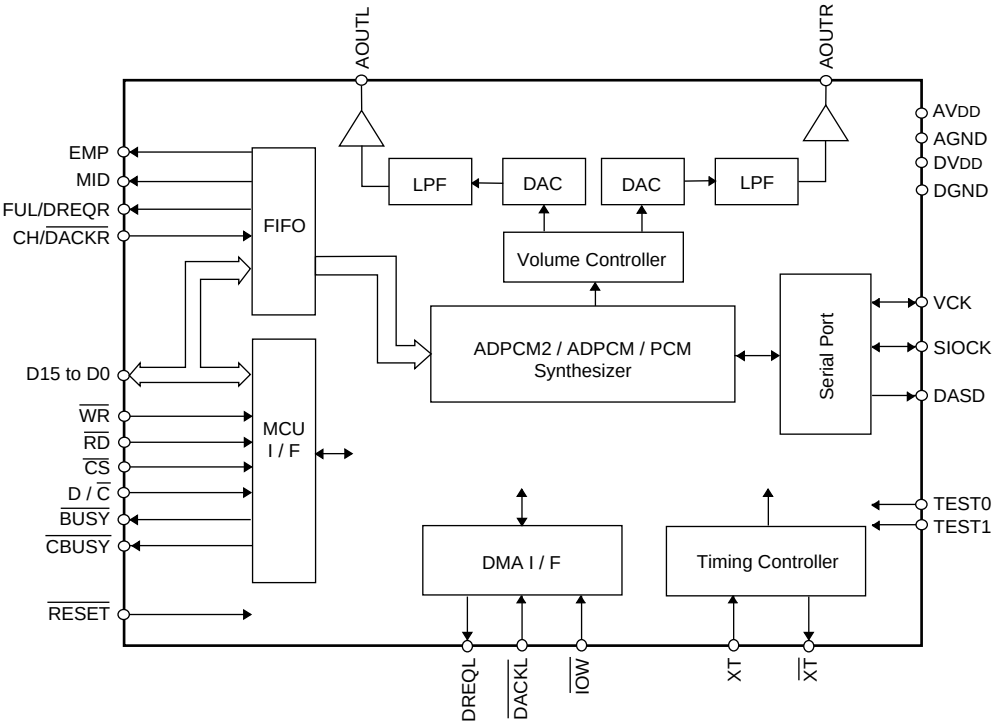
- 16/8-bit Bus Interface
- On-chip FIFO Memory Capacity : 1024 Bits 23 ms Buffering
  When Sampling Frequency at 8.0 kHz, 4-bit ADPCM and Monaural Playback selected
- Synthesis Algorithms for User's Selection
  4,5,6,7,8-bit OKI ADPCM2
  4-bit OKI ADPCM
  8/16-bit Straight PCM
  8-bit OKI Non-Linear PCM
- Oscillation Clock Frequency: 16.9344 MHz / 24.576 MHz
- Sampling Frequency:
  11.025 kHz, 22.05 kHz, 44.1 kHz at f_{OSC}=16.9344 MHz
  4.0 kHz, 6.4 kHz, 8.0 kHz, 12.8 kHz, 16.0 kHz, 32.0 kHz, 48.0 kHz at f_{OSC}=24.576 MHz
- Sound Level Control (8 levels, 0dB ~ -21dB)
- Built-in 14-bit D/A Converter
- 3 types of Serial Interface for External DAC
- Sampling Rate Conversion Function
- Packaging: 56-pin Plastic QFP (QFP56-P-910-0.65-2K)
  Product Code: MSM9844GA

■ Pin Layout (Top View)

56-pin Plastic QFP



■ Block Diagram



■ Pin Description

Pin No.	Symbol	I / O	Description
11 - 14 16 - 19	D15 to D8	I / O	When 8-bit bus interface selected, you can define, by using a command, these pins as input/output to/from external memory. When no definition made, these pins are output mode. When 16-bit bus interface selected, they are one half of bi-directional data bus for data input / output from/to external micro-controller and memory.
1 - 4 6 - 9	D7 to D0	I / O	Another half of bi-directional data bus for data input/output from/to external micro-controller and memory and for status output.
38	$\overline{WR}$	I	WRITE pulse input pin. Input "L" pulse before you can enter command and data to D15 to D0 pins.
39	$\overline{RD}$	I	READ pulse input pin. Input "L" pulse before the LSI can output status and data to D15 to D0 pins.
40	$\overline{CS}$	I	With this pin at "L" level, the LSI accepts WRITE or READ pulse input. At "H" level the LSI would not accept WRITE or READ pulse.
41	D / $\overline{C}$	I	While this pin being held "H", D15 to D0 pins are enabled to input/output sound data. While this pin being held "L", D7 to D0 pins are enabled to input a command or output status data.
42	$\overline{BUSY}$	O	Output "L" level during playback/PAUSE operation.
32	$\overline{CBUSY}$	O	Output "L" level when the LSI is ready to accept a command.
35	EMP	O	"H" level output from this pin indicates FIFO memory is empty. You can change this pin to "L" active by a command input.
36	MID	O	"H" level output from this pin indicates FIFO memory is more than half. During playback, voice synthesis starts when MID changes to "H" level. You can change this pin to "L" active by a command input. This pin outputs a synchro signal for voice data input / output when non-use of FIFO is selected.
37	FUL / DREQR	O	"H" level output from this pin indicates FIFO memory is full. During playback operation this pin is held "H" and FIFO memory is write -disabled. You can change this pin to "L" active by a command input. When DMA Transfer and stereo-playback selected by the command input, the output from this pin becomes DMA Transfer request signal. The pin outputs "H" when the right channel FIFO memory is empty. You can change this pin to "L" active by a command input.
34	CH / $\overline{DACKR}$	I	When stereo-playback selected, write sound data to the right channel FIFO at "H" level, while data to the left channel FIFO at "L" level. When monaural playback selected, keep this pin "L". You can change this pin to "L" active by a command input. When DMA Transfer and stereo-playback selected by the command input, this pin acknowledges the right channel DMA Transfer permission signal. With this pin at "L" level the LSI enabled the /IOW pin to accept the signal. You can change this pin to "H" active by a command input.
51	DREQL	O	Output "H" level to represent DMA Transfer request signal when FIFO gets empty. If stereo-playback selected, the pin outputs "H" level to represent DMA Transfer request signal when the left channel FIFO gets empty.
50	$\overline{DACKL}$	I	DMA Transfer Permission Acknowledgement signal. With this pin at "L" level the LSI enables the /IOW pin to accept the signal. When stereo-playback selected, the pin acknowledges DMA Transfer permission signal for the left channel FIFO. You can change this pin to "H" active by a command input. When DMA Transfer is not in use, keep the pin "H".

Pin No.	Symbol	I / O	Description
52	$\overline{IOW}$	I	When DMA Transfer selected, the signal to start writing external memory data to the MSM9844 is entered to this pin. When DMA Transfer is not use, keep the pin "H".
44	DASD	O	16-bit serial data output pin when the external DAC is in use.
43	SIOCK	I / O	Synchronizing clock signal for 16-bit serial data input/output when the external DAC is in use.
54 55	XT $\overline{XT}$	I O	Pins wired to the oscillator, When the external clock is used, input the clock signal to the XT pin and keep the /XT pin open.
46	VCK	I / O	Input/Output the sampling frequency in use. The signal is used as the synchronizing signal when the external DAC is in use.
33	$\overline{RESET}$	I	"L" level input to this pin turns the LSI to the initial status.
47,48 45,26	TEST0,1 TEST2,3	I	Pins for testing the LSI. Keep these pins "L".
28	AOUTL	O	The left channel output from the built-in LPF. Analog waveform output can be directly connected to an amplifirer to drive a speaker.
29	AOUTR	O	The right channel output from the built-in LPF. Analog waveform output can be directly connected to an amplifirer to drive a speaker.
31	DV_{DD}	—	Digital power supply pin. Insert a 0.1µF or larger bypass capacitor between this pin and the DGND pin.
21,49	DGND	—	Digital GND pin.
30	AV_{DD}	—	Analog power supply pin. Insert a 0.1µF or larger bypass capacitor between this pin and the AGND pin.
22	AGND	—	Analog GND pin.

■ Absolute Maximum Ratings

(GND = 0 V)

Parameter	Symbol	Conditions	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	- 0.3 to + 7.0	V
Input Voltage	V_{IN}		- 0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	——	- 55 to + 150	°C

■ Recommended Operating Ranges

(GND = 0 V)

Parameter	Symbol	Conditions	Rating	Unit
Power Supply Voltage	V_{DD}	DGND = AGND = 0V	+ 4.5 to + 5.5	V
Operating Temperature	T_{OP}	——	- 40 to + 85	°C
Master Clock Frequency	f_{OSC}	——	24.576	MHz

■ DC Characteristics

DV_{DD} = AV_{DD} = + 4.5 V to + 5.5 V
DGND = AGND = 0 V Ta = - 40 to + 85 °C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	——	V_{DD} x 0.85	——	——	V
"L" Input Voltage	V_{IL}	——	——	——	V_{DD} x 0.15	V
"H" Output Voltage note 1	V_{OH1}	I_{OH} = - 40 µA	V_{DD} - 0.3	——	——	V
"L" Output Voltage note 1	V_{OL1}	I_{OL} = 2 mA	——	——	0.45	V
"H" Output Voltage note 2	V_{OH2}	I_{OH} = - 40 µA	V_{DD} - 0.3	——	——	V
"L" Output Voltage note 2	V_{OL2}	I_{OL} = 2 mA	——	——	0.8	V
"H" Input Current note 3	I_{IH1}	V_{IH} = V_{DD}	——	——	10	µA
"H" Input Current note 4	I_{IH2}	V_{IH} = V_{DD}	——	——	20	µA
"L" Input Current note 5	I_{IL1}	V_{IL} = GND	- 10	——	——	µA
"L" Input Current note 4	I_{IL2}	V_{IL} = GND	- 20	——	——	µA
"L" Input Current note 6	I_{IL3}	V_{IL} = GND	- 400	——	- 20	µA
Operating Current Consumption	IDD	f_{OSC} = 24.576 MHz without load	——	——	40	mA
Standby Current Consumption	IDDS	At power down without load Ta = - 40 to + 70 °C	——	10	2 mA	µA
		At power down without load Ta = - 40 to + 85 °C	——	50	2 mA	µA

note 1) Applies to output pins excluding $\overline{XT}$ pin.
note 2) Applies to $\overline{XT}$ pin.
note 3) Applies to input pins excluding XT pin.
note 4) Applies to XT pins .
note 5) Applies to input pins without pull-up-register excluding XT pin.
note 6) Applies to input pins within pull-up-register excluding XT pin.

■ AC Characteristics

DVDD = AVDD = + 4.5 V to + 5.5 V
DGND = AGND = 0 V Ta = - 40 to + 85 °C

Parameter	Symbol	Min.	Typ.	Max.	Unit
$\overline{\text{RESET}}$ Pulse Width	tRSTW	300	——	——	ns
Setup Time after Rise of Power Supply for Fall of $\overline{\text{RESET}}$	tRSTD	500	——	——	ns
Time to Active First $\overline{\text{RD}}$, $\overline{\text{WR}}$ after Fall of $\overline{\text{RESET}}$	tRSTS	200	——	——	µs
$\overline{\text{RD}}$ Pulse Width	tRR	160	——	——	ns
CS, D/$\overline{\text{C}}$, CH Setup and Hold Time for $\overline{\text{RD}}$	tCR	30	——	——	ns
Time from Fall of $\overline{\text{RD}}$ till Data and Status Definition	tDRE	——	——	120	ns
Time from Fall of $\overline{\text{RD}}$ till Data Float	tDRF	——	10	50	ns
Time from Rise of $\overline{\text{RD}}$ till Fall of Next $\overline{\text{RD}}$	tCRC	500	——	——	ns
$\overline{\text{WR}}$ Pulse Width	tWW	160	——	——	ns
CS, D/$\overline{\text{C}}$, CH Setup and Hold Time for $\overline{\text{WR}}$	tCW	30	——	——	ns
Setup Time of Data, and Command for Rise of $\overline{\text{WR}}$	tDWS	100	——	——	ns
Hold Time of Data, and Command for Rise of $\overline{\text{WR}}$	tDWH	10	——	——	ns
Time from Rise of $\overline{\text{WR}}$ till Fall of Next $\overline{\text{WR}}$	tCWC	500	——	——	ns
$\overline{\text{IOW}}$ Pulse Width	tIOWW	160	——	——	ns
Setup and Hold Time of DACK for $\overline{\text{IOW}}$	tDW	10	——	——	ns
Setup Time of Data for Rise of $\overline{\text{IOW}}$	tIOWS	100	——	——	ns
Hold Time of Data for Rise of $\overline{\text{IOW}}$	tIOWH	10	——	——	ns
Time from Rise of $\overline{\text{IOW}}$ till Fall of Next $\overline{\text{IOW}}$	tIOWC	200	——	——	ns

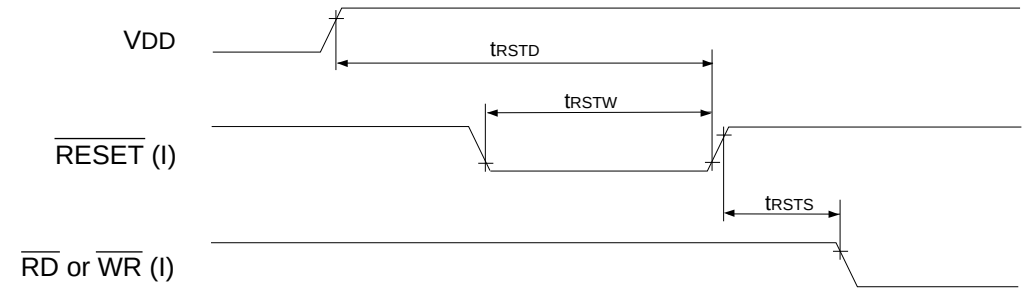
■ Analog Characteristics

DVDD = AVDD = + 4.5 V to + 5.5 V
DGND = AGND = 0 V Ta = - 40 to + 85 °C

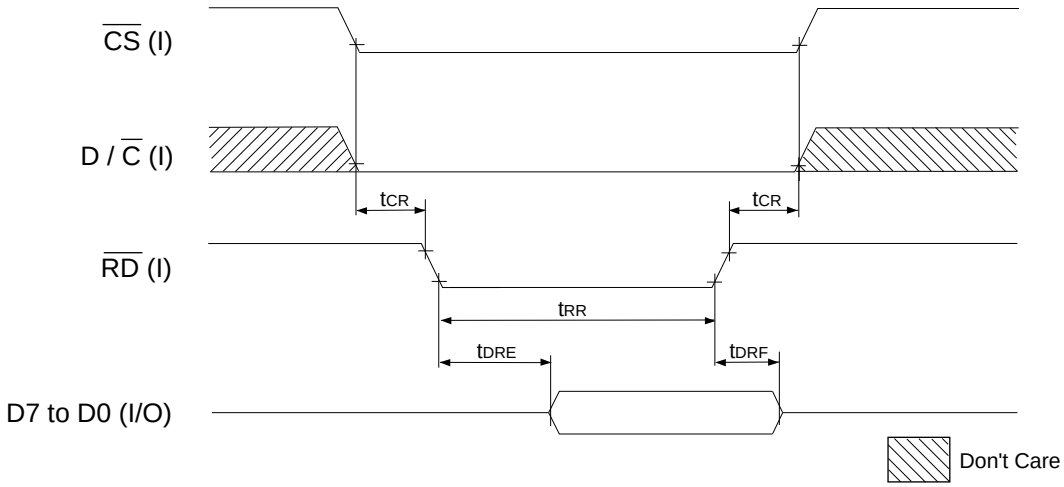
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
D/A Output Relative Error	$\lvert V_{DAE} \rvert$	No Load	——	——	10	mV
AOUT Output Load Resistance	R_{AOUT}	——	50	——	——	kΩ

■ Timing Chart

RESET Timing

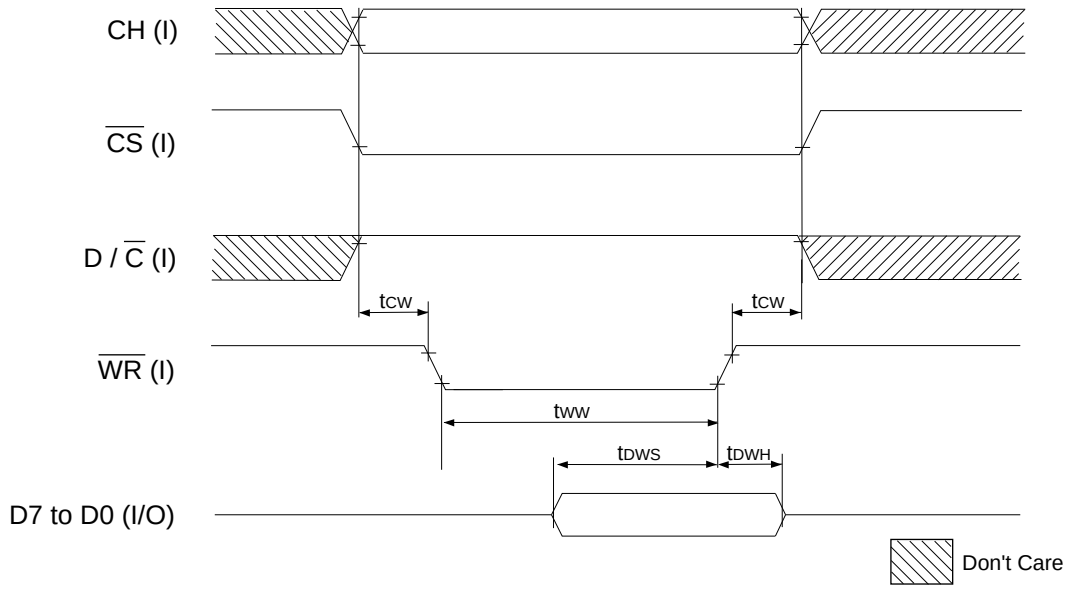


READ Timing Status READ

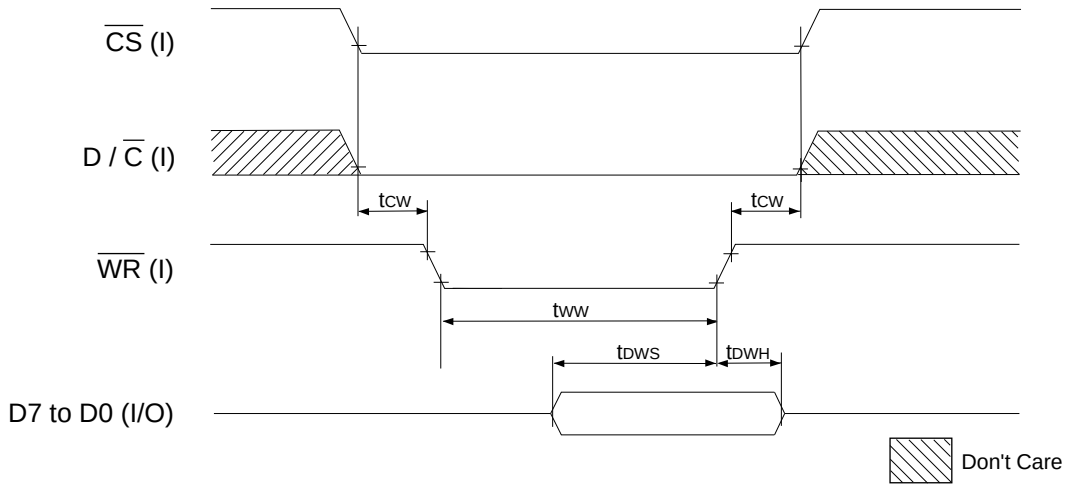


WRITE Timing

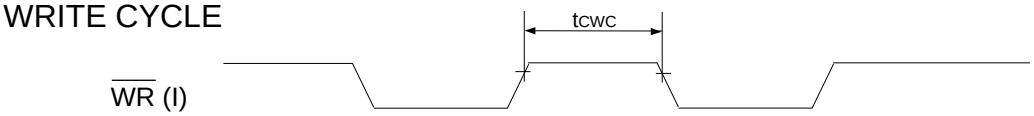
(1) DATA WRITE



(2) COMMAND WRITE

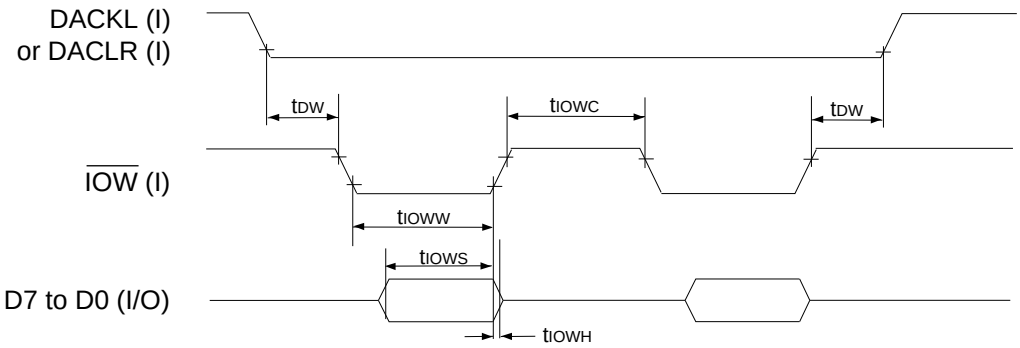


(3) WRITE CYCLE

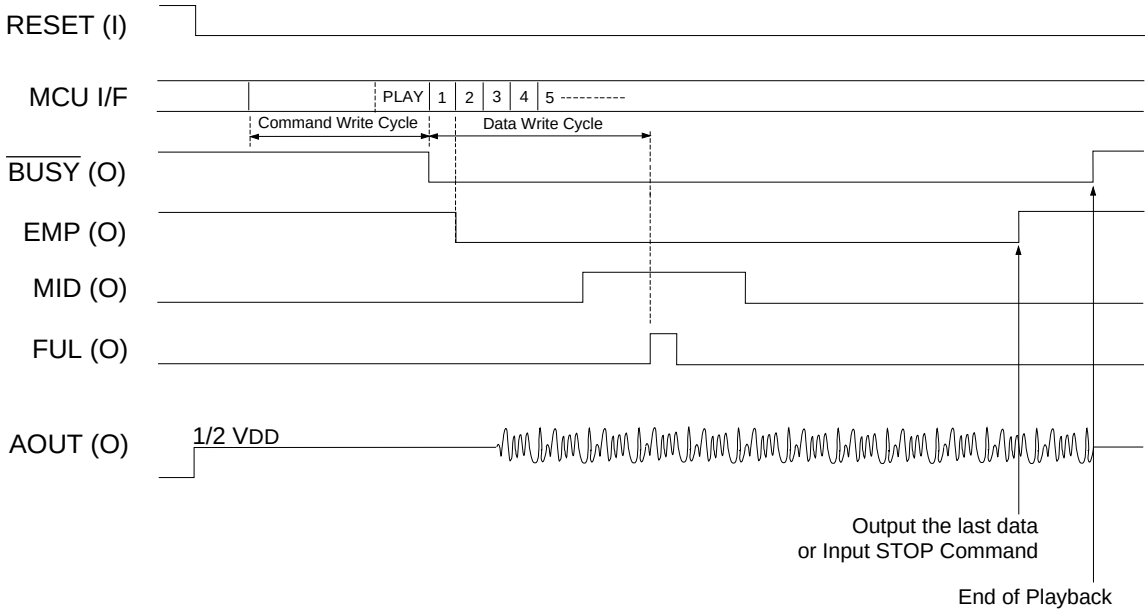


DMA Timing

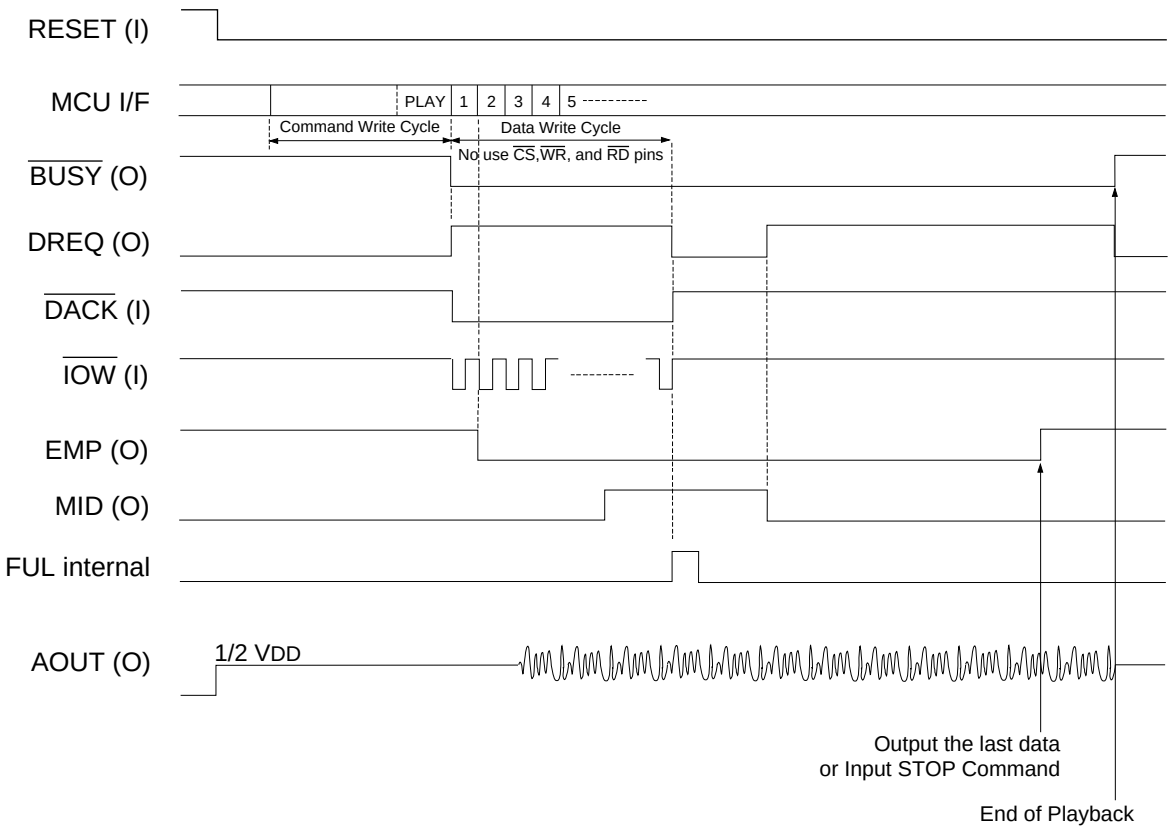
IOW Timing (for Playback and Write 2 bytes DATA)



Playback Timing with using External MCU and Memory



Playback Timing with using DMA Controller



■ Functional Description

• Voice Synthesis Algorithms

To meet user's varying sound quality requirements, 4 different types of voice synthesis algorithms are available for user's selection as follows:

1. OKI 4-bit ADPCM
2. OKI 4/5/6/7/8-bit ADPCM2
3. 8/16-bit Straight PCM
4. 8-bit Non-linear PCM

• Data Formats When 8-bit Bus Selected

1. Oki 4-bit ADPCM, Oki 4-bit ADPCM2

D7	D6	D5	D4	D3	D2	D1	D0
MSB1	3SB1	2SB1	LSB1	MSB2	3SB2	2SB2	LSB2
MSB3	3SB3	2SB3	LSB3	MSB4	3SB4	2SB4	LSB4

2. Oki 5-bit ADPCM2

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	MSB1	4SB1	3SB1	2SB1	LSB1
X	X	X	MSB2	4SB2	3SB2	2SB2	LSB2

3. Oki 6-bit ADPCM2

D7	D6	D5	D4	D3	D2	D1	D0
X	X	MSB1	5SB1	4SB1	3SB1	2SB1	LSB1
X	X	MSB2	5SB2	4SB2	3SB2	2SB2	LSB2

4. Oki 7-bit ADPCM2

D7	D6	D5	D4	D3	D2	D1	D0
X	MSB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1
X	MSB2	6SB2	5SB2	4SB2	3SB2	2SB2	LSB2

5. Oki 8-bit ADPCM2, 8-bit Linear PCM, and 8-bit Oki Non-Linear PCM

D7	D6	D5	D4	D3	D2	D1	D0
MSB1	7SB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1
MSB2	7SB2	6SB2	5SB2	4SB2	3SB2	2SB2	LSB2

6. 16-bit Linear PCM

D7	D6	D5	D4	D3	D2	D1	D0
MSB1	15SB1	14SB1	13SB1	12SB1	11SB1	10SB1	9SB1
8SB1	7SB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1

• Data Formats When 16-bit Bus Selected

1. Oki 4-bit ADPCM, Oki 4-bit ADPCM2

D15	D14	D13	D12	D11	D10	D9	D8
MSB1	3SB1	2SB1	LSB1	MSB2	3SB2	2SB2	LSB2
D7	D6	D5	D4	D3	D2	D1	D0
MSB3	3SB3	2SB3	LSB3	MSB4	3SB4	2SB4	LSB4

2. Oki 5-bit ADPCM2

D15	D14	D13	D12	D11	D10	D9	D8
X	X	X	MSB1	4SB1	3SB1	2SB1	LSB1
D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	MSB2	4SB2	3SB2	2SB2	LSB2

3. Oki 6-bit ADPCM2

D15	D14	D13	D12	D11	D10	D9	D8
X	X	MSB1	5SB1	4SB1	3SB1	2SB1	LSB1
D7	D6	D5	D4	D3	D2	D1	D0
X	X	MSB2	5SB2	4SB2	3SB2	2SB2	LSB2

4. Oki 7-bit ADPCM2

D15	D14	D13	D12	D11	D10	D9	D8
X	MSB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1
D7	D6	D5	D4	D3	D2	D1	D0
X	MSB2	6SB2	5SB2	4SB2	3SB2	2SB2	LSB2

5. Oki 8-bit ADPCM2, 8-bit Linear PCM, and 8-bit Oki Non-Linear PCM

D15	D14	D13	D12	D11	D10	D9	D8
MSB1	7SB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1
D7	D6	D5	D4	D3	D2	D1	D0
MSB2	7SB2	6SB2	5SB2	4SB2	3SB2	2SB2	LSB2

6. 16-bit Linear PCM

D15	D14	D13	D12	D11	D10	D9	D8
MSB1	15SB1	14SB1	13SB1	12SB1	11SB1	10SB1	9SB1
D7	D6	D5	D4	D3	D2	D1	D0
8SB1	7SB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1

• Playback Operation When Micro-controller Interface in Use

(1) Define a synthesis algorithm, sampling frequency, bus width, playback mode, and etc. as required, by using an appropriate command.

(2) To start playback, input the PLAY command. Or, write one word data to FIFO, letting the LSI ready for playback, and turn the EMP pin to "L" to initiate playback.

(3) Status shifting indicated by the EMP and FUL pins

(EMP="L", MID="L", FUL="L")

Indicates the state where no one-word data is written to FIFO memory.

(EMP="H", MID="L", FUL="L")

Indicates the state where one-word or more data is written to FIFO memory.

(EMP="L", MID="H", FUL="L")

Indicates the state where data is written to more than half of FIFO memory.

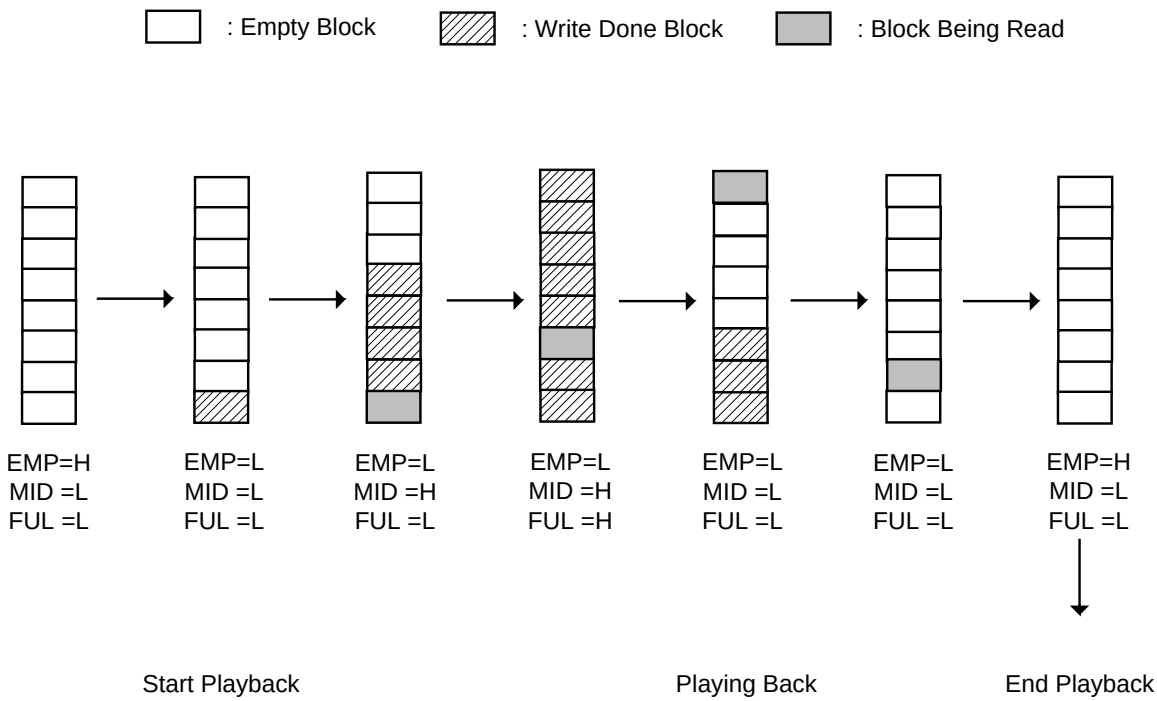
(EMP="L", MID="H", FUL="H")

Indicates the state where FIFO memory is full.

(4) Ending playback

When a write cycle is not completed within pre-fixed time, the LSI deems it as a completed write cycle and ends playback.

• FIFO Memory's Status Shift



•Playback Operation When DMA Interface in Use

MSM9844 issues a DMA Transfer request to the DMA Controller, and starts data transfer in sync with transfer cycles of the DMA Controller after acknowledging a DMA Transfer permission. Enable/Disable of DMA Transfer function can be defined by using the command.
The DREQL pin rises to "H" at the Start Playback command, requesting a write cycle to FIFO memory, and maintains "H" level until FIFO gets full.
At the point of time when one-word data is written to FIFO, playback starts. When FIFO becomes half, the DREQL returns to "H".

<DACKL Pin>
The pin is able to acknowledge a DMA Transfer permission signal from the DMA Controller. The /IOW pin is enabled with the /DACKL pin at "L".
During the period of /DACKL="L" , controls using the /RD, /WR, CS, D/C pins are disabled. Therefore, setups of MSM9844 has to be completed before you can enter into a DMA Transfer cycle.

</IOW Pin>
The pin is enabled at /DACKL="L", and thereafter controlled by the DMA Controller. The /IOW is an input pin to enable data transfer from external memory to the MSM9844.

•Pausing Playback

You can suspend on-going playback by using the Pause command. At this time, you may suspend Write operation to FIFO memory while in pause. Write is resumed from where having been paused, when playback restarts.
Or, you may continue Write operation to FIFO memory according to the EMP, MID and FUL pins' status.

•Stopping On-going Playback

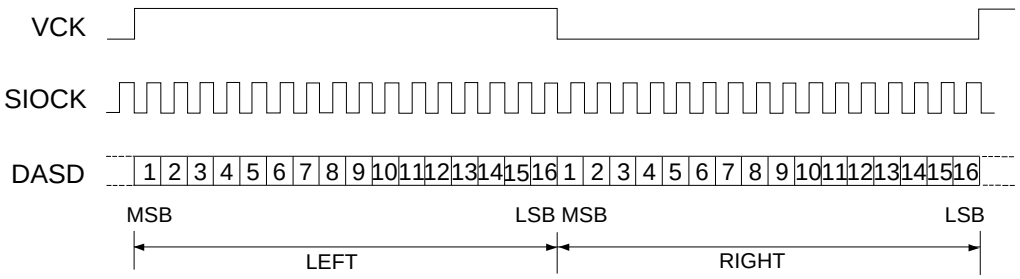
You can stop on-going playback by using the STOP command. When this happens, FIFO memory is cleared to return to the initial status.

•Serial Port Data Format

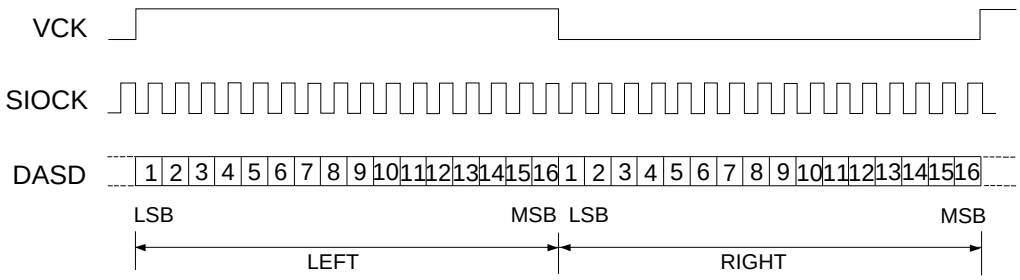
You can select one of the following three types of serial interface by using the command.

1. MSB First (Master/Slave)
2. LSB First (Master/Slave)
3. IIS Format (Master/Slave)

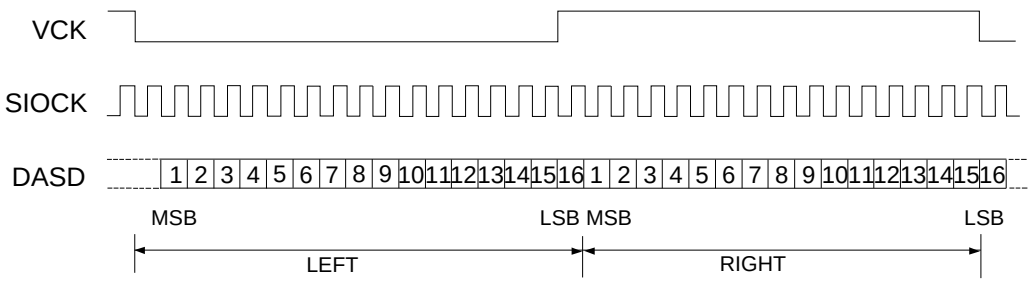
(1) MSB 16 bit (J1 = 0, J0 = 0)



(2) LSB 16 bit (J1 = 0, J0 = 1)



(3) MSB, VCK Inverted, and DASD Shifted 1 bit 16 bit (J1 = 1, J0 = 1)



• Sampling RATE Conversion

You can convert a sampling frequency for data output to another sampling frequency.
You can select an input sampling frequency with Sampling Rate Conversion Command and select SRC available.
The SRC function supports only to convert monaural 44.1 kHz sampling. Select 26H data with PLAY Command.
4.0, 6.4, 8.0, 12.8, 16.0kHz sampling frequencies are available to convert.
Master oscillation frequency is at 16.9344 MHz.

■ Command Code Format

D7	D6	D5	D4	D3	D2	D1	D0	Function
0	0	0	0	X	X	X	X	NOP
0	0	0	1	L3	L2	L1	L0	Sampling RATE Conversion
0	0	1	0	H3	S2	S1	S0	PLAY
0	0	1	1	C3	C2	X	X	STOP
0	1	0	0	C3	C2	C1	C0	PAUSE
0	1	0	1	H3	V2	V1	V0	VOLUME
0	1	1	0	W3	W2	X	X	POWER DOWN
0	1	1	1	P3	P2	P1	P0	SELECT ALGORITHM
1	0	0	0	R3	R2	R1	R0	ANALOG SETUP 1
1	0	0	1	A3	A2	E1	E0	ANALOG SETUP 2, BUS WIDTH
1	0	1	0	X	X	B1	B0	DEFINE FIFO SIZE
1	0	1	1	F3	D2	D1	D0	SIGNAL OUTPUT FORMAT
1	1	0	0	G2	G1	G0	X	SELECT DMA TRANSFER
1	1	0	1	I3	X	J1	J0	SELECT Serial Port FORMAT
1	1	1	0	X	X	X	X	NOP
1	1	1	1	T3	T2	T1	T0	TEST

X = Don't Care

1) NOP Command

D7	D6	D5	D4	D3	D2	D1	D0	Function
0	0	0	0	X	X	X	X	NOP
1	1	1	0	X	X	X	X	NOP

No particular function

2) Sampling RATE Conversion Command

D7	D6	D5	D4	D3	D2	D1	D0	Function
0	0	0	1	L3	L2	L1	L0	Sampling RATE Conversion

By using this command you can select enable / disable Sampling Rate Conversion and input sampling frequency when enable this function. Note that this command is enable with monaural playback.

L3	Function
0	NOT used Sampling Rate Conversion *
1	Used Sampling Rate Conversion

* Default

L2	L1	L0	Sampling Frequency
0	0	0	16.0 kHz
0	0	1	————
0	1	0	4.0 kHz
0	1	1	8.0 kHz
1	0	0	6.4 kHz
1	0	1	12.8 kHz
1	1	0	————
1	1	1	————

3) PLAY Command

D7	D6	D5	D4	D3	D2	D1	D0	Function
0	0	1	0	C3	S2	S1	S0	PLAY

To start playback, use this command. You can select either the left or right channel playback with C3, as well as sampling frequency with S2 ~ S0. When stereo-playback is selected, data at C3 is disregarded. You can select only one sampling frequency.
When the rate converter is used, the frequency defined by S2 ~ S0 is output sampling frequency.

C3	Function
0	PLAY LEFT *
1	PLAY RIGHT

* Default

S2	S1	S0	Sampling Frequency	
			XT = 16.9344MHz	XT = 24.576MHz
0	0	0	11.025 kHz *	16.0 kHz *
0	0	1	22.05 kHz	32.0 kHz
0	1	0	2.76 kHz	4.0 kHz
0	1	1	5.51 kHz	8.0 kHz
1	0	0	4.41 kHz	6.4 kHz
1	0	1	8.82 kHz	12.8kHz
1	1	0	44.1 kHz	———
1	1	1	———	48.0 kHz

* Default

4) STOP Command

D7	D6	D5	D4	D3	D2	D1	D0	Function
0	0	1	1	C3	C2	X	X	STOP

Use this command to stop playback. After the command input, FIFO data is cleared. C3 allows you to select the left channel or the right channel playback to be stopped. When you want to stop playback on both channels, use C2.

C3	C2	Function
0	0	STOP LEFT *
1	0	STOP RIGHT
X	1	STOP LEFT and RIGHT

* Default

5) PAUSE Command

D7	D6	D5	D4	D3	D2	D1	D0	Function
0	1	0	0	C3	C2	C1	X	PAUSE

Use this command to temporarily suspend on-going playback. C1 enables you to control PAUSE/reset. You can select either the left channel or right channel with C3. When you want to suspend playback on both channels, use C2.

C3	C2	Function
0	0	PAUSE LEFT *
1	0	PAUSE RIGHT
X	1	PAUSE LEFT and RIGHT

* Default

C1	Function
0	PAUSE
1	RESUME

6) VOLUME Command

D7	D6	D5	D4	D3	D2	D1	D0	Function
0	1	0	1	C3	V2	V1	V0	VOLUME

You can control sound level of playback by using this command. C3 is to select either the left channel or right channel, and V2 ~ V0 is to select a proper sound level.

C3	Function
0	LEFT VOLUME CONTROLL
1	RIGHT VOLUME CONTROLL

V2	V1	V0	VOL.VALUE
0	0	0	0 dB *
0	0	1	- 3 dB
0	1	0	- 6 dB
0	1	1	- 9 dB
1	0	0	- 12 dB
1	0	1	- 15 dB
1	1	0	- 18 dB
1	1	1	- 21 dB

* Default

7) POWER DOWN Command

D7	D6	D5	D4	D3	D2	D1	D0	Function
0	1	1	0	W3	W2	X	X	POWER DOWN

Inputting this command puts the LSI into power down status, where the LSI stops oscillation and minimize power consumption. Output from the AOUTL and AOUTR dropped down to the GND level instantaneously. W3 enables you to control power down/reset and W2 to define whether initialize the LSI or not.

W3	Function
0	RESUME POWER DOWN
1	POWER DOWN

W2	Function
0	NOT initialize the LSI
1	Initialize the LSI

8) Select Algorithm Command

D7	D6	D5	D4	D3	D2	D1	D0	Function
0	1	1	1	P3	P2	P1	P0	SELECT ALGORITHM

You can select a voice synthesis algorithm with this command. You can select one out of ten listed below with P3 ~ P0.
You cannot change the algorithm during playback operation.

P3	P2	P1	P0	Algorithm
0	0	0	0	———
0	0	0	1	4bit ADPCM2 *
0	0	1	0	5bit ADPCM2
0	0	1	1	6bit ADPCM2
0	1	0	0	7bit ADPCM2
0	1	0	1	8bit ADPCM2
0	1	1	0	4bit ADPCM
0	1	1	1	8bit Linear PCM
1	0	0	0	8bit Non-Linear PCM
1	0	0	1	16bit Linear PCM

* Default

9) Analog Setup 1 Command

D7	D6	D5	D4	D3	D2	D1	D0	Function
1	0	0	0	R3	R2	R1	R0	ANALOG SETUP 1

This command allows you to select either internal/external DAC to be used, binary or two's compliment and stereo or monaural for playback.
At powering up, output from the AOUTL and AOUTR pins rises to 1/2 VDD level instantaneously, disregarding the setup value at R0.

R3	Function
0	2's Complimentary Binary *
1	Binary

R2	Function
0	INTERNAL D/A C *
1	EXTERNAL D/A C

R1	Function
X	No particular function

R0	Function
0	Monaural PLAYBACK *
1	Stereo PLAYBACK

* Default

10) Analog Setup 2 Command

D7	D6	D5	D4	D3	D2	D1	D0	Function
1	0	0	1	A3	A2	E1	E0	ANALOG SETUP 2

You can select enable/disable driving amplifier and enable/ disable LPF for the AOUTL and AOUTR pins with A3 and A2.
You can also select a data bus width with E1 and E0, and when 8-bit bus selected, you can further select whether to use D15 ~ D8 pins for sound data transfer.

A3	Function
0	USED Output Amplifire *
1	NOT USED Output Amplifire

A2	Function
0	USED internal LPF *
1	NOT USED intrenal LPF

E1	E0	Function
0	0	8bit BUS Width, D15 to D8 unused *
0	1	8bit BUS Width, D15 to D8 used
1	X	16bit BUS Width

* Default

11) Define FIFO Size Command

D7	D6	D5	D4	D3	D2	D1	D0	Function
1	0	1	0	X	X	B1	B0	DEFINE FIFO SIZE

By using this command you can define the size of FIFO memory.

B1	B0	8bit BUS Width	16bit BUS Width
0	0	128 bytes	64 words
0	1	64 bytes	32 words
1	0	32 bytes	16 words
1	1	NOT USED FIFO Memory	

12) Signal Output Format Command

D7	D6	D5	D4	D3	D2	D1	D0	Function
1	0	1	1	F3	D2	D1	D0	SIGNAL OUTPUT FORMAT

By using this command you can select output format from the EMP, FUL and DREQL/R pins, and input format to the DACKL/R pins.

F3	Function
0	"H" Active for EMP, MID, and FUL Output *
1	"L" Active for EMP, MID, and FUL Output

D2	Function
0	"H" Active for DREQL, and DREQR Output *
1	"L" Active for DREQL, and DREQR Output

D1	Function
0	"L" Active for DACKL, and DACKR Input *
1	"H" Active for DACKL, and DACKR Input

D0	Function
0	No particular function
1	NOT USED

* Default

13) Select DMA Transfer Command

D7	D6	D5	D4	D3	D2	D1	D0	Function
1	1	0	0	G3	G2	G1	X	SELECT DMA TRANSFER

By using this command you can select enable/disable DMA Transfer and DMA Transfer mode.

G3	G2	G1	Function
0	X	X	Not used DMA Transfer *
1	0	0	DMA Transfer by Single Mode
1	0	1	DMA Transfer by Block Mode

* Default

14) Select Serial Port Data Format Command

D7	D6	D5	D4	D3	D2	D1	D0	Function
1	1	0	1	I3	X	J1	J0	SELECT PORT DATA FORMAT

By using this command you can select a data format for the Serial Port.
Note that this command is valid only when R2 value of the Analog Setup 1 command is set to “1”

I3	Function
0	VCK, SIOCK Master Mode *
1	VCK, SIOCK Slave Mode

J1	J0	Function
0	0	MSB First, 16 bit(Mode 1) *
0	1	LSB First
1	0	————
1	1	I IS FORMAT, 16bit(Mode2)

* Default

15) Test Command

D7	D6	D5	D4	D3	D2	D1	D0	Function
1	1	1	1	T3	T2	T1	T0	TEST

This command is used only for testing the LSI. You are not allowed to use the command.

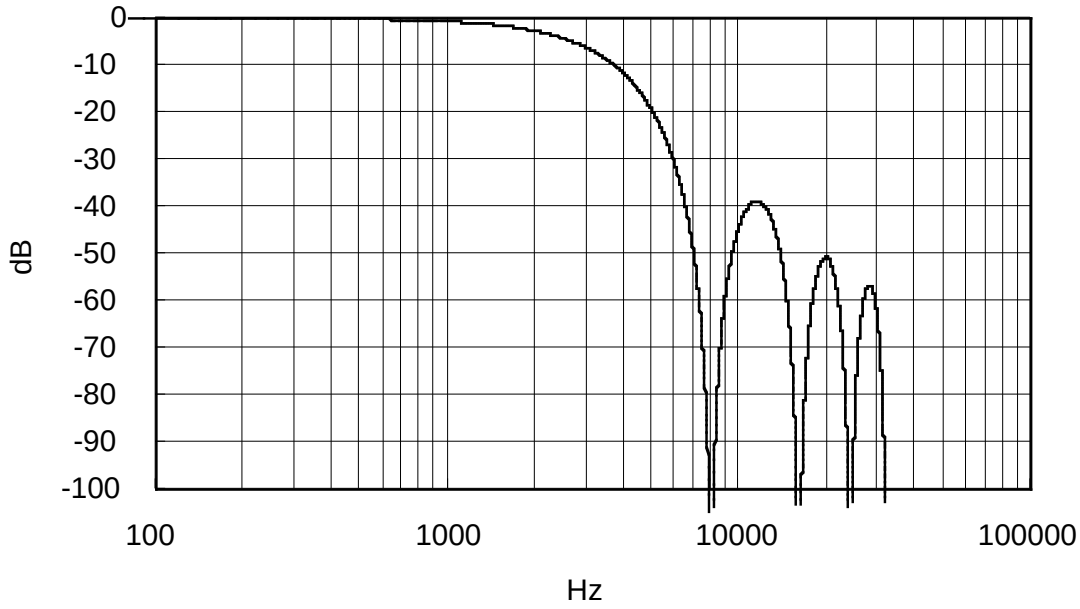
16) Status Read

You can monitor the MSM9844 internal status with read-out data from D7 to D0.
The table shows the each status from D7 to D0.

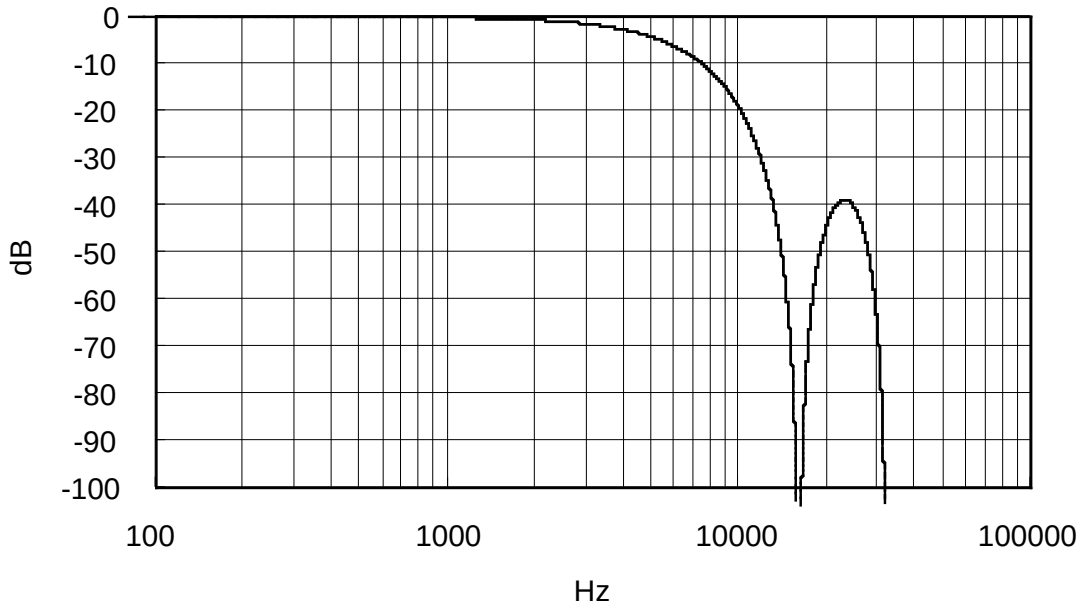
Pin Name	Status
D7	During Playback Lch
D6	During Playback Rch
D5	Pausing Lch
D4	Pausing Rch
D3	FIFO EMP Signal
D2	FIFO MID Signal
D1	FIFO FUL Signal
D0	Data is writen to FIFO at FUL status

• The Internal LPF Characteristics for AOUTL and AOUTR pins

There are two LPFs on MSM9844, which is consisted of Digital Filter Technology.
Figure shows each Frequency Characteristics of internal LPFs when the sampling frequency is at 8kHz and 16kHz.



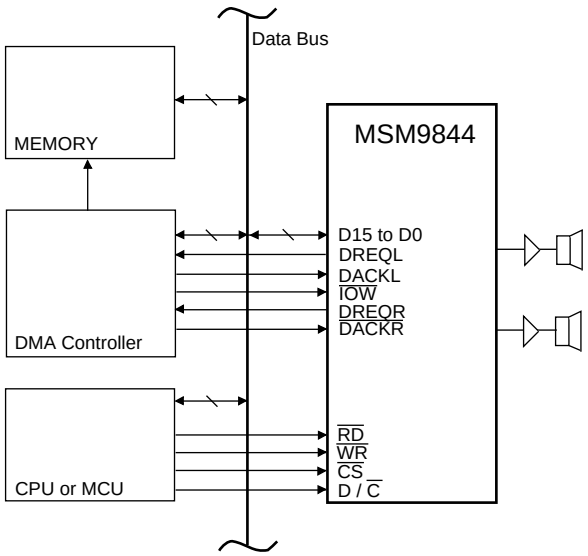
Frequency Characteristics of internal LPF at 8kHz sampling Frequency.



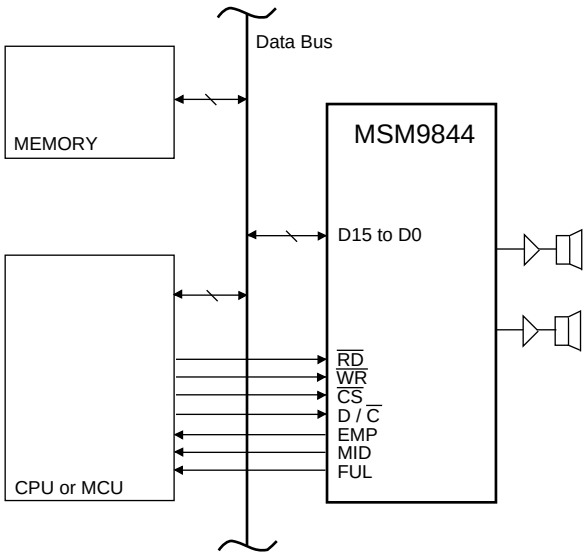
Frequency Characteristics of internal LPF at 16kHz sampling Frequency.

■ Application Circuit Sample

Sample 1 for interface with DMA Controller



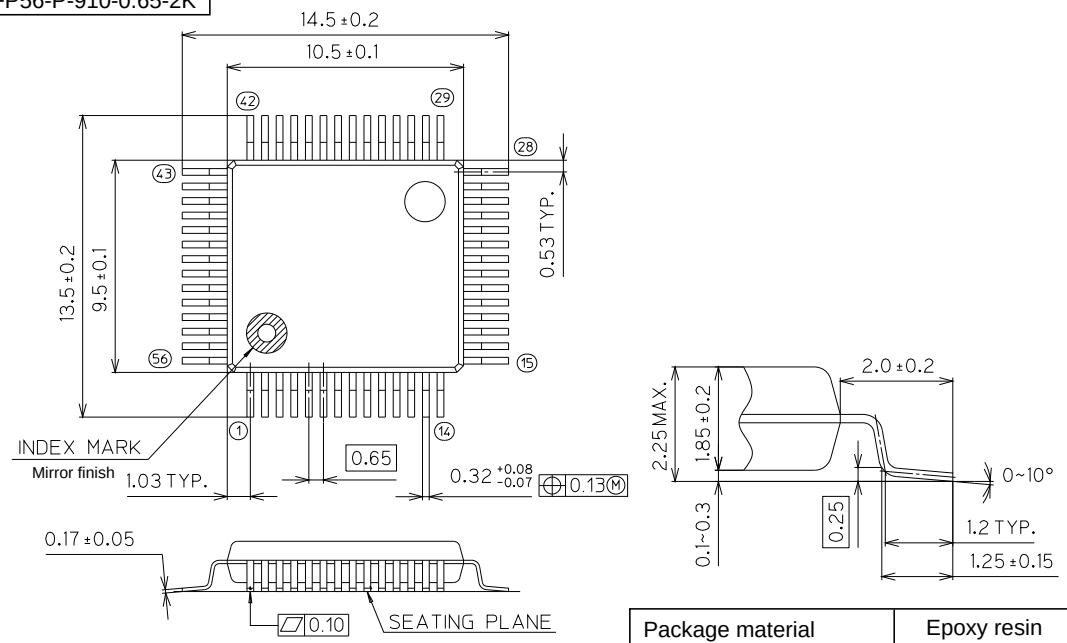
Sample 2 for interface with External Memory



■Package Dimensions

(Unit : mm)

QFP56-P-910-0.65-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5µm or more
Package weight (g)	0.43 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code, and desired mounting conditions (reflow method, temperature and times).

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