Dual 500mA/50MHz Current Feedback Line Driver Amplifier

FEATURES

- **500mA Output Drive Current**
- **50MHz Bandwidth, A_V = 2, R_L = 25Ω**
- **900V/µs Slew Rate, A_V = 2, R_L = 25Ω**
- **Low Distortion: –75dBc at 1MHz**
- High Input Impedance, 10MΩ
- Wide Supply Range, ±5V to ±15V
- Full Rate, Downstream ADSL Supported
- Low Power Shutdown Mode
- Power Saving Adjustable Supply Current
- Stable with C_L = 10,000pF
- Power Enhanced Small Footprint Packages TSSOP-20, S0-20 Wide
- Available in a 20-Lead TSSOP Package

APPLICATIONS

- ADSL HDSL2, G.lite Drivers
- Buffers
- Test Equipment Amplifiers
- Video Amplifiers
- Cable Drivers

DESCRIPTION

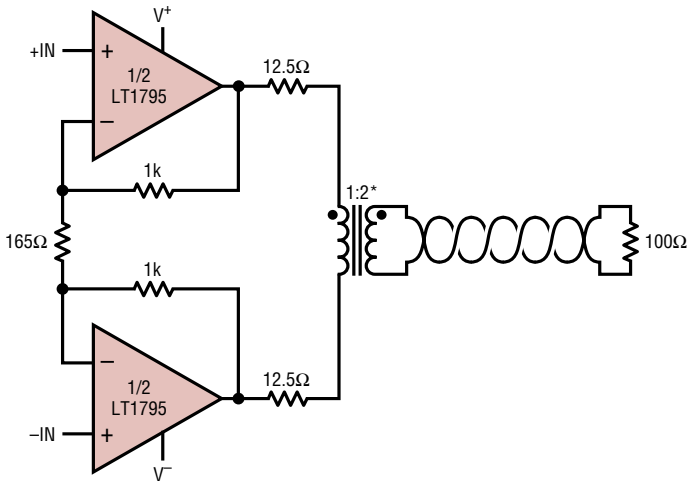
The LT®1795 is a dual current feedback amplifier with high output current and excellent large signal characteristics. The combination of high slew rate, 500mA output drive and up to ±15V operation enables the device to deliver significant power at frequencies in the 1MHz to 2MHz range. Short-circuit protection and thermal shutdown insure the device's ruggedness. The LT1795 is stable with large capacitive loads and can easily supply the large currents required by the capacitive loading. A shutdown feature switches the device into a high impedance, low current mode, reducing power dissipation when the device is not in use. For lower bandwidth applications, the supply current can be reduced with a single external resistor.

The LT1795 comes in the very small, thermally enhanced, 20-lead TSSOP package for maximum port density in line driver applications.

LT, LTC and LT are registered trademarks of Linear Technology Corporation.

TYPICAL APPLICATION

Low Loss, High Power Central Office ADSL Line Driver



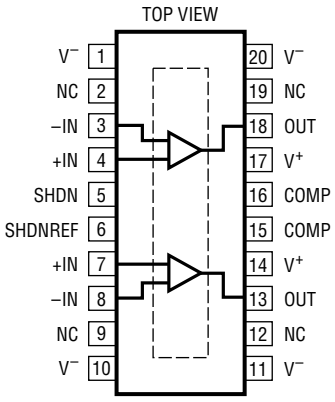
* MIDCOM 50215 OR EQUIVALENT

1795 TA01

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Input Current ..... ±15mA
Output Short-Circuit Duration (Note 2) ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range (Note 3) ... –40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

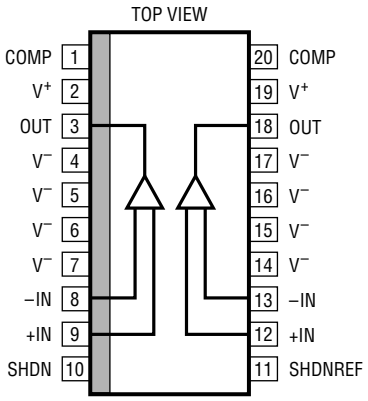


FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 150° C, θ_{JA} = 40°C/W (Note 4)

UNDERSIDE METAL INTERNALLY CONNECTED TO V^-
(PCB CONNECTION OPTIONAL)

ORDER PART NUMBER
LT1795CFE LT1795IFE



S PACKAGE
20-LEAD PLASTIC SW

T_{JMAX} = 150° C, θ_{JA} ≈ 40°C/W (Note 4)

ORDER PART NUMBER
LT1795CSW LT1795ISW

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. V_{CM} = 0V, ±5V ≤ V_S ≤ ±15V, pulse tested, V_{SHDN} = 2.5V, $V_{SHDNREF}$ = 0V unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage				±3	±13	mV
			●		±4.5	±17	mV
	Input Offset Voltage Matching				±1	±3.5	mV
			●		±1.5	±5.0	mV
	Input Offset Voltage Drift		●		10		µV/°C
I_{IN}^+	Noninverting Input Current				±2	±5	µA
			●		±8	±20	µA
	Noninverting Input Current Matching				±0.5	±2	µA
			●		±1.5	±7	µA
I_{IN}^-	Inverting Input Current				±10	±70	µA
			●		±20	±100	µA
	Inverting Input Current Matching				±10	±30	µA
			●		±20	±50	µA
e_n	Input Noise Voltage Density	f = 10kHz, R_F =1k, R_G = 10Ω, R_S = 0Ω			3.6		nV/√Hz
$+i_n$	Input Noise Current Density	f = 10kHz, R_F =1k, R_G = 10Ω, R_S = 10kΩ			2		pA/√Hz
$–i_n$	Input Noise Current Density	f = 10kHz, R_F =1k, R_G = 10Ω, R_S = 10kΩ			30		pA/√Hz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. V_{CM} = 0V, ±5V ≤ V_S ≤ ±15V, pulse tested, V_{SHDN} = 2.5V, $V_{SHDNREF}$ = 0V unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
R_{IN}^+	Input Resistance	V_{IN} = ±12V, V_S = ±15V V = ±2V, V_S = ±5V	● ●	1.5 0.5	10 5		MΩ MΩ
C_{IN}^+	Input Capacitance	V_{IN} = ±15V			2		pF
	Input Voltage Range (Note 5)	V_S = ±15V V_S = ±5V	● ●	±12 ±2	±13.5 ±3.5		V V
CMRR	Common Mode Rejection Ratio	V_S = ±15V, V_{CM} = ±12V V_S = ±5V, V_{CM} = ±2V	● ●	55 50	62 60		dB dB
	Inverting Input Current Common Mode Rejection	V_S = ±15V, V_{CM} = ±12V V_S = ±5V, V_{CM} = ±2V	● ●		1 1	10 10	µA/V µA/V
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	●	60	77		dB
	Noninverting Input Current Power Supply Rejection	V_S = ±5V to ±15V	●		30	500	nA/V
	Inverting Input Current Power Supply Rejection	V_S = ±5V to ±15V	●		1	5	µA/V
A_V	Large-Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, R_L = 25Ω V_S = ±5V, V_{OUT} = ±2V, R_L = 12Ω	● ●	55 55	68 68		dB dB
R_{OL}	Transresistance, $\Delta V_{OUT}/\Delta I_{IN}^-$	V_S = ±15V, V_{OUT} = ±10V, R_L = 25Ω V_S = ±5V, V_{OUT} = ±2V, R_L = 12Ω	● ●	75 75	200 200		kΩ kΩ
V_{OUT}	Maximum Output Voltage Swing	V_S = ±15V, R_L = 25Ω	 ●	±11.5 ±10.0	±12.5 ±11.5		V V
		V_S = ±5V, R_L = 12Ω	 ●	±2.5 ±2.0	±3 ±3		V V
I_{OUT}	Maximum Output Current	V_S = ±15V, R_L = 1Ω	●	0.5	1		A
I_S	Supply Current Per Amplifier	V_S = ±15V, V_{SHDN} = 2.5V	 ●		29	34 42	mA mA
	Supply Current Per Amplifier, R_{SHDN} = 51k, (Note 6)	V_S = ±15V	 ●		15	20 25	mA mA
	Positive Supply Current, Shutdown	V_S = ±15V, V_{SHDN} = 0.4V	●		1	200	µA
	Output Leakage Current, Shutdown	V_S = ±15V, V_{SHDN} = 0.4V			1	200	µA
	Channel Separation	V_S = ±15V, V_{OUT} = ±10V, R_L = 25Ω		80	110		dB
HD_2, HD_3	2nd and 3rd Harmonic Distortion Differential Mode	f = 1MHz, V_O = 20V_{P-P}, R_L = 50, A_V = 2			–75		dBc
SR	Slew Rate (Note 7)	A_V = 4, R_L = 400Ω		400	900		V/µs
	Slew Rate	A_V = 4, R_L = 25Ω			900		V/µs
BW	Small-Signal BW	A_V = 2, V_S = ±15V, Peaking ≤ 1.5dB R_F = R_G = 910Ω, R_L = 100Ω			65		MHz
		A_V = 2, V_S = ±15V, Peaking ≤ 1.5dB R_F = R_G = 820Ω, R_L = 25Ω			50		MHz

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Applies to short-circuits to ground only. A short-circuit between the output and either supply may permanently damage the part when operated on supplies greater than ±10V.

Note 3: The LT1795C is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet these extended temperature limits, but is not tested at –40°C and 85°C. The LT1795I is guaranteed to meet the extended temperature limits.

Note 4: Thermal resistance varies depending upon the amount of PC board metal attached to the device. If the maximum dissipation of the package is exceeded, the device will go into thermal shutdown and be protected.

Note 5: Guaranteed by the CMRR tests.

Note 6: R_{SHDN} is connected between the SHDN pin and V^+.

Note 7: Slew rate is measured at ±5V on a ±10V output signal while operating on ±15V supplies with R_F = 1k, R_G = 333Ω (A_V = +4) and R_L = 400Ω.

SMALL-SIGNAL BANDWIDTH

R_{SD} = 0Ω, I_S = 30mA per Amplifer, V_S = ±15V, Peaking ≤ 1dB, R_L = 25Ω

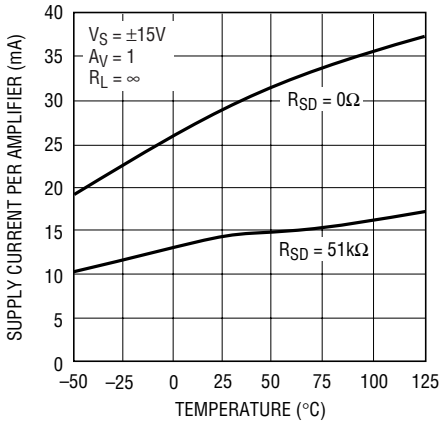
A_V	R_F	R_G	–3dB BW (MHz)
–1	976	976	44
1	1.15k	—	53
2	976	976	48
10	649	72	46

R_{SD} = 51kΩ, I_S = 15mA per Amplifer, V_S = ±15V, Peaking ≤ 1dB, R_L = 25Ω

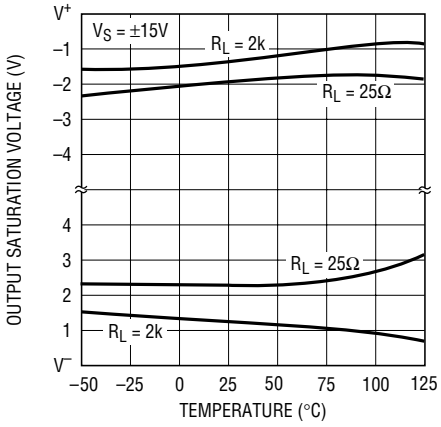
A_V	R_F	R_G	–3dB BW (MHz)
–1	976	976	30
1	1.15k	—	32
2	976	976	32
10	649	72	27

TYPICAL PERFORMANCE CHARACTERISTICS

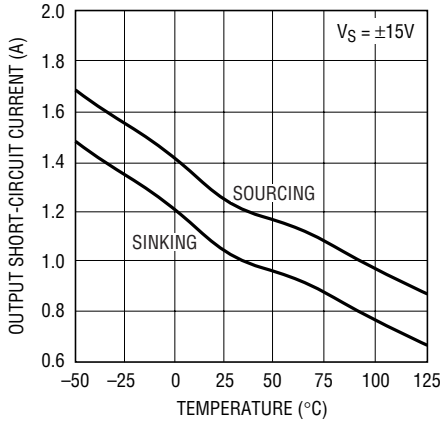
Supply Current vs Ambient Temperature



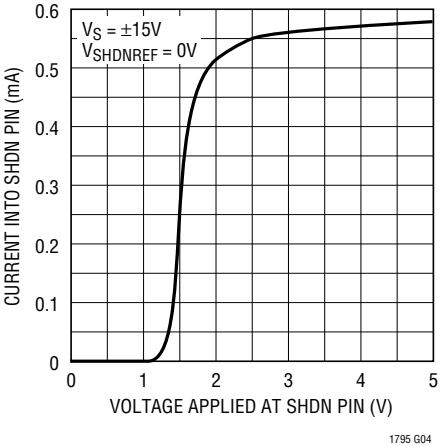
Output Saturation Voltage vs Junction Temperature



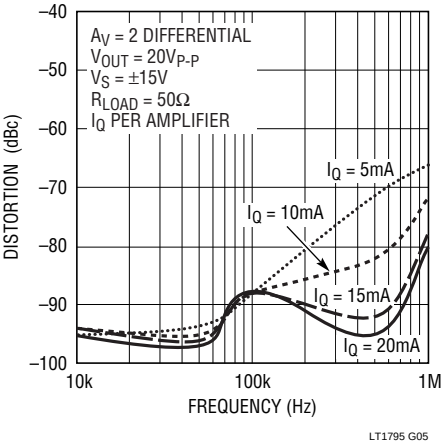
Output Short-Circuit Current vs Junction Temperature



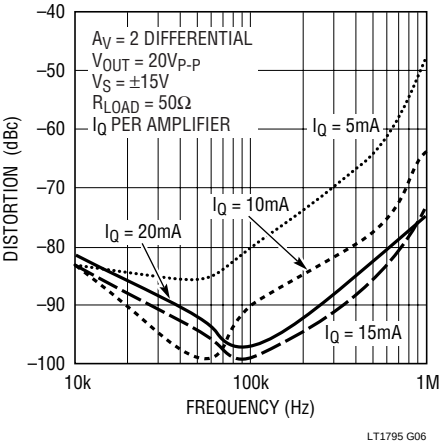
SHDN Pin Current vs Voltage



Second Harmonic Distortion vs Frequency

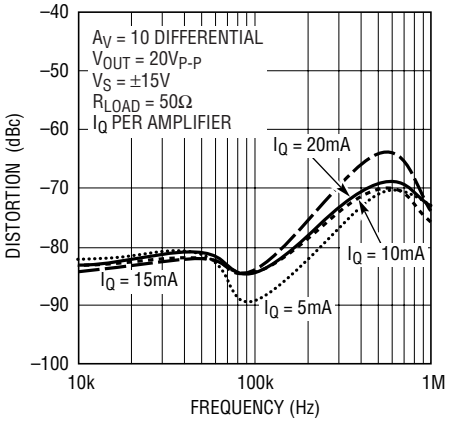


Third Harmonic Distortion vs Frequency

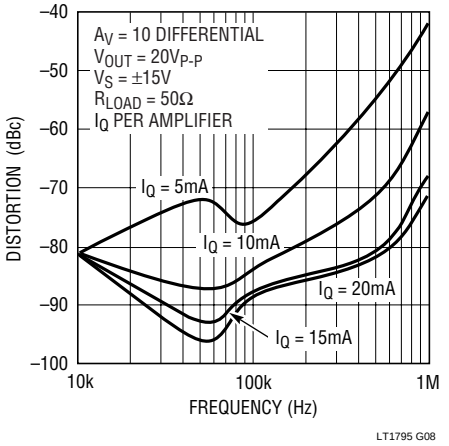


TYPICAL PERFORMANCE CHARACTERISTICS

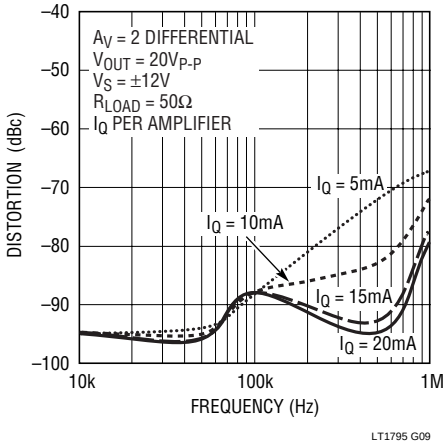
Second Harmonic Distortion vs Frequency



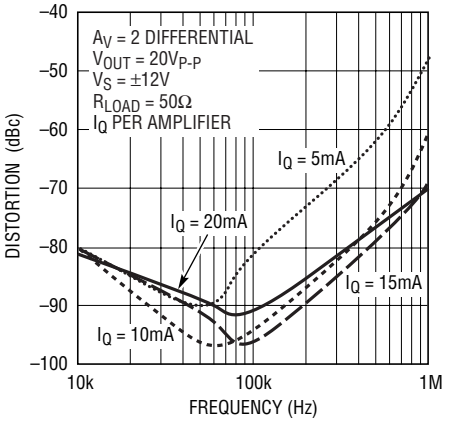
Third Harmonic Distortion vs Frequency



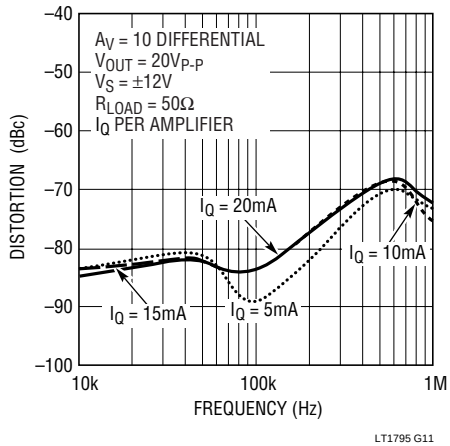
Second Harmonic Distortion vs Frequency



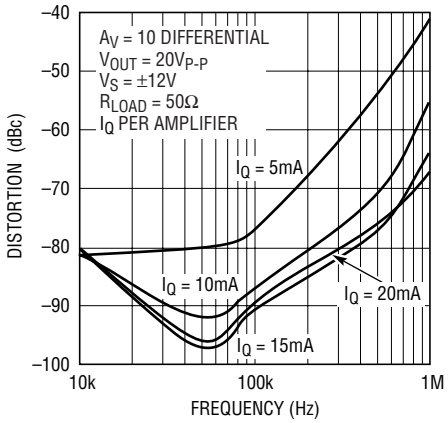
Third Harmonic Distortion vs Frequency



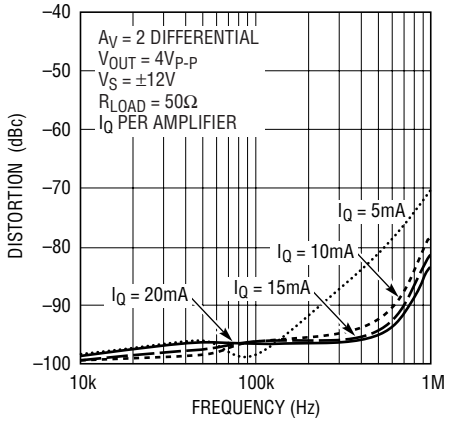
Second Harmonic Distortion vs Frequency



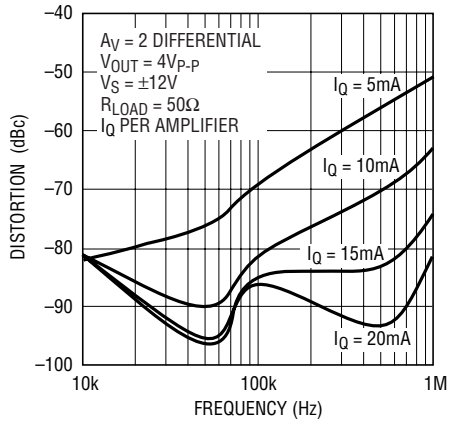
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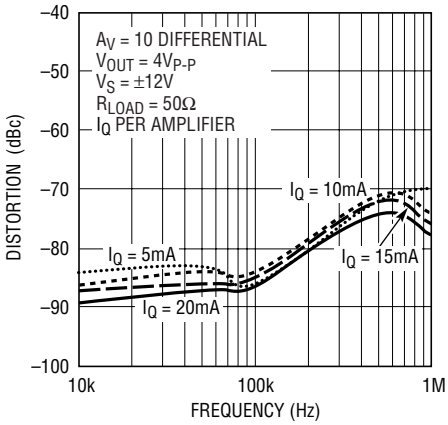
Second Harmonic Distortion vs Frequency



Third Harmonic Distortion vs Frequency

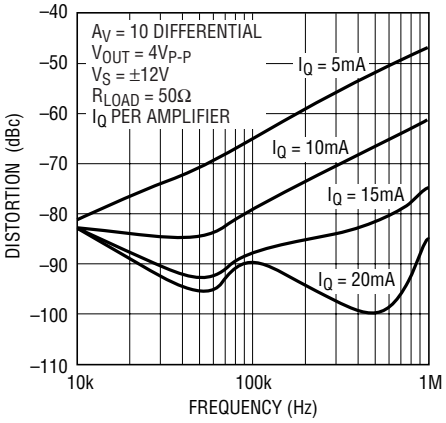


Second Harmonic Distortion vs Frequency



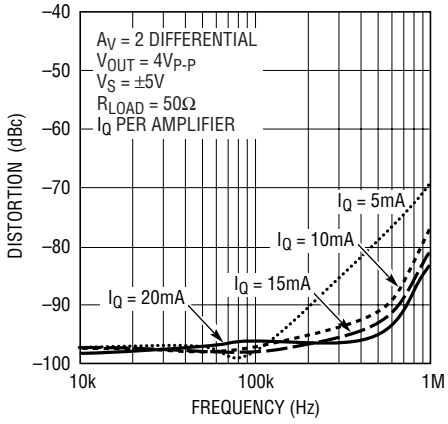
TYPICAL PERFORMANCE CHARACTERISTICS

Third Harmonic Distortion vs Frequency



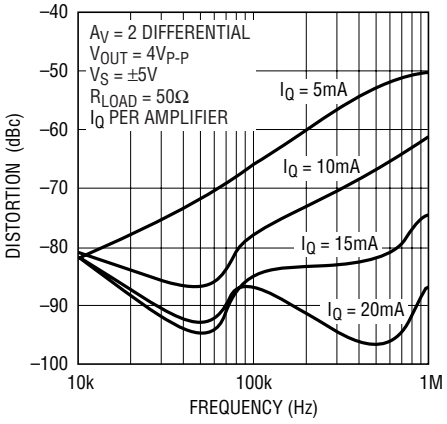
LT1795 G16

Second Harmonic Distortion vs Frequency



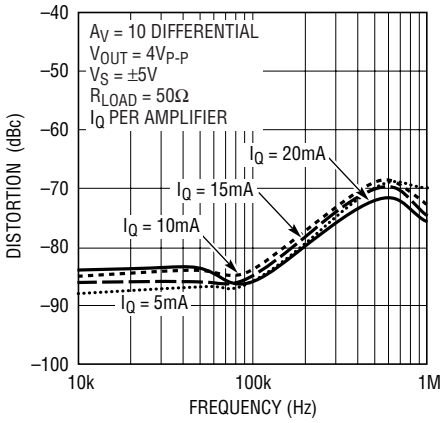
LT1795 G17

Third Harmonic Distortion vs Frequency



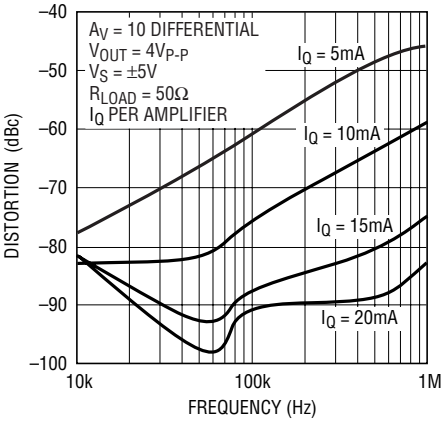
LT1795 G18

Second Harmonic Distortion vs Frequency



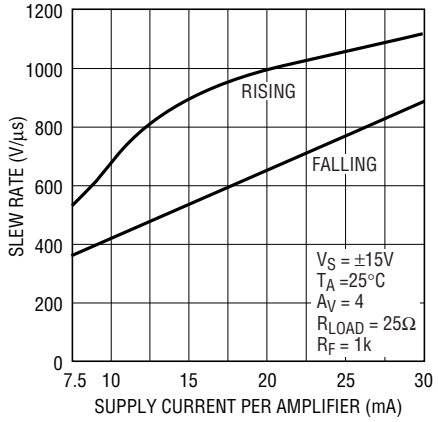
LT1795 G19

Third Harmonic Distortion vs Frequency



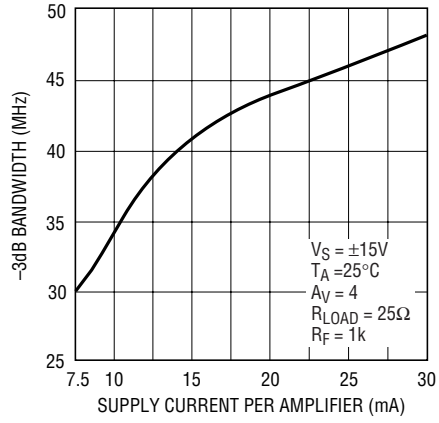
LT1795 G20

Slew Rate vs Supply Current



1795 • G21

–3dB Bandwidth vs Supply Current



1795 • G22

APPLICATIONS INFORMATION

The LT1795 is a dual current feedback amplifier with high output current drive capability. The amplifier is designed to drive low impedance loads such as twisted-pair transmission lines with excellent linearity.

SHUTDOWN/CURRENT SET

If the shutdown/current set feature is not used, connect SHDN to V⁺ and SHDNREF to ground.

The SHDN and SHDNREF pins control the biasing of the two amplifiers. The pins can be used to either turn off the amplifiers completely, reducing the quiescent current to less then 200µA, or to control the quiescent current in normal operation.

When $V_{SHDN} = V_{SHDNREF}$, the device is shut down. The device will interface directly with 3V or 5V CMOS logic when SHDNREF is grounded and the control signal is applied to the SHDN pin. Switching time between the active and shutdown states is about 1.5µs.

Figures 1 to 4 illustrate how the SHDN and SHDNREF pins can be used to reduce the amplifier quiescent current. In both cases, an external resistor is used to set the current. The two approaches are equivalent, however the required resistor values are different. The quiescent current will be approximately 115 times the current in the SHDN pin and 230 times the current in the SHDNREF pin. The voltage across the resistor in either condition is V⁺ – 1.5V. For example, a 50k resistor between V⁺ and SHDN will set the

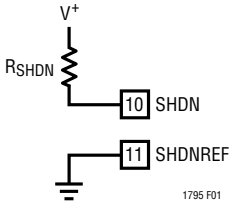


Figure 1. R_{SHDN} Connected Between V⁺ and SHDN (Pin 10); SHDNREF (Pin 11) = GND. See Figure 2

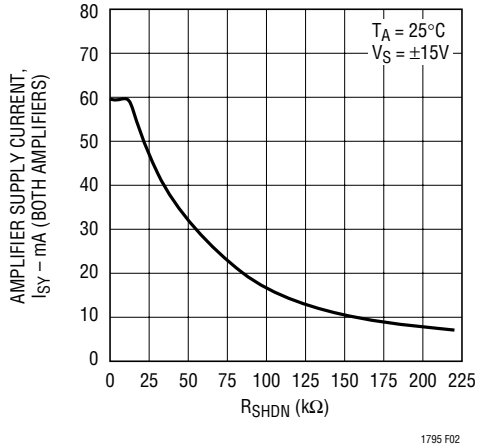


Figure 2. LT1795 Amplifier Supply Current vs R_{SHDN}. R_{SHDN} Connected Between V⁺ and SHDN, SHDNREF = GND (See Figure 1)

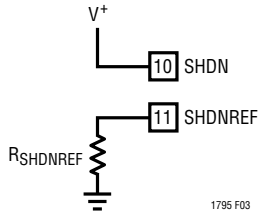


Figure 3. $R_{SHDNREF}$ Connected Between SHDNREF (Pin 11) and GND; SHDN (Pin 10) = V⁺. See Figure 4

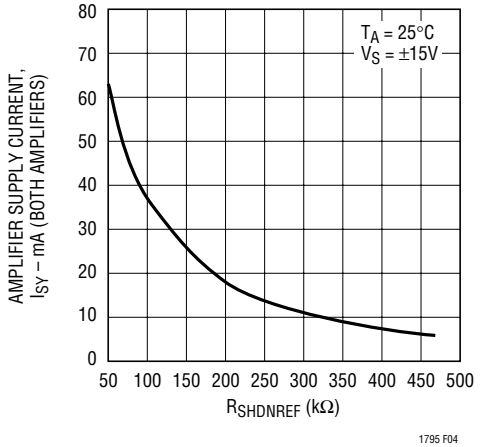


Figure 4. LT1795 Amplifier Supply Current vs $R_{SHDNREF}$. $R_{SHDNREF}$ Connected Between SHDNREF and GND, SHDN = V⁺ (See Figure 3)

APPLICATIONS INFORMATION

quiescent current to 33mA with V_S = ±15V. If ON/OFF control is desired in addition to reduced quiescent current, then the circuits in Figures 5 to 7 can be employed.

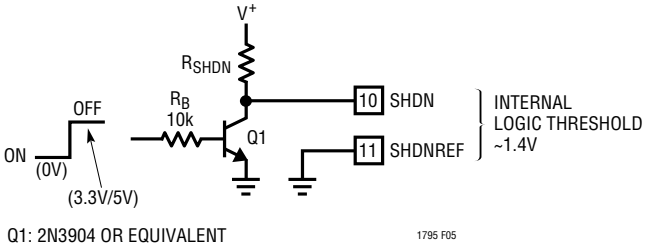


Figure 5. Setting Amplifier Supply Current Level with ON/OFF Control, Version 1

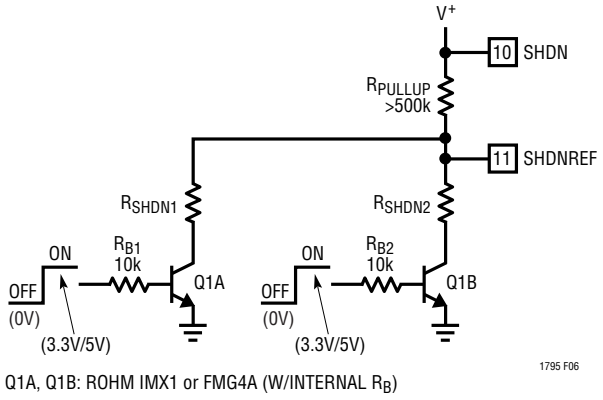


Figure 6. Setting Multiple Amplifier Supply Current Levels with ON/OFF Control, Version 2

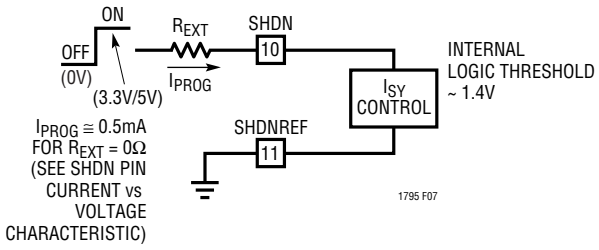


Figure 7. Setting Amplifier Supply Current Level with ON/OFF Control, Version 3

Figure 8 illustrates a partial shutdown with direct logic control. By keeping the output stage slightly biased on, the output impedance remains low, preserving the line termination. The design equations are:

$$R1 = \frac{115 \bullet V_H}{(I_S)_{ON} - (I_S)_{OFF}}$$

$$R2 = \frac{115 \bullet (V_{CC} - V_{SHDN})}{(V_{SHDN} / V_H) \bullet \left[(I_S)_{ON} - (I_S)_{OFF}\right] + (I_S)_{OFF}}$$

where

V_H = Logic High Level

$(I_S)_{ON}$ = Supply Current Fully On

$(I_S)_{OFF}$ = Supply Current Partially On

V_{SHDN} = Shutdown Pin Voltage ≈1.4V

V_{CC} = Positive Supply Voltage

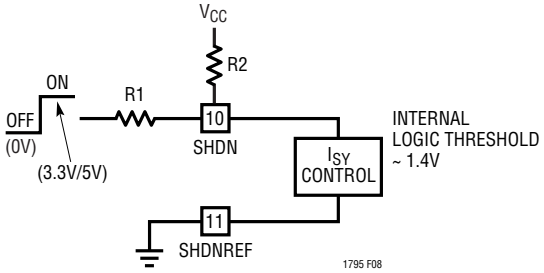


Figure 8. Partial Shutdown

THERMAL CONSIDERATIONS

The LT1795 contains a thermal shutdown feature that protects against excessive internal (junction) temperature. If the junction temperature of the device exceeds the protection threshold, the device will begin cycling between normal operation and an off state. The cycling is not harmful to the part. The thermal cycling occurs at a slow rate, typically 10ms to several seconds, which depends on the power dissipation and the thermal time constants of the package and heat sinking. Raising the ambient tempera-

APPLICATIONS INFORMATION

ture until the device begins thermal shutdown gives a good indication of how much margin there is in the thermal design.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. For the TSSOP package, power is dissipated through the exposed heatsink. For the SO package, power is dissipated from the package primarily through the V^- pins (4 to 7 and 14 to 17). These pins should have a good thermal connection to a copper plane, either by direct contact or by plated through holes. The copper plane may be an internal or external layer. The thermal resistance, junction-to-ambient will depend on the total copper area connected to the device. For example, the thermal resistance of the LT1795 connected to a 2×2 inch, double sided 2 oz copper plane is 40°C/W.

CALCULATING JUNCTION TEMPERATURE

The junction temperature can be calculated from the equation:

$$T_J = (P_D)(\theta_{JA}) + T_A$$

where

T_J = Junction Temperature

T_A = Ambient Temperature

P_D = Device Dissipation

θ_{JA} = Thermal Resistance (Junction-to-Ambient)

Differential Input Signal Swing

The differential input swing is limited to about ±5V by an ESD protection device connected between the inputs. In normal operation, the differential voltage between the input pins is small, so this clamp has no effect. However, in the shutdown mode, the differential swing can be the same as the input swing. The clamp voltage will then set the maximum allowable input voltage.

POWER SUPPLY BYPASSING

To obtain the maximum output and the minimum distortion from the LT1795, the power supply rails should be well bypassed. For example, with the output stage supplying 0.5A current peaks into the load, a 1Ω power supply impedance will cause a droop of 0.5V, reducing the available output swing by that amount. Surface mount tantalum and ceramic capacitors make excellent low ESR bypass elements when placed close to the chip. For frequencies above 100kHz, use 1µF and 100nF ceramic capacitors. If significant power must be delivered below 100kHz, capacitive reactance becomes the limiting factor. Larger ceramic or tantalum capacitors, such as 4.7µF, are recommended in place of the 1µF unit mentioned above.

Inadequate bypassing is evidenced by reduced output swing and "distorted" clipping effects when the output is driven to the rails. If this is observed, check the supply pins of the device for ripple directly related to the output waveform. Significant supply modulation indicates poor bypassing.

Capacitance on the Inverting Input

Current feedback amplifiers require resistive feedback from the output to the inverting input for stable operation. Take care to minimize the stray capacitance between the output and the inverting input. Capacitance on the inverting input to ground will cause peaking in the frequency response (and overshoot in the transient response), but it does not degrade the stability of the amplifier.

Feedback Resistor Selection

The optimum value for the feedback resistors is a function of the operating conditions of the device, the load impedance and the desired flatness of response. The Typical AC Performance tables give the values which result in less than 1dB of peaking for various resistive loads and operating conditions. If this level of flatness is not required, a higher bandwidth can be obtained by use of a lower feedback resistor.

For resistive loads, the COMP pin should be left open (see Capacitive Loads section).

Capacitive Loads

The LT1795 includes an optional compensation network for driving capacitive loads. This network eliminates most of the output stage peaking associated with capacitive loads, allowing the frequency response to be flattened.

APPLICATIONS INFORMATION

Figure 9 shows the effect of the network on a 200pF load. Without the optional compensation, there is a 6dB peak at 85MHz caused by the effect of the capacitance on the output stage. Adding a 0.01µF bypass capacitor between the output and the COMP pins connects the compensation and greatly reduces the peaking. A lower value feedback resistor can now be used, resulting in a response which is flat to ±1dB to 45MHz. The network has the greatest effect for C_L in the range of 0pF to 1000pF.

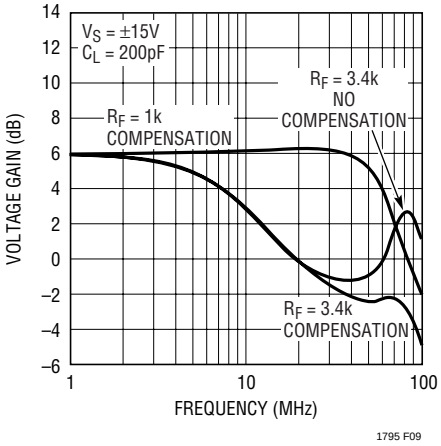


Figure 9

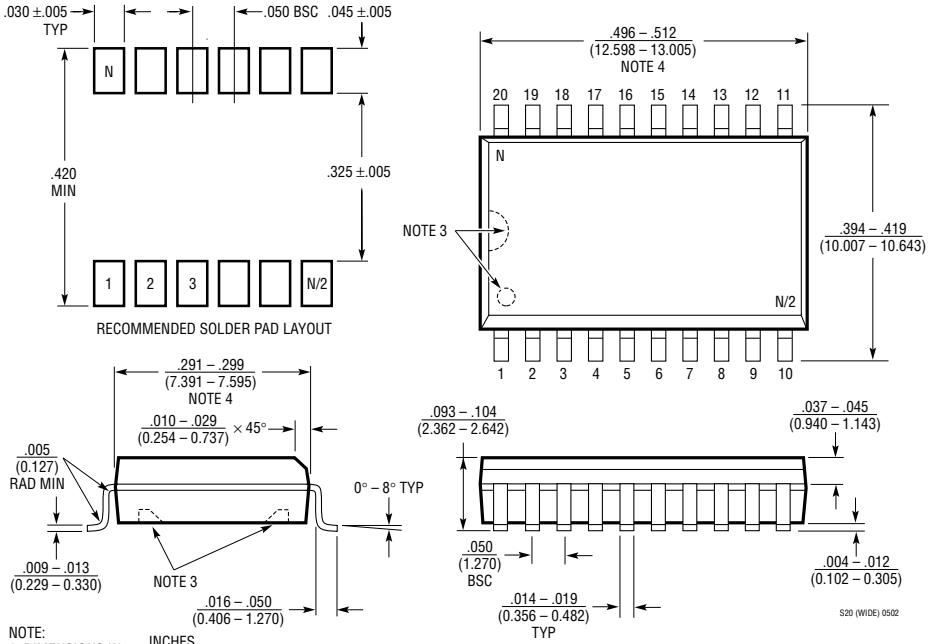
Although the optional compensation works well with capacitive loads, it simply reduces the bandwidth when it is connected with resistive loads. For instance, with a 25Ω load, the bandwidth drops from 48MHz to 32MHz when the compensation is connected. Hence, the compensation was made optional. To disconnect the optional compensation, leave the COMP pin open.

DEMO BOARD

A demo board (DC261A) is available for evaluating the performance of the LT1795. The board is configured as a differential line driver/receiver suitable for xDSL applications. For details, consult your local sales representative.

PACKAGE DESCRIPTION

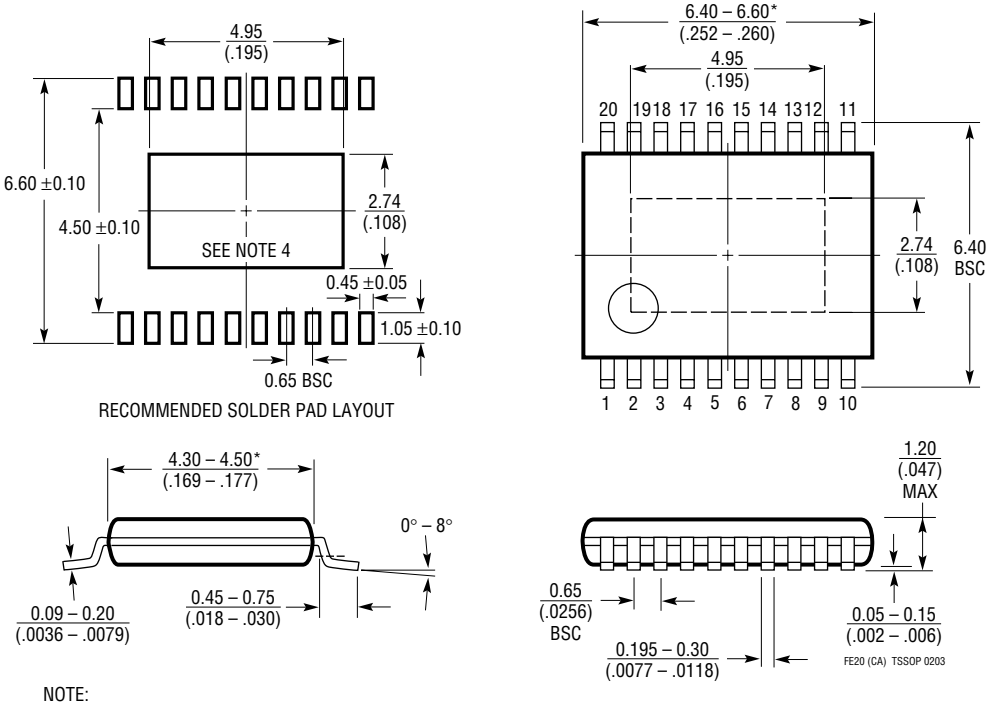
SW Package
20-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)



NOTE:
1. DIMENSIONS IN INCHES (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

PACKAGE DESCRIPTION

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation CA

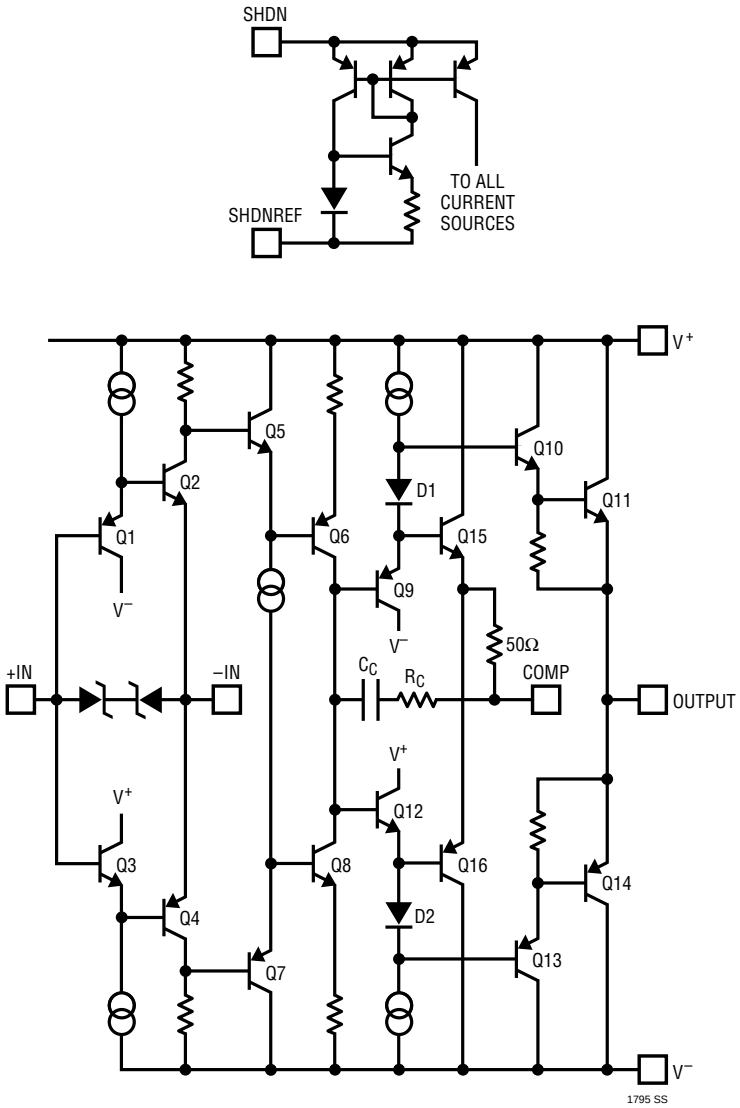


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

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SIMPLIFIED SCHEMATIC



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1497	Dual 125mA, 50MHz Current Feedback Amplifier	900V/µs Slew Rate
LT1207	Dual 250mA, 60MHz Current Feedback Amplifier	Shutdown/Current Set Function
LT1886	Dual 200mA, 700MHz Voltage Feedback Amplifier	Low Distortion: –72dBc at 200kHz

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