DATA SHEET

GPL81201A

Low Power 84 Dots LCD Controller with 8KB ROM

Oct. 01, 2014

Version 1.0

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LOW POWER 84 DOTS LCD CONTROLLER WITH 16KB OTP ROM

1. GENERAL DESCRIPTION

The GPL81201A, a chip designed for LCD display embedded with 128 bytes SRAM and 8K bytes ROM, features four timers and up to 15 software selectable general I/Os. It operates over a wide voltage range of 1.8 - 3.6V@4/8MHz and has a sleep mode for power saving mode, which retains the contents of RAM, but stops the oscillator and causes all other chip functions to be inoperative. Sleep mode can be released by using external wakeup sources or time base wakeup source. This device is applicable for many applications such as low power watch and other LCD-based products.

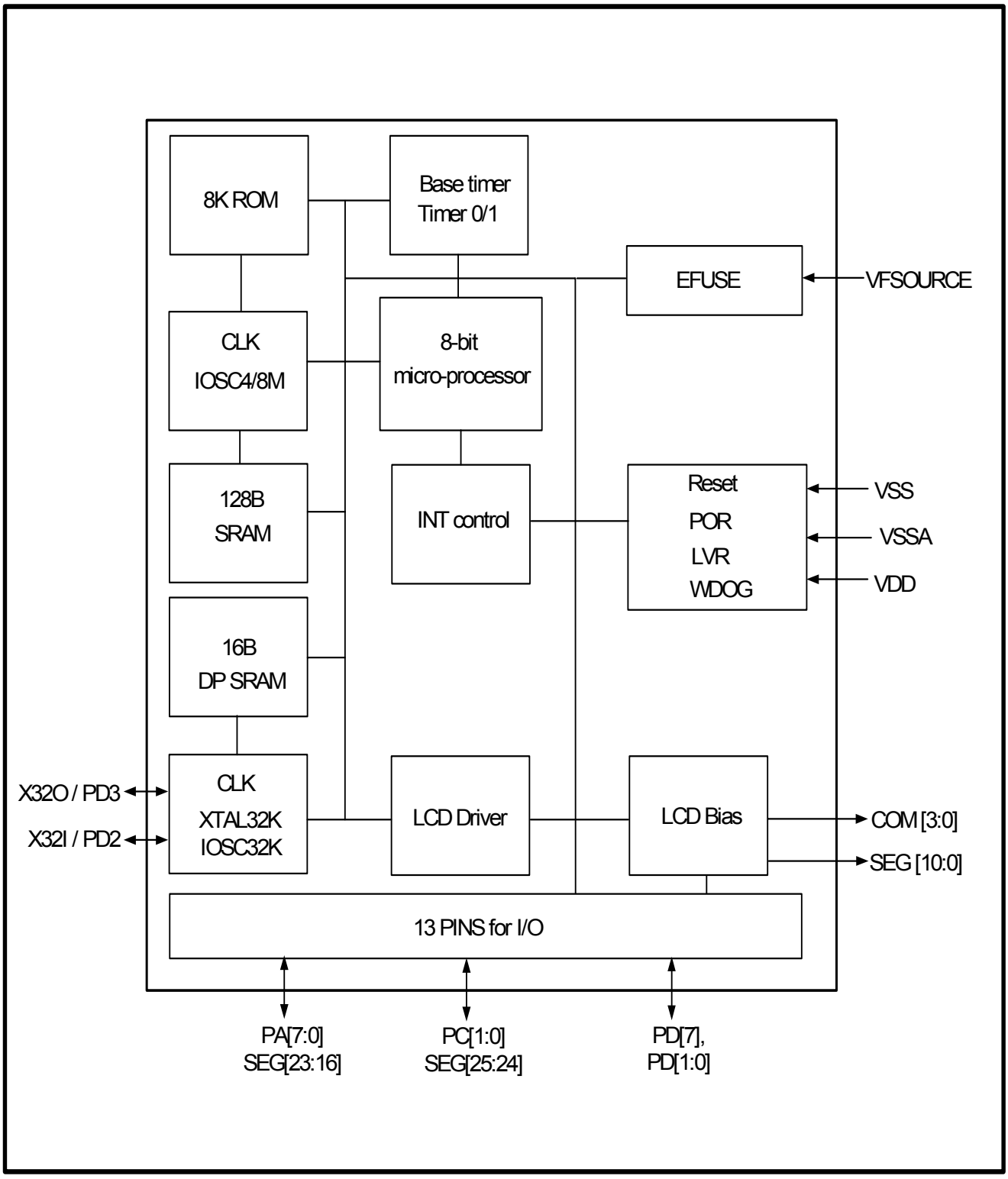
2. FEATURES

- Built-in 8-bit processor
- 128-byte SRAM
- 8K-byte ROM
- 128 bit DPRAM
- Built-in 4M/8MHz Crystal or IOSC for system operation
  - internal oscillator with ±5% precision
- Built-in 32KHz IOSC or 32768Hz Crystal oscillator circuit for timebase.
- Operating voltage:
  - 4.0MHz@1.8V~3.6V or 8.0MHz@1.8V~3.6V
- Built-in Standby mode (Clock Stop mode) & Halt mode(with LCD and 32K timer on) for power saving
  - Low standby current, ISTBY < 1u @3.6V, 25℃
  - Low halt mode current, Ihalt < 8u @3.6V, 25℃
- Up to 15 bi-directional tri-state I/O ports
  - Port A[7:0]: with programmable pull high / pull low / floating, share pads with SEGMENT[23:16]
  - Port C[1:0]: with programmable pull high / pull low / floating, share pads with SEGMENT[25:24].
  - Port D[7],D[1:0]: with programmable pull high / pull low / floating.
  - Port D[3:2]: with programmable pull high / pull low / floating, share pads with X32O, X32I.
- LCD configurations: 4 coms x 21 segs (MAX)
  - Frame rate is 85Hz.
  - LCD 1/3 bias; 1/3, 1/4 duty; VLCD = VDD
- Four timers
  - Basic timer provides Fosc/4194304 watch dog source;
  - Timer0 is a general purpose 8-bit timer with input clock selectable;
  - Timer1 is a general purpose 12-bit timer with input clock selectable
  - 32K timer is a time base wakeup source with frequency selectable
- 8 interrupt sources
  - TM0O, TM1O, CPUDiv1K, CPUDiv4K, CPUDiv32K, CPUDiv2M, TBHF, TBLF.
- Wakeup source
  - Key (Port C/D) change wakeup
  - 32K time base wakeup(TBHF/TBLF)
- LVD (Low voltage detect)
  - Sense VDD voltage@ 2.1V / 2.4V (register option)

Note1: TBHF: 128Hz, 256Hz, 512Hz or 1KHz

Note2: TBLF: 2Hz, 4Hz, 8Hz or 16Hz

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

4.1. Pin Description

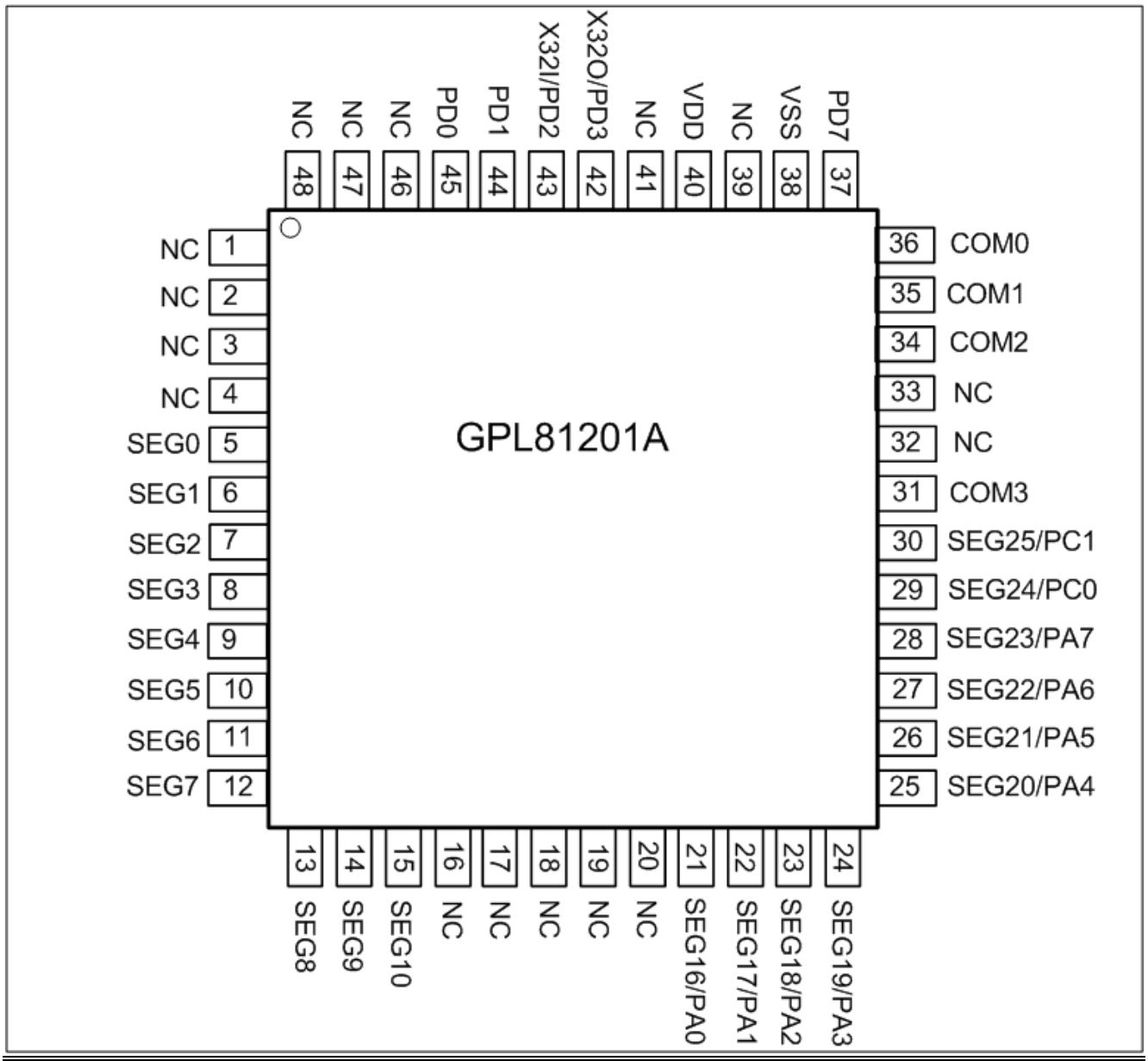
Type: I = Input, O = Output, S = Supply

Pin Name	Dice Pin No.	PKG Pin No.	Type	Main Function	Alternate Function
SEG[0:10]	1~11	5~15	O	LCD driver segment output	
PA0/SEG16	12	21	I/O	**PortA[7:0]:** Bi-directional programmable Input / Output port. It can be configured as pull_high resistor, pull_low resistor, floating input or CMOS output. **SEG[23:16]:** LCD driver segment output	
PA1/SEG17	13	22	I/O		
PA2/SEG18	14	23	I/O		
PA3/SEG19	15	24	I/O		
PA4/SEG20	16	25	I/O		
PA5/SEG21	17	26	I/O		
PA6/SEG22	18	27	I/O		
PA7/SEG23	19	28	I/O		
PC0/SEG24	20	29	I/O	**PortC[1:0]:** Bi-directional programmable Input/Output port. It can be configured as pull_high resistor, pull_low resistor, floating input or CMOS output. **Normal wakeup**; if a key is changed, the chip can be wakened from sleep mode. **SEG[25:24]:** LCD driver segment output	
PC1/SEG25	21	30	I/O		
COM[3:0]	22~25	31~36	O	LCD driver common output	
PD7	26	37	I/O	**PortD[7]:** Bi-directional programmable Input/Output port. It can be configured as pull_high resistor, pull_low resistor, floating input or CMOS output. **Normal wakeup;** if a key is changed, the chip can be wakened from sleep mode.	
VSSA	27	38	S	**Ground**	
VSS	28	38	S	**Ground**	
VFSOURCE	29	NC	S	**Test pin.** **Keep it at floating state.**	
VDD	30	40	S	**power supply**	
X32O/PD3	31	42	I/O	**PortD[3]:** Bi-directional programmable Input/Output port. It can be configured as pull_high resistor, pull_low resistor, floating input or CMOS output. **Normal wakeup;** if a key is changed, the chip can be wakened from sleep mode. **Crystal Output:** It is connected with external crystal for 32K crystal oscillation circuitry in crystal mode.	
X32I/PD2	32	43	I/O	**PortD[2]:** Bi-directional programmable Input/Output port. It can be configured as pull_high resistor, pull_low resistor, floating input or CMOS output. **Normal wakeup;** if a key is changed, the chip can be wakened from sleep mode. **Crystal Input:** It is connected with external crystal for 32K crystal oscillation circuitry in crystal mode.	

Pin Name	Dice Pin No.	PKG Pin No.	Type	Main Function	Alternate Function
PD1	33	44	I/O	**PortD[1]:** Bi-directional programmable Input/Output port. It can be configured as pull_high resistor, pull_low resistor, floating input or CMOS output. **Normal wakeup;** if a key is changed, the chip can be awakened from sleep mode.	
PD0	34	45	I/O	**PortD[0]:** Bi-directional programmable Input/Output port. It can be configured as pull_high resistor, pull_low resistor, floating input or CMOS output. **Normal wakeup;** if a key is changed, the chip can be awakened from sleep mode.	

4.2. PIN Assignment (Top View)

4.2.1. LQFP48 Package for GPL81201A



5. FUNCTION DESCRIPTIONS

5.1. CPU

The 8-bit microprocessor in GPL81201A is a high performance processor equipped with Accumulator, Program Counter, X Register, Y Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure).

5.2. Clock Source

The GPL81201A equips two types of clock sources:

(1) High speed frequency to support the whole system operation. There are two frequency options: 4MHz/8MHz and can be selected by register based on various user's application needs. It comes from IOSC8M

(2) Low speed frequency to control LCD frame rate and time base timer. It is derived from IOSC32K or XTAL32K.

5.3. ROM/RAM Area

The GPL81201A features 8K-byte ROM that can be defined as the program area, address located from $E000H to $FFFFH. Its RAM consists of 128 bytes (including Stack) at locations $80H~$FFH mapping to $180H~$1FFH.

5.4. Stop Clock Mode

The GPL81201A equips a power saving mode for those applications requiring very low standby current. Users can simply enable the wakeup sources to stop CPU clock by writing the STOP CLOCK Register. By doing that, CPU will enter standby mode and the RAM and I/Os remain at their previous states until being awakened. There are two types of wakeup sources in the GPL81201A, I/O PAD data transient (PortC/D Key change) and 32K timer base wakeup source(TBHF/TBLF). After the GPL81202A wakes up, CPU will go to the next state of where CPU enters sleep mode. Wake-up action will not influence RAM and I/Os.

Note1: TBHF: 128Hz, 256Hz, 512Hz or 1KHz

Note2: TBLF: 2Hz, 4Hz, 8Hz or 16Hz

5.5. I/O Ports

The GPL81201A has three IO ports: PortA, PortC and PortD. These port pins may be multiplexed with an alternate function for the peripheral features on the device. In general, when an initial reset state occurs, all ports are used as a general purpose input port. There are three parts in IO structure: data, direction and attribution registers. Each corresponding bit in these ports should be given a value.

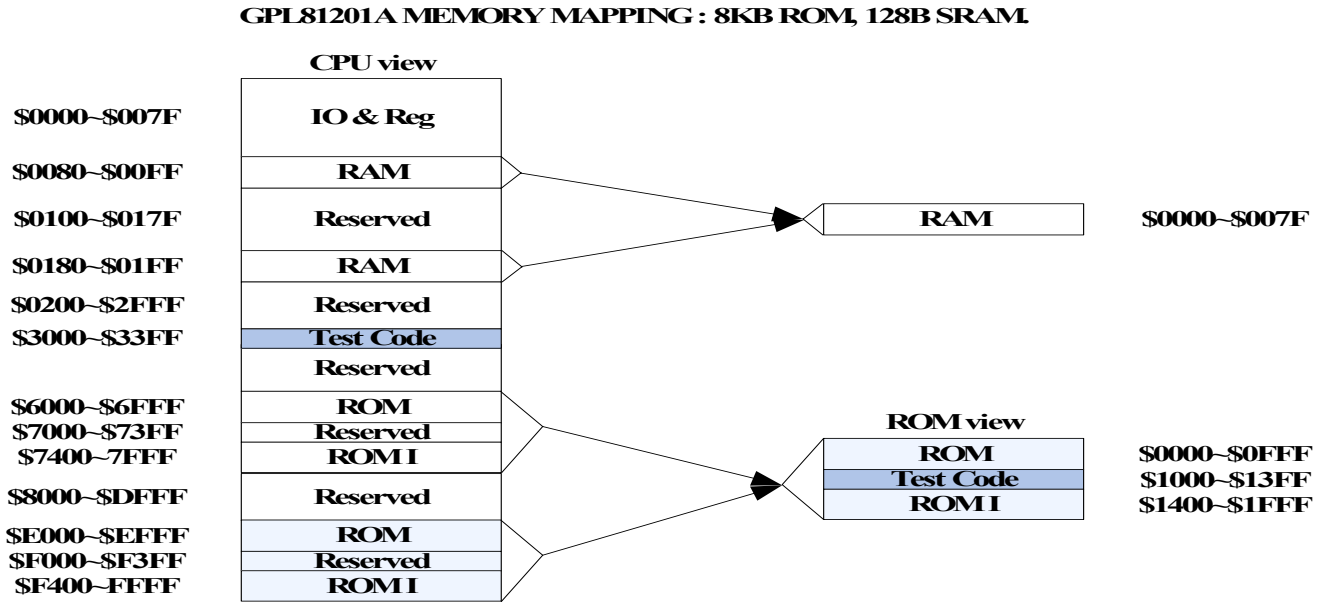
[Table] 5-1 I/O configurations

Attribution (P_IOX_ATT)	Direction (P_IOX_DIR)	Data (P_IOX_DAT)	Function	Description
0	0	0	Floating	Input with float
0	0	1	Pull low	Input with pull-low
0	1	0	Driving low	Output Data
0	1	1	Driving High	Output Data
1	0	0	Floating	Input with float
1	0	1	Pull high	Input with pull-high
1	1	0	Driving High	Output Data
1	1	1	Driving low	Output Data

5.6. LCD Controller

GPL81201A contains a LCD controller/driver that provides the capability to drive 4 commons and 21 segments LCD. To reduce CPU overhead, a display buffer is designed for LCD mappings. A LCD dot/pattern is set ON or OFF by programming the corresponding bit in the display buffer. In addition, the LCD can be programmed as 1/3duty with 1/3bias or 1/4duty with 1/3bias. The VLCD level is equal VDD. The LCD driver can also operate during sleep by keeping 32KHz oscillator running.

5.7. Map of Memory



6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 4.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +70℃
Storage Temperature	T_{STO}	-50℃ to +150℃
VDD Total MAX Current	I_{VDDM}	100mA
VSS Total MAX Current	I_{VSSM}	200mA

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions, see AC/DC Electrical Characteristics.

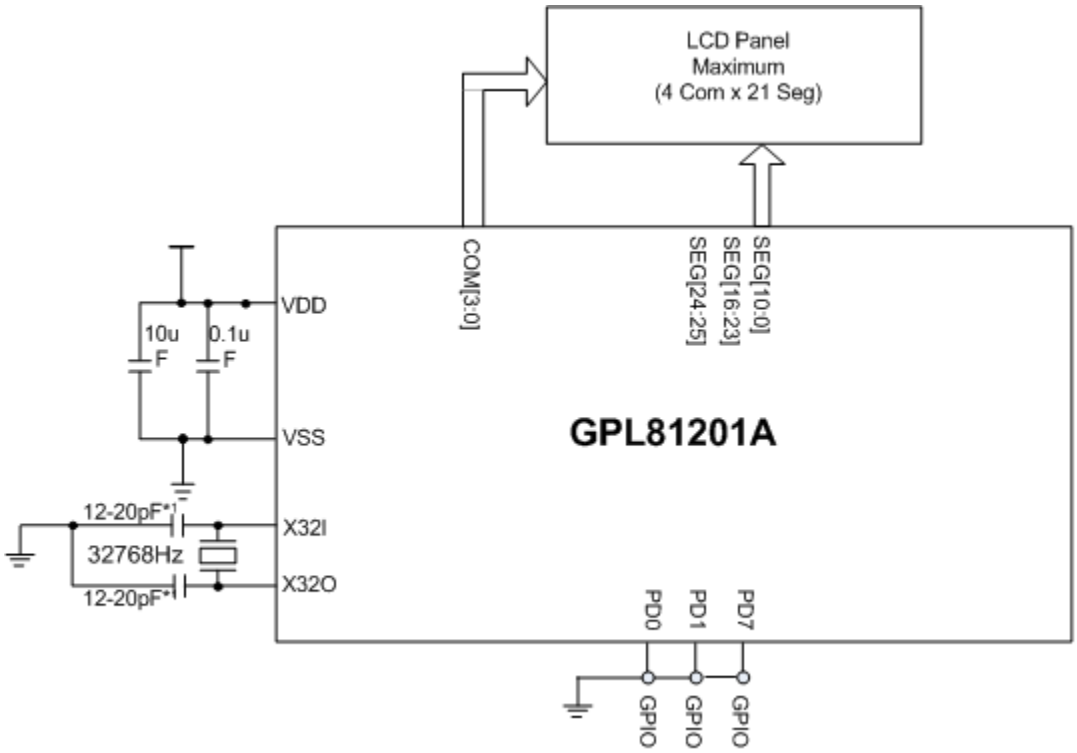
6.2. AC Characteristics

Characteristics	Limit			Unit	Test Condition
	Min.	Typ.	Max.		
OSC Accuracy @ Freq=4MHz					
OSC Variation	-3.0	±1.5	3.0	%	VDD = 1.8 - 3.6V, TEMP:0C~70C
OSC Accuracy @ Freq=32768Hz					
OSC Variation	-7.0	±3.5	7.0	%	VDD = 1.8 - 3.6V, TEMP:0C~70C

6.3. DC Characteristics (VDD = 3.0V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	1.8	-	3.6	V	F_{CPU} = 8.0MHz, For 2-battery
Operating Current	I_{OP}	-	2.0	3.0	mA	F_{CPU} = 8.0MHz @ 3.6V, no load
Standby Current	I_{STBY}	-	-	1.0	uA	VDD = 3.8V, all clock off.
Halt mode current	I_{halt}	-	5.0	10.0	uA	VDD = 3.8V, LCD on, no load.
Green Mode current	I_{green}	-	4.0	9.0	uA	VDD = 3.8V, LCD on, no load.
Input High Level	V_{IH}	0.7VDD	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.3VDD	V	VDD = 3.0V
Output High Level PA, PC, PD	V_{OH}	0.8VDD	-	-	V	VDD = 3.0V I_{OH} = -6mA
Output Low Level PA, PC, PD	V_{OL}	-	-	0.2VDD	V	VDD = 3.0V I_{OL} = 16mA
Input Pull High Resistor PA, PC, PD	R_H	30	50	70	Kohm	Pull High VDD = 3.0V
Input Pull Low Resistor PA, PC, PD	R_L	30	50	70	Kohm	Pull Low VDD = 3.0V

7. APPLICATION CIRCUITS



Note1: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GPL81201A -NnnV - C	Chip form
GPL81201A -NnnV – QL23x	Halogen Free 48 pin LQFP Package

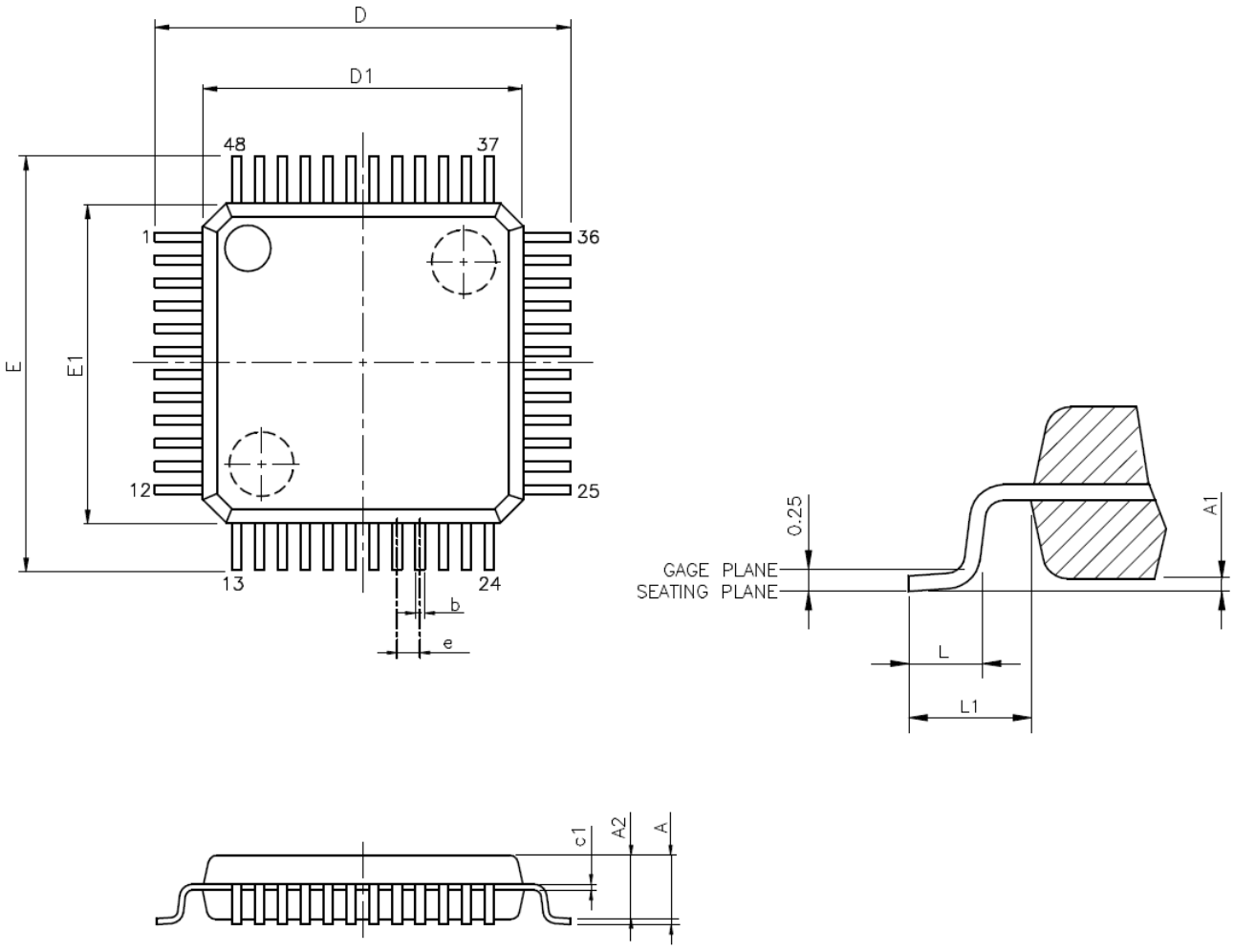
Note1: Code number (NnnV) is assigned for customer.

Note2: Code number (N = A-Z or 0-9, nn=00-99); version (V = A - Z)

Note3: Package form number (x = 0-9, serial number)

8.2. Package Information

8.2.1. LQFP 48L outline dimensions



Symbol	Millimeter		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	9.00 BSC.		
D1	7.00 BSC.		
E	9.00 BSC.		

Symbol	Millimeter		
	Min.	Nom.	Max.
E1	7.00 BSC.		
e	0.5 BSC.		
b	0.17	0.22	0.27
C1	0.09	-	0.16
L	0.45	0.60	0.75
L1	1.00 REF		

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10. REVISION HISTORY

Date	Revision #	Description	Page
Oct. 01, 2012	1.0	Original	14