BURR-BROWN®



DIR1700

**PRELIMINARY INFORMATION
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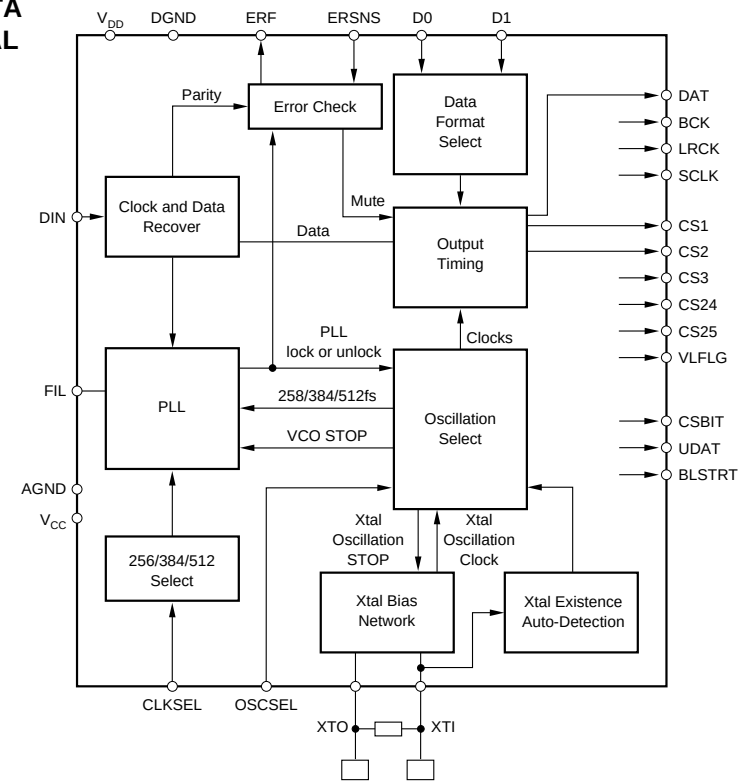
DIGITAL AUDIO INTERFACE RECEIVER

FEATURES

- **STANDARD DIGITAL AUDIO INTERFACE RECEIVER (EIAJ1201)**
- **SAMPLING RATE: 32/44.1/48/96kHz**
- **RECOVERS 256/384/512f_S SYSTEM CLOCKS**
- **VERY LOW CLOCK JITTER: 100ps (with 20pF load)**
- **FLEXIBLE SYSTEM CLOCK OUTPUT**
- **SELECTABLE OUTPUT PCM AUDIO DATA FORMAT**
- **XTAL CLOCK/PLL CLOCK OPERATION MODES**
- **SELECTABLE ERROR FLAG FUNCTION**
- **OUTPUTS CHANNEL STATUS DATA FLAG WITH BLOCK START SIGNAL**
- **OUTPUTS USER BIT DATA**
- **SINGLE +5V POWER SUPPLY**
- **28-LEAD SSOP PACKAGE**

DESCRIPTION

DIR1700 is a Digital Audio Interface Receiver (DIR) which is designed for consumer and professional digital audio applications, such as digital AV receivers. DIR1700 has two system clock operation modes: internal PLL operation mode and XTAL clock operation mode for systems which contain both digital and analog inputs. The advantages of the DIR1700 are very low clock jitter, and 96kHz sampling rate capability. These features are now required for consumer and professional audio systems.



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PDS-1416 Printed in U.S.A. September, 1998

SPECIFICATIONS—Preliminary

All specifications at +25°C and V_{CA} = V_{CP} = V_{DD} = +5V, unless otherwise noted.

PARAMETER	CONDITIONS	DIR1700E MIN	DIR1700E TYP	DIR1700E MAX	UNITS
DIGITAL FILTER PERFORMANCE					
Input Logic Level: V_{IH}(1)		2.0			VDC
V_{IL}(1)				0.8	VDC
$V_{IH}2$(2)		70% V_{DD}			VDC
$V_{IL}2$(2)				30% V_{DD}	VDC
$V_{IH}3$(3)		TBD			VDC
$V_{IL}3$(3)				TBD	VDC
Output Logic Level: V_{OH}(4)	I_O = 2mA	V_{DD} 0.4			VDC
V_{OL}(4)	I_O = –4mA			0.5	VDC
Input Leakage Current: I_{IN}			±1.0	±10	µA
Input Sampling Frequency: f_S		+32		96	kHz
System Clock Frequency SCLK(5)		8.192	256, 384, 512f_S	36.864	MHz
SCLK Clock Jitter			100		ps rms
SCLK Duty Cycle			50		%
Crystal Resonator Frequency		8.192		24.576	MHz
POWER SUPPLY REQUIREMENTS					
Voltage Range	V_{DD}, V_{CC}	+4.5	+5	+5.5	VDC
Supply Current: I_A (V_{CC})			TBD		mA
I_D (V_{DD})			TBD		mA
Power Consumption	P_D		TBD		mA

NOTES: (1) Except CLKSEL DIN; TTL Compatible. (2) CLKSEL. (3) DIN, CMOS Logic Level. (4) Pins 6-8, 11-21, and 23. (5) f_S is defined as the incoming audio sampling frequency per channel. (6) DIR1700 without load at SCLK, LRCK, BCK, DAT. Power supply current varies with system clock frequency.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages: +V_{DD} ..... ±6.5V
+V_{CC} ..... ±6.5V
Input Voltage ..... –0.3 to V_{DD} +0.3V
Input Current ..... ±10mA
Operating Temperature Range ..... –25°C to +85°C
Storage Temperature Range ..... –55°C to +125°C

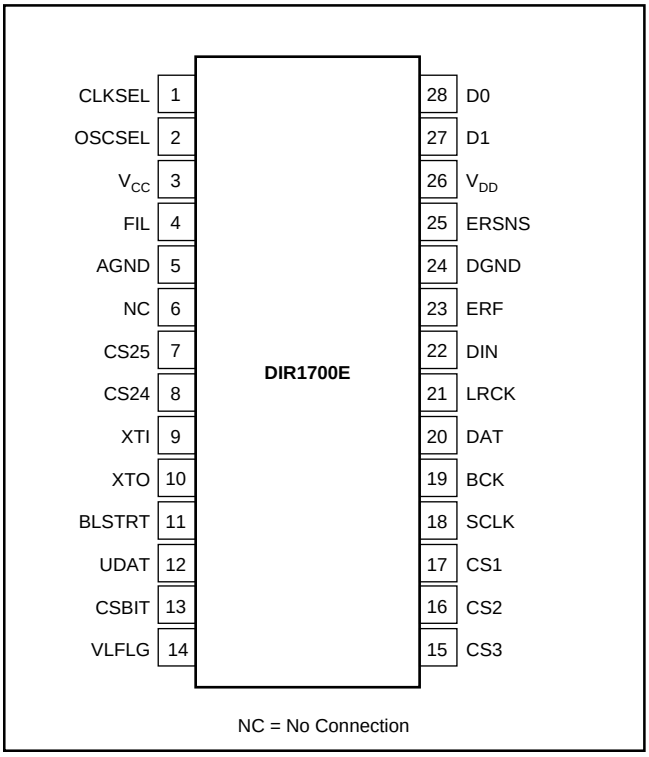
PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
DIR1700E	28-Lead SSOP	324

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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PIN CONFIGURATION



PIN ASSIGNMENTS

PIN	NAME	I/O	DESCRIPTION
1	CLKSEL	In	Clock Select (256f_S, 384f_S and 512f_S)(1)
2	OSCSEL	In	Oscillation Select (PLL/Xtal)(2)
3	V_{CC}	—	Analog Power Supply
4	FIL	—	PLL Filter
5	AGND	—	Analog Ground
6	NC	—	No Connection
7	CS25	Out	f_S Rate Flag (32k, 44.1k and 48k)(4)
8	CS24	Out	f_S Rate Flag (32k, 44.1k and 48k)(4)
9	XTI	In	Crystal In
10	XTO	Out	Crystal Out
11	BLSTRT	Out	Block Start Clock(5)
12	UDAT	Out	User Data Out(5)
13	CSBIT	Out	Channel Status Bit(5)
14	VLFLG	Out	Validity Flag
15	CS3	Out	Emphasis Flag(4)
16	CS2	Out	Copy Guard Flag(4)
17	CS1	Out	Audio Data Flag (PCM/DATA)(4)
18	SCLK	Out	Audio System Clock Out
19	BCK	Out	Audio Bit Clock Out
20	DAT	Out	Audio Data Out
21	LRCK	Out	Audio Left/Right Clock Out
22	DIN	In	Data Input
23	ERF	Out	Error Flag Out (PLL Unlock/Parity Error)
24	DGND	—	Digital Ground
25	ERSNS	In	Error Sense Switch(2)
26	V_{DD}	—	Digital Power Supply
27	D1	In	Data Format Select 1(3)
28	D0	In	Data Format Select 0(3)

NOTES: (1) When "CLKSEL" is open, input level becomes 1/2 V_{DD} by pull-up and pull-down resistors. (2) Pull-up. (3) Pull-down. (4) Channel status output pins become active for consumer applications. (5) Serial outputs are utilized for both consumer and professional applications.