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EXAR'S XR17C154 COMPARED WITH OXFORD'S OX16PCI954

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1.0 INTRODUCTION

This application note describes the major hardware and firmware differences between Exar's XR17C154 and Oxford's OX16PCI954.

1.1 HARDWARE DIFFERENCES

- The XR17C154 is available in a smaller 144-pin TQFP package than the OX16PCI954 which is available in a 160-pin TQFP package. They are not available in the same packages therefore they are not pin-to-pin compatible. The XR17C154 is pin-to-pin and software compatible with the XR17C158 in case there is ever a need to migrate to the PCI Octal UART.
- The XR17C154 is specifically a PCI Quad UART. The OX16PCI954 is a PCI Quad UART with a parallel port.

1.2 FIRMWARE DIFFERENCES

- The internal registers of the XR17C154 are much simpler than the internal registers of the OX16PCI954. The XR17C154 has a flat sequential register set while the OX16PCI954 has 3 levels of shadow registers. The XR17C154 uses 4 address lines to access the internal registers instead of the traditional 3 address lines therefore eliminating having to deal with shadow registers. The 16C550 Standard Register Set and the Enhanced Register Set can all be accessed from the same location. Note that the XR17C154 has more registers in the Enhanced Register Set than the OX16PCI954 has in its Enhanced Register Set. The OX16PCI954 has a Standard Register Set, Enhanced Register Set, Indexed Control Register Set and Additional Status Register Set. As long as the last value written to LCR was not 0xBF, the Index Control Register (ICR) is accessed by writing the desired address offset for the ICR to the Scratchpad register and then writing to the ICR. Note that this is for writing to the ICR only. To read from ICR, you must write to a bit in one of the Indexed Control Registers to enable reading from the ICR. The Additional Status Registers can only be read when another bit in the Indexed Control Registers is set.
- The XR17C154 has the ability to write to all channels simultaneously (via Device Configuration Register REGB bit-0) for smaller and quicker initialization routines. Once simultaneous write has been enabled for the XR17C154, writing to any channel register will write to the same register of all channels. In the OX16PCI954, it is necessary to initialize each channel individually.
- The XR17C154 can perform DWORD (4 bytes) reads from the RX FIFO therefore unloading up to 4 bytes per read cycle from the RX FIFO. The same concept applies when performing DWORD writes to the TX FIFO. Up to 4 bytes can be loaded per write cycle into the TX FIFO. The OX16PCI954 can only read or write one byte at a time, hence a lower throughput.
- The XR17C154 supports Burst Read and Burst Write PCI bus transactions (refer to PCI Local Bus Specifications Revision 2.2). In Burst Read Mode, the XR17C154 can unload up to 64 bytes from the RX FIFO in a single PCI bus transaction. In Burst Write Mode, the XR17C154 can load up to 64 bytes into the TX FIFO in a single PCI bus transaction. The OX16PCI954 does not support burst read or burst write and any attempt to burst will be terminated with Disconnect with Data. It is only capable of unloading one data byte from the RX FIFO and loading one data byte to the TX FIFO per transaction.
- The XR17C154 has Automatic 1 or 2 character Xon/Xoff Software Flow Control. In the Automatic 1 character Xon/Xoff Software Flow Control, an Xoff will be sent to the remote transmitter when the local RX FIFO reaches the trigger level to halt remote data transmission and an Xon will be sent when the FIFO falls below the the trigger level to resume data transmission. In Automatic 2 character Xon/Xoff Software Flow Control, two Xoff and Xon characters are sent at the appropriate times instead of just a single character. This is to

ensure that the first character is not accidentally interpreted as a software flow control character if it was not meant to be. The Automatic 2 Character Flow Control provides a much more reliable mechanism. The OX16PCI954 only has the Automatic 1 character Xon/Xoff Software Flow Control.

- The XR17C154 has an Automatic RS485 Half-Duplex Control with Turn-Around Delay. RTS# or DTR# output is a logic one while transmitting and becomes a logic zero after a specified delay (programmed into MSR bits 7-4) following the last stop bit of the last character that has been transmitted. This helps in turning around the transceiver to receive the remote stations's response. The delay optimizes the time needed for the last transmission to completely reach the farthest station on a long and heavily loaded cable network before switching off the line driver. This turn-around delay prevents any data loss and inproves polling time. The OX16PCI954 does not have the Turn-Around Delay feature.
- The XR17C154 has 16 selectable levels of RTS Hysteresis ranging from ±4 to ±52. For example if the RX Trigger Level was programmed for 32 bytes and the RTS Hysteresis was selected at ±20, the RTS# pin will not be forced to a logic 1 (RTS off) until the receive FIFO reaches 52 bytes. The RTS# pin will return to a logic 0 (RTS on) after the RX FIFO is unloaded to 12 bytes. The OX16PCI954 has a similar feature. For the OX16PCI954, the software driver has to manually select the upper level to halt transmission and the lower level to resume transmission independent of the RX Trigger Level. It is also up to the software driver to ensure that the upper level is greater than the lower level since the device does not perform that check.
- The OX16PCI954 can be programmed to operate in a wake-up mode for Multidrop applications. This feature is not available in the XR17C154.
- The OX16PCI954 can disable and enable the TX or RX output. This feature is not available in the XR17C154.
- The XR17C154 has a BRG prescaler of 1 or 4. The OX16PCI954 has a Baud Rate Generator Prescaler of 1 to 31.875.
- The XR17C154 has a Data Sampling Rate of 8X or 16X. The OX16PCI954 has a Data Sampling Rate of 4X to 16X.
- The XR17C154 has TX and RX FIFOs of 64 bytes deep and the OX16PCI954 has TX and RX FIFOs of 128 bytes deep.

1.3 REPLACING THE OX16PCI954 WITH THE XR17C154

Replacing the OX16PCI954 with the XR17C154 will require a new design since the XR17C154 comes in a smaller 144-pin TQFP package. The XR17C158 is also available in the 144-pin TQFP package and is pin-to-pin and software compatible with the XR17C154.

The software will need to be updated to take advantage of the enhanced features of the XR17C154 that are not available in or different from the OX16PCI954.

In a nutshell, the XR17C154 has a much simpler internal register set than the OX16PCI954 for faster throughput and easier software development, and has more enhanced features for higher throughput and performance. The XR17C154 is also migratable to the XR17C158 in the same package.

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