# NLAS3158

# Low Voltage Dual SPDT Analog Switch Dual 2:1 Multiplexer

The NLAS3158 is an advanced CMOS analog switch fabricated with silicon gate CMOS technology. It achieves very low propagation delay and $RDS_{ON}$ resistances while maintaining CMOS low power dissipation. Analog and digital voltages that may vary across the full power−supply range (from $V_{CC}$ to GND). This device is a drop in replacement for the PI5A3158.

The select pin has overvoltage protection that allows voltages above $V_{CC}$, up to 7.0 V to be present on the pin without damage or disruption of operation of the part, regardless of the operating voltage.

### Features

- High Speed: $t_{PD}$ = 1.0 ns (Typ) at $V_{CC}$ = 5.0 V
- Low Power Dissipation: $I_{CC}$ = 1.0 μA (Max) at $T_A$ = 25°C
- Standard CMOS Logic Levels
- High Bandwidth, Improved Linearity
- Low $RDS_{ON}$: 8 Ω Max at 3 V
- Break Before Make Circuitry, Prevents Inadvertent Shorts
- This is a Pb−Free Device

### Typical Applications

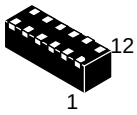
- Switches Standard NTSC/PAL Video, Audio, SPDIF and HDTV
- May be used for Clock Switching, Data MUX'ing, etc.
- Can Switch Balanced Signal Pairs, e.g. LVDS > 200 Mb/s

### Important Information

- Latchup Performance Exceeds 300 mA
- Pin for Pin Drop in for PI5A3158
- TDFN Package, 3x1 mm
- ESD Performance: Human Body Model; > 2000 V;
  Machine Model; > 200 V
- Extended Automotive Temperature Range −55°C to +125°C (See Appendix A)

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**DFN12**
**MN SUFFIX**
**CASE 485AG**

**MARKING DIAGRAM**




AS = Specific Device Code
$\overline{M}$ = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

**FUNCTION TABLE**

| Select Input | Function |
|---|---|
| L | B0 Connected to A |
| H | B1 Connected to A |

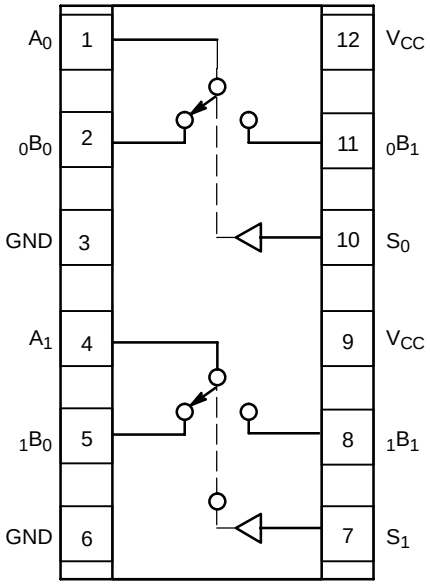



**Figure 1. Pinout** (Top View)

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

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**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.5 to +7.0 | V |
| DC Switch Input Voltage (Note 1) | $V_{IS}$ | −0.5 to $V_{CC}$ + 0.5 | V |
| DC Input Voltage (Note 1) | $V_{IN}$ | −0.5 to + 7.0 | V |
| DC Input Diode Current @ $V_{IN} < 0$ V | $I_{IK}$ | −50 | mA |
| DC Output Current | $I_{OUT}$ | 128 | mA |
| DC $V_{CC}$ or Ground Current | $I_{CC}/I_{GND}$ | +100 | mA |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Junction Temperature Under Bias | $T_J$ | 150 | °C |
| Junction Lead Temperature (Soldering, 10 Seconds) | $T_L$ | 260 | °C |
| Power Dissipation @ +85°C | $P_D$ | 180 | mW |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS** (Note 2)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage Operating | $V_{CC}$ | 1.65 | 5.5 | V |
| Select Input Voltage | $V_{IN}$ | 0 | $V_{CC}$ | V |
| Switch Input Voltage | $V_{IS}$ | 0 | $V_{CC}$ | V |
| Output Voltage | $V_{OUT}$ | 0 | $V_{CC}$ | V |
| Operating Temperature | $T_A$ | −55 | +125 | °C |
| Input Rise and Fall Time<br>Control Input $V_{CC}$ = 2.3 V−3.6 V<br>Control Input $V_{CC}$ = 4.5 V−5.5 V | $t_r$, $t_f$ | <br>0<br>0 | <br>10<br>5.0 | ns/V |
| Thermal Resistance | $\theta_{JA}$ | − | 350 | °C/W |

2. Select input must be held HIGH or LOW, it must not float.

**DC ELECTRICAL CHARACTERISTICS** ($T_A$ = −40°C to +85°C)

| Symbol | Parameter | Test Conditions | $V_{CC}$ (V) | $T_A$ = +25°C | | | $T_A$ = −40°C to +85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IH}$ | HIGH Level Input Voltage | | 1.65−1.95<br>2.3−5.5 | | | | 0.75 $V_{CC}$<br>0.7 $V_{CC}$ | | V |
| $V_{IL}$ | LOW Level Input Voltage | | 1.65−1.95<br>2.3−5.5 | | | | | 0.25 $V_{CC}$<br>0.3 $V_{CC}$ | V |
| $I_{IN}$ | Input Leakage Current | 0 ≤ $V_{IN}$ ≤ 5.5 V | 0−5.5 | | ±0.05 | ±0.1 | | ±1 | μA |
| $I_{OFF}$ | OFF State Leakage Current | 0 ≤ A, B ≤ $V_{CC}$ | 1.65−5.5 | | ±0.05 | ±0.1 | | ±1 | μA |
| $R_{ON}$ | Switch On Resistance (Note 3) | $V_{IN}$ = 0 V, $I_O$ = 30 mA<br>$V_{IN}$ = 2.4 V, $I_O$ = −30 mA<br>$V_{IN}$ = 4.5 V, $I_O$ = −30 mA | 4.5 | | 3.0<br>5.0<br>7.0 | 6.0<br>8.0<br>13 | | 6.0<br>8.0<br>13 | Ω |
| | | $V_{IN}$ = 0 V, $I_O$ = 24 mA<br>$V_{IN}$ = 3 V, $I_O$ = −24 mA | 3.0 | | 4.0<br>10 | 8.0<br>19 | | 8.0<br>19 | Ω |
| | | $V_{IN}$ = 0 V, $I_O$ = 8 mA<br>$V_{IN}$ = 2.3 V, $I_O$ = −8 mA | 2.3 | | 5.0<br>13 | 9.0<br>24 | | 9.0<br>24 | Ω |
| | | $V_{IN}$ = 0 V, $I_O$ = 4 mA<br>$V_{IN}$ = 1.65 V, $I_O$ = −4 mA | 1.65 | | 6.5<br>17 | 12<br>39 | | 12<br>39 | Ω |
| $I_{CC}$ | Quiescent Supply Current<br>All Channels ON or OFF | $V_{IN}$ = $V_{CC}$ or GND<br><br>$I_{OUT}$ = 0 | 5.5 | | | 1.0 | | 10 | μA |
| | Analog Signal Range | | $V_{CC}$ | 0 | | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $R_{RANGE}$ | On Resistance Over Signal Range (Note 3) (Note 7) | $I_A$ = −30 mA, 0 ≤ $V_{Bn}$ ≤ $V_{CC}$<br>$I_A$ = −24 mA, 0 ≤ $V_{Bn}$ ≤ $V_{CC}$<br>$I_A$ = −8 mA, 0 ≤ $V_{Bn}$ ≤ $V_{CC}$<br>$I_A$ = −4 mA, 0 ≤ $V_{Bn}$ ≤ $V_{CC}$ | 4.5<br>3.0<br>2.3<br>1.65 | | | | | 25<br>50<br>100<br>300 | Ω |
| $\Delta R_{ON}$ | On Resistance Match Between Channels (Note 3) (Note 4) (Note 5) | $I_A$ = −30 mA, $V_{Bn}$ = 3.15<br>$I_A$ = −24 mA, $V_{Bn}$ = 2.1<br>$I_A$ = −8 mA, $V_{Bn}$ = 1.6<br>$I_A$ = −4 mA, $V_{Bn}$ = 1.15 | 4.5<br>3.0<br>2.3<br>1.65 | | 0.15<br>0.2<br>0.5<br>0.5 | | | | Ω |
| $R_{flat}$ | On Resistance Flatness (Note 3) (Note 4) (Note 6) | $I_A$ = −30 mA, 0 ≤ $V_{Bn}$ ≤ $V_{CC}$<br>$I_A$ = −24 mA, 0 ≤ $V_{Bn}$ ≤ $V_{CC}$<br>$I_A$ = −8 mA, 0 ≤ $V_{Bn}$ ≤ $V_{CC}$<br>$I_A$ = −4 mA, 0 ≤ $V_{Bn}$ ≤ $V_{CC}$ | 5.0<br>3.3<br>2.5<br>1.8 | | 5.0<br>10<br>24<br>110 | | | | Ω |

3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).
4. Parameter is characterized but not tested in production.
5. $\Delta R_{ON}$ = $R_{ON}$ max − $R_{ON}$ min measured at identical $V_{CC}$, temperature and voltage levels.
6. Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.
7. Guaranteed by Design.

**AC ELECTRICAL CHARACTERISTICS** ($T_A$ = −40°C to +85°C)

| Symbol | Parameter | Test Conditions | $V_{CC}$ (V) | $T_A$ = +25°C | | | $T_A$ = −40°C to +85°C | | Unit | Figure Number |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | | |
| $t_{PHL}$<br>$t_{PLH}$ | Propagation Delay Bus to Bus (Note 9) | $V_I$ = OPEN | 1.65−1.95<br>2.3−2.7<br>3.0−3.6<br>4.5−5.5 | | | <br>1.2<br>0.8<br>0.3 | | | ns | Figures 2, 3 |
| $t_{PZL}$<br>$t_{PZH}$ | Output Enable Time Turn On Time (A to $B_n$) | $V_I$ = 2 × $V_{CC}$ for $t_{PZL}$<br>$V_I$ = 0 V for $t_{PZH}$ | 1.65−1.95<br>2.3−2.7<br>3.0−3.6<br>4.5−5.5 | | | 23<br>13<br>6.9<br>5.2 | 7.0<br>3.5<br>2.5<br>1.7 | 24<br>14<br>7.6<br>5.7 | ns | Figures 2, 3 |
| $t_{PLZ}$<br>$t_{PHZ}$ | Output Disable Time Turn Off Time (A Port to B Port) | $V_I$ = 2 × $V_{CC}$ for $t_{PLZ}$<br>$V_I$ = 0 V for $t_{PHZ}$ | 1.65−1.95<br>2.3−2.7<br>3.0−3.6<br>4.5−5.5 | | | 12.5<br>7.0<br>5.0<br>3.5 | 3.0<br>2.0<br>1.5<br>0.8 | 13<br>7.5<br>5.3<br>3.8 | ns | Figures 2, 3 |
| $t_{BBM}$ | Break Before Make Time (Note 8) | $R_L$ = 50 Ω<br>$C_L$ = 35 pF | 1.65−1.95<br>2.3−2.7<br>3.0−3.6<br>4.5−5.5 | 0.5<br>0.5<br>0.5<br>0.5 | | | 0.5<br>0.5<br>0.5<br>0.5 | | ns | Figure 4 |
| Q | Charge Injection (Note 8) | $C_L$ = 0.1 nF, $V_{GEN}$ = 0 V<br>$R_{GEN}$ = 0 Ω | 5.0<br>3.3 | | 7.0<br>3.0 | | | | pC | Figure 5 |
| OIRR | Off Isolation (Note 10) NO | $R_L$ = 50 Ω<br>f = 10 MHz | 1.65−5.5 | | −55 | | | | dB | Figures 6, 16 |
| OIRR | Off Isolation (Note 10) NC | $R_L$ = 50 Ω<br>f = 10 MHz | 1.65−5.5 | | −48 | | | | dB | Figures 6, 16 |
| Xtalk | Crosstalk | $R_L$ = 50 Ω<br>f = 10 MHz | 1.65−5.5 | | −54 | | | | dB | Figure 7 |
| BW | −3 dB Bandwidth | $R_L$ = 50 Ω | 2.5−5.5 | | 250 | | | | MHz | Figures 10, 15 |
| THD | Total Harmonic Distortion (Note 8) | $R_L$ = 600 Ω<br>0.5 $V_{P-P}$<br>f = 600 Hz to 20 kHz | 2.5<br>5.0 | | 0.014<br>0.004 | | | | % | Figure 11 |

**CAPACITANCE** (Note 11)

| Symbol | Parameter | Test Conditions | Typ | Max | Unit | Figure Number |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Select Pin Input Capacitance | $V_{CC}$ = 0 V | 2.3 | | pF | |
| $C_{IO-B}$ | B Port Off Capacitance | $V_{CC}$ = 5.0 V | 6.5 | | pF | Figure 8 |
| $C_{IOA-ON}$ | A Port Capacitance when Switch is Enabled | $V_{CC}$ = 5.0 V | 18.5 | | pF | Figure 9 |

8. Guaranteed by Design.
9. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 35 pF load capacitance, when driven by an ideal voltage source (zero output impedance).
10. Off Isolation = 20 $\log_{10}$ [$V_A$/$V_{Bn}$].
11. $T_A$ = +25°C, f = 1 MHz, Capacitance is characterized but not tested in production.

## APPENDIX A

**DC ELECTRICAL EXTENDED AUTOMOTIVE TEMPERATURE RANGE CHARACTERISTICS** (Note 14)

| Symbol | Parameter | Test Conditions | $V_{CC}$ (V) | $T_A$ = +25°C | | | $T_A$ = −55°C to +125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IH}$ | HIGH Level Input Voltage | | 1.65−1.95<br>2.3−5.5 | | | | 0.75 $V_{CC}$<br>0.7 $V_{CC}$ | | V |
| $V_{IL}$ | LOW Level Input Voltage | | 1.65−1.95<br>2.3−5.5 | | | | | 0.25 $V_{CC}$<br>0.3 $V_{CC}$ | V |
| $I_{IN}$ | Input Leakage Current | 0 ≤ $V_{IN}$ ≤ 5.5 V | 0−5.5 | | ±0.05 | ±0.1 | | ±1 | μA |
| $I_{OFF}$ | OFF State Leakage Current | 0 ≤ A, B ≤ $V_{CC}$ | 1.65−5.5 | | ±0.05 | ±0.1 | | ±1 | μA |
| $R_{ON}$ | Switch On Resistance (Note 12) | $V_{IN}$ = 0 V, $I_O$ = 30 mA<br>$V_{IN}$ = 2.4 V, $I_O$ = −30 mA<br>$V_{IN}$ = 4.5 V, $I_O$ = −30 mA | 4.5 | | 3.0<br>5.0<br>7.0 | | | 8.5<br>13.0<br>15.0 | Ω |
| | | $V_{IN}$ = 0 V, $I_O$ = 24 mA<br>$V_{IN}$ = 3 V, $I_O$ = −24 mA | 3.0 | | 4.0<br>10 | | | 11<br>20 | |
| | | $V_{IN}$ = 0 V, $I_O$ = 8 mA<br>$V_{IN}$ = 2.3 V, $I_O$ = −8 mA | 2.3 | | 5.0<br>13 | | | 12<br>30 | |
| | | $V_{IN}$ = 0 V, $I_O$ = 4 mA<br>$V_{IN}$ = 1.65 V, $I_O$ = −4 mA | 1.65 | | 6.5<br>17 | | | 20<br>50 | |
| $I_{CC}$ | Quiescent Supply Current<br>All Channels ON or OFF | $V_{IN}$ = $V_{CC}$ or GND<br><br>$I_{OUT}$ = 0 | 5.5 | | | 1.0 | | 10 | μA |
| | Analog Signal Range | | $V_{CC}$ | 0 | | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $R_{RANGE}$ | On Resistance Over Signal Range (Note 12) (Note 13) | $I_A$ = −30 mA, 0 ≤ $V_{Bn}$ ≤ $V_{CC}$<br>$I_A$ = −24 mA, 0 ≤ $V_{Bn}$ ≤ $V_{CC}$<br>$I_A$ = −8 mA, 0 ≤ $V_{Bn}$ ≤ $V_{CC}$<br>$I_A$ = −4 mA, 0 ≤ $V_{Bn}$ ≤ $V_{CC}$ | 4.5<br>3.0<br>2.3<br>1.65 | | | | | 25<br>50<br>100<br>300 | Ω |

12. Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).
13. Guaranteed by Design.
14. For $\Delta R_{ON}$, $R_{FLAT}$ see −40°C to +85°C section.

## APPENDIX A

### AC ELECTRICAL EXTENDED AUTOMOTIVE TEMPERATURE RANGE CHARACTERISTICS

| Symbol | Parameter | Test Conditions | $V_{CC}$ (V) | $T_A$ = +25°C | | | $T_A$ = −55°C to +125°C | | Unit | Figure Number |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | | |
| $t_{PHL}$<br>$t_{PLH}$ | Propagation Delay<br>Bus to Bus (Note 16) | $V_I$ = OPEN | 1.65−1.95<br>2.3−2.7<br>3.0−3.6<br>4.5−5.5 | | | | | <br>1.2<br>0.8<br>0.3 | ns | Figures<br>2, 3 |
| $t_{PZL}$<br>$t_{PZH}$ | Output Enable Time<br>Turn On Time<br>(A to $B_n$) | $V_I$ = 2 × $V_{CC}$ for $t_{PZL}$<br>$V_I$ = 0 V for $t_{PZH}$ | 1.65−1.95<br>2.3−2.7<br>3.0−3.6<br>4.5−5.5 | | | 23<br>13<br>6.9<br>5.2 | 7.0<br>3.5<br>2.5<br>1.7 | 24<br>14<br>9.0<br>7.0 | ns | Figures<br>2, 3 |
| $t_{PLZ}$<br>$t_{PHZ}$ | Output Disable Time<br>Turn Off Time<br>(A Port to B Port) | $V_I$ = 2 × $V_{CC}$ for $t_{PLZ}$<br>$V_I$ = 0 V for $t_{PHZ}$ | 1.65−1.95<br>2.3−2.7<br>3.0−3.6<br>4.5−5.5 | | | 12.5<br>7.0<br>5.0<br>3.5 | 3.0<br>2.0<br>1.5<br>0.8 | 13<br>7.5<br>6.5<br>5.0 | ns | Figures<br>2, 3 |
| $t_{B-M}$ | Break Before Make Time (Note 15) | | 1.65−1.95<br>2.3−2.7<br>3.0−3.6<br>4.5−5.5 | | | | 0.5<br>0.5<br>0.5<br>0.5 | | ns | Figure 4 |

15. Guaranteed by Design.
16. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

## AC LOADING AND WAVEFORMS

NOTE: Input driven by 50 Ω source terminated in 50 Ω
NOTE: $C_L$ includes load and stray capacitance
NOTE: Input PRR = 1.0 MHz; $t_W$ = 500 ns

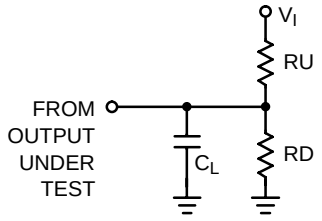



**Figure 2. AC Test Circuit**

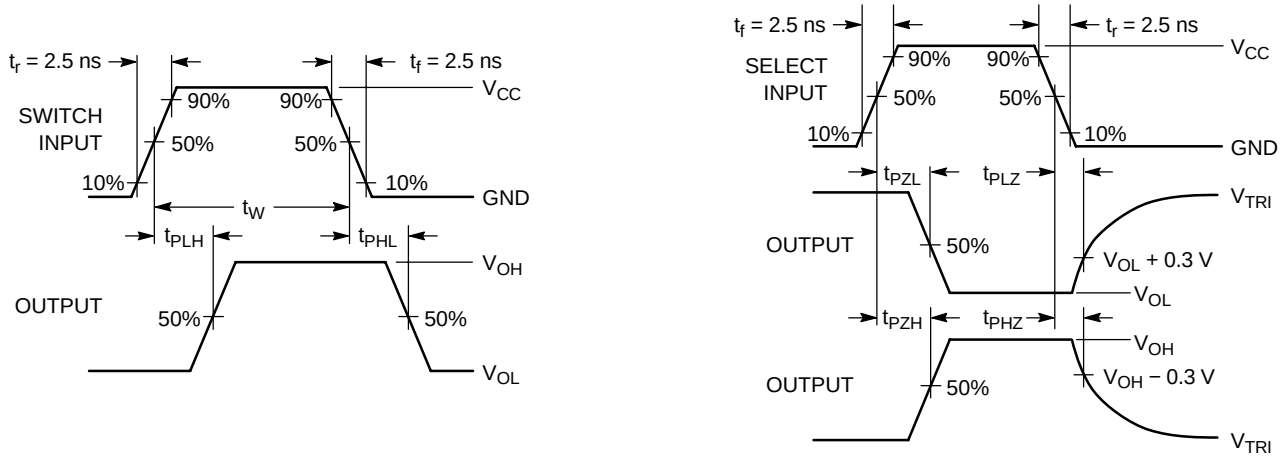



**Figure 3. AC Waveforms**




**Figure 4. Break Before Make Interval Timing**

## AC LOADING AND WAVEFORMS

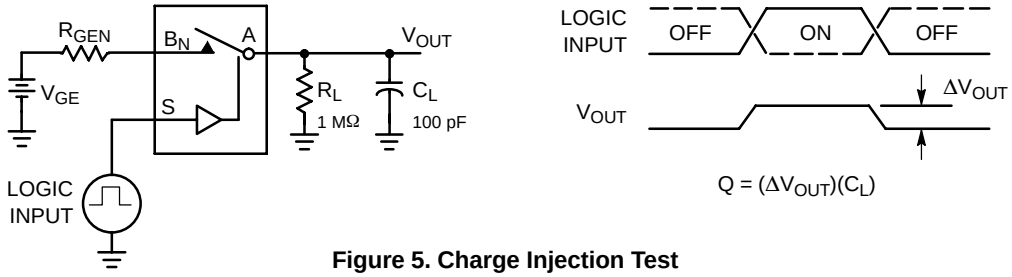



**Figure 5. Charge Injection Test**

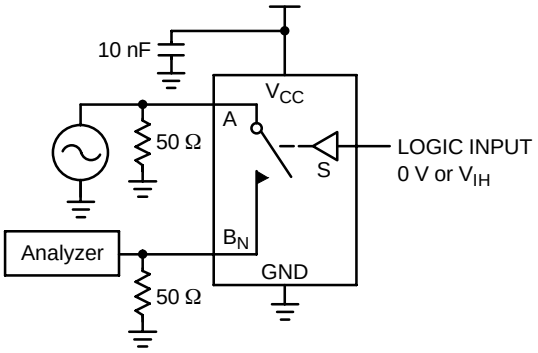



**Figure 6. Off Isolation**

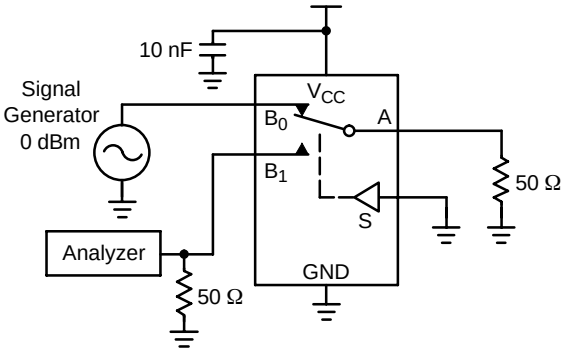



**Figure 7. Crosstalk**

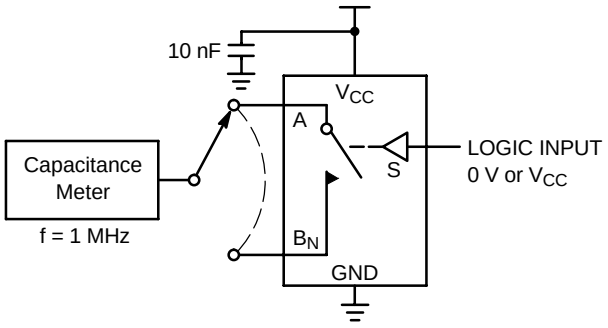



**Figure 8. Channel Off Capacitance**

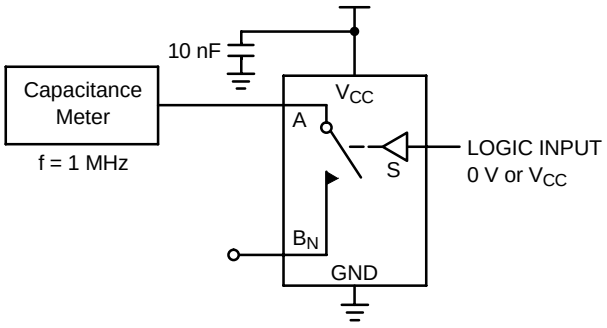



**Figure 9. Channel On Capacitance**

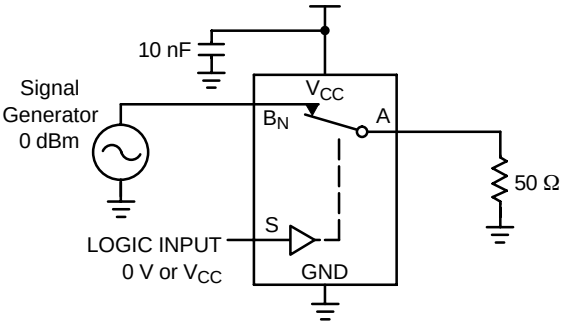



**Figure 10. Bandwidth**

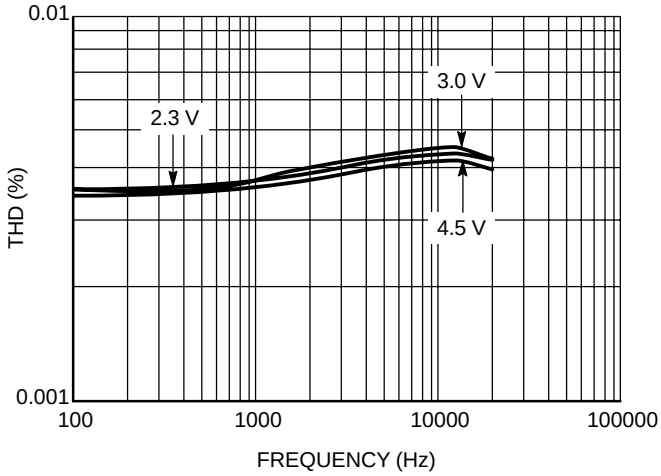



**Figure 11. Total Harmonic Distortion vs. Frequency**

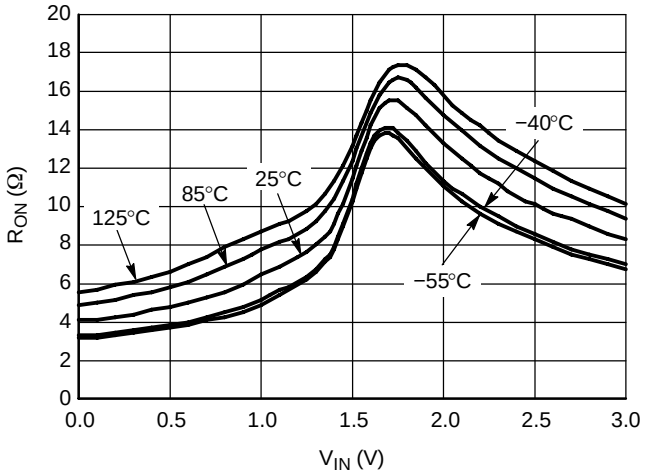



**Figure 12. $R_{ON}$ vs. $V_{IN}$ vs. Temperature @ $V_{CC}$ = 3.0 V**

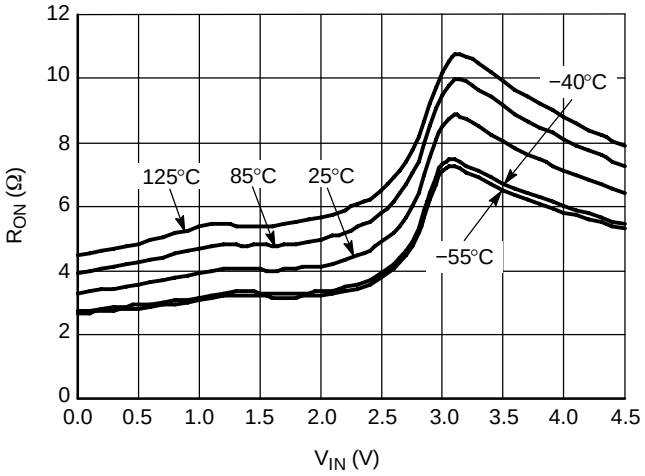



**Figure 13. $R_{ON}$ vs. $V_{IN}$ vs. Temperature @ $V_{CC}$ = 4.5 V**

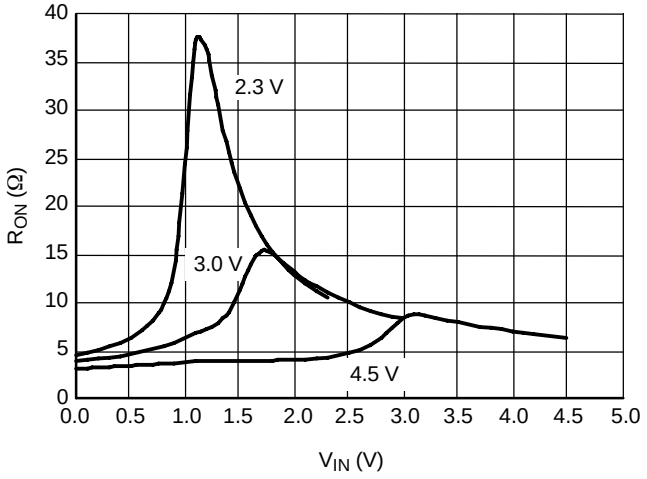



**Figure 14. On−Resistance vs. Input Voltage**

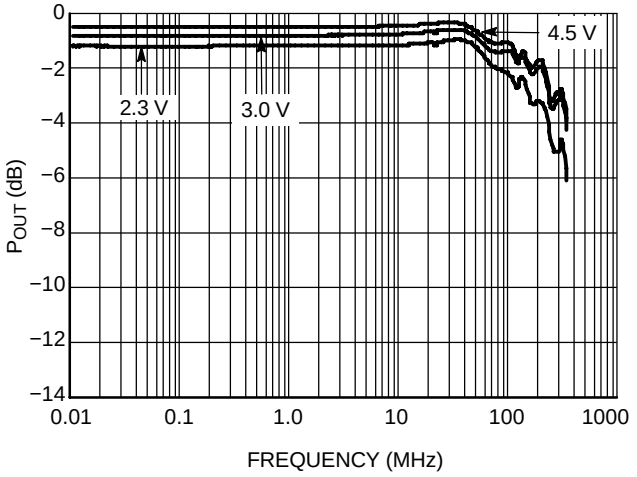



**Figure 15. Bandwidth vs. Frequency**

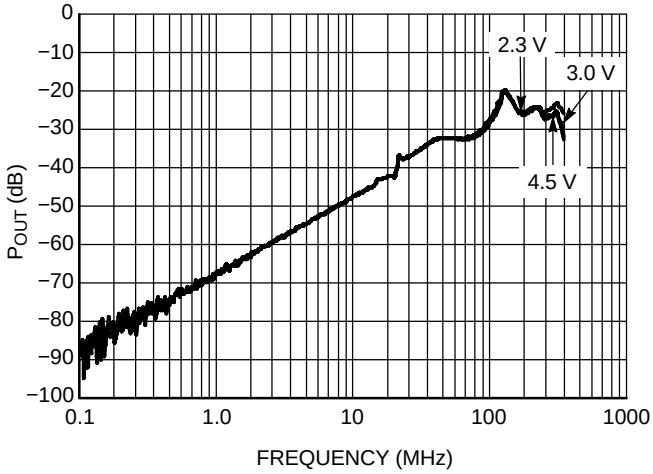



**Figure 16. Off−Isolation vs. Frequency**

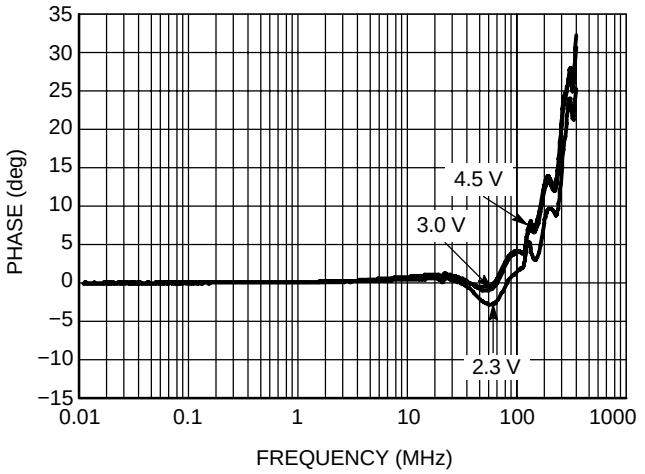



**Figure 17. Phase Angle vs. Frequency**

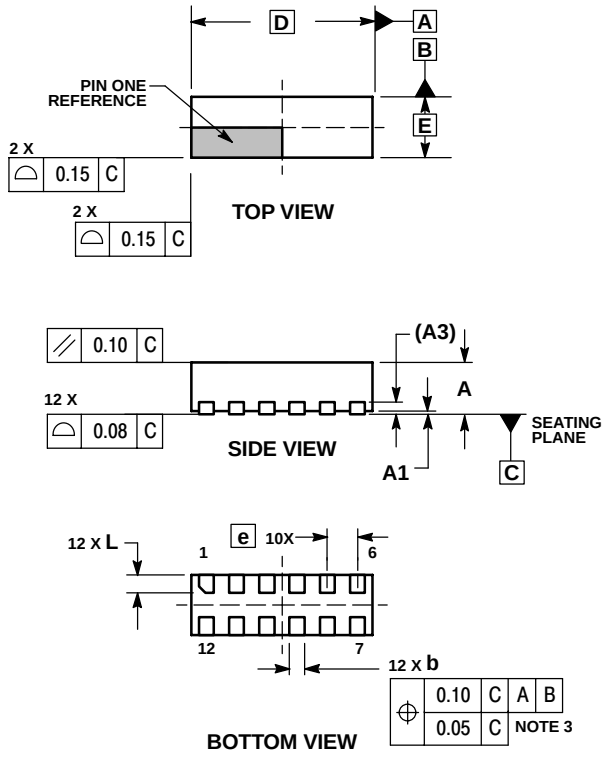
## DEVICE ORDERING INFORMATION

| Device Order Number | Device Nomenclature | | | | | Package Type | Tape & Reel Size† |
|---|---|---|---|---|---|---|---|
| | Circuit Indicator | Technology | Device Function | Package Suffix | Tape & Reel Suffix | | |
| NLAS3158MNR2G | NL | AS | 3158 | MN | R2 | QFN (Pb−Free) | 3000 Unit / Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

**DFN12 3.0*1.0*0.8 MM**
CASE 485AG−01
ISSUE O




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION b APPLIES TO TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.70 | 0.90 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.18 | 0.30 |
| D | 3.00 BSC | |
| E | 1.00 BSC | |
| e | 0.50 BSC | |
| L | 0.20 | 0.40 |

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