LM3556 1.5-A Synchronous Boost LED Flash Driver With High-Side Current Source

1 Features

- Grounded Cathode LED Operation for Improved Thermal Management
- 1.5-A High-Side Current Source for Single LED
- Accurate and Programmable LED Current from 46.9 mA to 1.5 A
- > 85% Efficiency in Torch Mode (at 100 mA) and Flash Mode (at 1 A to 1.5 A)
- Small Solution Size: < 20 mm^2
- LED Thermal Sensing and Current Scale-Back
- Soft-Start Operation for Battery Protection
- Hardware Enable Pin
- Hardware Torch Enable
- Hardware Strobe Enable
- Synchronization Input for RF Power Amplifier Pulse Events
- V_{IN} Flash Monitor Optimization
- 400-kHz I^2C-Compatible Interface
- I^2C-Compatible Programmable NTC Trip Point
- 0.4-mm Pitch, 16-Pin DSBGA Package

2 Applications

Camera Phone LED Flash

3 Description

The LM3556 is a 4-MHz fixed-frequency synchronous boost converter plus 1.5-A constant current driver for a high-current white LED. The high-side current source allows for grounded cathode LED operation providing flash current up to 1.5 A. An adaptive regulation method ensures the current source remains in regulation and maximizes efficiency.

The LM3556 is controlled via an I^2C-compatible interface. Features include: a hardware flash enable (STROBE) allowing a logic input to trigger the flash pulse, a hardware torch enable (TORCH) for Movie Mode or flashlight functions, a TX input which forces the flash pulse into a low-current Torch Mode allowing for synchronization to RF power amplifier events or other high-current conditions, and an integrated comparator designed to monitor an NTC thermistor and provide an interrupt to the LED current. With a fast 1-µs transition from 0 mA to 46.9 mA, the TORCH input pin can be used to develop custom LED current waveforms.

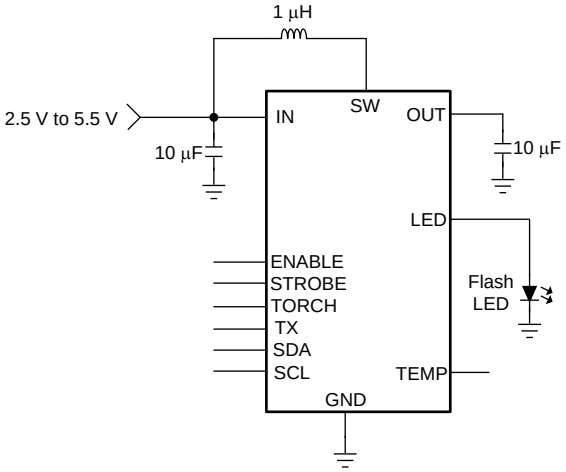
The 4-MHz switching frequency, overvoltage protection and adjustable current limit allow for the use of tiny, low-profile inductors and 10-µF ceramic capacitors. The device is operates over a −40°C to +85°C temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (MAX)
LM3556	DSBGA (16)	1.69 mm × 1.64 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

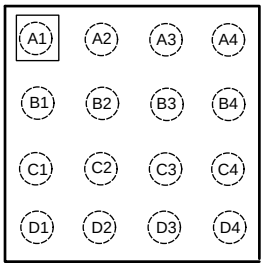
Changes from Revision C (April 2013) to Revision D **Page**

- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Rating* table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1

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5 Pin Configuration And Functions

YFQ Package
16-Pin DSBGA
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
A1, B1	LED	Power	High-side current source output for flash LED. Both pins must be connected for proper operation.
B2, A2	OUT	Power	Step-up DC-DC converter output. Connect a 10-µF ceramic capacitor between this pin and GND.
B3, A3	SW	Power	Drain connection for internal NMOS and synchronous PMOS switches.
A4, B4	GND	Ground	Ground
C1	TEMP	Power	Threshold detector for LED temperature sensing and current scale back.
C2	TORCH	Power	Active high hardware torch enable. Drive TORCH high to turn on Torch or Movie mode. Used for external PWM Mode. Has an internal pulldown resistor of 300 kΩ between TORCH and GND.
C3	STROBE	I/O	Active high hardware flash enable. Drive STROBE high to turn on flash pulse. STROBE overrides TORCH. Has an internal pulldown resistor of 300 kΩ between STROBE and GND.
C4	IN	Input	Input voltage connection. Connect IN to the input supply, and bypass to GND with a 10-µF or larger ceramic capacitor.
D1	TX	I/O	Configurable dual polarity power amplifier synchronization input. Has an internal pulldown resistor of 300 kΩ between TX and GND.
D2	SDA	I/O	Serial data input/output.
D3	SCL	Input	Serial clock input.
D4	ENABLE	Power	Active high enable pin. High = standby, low = shutdown/reset. There is no internal pulldown resistor on this pin.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

	MIN	MAX	UNIT
V_{IN}, V_{SW} ,V_{OUT}	–0.3	6	V
V_{SCL}, V_{SDA}, V_{ENABLE}, V_{STROBE}, V_{TX}, V_{TORCH}, V_{LED}, V_{TEMP}	−0.3 V to the lesser of (V_{IN} + 0.3 V) w/ 6 V maximum		
Continuous power dissipation(3)	Internally limited		
Junction temperature, T_{J-MAX}		150	°C
Maximum lead temperature (soldering)	See(4)		°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typical) and disengages at T_J = 135°C (typical). Thermal shutdown is ensured by design.
(4) For detailed soldering specifications and information, refer to Texas Instruments Application Note 1112: *DSBGA Wafer Level chip Scale Package* (SNVA009).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	NOM	MAX	UNIT
V_{IN}	2.5		5.5	V
Junction temperature, T_J	−40		125	°C
Ambient temperature, T_A(2)	−40		85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.

6.4 Thermal Information

THERMAL METRIC(1)		LM3556 YFQ (DSBGA) 16 PINS	UNIT
$R_{\theta JA}$(2)	Junction-to-ambient thermal resistance	60	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Junction-to-ambient thermal resistance ($R_{\theta JA}$) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 102 mm × 76 mm × 1.6 mm with a 2 × 1 array of thermal vias. The ground plane on the board is 50 mm × 50 mm. Thickness of copper layers are 36 µm/18 µm/18 µm/36 µm (1.5 oz/1 oz/1 oz/1.5 oz). Ambient temperature in simulation is 22°C, still air. Power dissipation is 1 W.

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6.5 Electrical Characteristics

Unless otherwise specified, V_{IN} = 3.6 V, typical limits apply for T_A = 25°C, and minimum (MIN) and maximum (MAX) limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ +85°C).(1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT SOURCE SPECIFICATIONS							
I_{LED}	Current source accuracy	1.5-A Flash, V_{OUT} = 4 V		1.425 (–5%)	1.5	1.575 (+5%)	A
		46.88-mA Torch, V_{OUT} = 3.6 V		42.3 (−10%)	47	51.7 (+10%)	mA
V_{HR}	Current source regulation voltage	I_{LED} = 1.5 A	Flash		250	280 (+12%)	mV
		I_{LED} = 46.88 mA	Torch		150	172.5 (+15%)	
V_{OVP}	Output overvoltage protection trip point	ON Threshold		4.86	5	5.1	V
		OFF Threshold		4.75	4.88	4.99	
STEP-UP DC-DC CONVERTER SPECIFICATIONS							
R_{PMOS}	PMOS switch on-resistance	I_{PMOS} = 1 A			85		mΩ
R_{NMOS}	NMOS switch on-resistance	I_{NMOS} = 1 A			65		
I_{CL}	Switch current limit			−12%	1.7	12%	A
				−12%	1.9	12%	
				−10%	2.5	10%	
				−12%	3.1	12%	
V_{TRIP}	NTC comparator trip threshold	Configuration Register, bit [1] = 1		−6%	600	6%	mV
UVLO	Undervoltage lockout threshold	Falling V_{IN}		2.74	2.8	2.85	V
I_{NTC}	NTC current			−6%	75	6%	µA
V_{IVFM}	Input voltage flash monitor trip threshold			–3.2%	2.9	3.2%	V
f_{SW}	Switching frequency	2.5 V ≤ V_{IN} ≤ 5.5 V		3.72	4	4.28	MHz
I_Q	Quiescent supply current	Device not switching Pass Mode			0.6	0.75	mA
I_{SD}	Shutdown supply current	Device disabled, EN = 0V 2.5 V ≤ V_{IN} ≤ 5.5 V			0.1	1.3	µA
I_{SB}	Standby supply current	Device disabled, EN = 2 V 2.5 V ≤ V_{IN} ≤ 5.5 V			2.5	4	µA
t_{TX}	Flash-to-torch LED current settling time	TX low to high, I_{LED} = 1.5 A to 46.88 mA			4		µs
I_{OS}	I_{LED} overshoot in external indicator mode	0 mA to I_{TORCH}			8%		
ENABLE, STROBE, TORCH, TX VOLTAGE SPECIFICATIONS							
V_{IL}	Input logic low	2.5 V ≤ V_{IN} ≤ 5.5 V		0		0.4	V
V_{IH}	Input logic high			1.2		V_{IN}	
I^2C-COMPATIBLE INTERFACE SPECIFICATIONS (SCL, SDA)							
V_{IL}	Input logic low	2.5 V ≤ V_{IN} ≤ 4.2 V		0		0.4	V
V_{IH}	Input logic high			1.2		V_{IN}	
V_{OL}	Output logic low	I_{LOAD} = 3 mA				400	mV

(1) Minimum and maximum limits are specified by design, test, or statistical analysis. Typical numbers are not verified, but do represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: V_{IN} = 3.6 V and T_A = 25°C.
(2) All voltages are with respect to the potential at the GND pin.

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6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
t_1	SCL clock frequency	2.4			µs
t_2	Data in setup time to SCL high	100			ns
t_3	Data out stable after SCL low	0			ns
t_4	SDA low setup time to SCL low (start)	100			ns
t_5	SDA high hold time after SCL high (stop)	100			ns

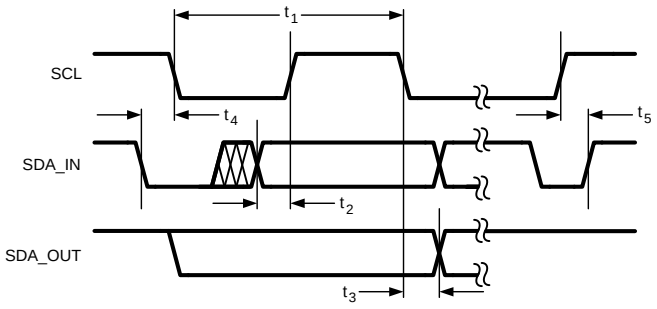
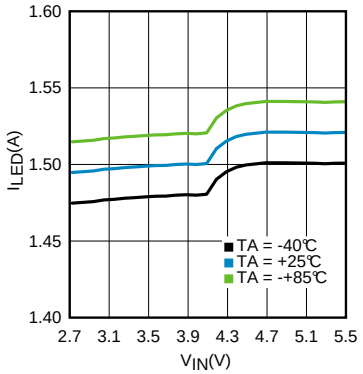


Figure 1. I²C-Compatible Timing Diagram

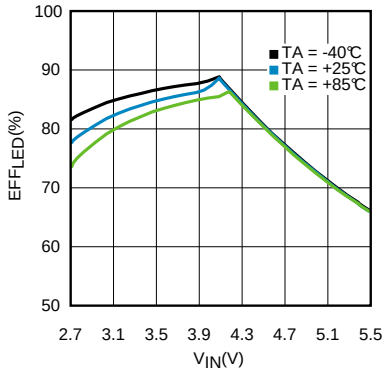
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6.7 Typical Characteristics



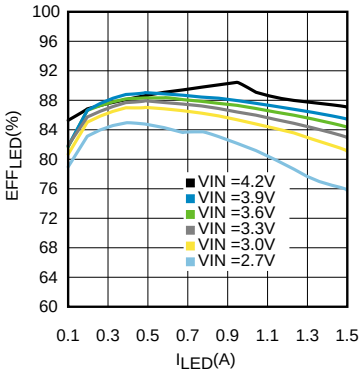
V_{LED} = 3.6 V I_{LED} = 1.5 A

Figure 2. Flash LED Current vs V_{IN}



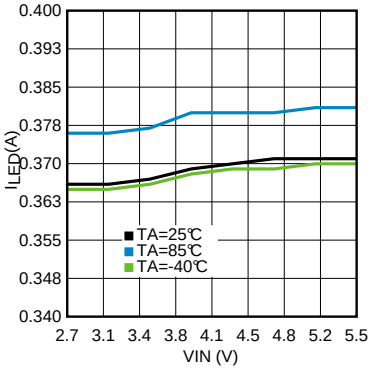
V_{LED} = 3.6 V I_{LED} = 1.5 A

Figure 3. Flash LED Efficiency vs V_{IN}



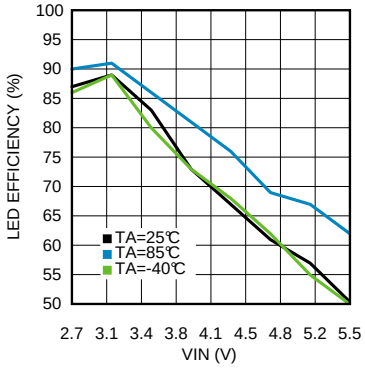
V_{LED} = 3.8 V

Figure 4. Flash LED Efficiency vs Flash LED Current



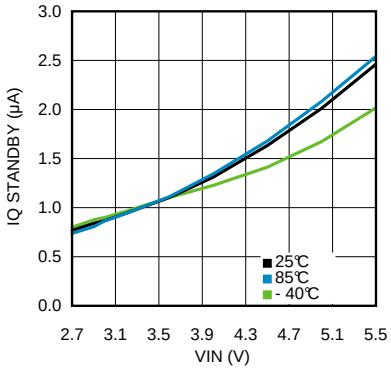
V_{LED} = 3 V I_{LED} = 375 mA

Figure 5. Torch LED Current vs V_{IN}



V_{LED} = 3 V

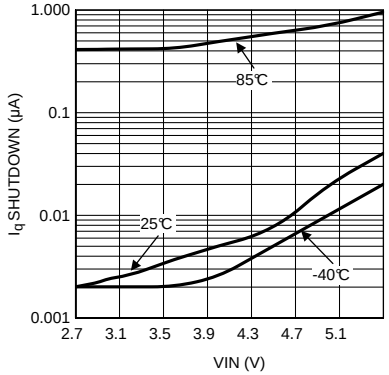
Figure 6. Torch LED Efficiency vs V_{IN}



EN = 1.8 V

Figure 7. I_Q Standby vs V_{IN}

Typical Characteristics (continued)



EN = 0 V

Figure 8. I_Q Shutdown vs V_{IN}

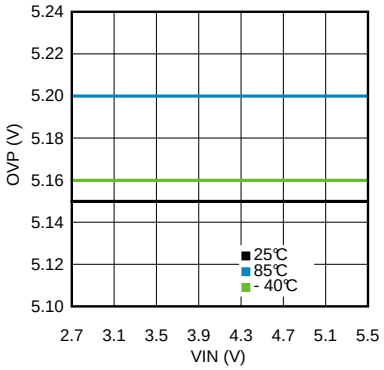


Figure 9. Variation of OVP With V_{IN}

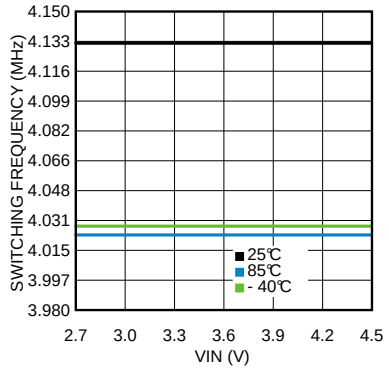
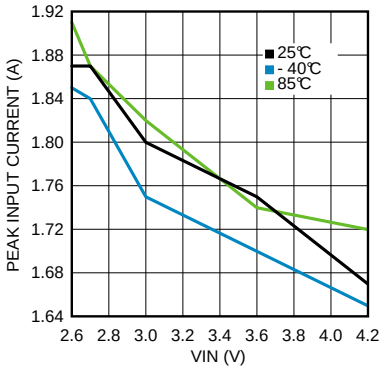
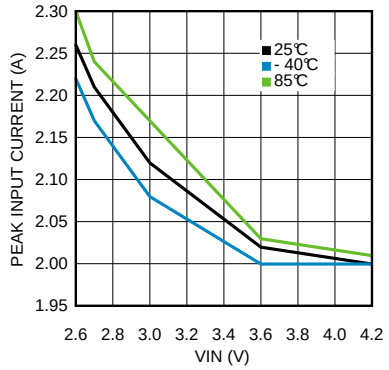


Figure 10. Frequency With V_{IN} and Over Temperature



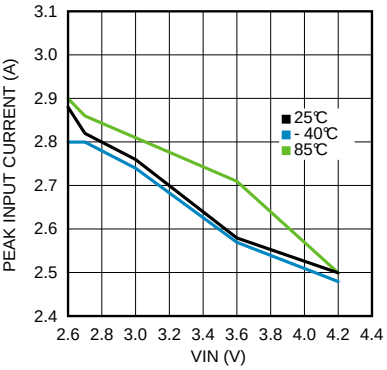
Current Limit = 1.7 A

Figure 11. Input Current Limit Over Temperature and V_{IN}



Current Limit = 1.9 A

Figure 12. Input Current Limit Over Temperature and V_{IN}

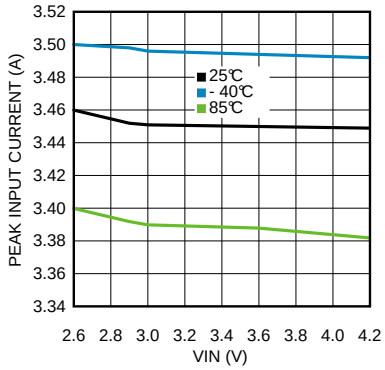


Current Limit = 2.5 A

Figure 13. Input Current Limit Over Temperature and V_{IN}

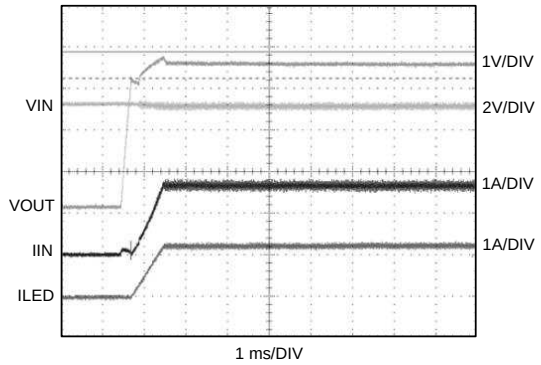
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Typical Characteristics (continued)



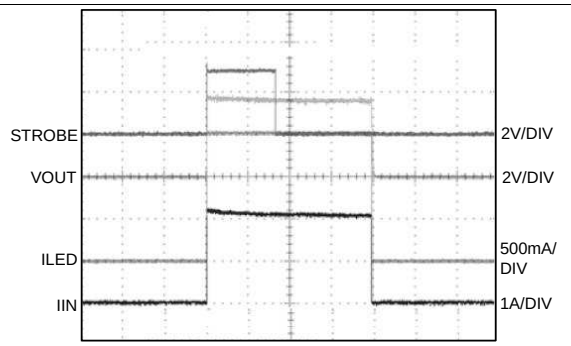
Current Limit = 3.1 A

Figure 14. Input Current Limit Over Temperature and V_{IN}



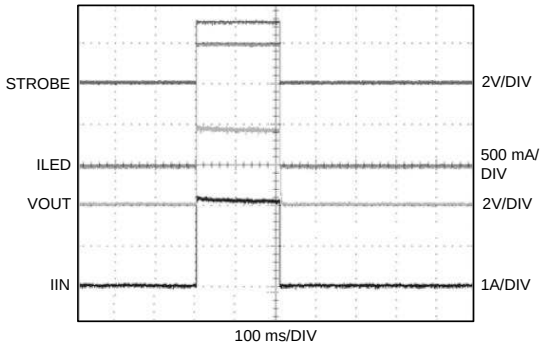
Current Limit = 1.7 A

Figure 15. Start-Up Plot With Part In Boost Mode Current Limit



400 ms

Figure 16. Strobe With Edge-Triggered Signal



400 ms

Figure 17. Strobe With Level-Triggered Signal

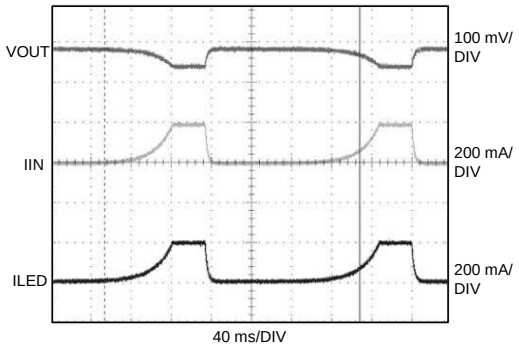


Figure 18. Internal Indicator Operation

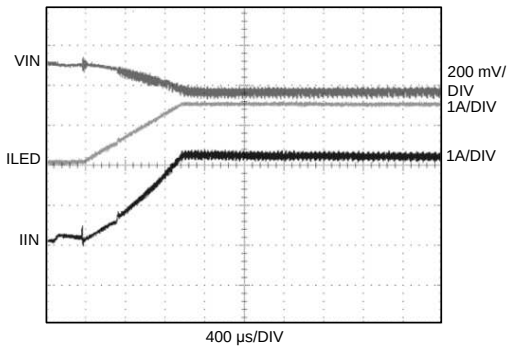


Figure 19. Input Voltage Flash Monitor Report Mode With Default Settings

Typical Characteristics (continued)

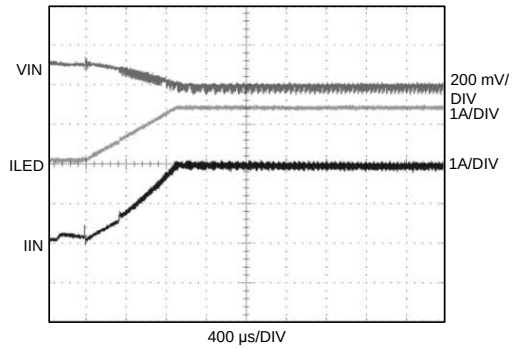


Figure 20. Input Voltage Flash Monitor Stop and Hold Mode With Default Settings

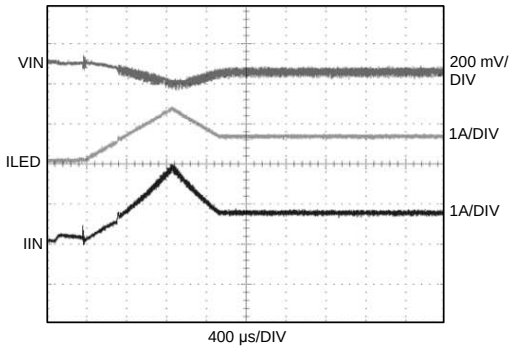


Figure 21. Input Voltage Flash Monitor Down Mode With Default Settings

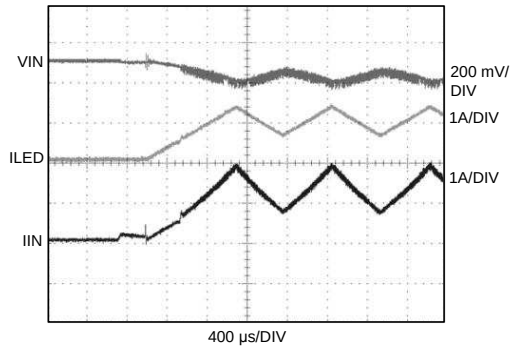
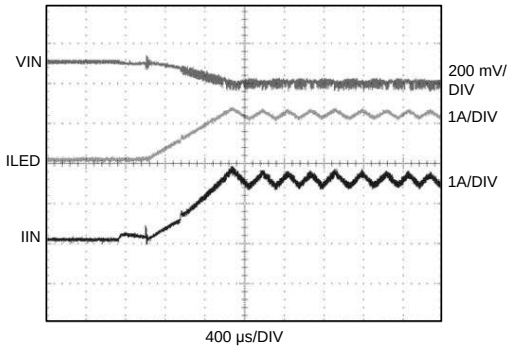
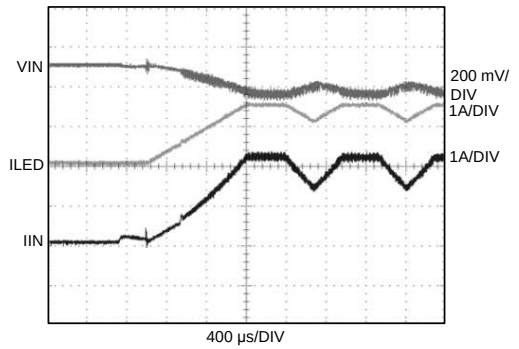


Figure 22. Input Voltage Flash Monitor Up and Down Mode With Default Settings



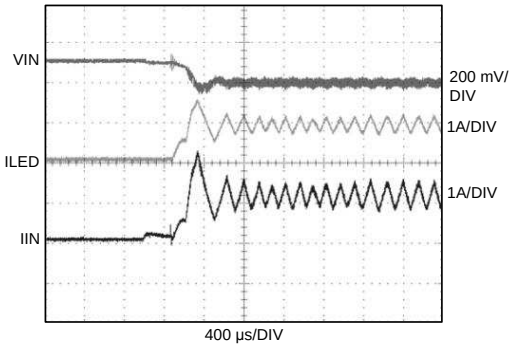
0-mV Hysteresis 1/2 Step Filter Time

Figure 23. Input Voltage Flash Monitor, Up and Down Mode



0-mV Hysteresis 512-ms Filter Time

Figure 24. Input Voltage Flash Monitor, Up and Down Mode



256-µs Flash Ramp 1/2 Step Filter Time

Figure 25. Input Voltage Flash Monitor, Up and Down Mode

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Typical Characteristics (continued)

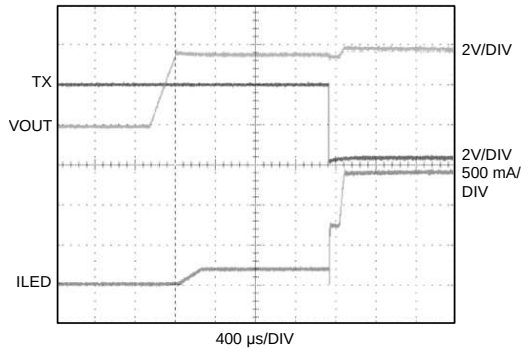


Figure 26. Impact on LED Current With a TX Event

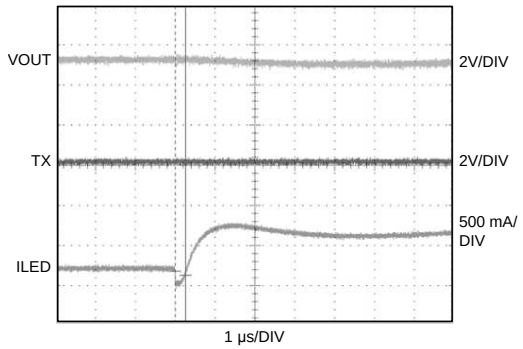


Figure 27. Time Taken for LM3556 to Ramp from Torch to Flash After TX Event

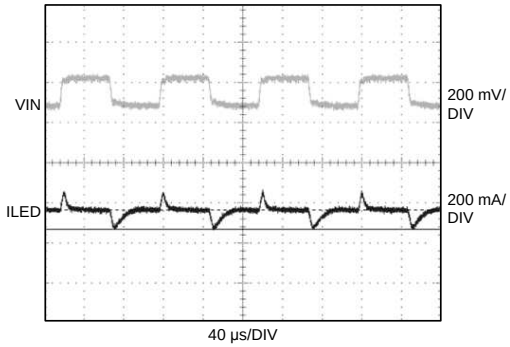


Figure 28. Transient Plot When V_{IN} Stepped from 3 → 2.9 V

7 Detailed Description

7.1 Overview

The LM3556 is a high-power white LED flash driver capable of delivering up to 1.5 A into a single high-powered LED. The device incorporates a 4-MHz constant-frequency synchronous current-mode PWM boost converter, and a single high-side current source to regulate the LED current over the 2.5-V to 5.5-V input voltage range.

The LM3556 PWM converter switches and maintains at least V_{HR} across the current source (LED). This minimum headroom voltage ensures that the current source remains in regulation. If the input voltage is above the LED voltage plus current source headroom voltage, the device does not switch, and turns the PFET on continuously (Pass Mode). In Pass Mode the difference between (V_{IN} − I_{LED} × R_{PMOS}) and the voltage across the LED is dropped across the current source.

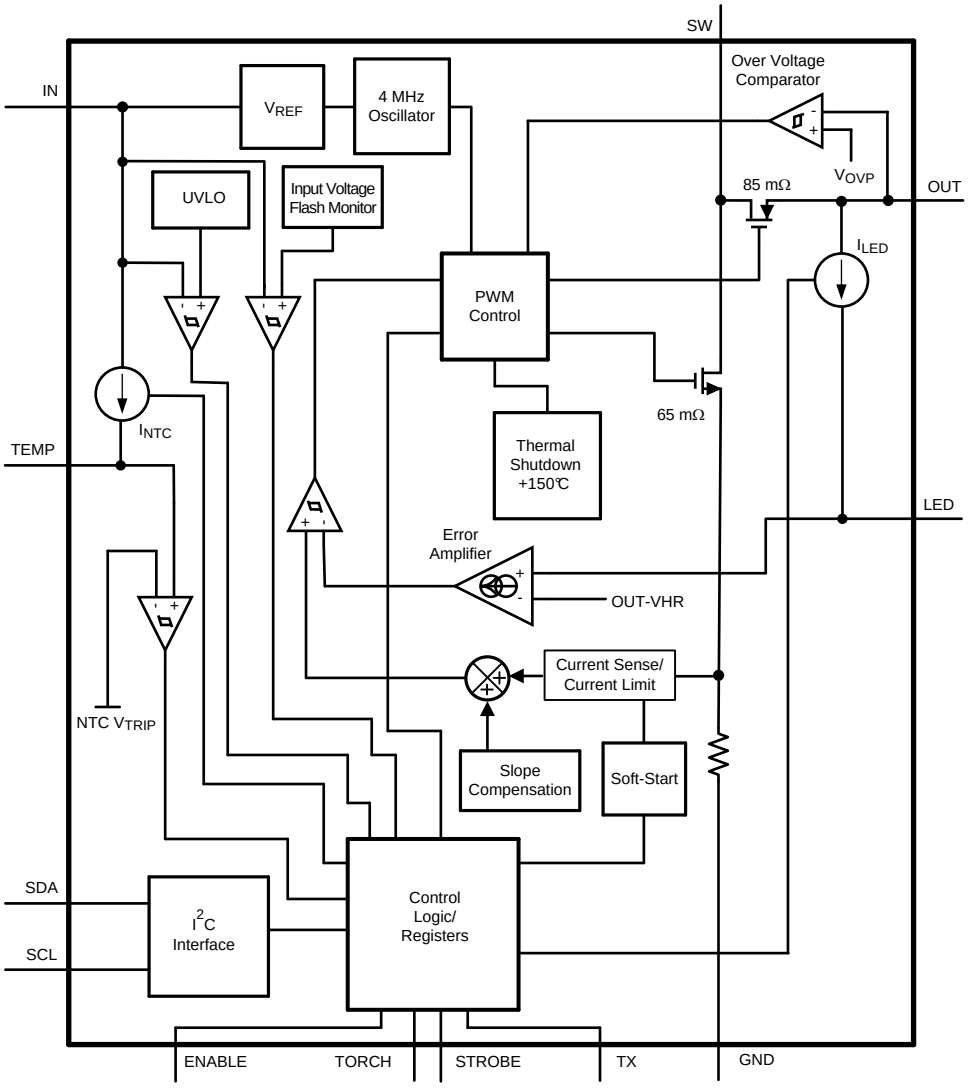
The LM3556 has three logic inputs including a hardware flash enable (STROBE), a hardware torch enable (TORCH) used for external torch mode control and custom LED indication waveforms, and a flash interrupt input (TX) designed to interrupt the flash pulse during high battery-current conditions. All three logic inputs have internal 300-kΩ (typical) pulldown resistors to GND.

Additional features of the LM3556 include an internal comparator for LED thermal sensing via an external NTC thermistor and an input voltage monitor that can reduce the Flash current (during low V_{IN} conditions).

Control of the LM3556 is done via an I^2C-compatible interface. This includes adjustment of the flash and torch current levels, changing the flash time-out duration, changing the switch current limit, and enabling the NTC block. Additionally, there are flag and status bits that indicate flash current time-out, LED overtemperature condition, LED failure (open or short), device thermal shutdown, TX interrupt, and V_{IN} undervoltage conditions.

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7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power-Amplifier Synchronization (TX)

The TX pin is a power-amplifier synchronization input. It is designed to reduce the flash LED current and thus limit the battery current during high battery-current conditions such as PA transmit events. When the LM3556 is engaged in a flash event, and the TX pin is pulled high, the LED current is forced into Torch Mode at the programmed torch current setting or shutdown. If the TX pin is then pulled low before the flash pulse terminates, the LED current returns to the previous flash current level. At the end of the flash time-out, whether the TX pin is high or low, the LED current turns off. The polarity of the TX input can be changed from active high to active low through the *Configuration Register (0x07)* and can be disabled/enabled by setting the TX Enable bit in the *Enable Register (0x0A)* to a '0'.

7.3.2 Input Voltage Flash Monitor (IVFM)

The LM3556 device can adjust the flash current based upon the voltage level present at the IN pin using an input voltage flash monitor. Two adjustable thresholds (IVM-D and IVM-U) ranging from 2.9 V to 3.6 V in 100-mV steps, and four different usage modes (Report Mode, Stop and Hold Mode, Adjust Down Only Mode, Adjust Up and Down Mode), are provided. The Flags Register has the fault flag set when the input voltage crosses the IVM-D value. In Report Mode, apart from the fault flag triggering, no action is taken on the LED current.

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Feature Description (continued)

Additionally, the IVM-D threshold sets the input voltage boundary that forces the LM3556 to either stop ramping the flash current during start-up (Stop and Hold Mode) or to start decreasing the LED current during the flash (Adjust Down Only Mode and Adjust Down and Up Mode). The IVM-U threshold sets the input voltage boundary that forces the LM3556 to start ramping the flash current back up towards the target (Adjust Up and Down Mode). The IVM-U threshold is equal to the IVM-D value plus the programmed hysteresis value also stored in the *Input Voltage Flash Monitor (IVFM) Mode Register (0x01)*.

To help prevent a premature current reduction, the LM3556 has four different filter timers that start once the input voltage decreases below the IVM-D line. These filter times are set in the *Silicon Revision and Filter Time Register (0x00)*. For more information, refer to *Input Voltage Flash Monitor (IVFM) Mode Register (0x01)* and *Configuration Register (0x07)*.

7.3.3 Fault Protections

7.3.3.1 Fault Operation

Upon entering a fault condition, the LM3556 sets the appropriate flag in the *Flags Register (0x0B)*, placing the part into standby by clearing and locking the Torch Enable bit (TEN), Pre-Charge bit, and Mode bits (M1, M0) in the *Enable Register (0x0A)*, until the *Flags Register (0x0B)* is read back via I^2C.

7.3.3.2 Flash Time-Out

The Flash time-out period sets the amount of time that the flash current is being sourced from the current source (LED). The LM3556 has 8 time-out levels ranging 100 ms to 800 ms in 100-ms steps. The flash time-out period is controlled in the *Flash Features Register (0x08)*. Flash time-out only applies to the Flash Mode operation. The mode bits are cleared upon a flash time-out.

7.3.3.3 Overvoltage Protection (OVP)

The output voltage is limited to typically 5 V (see V_{OVP} in *Electrical Characteristics* . In situations such as an open LED, the LM3556 device raises the output voltage in order to keep the LED current at its target value. When V_{OUT} reaches 5 V (typical), the overvoltage comparator trips and turns off the internal NFET. When V_{OUT} falls below the V_{OVP} off threshold, the LM3556 begins switching again. The mode bits in the *Enable Register (0x0A)* are not cleared upon an OVP.

7.3.3.4 Current Limit

The LM3556 features selectable inductor-current limits that are programmable through the *Flash Features Register (0x08)* of the I^2C-compatible interface. When the inductor-current limit is reached, the LM3556 terminates the charging phase of the switching cycle.

Because the current limit is sensed in the NMOS switch, there is no mechanism to limit the current when the device operates in Pass Mode. In Boost Mode or Pass Mode, if V_{OUT} falls below 2.3 V, the device stops switching, and the PFET operates as a current source limiting the current to 200 mA. This prevents damage to the LM3556 and excessive current draw from the battery during output short-circuit conditions. The mode bits in the *Enable Register (0x0A)* are not cleared upon a current limit event.

Pulling additional current from the V_{OUT} node during normal operation is not recommended.

7.3.3.5 NTC Thermistor Input (TEMP)

The TEMP pin serves as a threshold detector for negative temperature coefficient (NTC) thermistors. It interrupts the LED current when the voltage at TEMP goes below the programmed threshold. The NTC threshold voltage is adjustable from 200 mV to 900 mV in 100-mV steps. The NTC current is adjustable from 25 µA to 100 µA in 25-µA steps. When an overtemperature event is detected, the LM3556 can be set to force the LED current from Flash Mode into Torch Mode or into shutdown. These settings are adjusted via the *NTC Settings Register (0x02)*, and the NTC detection circuitry can be enabled or disabled via the *Enable Register (0x0A)*. If enabled, the NTC block turns on and off during the start and stop of a flash, torch, or indicator event. The NTC mode of operation is set by adjusting the NTC Mode bit in the *Configuration Register (0x07)*. See *NTC Settings Register (0x02)* for more details. The mode bits in the *Enable Register (0x0A)* are cleared upon an NTC event.

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Feature Description (continued)

7.3.3.6 Undervoltage Lockout (UVLO)

The LM3556 has an internal comparator that monitors the voltage at IN and forces the LM3556 into shutdown if the input voltage drops to 2.8 V. If the UVLO monitor threshold is tripped, the UVLO flag bit is set in the *Flags Register (0x0B)*. If the input voltage rises above 2.8 V, the device is available for operation until there is an I^2C read command initiated for the *Flags Register (0x0B)*. Upon a read, the Flags Register is cleared, and normal operation can resume. This feature can be disabled by writing a '0' to the UVLO EN bit in the *Input Voltage Flash Monitor (IVFM) Mode Register (0x01)*. The mode bits in the *Enable Register (0x0A)* are cleared upon a UVLO event.

7.3.3.7 Thermal Shutdown (T_{SD})

When the LM3556 device's die temperature reaches 150°C, the boost converter shuts down, and the NFET and PFET turn off, as does the current source (LED). When the thermal shutdown threshold is tripped, a '1' gets written to the corresponding bit of the *Flags Register (0x0B)* (T_{SD} bit), and the device goes into standby. The LM3556 can only restart after the *Flags Register (0x0B)* is read, clearing the fault flag. Upon restart, if the die temperature is still above 150°C, the device resets the fault flag and re-enters standby. The mode bits in the *Enable Register (0x0A)* are cleared upon a T_{SD}.

7.3.3.8 LED and/or V_{OUT} Fault

The LED fault flag in the *Flags Register (0x0B)* reads back a '1' if the part is active in Flash Mode or Torch Mode, and the LED output or the V_{OUT} node experiences a short condition. The LM3556 determines an LED open condition if the OVP threshold is crossed at the OUT pin while the device is in Flash or Torch Mode. An LED short condition is determined if the voltage at LED goes below 500 mV (typical) while the device is in either Torch or Flash Mode. There is a delay of 256-µs deglitch time before the LED flag is valid, and 2.048 ms before the V_{OUT} flag is valid. This delay is the time between when the flash or torch current is triggered and when the LED voltage and the output voltage are sampled. The LED flag can only be reset to '0' by removing power to the LM3556, or by reading back the *Flags Register (0x0B)*. The mode bits in the *Enable Register (0x0A)* are cleared upon an LED and/or V_{OUT} fault.

7.4 Device Functional Modes

7.4.1 Start-Up (Enabling The Device)

Turnon of the LM3556 Torch and Flash Modes can be done through the *Enable Register (0x0A)*. On start-up, when V_{OUT} is less than V_{IN} the internal synchronous PFET turns on as a current source and delivers 200 mA (typical) to the output capacitor. During this time the current source (LED) is off. When the voltage across the output capacitor reaches 2.2 V (typical) the current source turns on. At turnon the current source steps through each FLASH or TORCH level until the target LED current is reached. This gives the device a controlled turnon and limits inrush current from the V_{IN} supply.

7.4.2 Pass Mode

The LM3556 starts up in Pass Mode and stays there until Boost Mode is needed to maintain regulation. If the voltage difference between V_{OUT} and V_{LED} falls below V_{HR}, the device switches to Boost Mode. In Pass Mode the boost converter does not switch, and the synchronous PFET fully turns on bringing V_{OUT} up to (V_{IN} − I_{LED} × R_{PMOS}). In Pass Mode the inductor current is not limited by the peak current limit. In this situation the output current must be limited to 2 A.

7.4.3 Flash Mode

In Flash Mode, the LED current source (LED) provides 16 target current levels from 93.75 mA to 1500 mA. The Flash currents are adjusted via the *Current Control Register (0x09)*. Flash mode is activated by the *Enable Register (0x0A)*, or by pulling the STROBE pin HIGH. Once the Flash sequence is activated the current source (LED) ramps up to the programmed Flash current by stepping through all current steps until the programmed current is reached.

When the device is enabled in Flash Mode through the Enable Register, all mode bits in the Enable Register are cleared after a flash time-out event.

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Device Functional Modes (continued)

Data can be written to the mode bits (bits[1:0]) in *Enable Register (0x0A)* only after the flash has ramped down to the desired value, and V_{OUT} has decayed.

Table 1 shows the I^2C commands and the state of the mode bits, if the STROBE pin is used to enable the Flash Mode.

Table 1. I^2C Commands and the State of the Mode Bits

MODE CHANGE REQUIRED	ENABLE AND CONFIGURATION REGISTER SETTING (0x0A=Enable Register, 0x07=Configuration Register)	STATUS OF MODE BITS IN THE ENABLE REGISTER AFTER A FLASH
Using edge-triggered STROBE to Flash	0x0A = 0x23; 0x07 = 0x78 (default setting)	Mode bits are cleared after a single flash. To reflash, 0x23 has to be written to 0x0A.
Using level-triggered STROBE to Flash	0x0A = 0x23; 0x07 = 0xF8	Mode bits are cleared after a single flash. To reflash, 0x23 has to be written to 0x0A.
Part is required to go from external TORCH Mode to external STROBE mode using edge-triggered STROBE	0x0A = 0x33; 0x07 = 0x78 (default setting)	Mode bits are cleared after a single flash. To reflash, 0x33 has to be written to 0x0A.
Part is required to go from external TORCH Mode to external STROBE mode using Level Triggered STROBE	0x0A = 0x33; 0x0 7= 0xF8	Mode bits are cleared only if the part has an internal flash time-out event happening before the STROBE level goes low. To re-flash, 0x33 has to be written to 0x0A. If the STROBE level goes low before an internal flash time-out event, then mode bits are not cleared.

7.4.4 Torch Mode

In Torch Mode, the current source (LED) is programmed via the *Current Control Register (0x09)*. Torch Mode is activated by the *Enable Register (0x0A)* or by the hardware TORCH input. Once the Torch Mode is enabled the current source ramps up to the programmed torch current level. The ramp-up and ramp-down times are independently adjustable via the *Torch Ramp Time Register (0x06)*. Torch Mode is not affected by flash timeout.

7.4.5 Indicator Mode

This mode has two options: the Internal Indicator Mode and the External Indicator mode. Both these modes are activated by the Configuration Register (0x07) in addition to the *Enable Register (0x0A)*.

In the Internal Indicator Mode, the current source (LED) can be programmed to 8 different intensity levels, with current values being 1/8th the values in *Current Control Register (0x09)* bits [6:4]. The ramp-up, ramp-down, the pulse time, number of blanks and periods of the desired output current can be independently controlled via the *Indicator Ramp Time Indicator (0x03)*, *Indicator Blinking Register (0x04)* and the *Indicator Period Count Register (0x05)*.

In the External Indicator Mode, the current source (LED) is controlled via the TORCH pin. An external PWM signal can be input to the part via the TORCH pin to choose any one of the 8 available intensity settings (bits [6:4] of the *Current Control Register (0x09)*) for the current source (LED).

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7.5 Programming

7.5.1 I²C-Compatible Interface

7.5.1.1 Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when SCL is LOW.

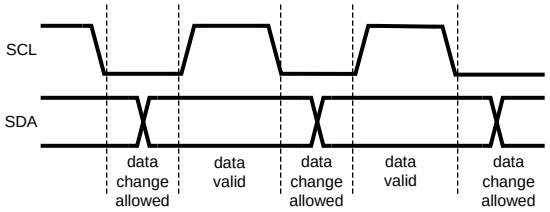


Figure 29. Data Validity Diagram

A pullup resistor between the controller's VIO line and SDA must be greater than [(VIO – V_{OL}) / 3mA] to meet the V_{OL} requirement on SDA. Using a larger pullup resistor results in lower switching current with slower edges, while using a smaller pullup results in higher switching currents with faster edges.

7.5.1.2 Start and Stop Conditions

START and STOP conditions classify the beginning and the end of the I²C session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP conditions. The I²C bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

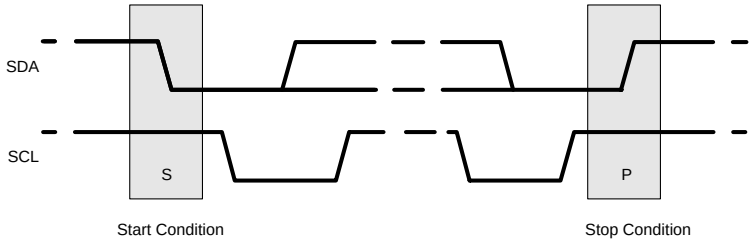


Figure 30. Start and Stop Conditions

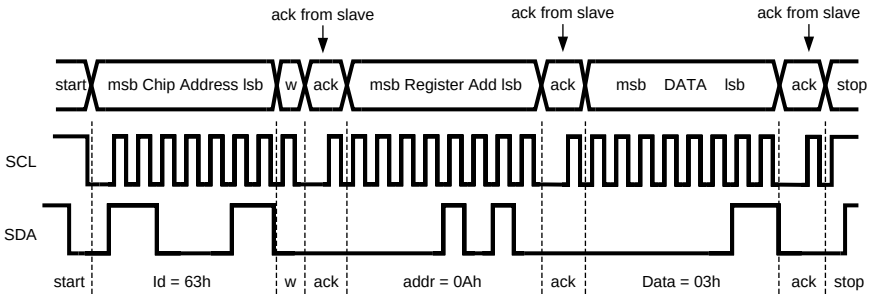
7.5.1.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LM3556 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LM3556 generates an acknowledge after each byte is received. There is no acknowledge created after data is read from the LM3556.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM3556 7-bit address is 0x63. For the eighth bit, a '0' indicates a WRITE and a '1' indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

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Programming (continued)



W = Write (SDA = '0')
R = Read (SDA = '1')
Ack = Acknowledge (SDA Pulled Down By Either Master Or Slave)
ID= Chip Address, 63h For LM3556

Figure 31. Write Cycle

7.5.1.4 I²C-Compatible Chip Address

The device address for the LM3556 is 1100011 (63). After the START condition, the I²C-compatible master sends the 7-bit address followed by an eighth read or write bit (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data will be written. The third byte contains the data for the selected register.

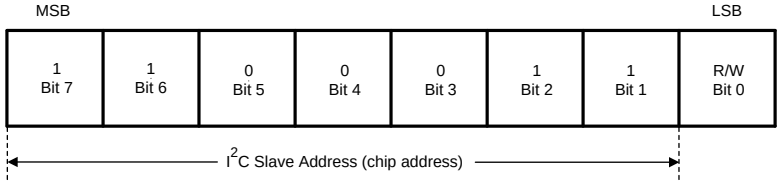


Figure 32. I²C-Compatible Device Address

7.5.1.5 Transferring Data

Every byte on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data must be followed by an acknowledge bit (ACK). The acknowledge related clock pulse (9th clock pulse) is generated by the master. The master releases SDA (HIGH) during the 9th clock pulse. The LM3556 pulls down SDA during the 9th clock pulse, signifying an acknowledge. An acknowledge is generated after each byte has been received.

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7.6 Register Maps

7.6.1 Register Descriptions

REGISTER NAME	INTERNAL HEX ADDRESS	POWER ON/RESET VALUE
Silicon Revision and Filter Time Register	0x00	0x04
IVFM Mode Register	0x01	0x80
NTC Settings Register	0x02	0x12
Indicator Ramp Time Register	0x03	0x00
Indicator Blinking Register	0x04	0x00
Indicator Period Count Register	0x05	0x00
Torch Ramp Time Register	0x06	0x00
Configuration Register	0x07	0x78
Flash Features Register	0x08	0xD2
Current Control Register	0x09	0x0F
Enable Register	0x0A	0x00
Flags Register	0x0B	0x00

7.6.1.1 Silicon Revision and Filter Time Register (0x00)

Table 2. Silicon Revision and Filter Time Register Description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	**RFU**	**RFU**	**IVFM Filter Times** '00' = 1/2 of the Current Step Time '01' = 256 µs '10' =512 µs '11' = 1024 µs		Bits available for Silicon Revision Current Value = '100'		

7.6.1.2 Input Voltage Flash Monitor (IVFM) Mode Register (0x01)

Table 3. Input Voltage Flash Monitor (IVFM) Mode Register Description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1 = UVLO EN (default)	**Hysteresis Level** 00 = 50 mV (default) 01 = 100 mV 10 = 150 mV 11 = Hysteresis Disabled		**IVM-D (Down) Threshold** 000 = 2.9 V (default) 001 = 3 V 010 = 3.1 V 011 = 3.2 V 100 = 3.3 V 101 = 3.4 V 110 = 3.5 V 111 = 3.6 V			**IVFM Adjust Mode** 00 = Report Mode (default) 01 = Stop and Hold Mode 10 = Down Mode 11 = Up and Down Mode	

00 = Report Mode Sets IVFM flag in Flags Register upon crossing IVM-D line Only. Does not adjust current.

01 = Stop and Hold Mode Stops current ramp and holds the level for the remaining flash if V_{IN} crosses IVM-D Line. Sets IVFM flag in Flags Register upon crossing IVM-D line.

10 = Down Mode Adjusts current down if V_{IN} crosses IVM-D Line and stops decreasing once V_{IN} rises above the IVM-D line plus the IVFM hystersis setting. The LM3556 decreases the current throughout the flash pulse anytime the input voltage falls below the IVM-D line, and not just once. The flash current does not increase again until the next flash. Sets IVFM flag in Flags Register upon crossing IVM-D Line.

11 = Up and Down Mode Adjusts current down if V_{IN} crosses IVM-D Line and adjusts current up if V_{IN} rises above the IVM-D line plus the IVFM hystersis setting. In this mode, the current continually adjusts with the rising and falling of the input voltage throughout the entire flash pulse. Sets IVFM flag in Flags Register upon crossing IVM-D Line.

UVLO EN If enabled and V_{IN} drops below 2.8 V, the LM3556 enters standby and sets the UVLO flag in the Flags Register. Enabled = '1', Disabled = '0'

IVM-U = IVM-D + IVFM Hysteresis

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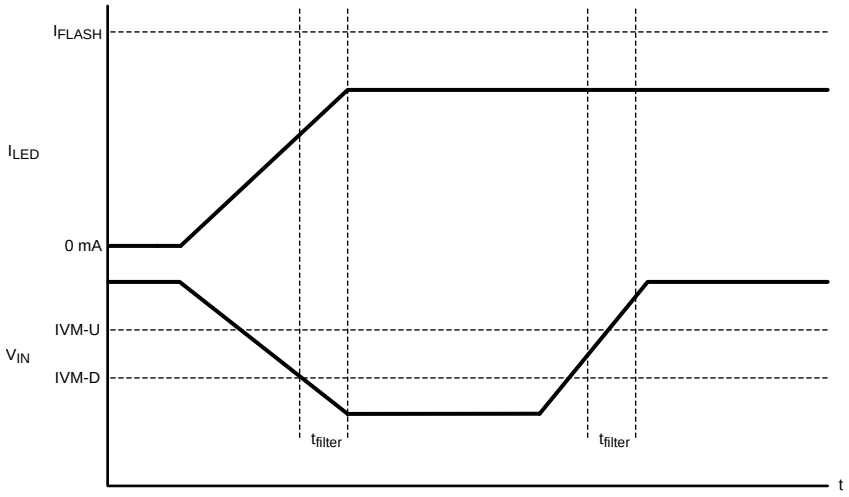


Figure 33. Stop and Hold Mode

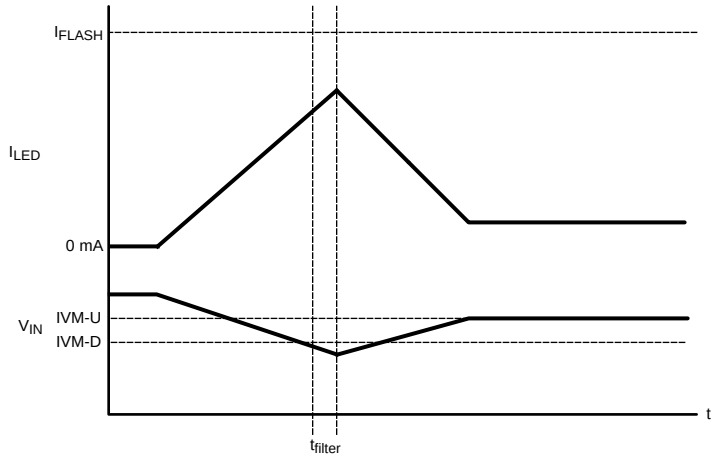


Figure 34. Adjust Down-Only Mode

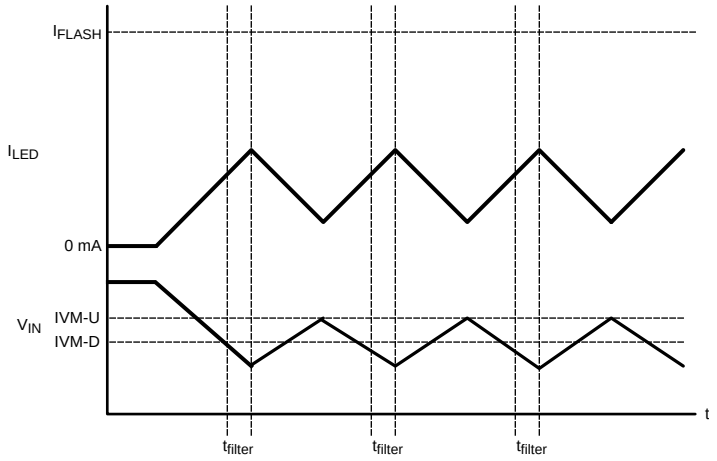


Figure 35. Adjust Up and Down Mode

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7.6.1.3 NTC Settings Register (0x02)

Table 4. NTC Settings Register Description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	**RFU**	**NTC Event Level** 0 = Go to standby (default) 1 = Reduce to minimum torch current	**NTC Trip Thresholds** 000 = 200 mV 001 = 300 mV 010 = 400 mV 011 = 50 mV 100 = 600 mV (default) 101 = 700 mV 110 = 800 mV 111 = 900 mV			**NTC Bias Current Level** 00 = 25 µA 01 = 50 µA 10 = 75 µA (default) 11 = 100 µA	

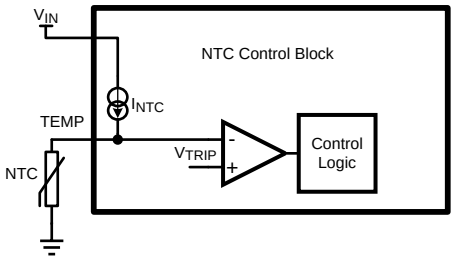


Figure 36. NTC Control Block

The TEMP node is connected to an NTC resistor as shown in Figure 36 above. A constant current source from the input is connected to this node. Any change in the voltage because of a change in the resistance of the NTC resistor is compared to a set V_{TRIP}. The trip thresholds are selected by Bits[4:2] of the NTC Register. The output of the Control Logic upon an NTC trip is selected through Bit[5].

7.6.1.4 Indicator Ramp Time Indicator (0x03)

Table 5. Indicator Ramp Time Indicator Description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	**RFU**	**Indicator Ramp-Up Time (t_R)** 000 = 16 ms (default) 001 = 32 ms 010 = 64 ms 011 = 128 ms 100 = 256 ms 101 = 512 ms 110 = 1.024 s 111 = 2.048 s			**Indicator Ramp-Down Time (t_F)** 000 = 16 ms (default) 001 = 32 ms 010 = 64 ms 011 = 128 ms 100 = 256 ms 101 = 512 ms 110 = 1.024 s 111 = 2.048 s		

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7.6.1.5 Indicator Blinking Register (0x04)

Table 6. Indicator Blinking Register Description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N_{BLANK} 0000 = 0 (default) 0001 = 1 0010 = 2 0011 = 3 0100 = 4 0101 = 5 0110 = 6 0111 = 7 1000 = 8 1001 = 9 1010 = 10 1011 = 11 1100 = 12 1101 = 13 1110 = 14 1111 = 15				Pulse Time (t_{PULSE}) 0000 = 0 (default) 0001 = 32 ms 0010 = 64 ms 0011 = 92 ms 0100 = 128 ms 0101 = 160 ms 0110 = 196 ms 0111 = 224 ms 1000 = 256 ms 1001 = 288 ms 1010 = 320 ms 1011 = 352 ms 1100 = 384 ms 1101 = 416 ms 1110 = 448 ms 1111 = 480 ms			

7.6.1.6 Indicator Period Count Register (0x05)

Table 7. Indicator Period Count Register Description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	RFU	RFU	RFU	RFU	N_{PERIOD} 000 = 0 (default) 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = 7		

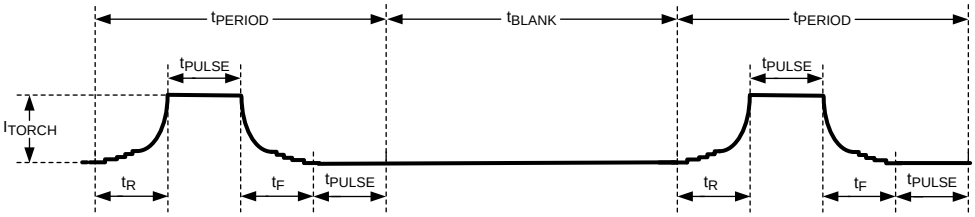


Figure 37. Indicator Usage

1. Number of periods ($t_{PERIOD} = t_R + t_F + t_{PULSE} \times 2$)
2. Active Time ($t_{ACTIVE} = t_{PERIOD} \times N_{PERIOD}$)
3. Blank Time ($t_{BLANK} = t_{ACTIVE} \times N_{BLANK}$)

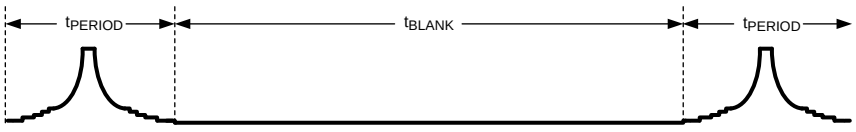


Figure 38. Single Pulse With Dead Time

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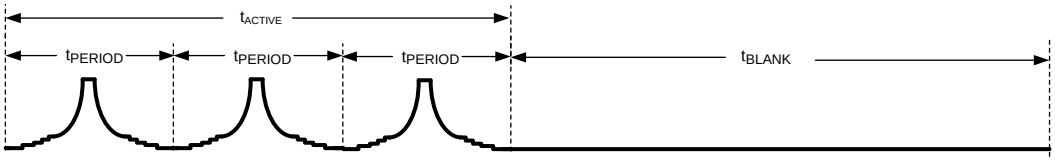


Figure 39. Multiple Pulse With Dead Time

7.6.1.7 Torch Ramp Time Register (0x06)

Table 8. Torch Ramp Time Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	**RFU**	**Torch Ramp-Up Time** 000 = 16 ms (default) 001 = 32 ms 010 = 64 ms 011 = 128 ms 100 = 256 ms 101 = 512 ms 110 = 1.024 s 111 = 2.048 s			**Torch Ramp-Down Time** 000 = 16 ms (default) 001 = 32 ms 010 = 64 ms 011 = 128 ms 100 = 256 ms 101 = 512 ms 110 = 1.024 s 111 = 2.048 s		

7.6.1.8 Configuration Register (0x07)

Table 9. Configuration Register Description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Strobe Usage 0 = Edge (default) 1 = Level	**Strobe Pin Polarity** 0 = Active Low 1 = Active High (default)	**Torch Pin Polarity** 0 = Active Low 1 = Active High (default)	**TX Pin Polarity** 0 = Active Low 1 = Active High (default)	**TX Event Level** 0 = Off 1 = Torch Current (default)	**IVFM Enable** 0 = Disabled (default) 1 = Enabled	**NTC Mode** 0 = Normal (default) 1 = Monitor	**Indicator Mode** 0 = Internal (default) 1 = External

Strobe Usage Level or edge. Flash follows strobe timing if Level and internal timing if edge.

Strobe Polarity Active high or active low select.

Torch Polarity Active high or active low select.

TX Polarity Active high or active low select.

TX Event Level Transition to torch current level or off setting if TX event occurs.
The TX Event Level off setting is designed to force a shutdown only during a flash event. When Torch or Indicator Mode is enabled, and a TX event occurs with the TX event level set to Off , the LM3556 does not shut down. The TX flag bit (bit7 in the Table 14) is set, and the mode bits (bit0 and bit1 in Table 12) get locked out until the fault register is cleared via an I^2C read. Because a TX event is periodic and frequently occurring, clearing the fault register becomes more difficult. Depending on the I^2C read/write speed and TX event frequency, it may be necessary to set the TX enable bit (bit6 in the Table 12) to a '0' before clearing the fault register to prevent future flag sets.

IVFM Enable Enables input voltage flash monitoring.

NTC Mode Monitor Mode (report only) or Normal Mode (reduce current or shutdown).

Indicator Mode Externally generated via TORCH pin or internally generated PWM.

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7.6.1.9 Flash Features Register (0x08)

Table 10. Flash Features Register Description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Inductor Current Limit 00 =1.7 A 01 = 1.9 A 10 = 2.5 A 11 = 3.1 A (default)		**Flash Ramp Time** 000 = 256 µs 001 = 512 µs 010 = 1.024 ms (default) 011 = 2.048 ms 100 = 4.096 ms 101 = 8.192 ms 110 = 16.384 ms 111 = 32.768 ms			**Flash Time-Out Time** 000 = 100 ms 001 = 200 ms 010 = 300 ms (default) 011 = 400 ms 100 = 500 ms 101 = 600 ms 110 = 700 ms 111 = 800 ms		

7.6.1.10 Current Control Register (0x09)

Table 11. Current Control Register Description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	**Torch Current** 000 = 46.88 mA (default) 001 =93.75 mA 010 =140.63 mA 011 = 187.5 mA 100 =234.38 mA 101 = 281.25 mA 110 = 328.13 mA 111 =375 mA			**Flash Current** 0000 = 93.75 mA 0001 = 187.5 mA 0010 = 281.25 mA 0011 = 375 mA 0100 = 468.75 mA 0101 = 562.5mA 0110 = 656.25 mA 0111 = 750 mA 1000 = 843.75 mA 1001 = 937.5 mA 1010 = 1031.25 mA 1011 = 1125 mA 1100 = 1218.75 mA 1101 = 1312.5 mA 1110 = 1406.25 mA 1111 = 1500 mA (default)			

7.6.1.11 Enable Register (0x0A)

Table 12. Enable Register Description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NTC Enable 0 = Disabled (default) 1 = Enabled	**TX Pin Enable** 0 = Disabled (default) 1 = Enabled	**STROBE Pin Enable** 0 = Disabled (default) 1 = Enabled	**TORCH Pin Enable** 0 = Disabled (default) 1 = Enabled	**PreCharge Mode Enable** 0 = Normal (default) 1 = PreCharge	**Pass-Mode Only Enable** 0 = Normal (default) 1 = Pass Only	**Mode Bits: M1, M0** 00 = Standby (default) 01 = Indicator 10 = Torch 11 = Flash	

NTC EN Enables NTC block.

TX EN Allows TX events to change the current.

Strobe EN Enables STROBE pin to start a flash event.

Torch EN Enables TORCH pin to start a torch event.

PreCharge Mode EN Enables Pass Mode to pre-charge the output cap.

Pass-Only Mode EN Only allows Pass Mode and disallows Boost Mode.
If Pass-Only Mode is enabled during any LED mode (Indicator, Torch or Flash), it remains enabled until the LM3556 enters the standby state regardless of whether the Pass-Only Mode bit is reset or not during the following command.

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7.6.1.11.1 Enable Register Mode Bits

00–Standby Off

01–Indicator Sets Indicator Mode. Default Indicator Mode uses external pattern on TORCH pin.

10–Torch Sets Torch Mode with ramping. If Torch EN = 0, Torch starts after I^2C-compatible command.

11–Flash Sets Flash Mode with ramping. If Strobe EN = 0, Flash starts after I^2C-compatible command.

7.6.1.11.2 Control Logic Delays

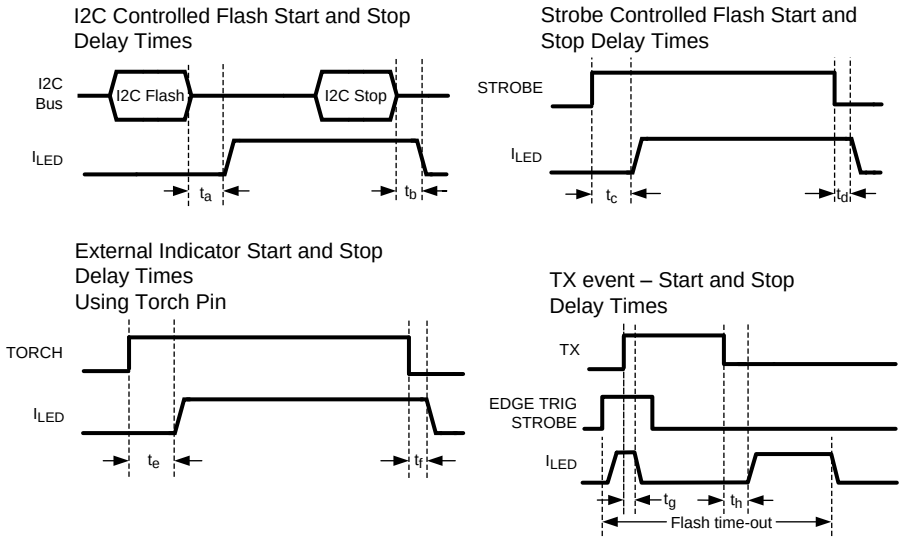


Figure 40. Control Logic Delays

Table 13. Control Logic Delay Timing

DELAY	EXPLANATION	TIME
t_a	Time for the LED current to start ramping up after an I^2C Write command.	554 µs
t_b	Time for the LED current to start ramping down after an I^2C Stop command.	32 µs
t_c	Time for the LED current to start ramping up after the STROBE pin is raised high.	400 µs
t_d	Time for the LED current to start ramping down after the STROBE pin is pulled low.	16 µs
t_e	Time for the LED current to start ramping up after the TORCH pin is raised high.	300 µs
t_f	Time for the LED current to start ramping down after the TORCH pin is pulled low.	16 µs
t_g	Time for the LED current to start ramping down after the TX pin is pulled high.	3 µs
t_h	Time for the LED current to start ramping up after the TX pin is pulled low, provide the part has not timed out in Flash Mode.	2 µs

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7.6.1.12 Flags Register (0x0B)

Table 14. Flags Register Description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX Event 0 = Default	**NTC Trip** 0 = Default	IVFM 0 = Default	**UVLO** 0 = Default	**OVP** 0 = Default	**LED or VOUT Short Fault** 0 = Default	**Thermal Shutdown** 0 = Default	**Flash Time-out** 0 = Default

TX Event Flag TX event occurred.

NTC Trip Flag NTC threshold crossed.

IVFM Flag IVFM block reported and/or adjusted LED current.

UVLO Fault UVLO threshold crossed.

OVP Flag Overvoltage Protection tripped. Open output capacitor or open LED.

LED Short Fault LED short detected.

Thermal Shutdown Fault LM3556 die temperature reached thermal shutdown value.

Time-Out Flag Flash Timer tripped.

NOTE

Faults require a read-back of the Flags Register to resume operation. Flags report an event occurred, but do not inhibit future functionality. A read-back of the Flags Register updates again if the fault or flags are still present upon a restart.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM3556 can drive one flash LED at currents up to 1.5 A. The 4-MHz DC-DC boost regulator allows for the use of small-value discrete external components.

8.2 Typical Application

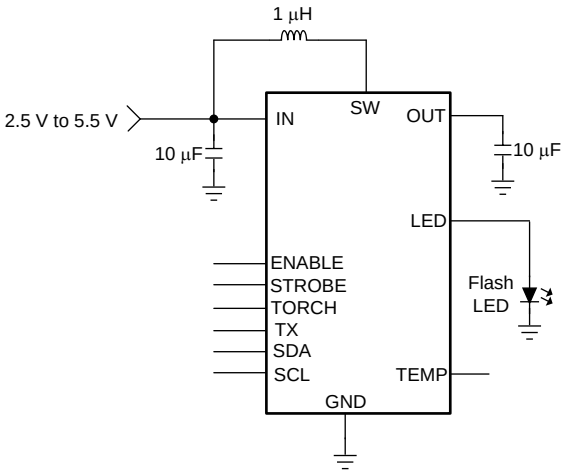


Figure 41. LM3556 Typical Application

8.2.1 Design Requirements

Example requirements based on default register values are listed in Table 15:

Table 15. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	2.5 V to 5.5 V
Brightness Control	I2C Register
Output current	1.5 A
LED Configuration	1 Flash LED
Switching frequency	4 MHz (typical)

8.2.2 Detailed Design Procedure

8.2.2.1 Output Capacitor Selection

The LM3556 is designed to operate with a ceramic output capacitor of at least 10 µF. When the boost converter is running, the output capacitor supplies the load current during the boost converter's on-time. When the NMOS switch turns off, the inductor energy is discharged through the internal PMOS switch, supplying power to the load and restoring charge to the output capacitor. This causes a sag in the output voltage during the on-time and a rise in the output voltage during the off-time. The output capacitor is therefore chosen to limit the output ripple to an acceptable level depending on load current and input/output voltage differentials and also to ensure the converter remains stable.

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Larger capacitors (for example, a 22-µF capacitor) or capacitors in parallel may be used if lower output voltage ripple is desired. To estimate the output voltage ripple, considering the ripple due to capacitor discharge (ΔV_Q) and the ripple due to the capacitors equivalent series resistance (ESR) (ΔV_{ESR}), use Equation 1 and Equation 2.

For continuous conduction mode, the output voltage ripple due to the capacitor discharge is:

$$\Delta V_Q = \frac{I_{LED} \times (V_{OUT} - V_{IN})}{f_{SW} \times V_{OUT} \times C_{OUT}} \quad (1)$$

The output voltage ripple due to the ESR of the output capacitor is found by:

$$\Delta V_{ESR} = R_{ESR} \times \left(\frac{I_{LED} \times V_{OUT}}{V_{IN}} \right) + \Delta I_L$$

where

$$\Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \quad (2)$$

In ceramic capacitors the ESR is very low so the assumption is that 80% of the output voltage ripple is due to capacitor discharge and 20% from ESR. Table 16 lists different manufacturers for various output capacitors and their case sizes suitable for use with the LM3556.

8.2.2.2 Input Capacitor Selection

Choosing the correct size and type of input capacitor helps minimize the voltage ripple caused by the switching of the LM3556 device's boost converter and reduces noise on the boost converter's input terminal that can feed through and disrupt internal analog signals. In the Figure 41 a 10-µF ceramic input capacitor works well. It is important to place the input capacitor as close as possible to the LM3556's input (IN) pin. This reduces the series resistance and inductance that can inject noise into the device due to the input switching currents. Table 16 lists various input capacitors recommended for use with the LM3556.

Table 16. Recommended Input/Output Capacitors (X5R/X7R Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	VOLTAGE RATING
TDK Corporation	C1608JB0J106M	10 µF	0603 (1.6 mm × 0.8 mm × 0.8 mm)	6.3 V
TDK Corporation	C2012JB1A106M	10 µF	0805 (2 mm × 1.25 mm × 1.25 mm)	10 V
Murata	GRM188R60J106M	10 µF	0603 (1.6 mm x 0.8 mm x 0.8 mm)	6.3 V
Murata	GRM21BR61A106KE19	10 µF	0805 (2 mm × 1.25 mm × 1.25 mm)	10 V

8.2.2.3 Inductor Selection

The LM3556 is designed to use a 1-µH or 0.47-µH inductor. Table 17 lists various inductors and their manufacturers that work well with the LM3556. When the device is boosting ($V_{OUT} > V_{IN}$) the inductor is typically the largest area of efficiency loss in the circuit. Therefore, choosing an inductor with the lowest possible series resistance is important. Additionally, the saturation rating of the inductor must be greater than the maximum operating peak current of the LM3556. This prevents excess efficiency loss that can occur with inductors that operate in saturation. For proper inductor operation and circuit performance, ensure that the inductor saturation and the peak current limit setting of the LM3556 are greater than I_{PEAK} in Equation 3:

$$I_{PEAK} = \frac{I_{LOAD}}{\eta} \times \frac{V_{OUT}}{V_{IN}} + \Delta I_L \quad \text{where} \quad \Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \quad (3)$$

where

- f_{SW} = 4 MHz
- Efficiency can be found in *Typical Characteristics*.

Table 17. Recommended Inductors

MANUFACTURER	L	PART NUMBER	DIMENSIONS (L × W × H)	I_{SAT}	R_{DC}
TOKO	1 µH	FDSD0312	3 mm x 3 mm x 1.2 mm	4.5 A	43 mΩ
TOKO	1 µH	DFE252010C	2.5 mm × 2 mm × 1 mm	3.4 A	60 mΩ
TOKO	1 µH	DFE252012C	2.5 mm × 2 mm × 1.2 mm	3.8 A	45 mΩ

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8.2.2.4 NTC Thermistor Selection

The TEMP pin is a comparator input for flash LED thermal sensing. NTC mode is intended to monitor an external thermistor which monitors LED temperature and prevents LED overheating. An internal comparator checks the voltage on the TEMP pin against the trip point programmed in the *NTC Settings Register (0x02)*. The thermistor is driven by an internally regulated current source, and the voltage on the TEMP pin is related to the source current and the NTC resistance.

NTC thermistors have a temperature to resistance relationship of:

$$R(T) = R_{25°C} \times e^{\left[\beta\left(\frac{1}{T\,°C + 273} - \frac{1}{298}\right)\right]} \quad (4)$$

where

- β is given in the thermistor datasheet
- $R_{25°C}$ is the thermistor's value at 25°C.

8.2.3 Application Curves

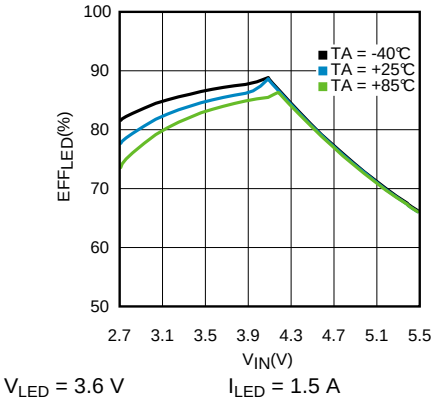


Figure 42. Flash LED Efficiency vs V_{IN}

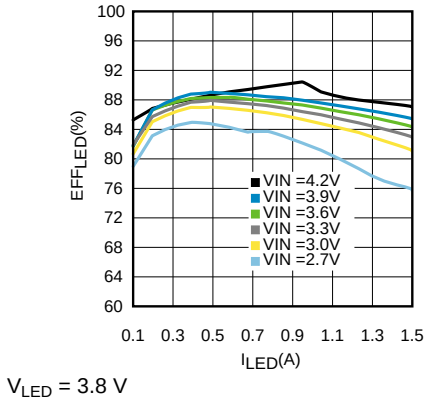


Figure 43. Flash LED Efficiency vs Flash LED Current

9 Power Supply Recommendations

The LM3556 is designed to operate from an input supply range of 2.5 V to 5.5 V. This input supply must be well regulated and provide the peak current required by the LED configuration and inductor selected.

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10 Layout

10.1 Layout Guidelines

The high switching frequency and large switching currents of the LM3556 make the choice of layout important. The following steps should be used as a reference to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range.

1. Place C_{IN} on the top layer (same layer as the device), as close as possible to the device. The input capacitor conducts the driver currents during the low-side MOSFET turnon and turnoff and can see current spikes over 1 A in amplitude. Connecting the input capacitor through short, wide traces to both the IN and GND pins reduces the inductive voltage spikes that occur during switching which can corrupt the V_{IN} line.
2. Place C_{OUT} on the top layer (same layer as the device) and as close as possible to the OUT and GND pins. The returns for both C_{IN} and C_{OUT} must come together at one point, as close as possible to the GND pin. Connecting C_{OUT} through short, wide traces reduces the series inductance on the OUT and GND pins that can corrupt the V_{OUT} and GND lines and cause excessive noise in the device and surrounding circuitry.
3. Connect the inductor on the top layer close to the SW pin. There must be a low-impedance connection from the inductor to SW due to the large DC inductor current, and at the same time the area occupied by the SW node must be small to reduce the capacitive coupling of the high dV/dt present at SW that can couple into nearby traces.
4. Logic traces must not be routed near the SW node to avoid any capacitively coupled voltages from SW onto any high-impedance logic lines such as TORCH, STROBE, HWEN, TEMP, SDA, and SCL. A good approach is to insert an inner layer GND plane underneath the SW node and between any nearby routed traces. This creates a shield from the electric field generated at SW.
5. Terminate the flash LED cathodes directly to the GND pin of the LM3556. If possible, route the LED returns with a dedicated path to keep the high amplitude LED currents out of the GND plane. For flash LEDs that are routed relatively far away from the device, sandwich the forward and return current paths over the top of each other on two layers. This helps reduce the inductance of the LED current paths.

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10.2 Layout Example

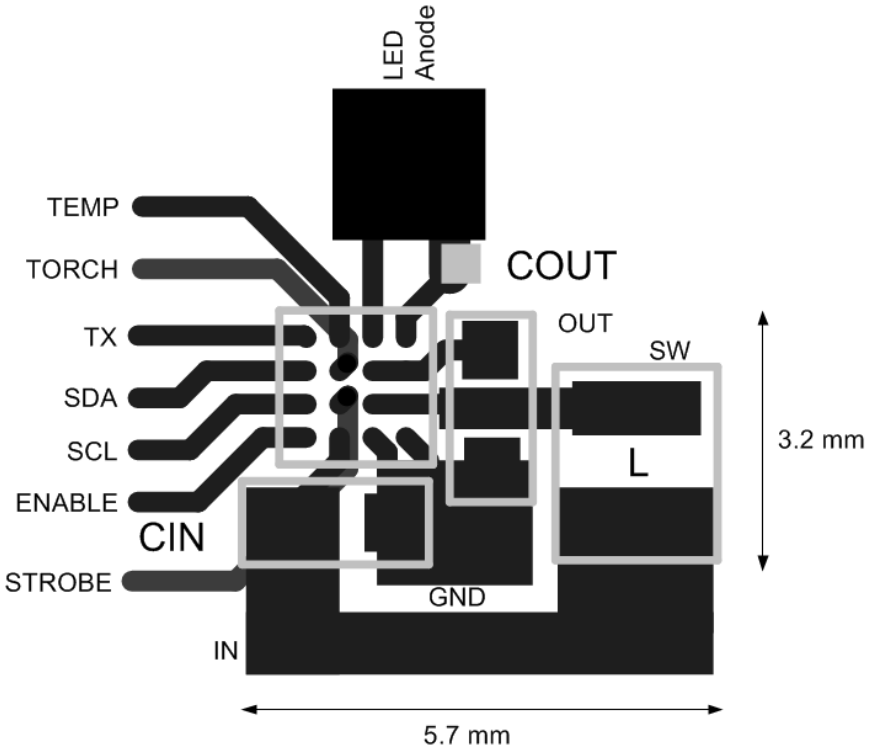


Figure 44. LM3556 Layout Example

11 Device And Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For additional information, see the following:

TI Application Note *DSBGA Wafer Level Chip Scale Package* (SNVA009)

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, And Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3556TME/NOPB	ACTIVE	DSBGA	YFQ	16	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		D36	Samples
LM3556TMX/NOPB	ACTIVE	DSBGA	YFQ	16	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		D36	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

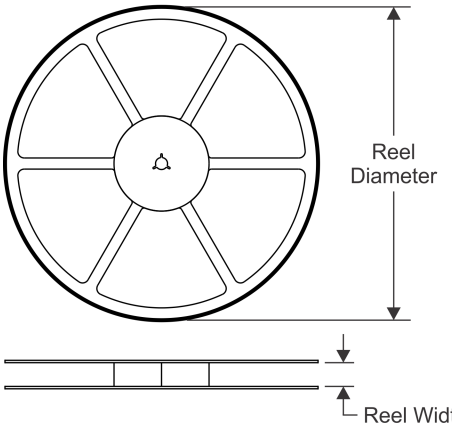
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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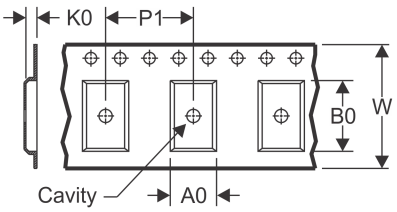
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

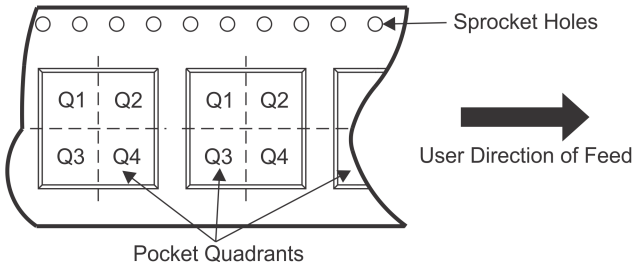


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

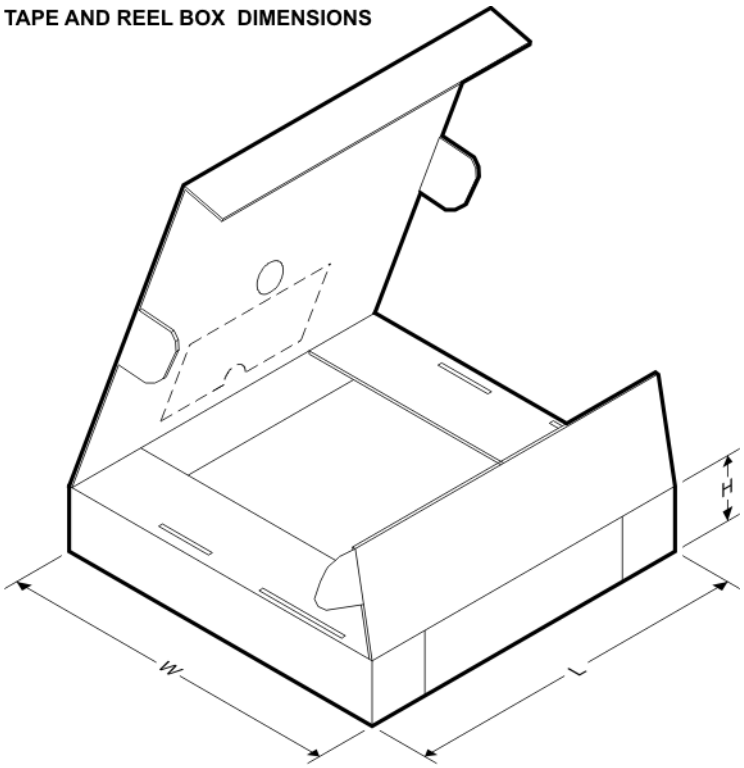
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3556TME/NOPB	DSBGA	YFQ	16	250	178.0	8.4	1.78	1.78	0.69	4.0	8.0	Q1
LM3556TMX/NOPB	DSBGA	YFQ	16	3000	178.0	8.4	1.78	1.78	0.69	4.0	8.0	Q1

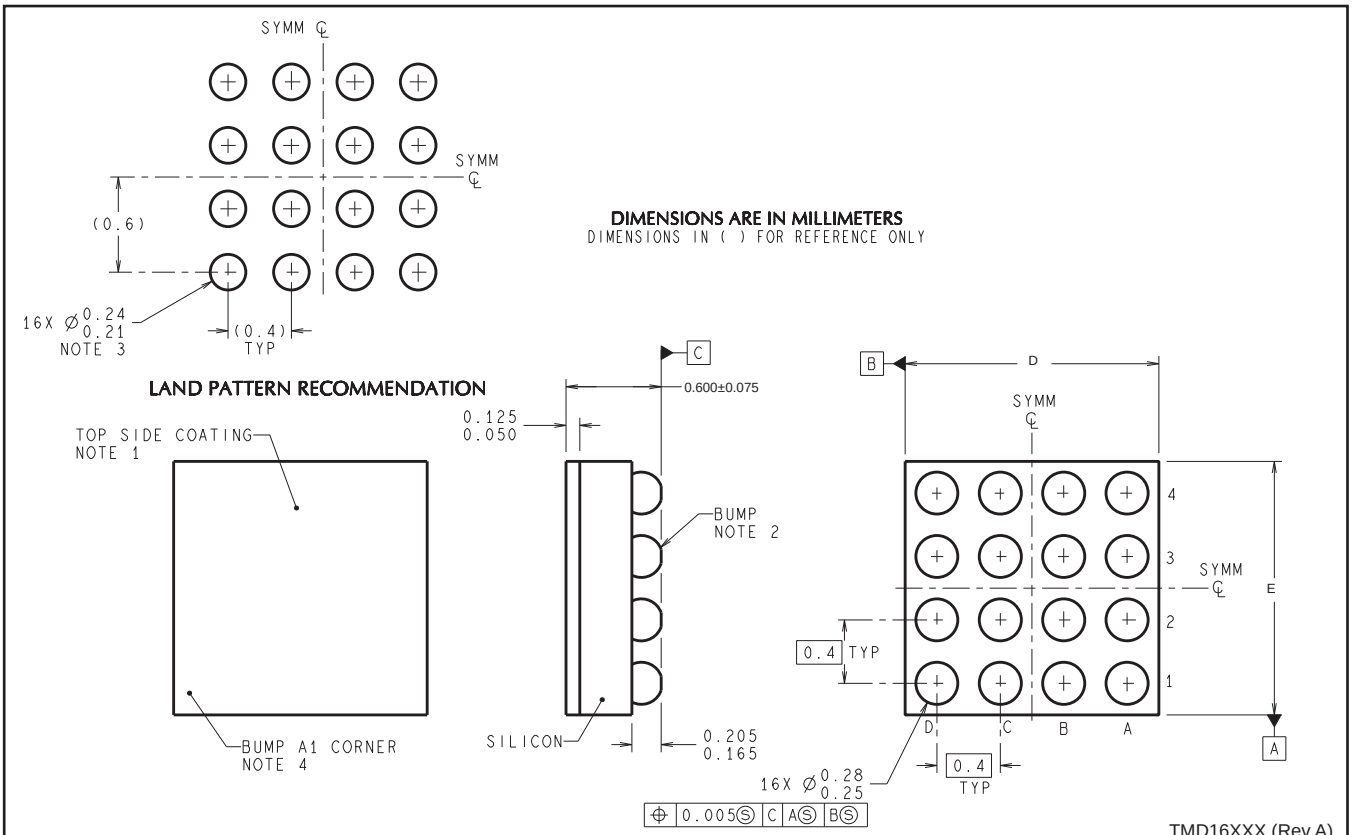
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3556TME/NOPB	DSBGA	YFQ	16	250	210.0	185.0	35.0
LM3556TMX/NOPB	DSBGA	YFQ	16	3000	210.0	185.0	35.0

YFQ0016



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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