Very Low Noise, High Frequency Active RC, Filter Building Block

FEATURES

- **Up to 10MHz Center Frequency on a Single 3V Supply**
- **Easy to Use—A Single Resistor Value Sets Lowpass Cutoff Frequency (200kHz ≤ f_C ≤ 5MHz), Unequal Resistor Values Extend Cutoff Frequency Up to 10MHz**
- **Extremely Flexible—Different Resistor Values Allow Lowpass Transfer Functions with or Without Gain (Butterworth, Chebyshev or Custom)**
- **SNR = 92dB (f_C = 2MHz, 2V_{P-P})**
- **THD = –84dB (f_C = 2MHz, 1V_{P-P})**
- Internal Capacitors Trimmed to ±0.75%
- Single 4-Pole Lowpass Filter or **Matched Pair** of 2-Pole Lowpass Filters
- Can be Connected as a Bandpass Filter
- Single-Ended or Differential Output
- Operates from Single 3V (2.7V Min) to ±5V Supply
- Rail-to-Rail Input and Output Voltages

APPLICATIONS

- Replaces Discrete RC Active Filters and LC Filter Modules
- Antialiasing/Reconstruction Filters
- Dual or I-and-Q Channels (Two Matched 2nd Order Filters in One Package)
- Single-Ended to Differential Conversion
- Video Signal Processing

DESCRIPTION

The LT®1568 is an easy-to-use, active-RC filter building block with rail-to-rail inputs and outputs. The internal capacitors of the IC and the GBW product of the internal low noise op amps are trimmed such that consistent and repeatable filter responses can be achieved. With a single resistor value, the LT1568 provides a pair of **matched** 2-pole Butterworth lowpass filters with unity gain suitable for I/Q channels.

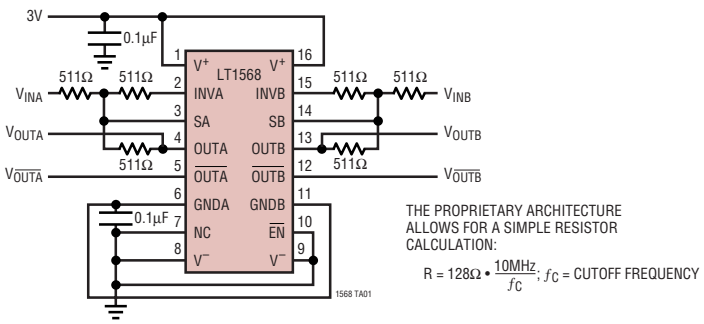
By using unequal-valued external resistors, the two 2-pole sections can create different frequency responses or gains. In addition, the two stages may be cascaded to create a single 4-pole filter with a programmable response. Capable of cutoff frequencies up to 10MHz, the LT1568 is ideal for antialiasing or channel filtering in high speed data communications systems. The LT1568 can also be used as a bandpass filter.

The LT1568 features very low noise, supporting signal-to-noise ratios of over 90dB. It also provides single-ended to differential signal conversion for directly driving high speed A/D converters. The LT1568 has a shutdown mode that reduces supply current to approximately 0.5mA on a 5V supply.

The LT1568 is available in a narrow 16-lead SSOP package.

TYPICAL APPLICATION

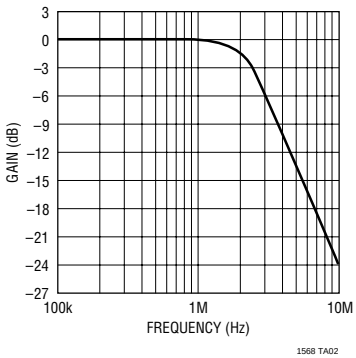
Amplitude and Phase Matched Dual Butterworth 2.5MHz Lowpass Filter with Differential Output. Single 3V Supply Operation



THE PROPRIETARY ARCHITECTURE ALLOWS FOR A SIMPLE RESISTOR CALCULATION:

$R = 128\Omega \bullet \frac{10MHz}{f_C}$; f_C = CUTOFF FREQUENCY

Amplitude Response

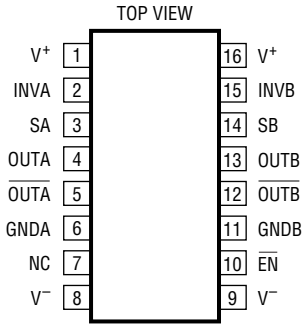


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 11.6V
Input Voltage on INVA, INVB, GNDA and GNDB Pins ..... V^+ to V^-
Input Current on INVA, INVB, GNDA and GNDB Pins (Note 2) ..... ±10mA
Output Short-Circuit Duration on OUTA, OUTB, $\overline{OUTA}$ and $\overline{OUTB}$ Pins ..... Indefinite
Maximum Continuous Output Current (Note 3)
DC ..... ±100mA
Specified Temperature Range (Note 9)
LT1568C ..... –40°C to 85°C
LT1568I ..... –40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 135°C/W

ORDER PART NUMBER
LT1568CGN LT1568IGN
GN PART MARKING
1568 1568I

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications and typical values are at T_A = 25°C. V_S = single 5V, $\overline{EN}$ pin to logic "low," R_L = 400Ω, connected to midsupply, R_{FIL} = R11 = R21 = R31 = R12 = R22 = R32, unless otherwise noted (see Block Diagram).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_S	Total Supply Voltage		●	2.7		11	V
I_S	Supply Current	V_S = 3V	●		24	35	mA
		V_S = 5V	●		26	36	mA
		V_S = ±5V	●		28	38	mA
	Shutdown Supply Current	V_S = 3V, $V_{\overline{EN}}$ = 2.4V	●		0.3	1.0	mA
		V_S = 5V, $V_{\overline{EN}}$ = 4.4V	●		0.5	1.3	mA
		V_S = ±5V, $V_{\overline{EN}}$ = 4.4V	●		1.0	2.5	mA
	Output Voltage Swing High (OUTA, $\overline{OUTA}$, OUTB, $\overline{OUTB}$ Pins)	V_S = 3V, R_{FIL} = 1.28k, R_L = 1k	●	2.75	2.85		V
		V_S = 5V, R_{FIL} = 1.28k, R_L = 1k	●	4.60	4.80		V
		V_S = 5V, R_{FIL} = 128Ω, R_L = 400Ω	●	4.50	4.65		V
		V_S = ±5V, R_{FIL} = 1.28k, R_L = 1k	●	4.60	4.75		V
	Output Voltage Swing Low (OUTA, $\overline{OUTA}$, OUTB, $\overline{OUTB}$ Pins)	V_S = 3V, R_{FIL} = 1.28k, R_L = 1k	●		0.05	0.12	V
		V_S = 5V, R_{FIL} = 1.28k, R_L = 1k	●		0.07	0.15	V
		V_S = 5V, R_{FIL} = 128Ω, R_L = 400Ω	●		0.20	0.40	V
		V_S = ±5V, R_{FIL} = 1.28k, R_L = 1k	●			–4.7	V
I_{OUT}	Maximum Output Current				±80		mA
	Op Amp Input Offset Voltage	V_S = 3V	●	–2.5	–0.5	1.5	mV
		V_S = 5V	●	–2.5	0.2	2.5	mV
		V_S = ±5V	●	–2.0	1.2	4.5	mV
	Inverter Output Offset Voltage	V_S = 3V	●	–2	2.5	7.0	mV
		V_S = 5V	●	–10	0.6	4.5	mV
		V_S = ±5V	●	–12	–4.0	2.0	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications and typical values are at T_A = 25°C. V_S = single 5V, $\overline{EN}$ pin to logic "low," R_L = 400Ω, connected to midsupply, R_{FIL} = R11 = R21 = R31 = R12 = R22 = R32, unless otherwise noted (see Block Diagram).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_B	Op Amp Input Bias Current	V_S = 3V V_S = 5V V_S = ±5V	● ● ●		0.5 0.4 –0.2	2 2 2	µA µA µA
	Inverter Bandwidth (Note 4)				55		MHz
	Inverter Gain (Sections A and B, Note 5)	Frequency = DC Frequency = 2MHz Frequency = 10MHz	●	–0.2	0.01 0.01 0.27	0.2	dB dB dB
	Inverter Phase Shift (Sections A and B, Note 5)	Frequency = DC Frequency = 2MHz Frequency = 10MHz			180 179 176		DEG DEG DEG
SR	Slew Rate (OUTA, OUTB, $\overline{OUTA}$, $\overline{OUTB}$) Pins				53		V/µs
V_{CM}	Common Mode Input Voltage Range (GNDA and GNDB Pins, Note 6)	V_S = 3V V_S = ±5V			1 to 1.9 –3.4 to 2.7		V V
	Single Supply GND Reference Voltage	V_S = 5V, GNDA Tied to GNDB			2.5		V
V_{IL}	$\overline{EN}$ Input Logic Low Level	V_S = 3V, 5V or ±5V	●			V^+ – 2.1	V
V_{IH}	$\overline{EN}$ Input Logic High Level	V_S = 3V, 5V or ±5V	●	V^+ – 0.6			V
	$\overline{EN}$ Input Pull-Up Resistor			30	40		kΩ
t_{DIS}	Disable (Shutdown) Time	$\overline{EN}$ Pin Steps from 0V to V^+			20		µs
t_{EN}	Enable (Start-Up) Time	$\overline{EN}$ Pin Steps from V^+ to 0V			100		µs

FILTER ELECTRICAL CHARACTERISTICS

Specifications are for the output (OUTA or OUTB) of a *single 2nd order section* (A or B) with respect to V_{GND} = V_{GNDA} = V_{GNDB}, gain = –1, R_{FIL} = R11 = R21 = R31 = R12 = R22 = R32, (see Block Diagram). The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications and typical values are at T_A = 25°C. V_S = single 5V, $\overline{EN}$ pin to logic "low," R_L = 400Ω, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ADC	DC Gain		●	–1.01	–1	–0.99	V/V
$V_{OS(OUT)}$	DC Offset Voltage (V_{OUTA} – V_{GNDA}) or (V_{OUTB} – V_{GNDB})	V_S = 3V, f_C = 1MHz, R_{FIL} = 1.28k V_S = 5V, f_C = 1MHz, R_{FIL} = 1.28k V_S = ±5V, f_C = 1MHz, R_{FIL} = 1.28k	● ● ●	–5 –10 –12	2.6 0.6 –4.0	15 10 4	mV mV mV
$\Delta V_{OS(OUT)}$	DC Offset Voltage Mismatch (V_{OUTA} – V_{GNDA}) – (V_{OUTB} – V_{GNDB})	V_S = 3V, f_C = 1MHz, R_{FIL} = 1.28k V_S = 5V, V_S = ±5V, f_C = 1MHz, R_{FIL} = 1.28k	● ●	–8 –10	±4 ±4	8 10	mV mV
Transfer Function Characteristics for Each Section (A or B) to Single-Ended Output (OUTA or OUTB)							
f_C	Cutoff Frequency Range (Note 7)	V_S = 3V, V_S = 5V, V_S = ±5V	●	0.2		10	MHz
TC	Cutoff Frequency Temperature Coefficient		●		±1		ppm/°C

FILTER ELECTRICAL CHARACTERISTICS

Specifications are for the output *(OUTA or OUTB) of a single 2nd order section* (A or B) with respect to $V_{GND} = V_{GNDA} = V_{GNDB}$, gain = –1, $R_{FIL} = R11 = R21 = R31 = R12 = R22 = R32$, (see Block Diagram). The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications and typical values are at $T_A = 25°C$. V_S = single 5V, $\overline{EN}$ pin to logic "low," $R_L = 400\Omega$ connected to midsupply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Filter Gain, f_C = 1MHz, V_S = 5V, R_{FIL} = 1.28k (Measured with Respect to DC Gain)	Test Frequency = 300kHz (0.3 • f_C) Test Frequency = 750kHz (0.75 • f_C) Test Frequency = 1MHz (1 • f_C) Test Frequency = 2MHz (2 • f_C) Test Frequency = 4MHz (4 • f_C)	● ● ● ● 	–0.05 –1.45 –3.60 –13.7 	0.05 –1.20 –3.20 –13.2 –25.0	0.25 –0.85 –2.80 –12.5 	dB dB dB dB dB
	Filter Gain, f_C = 10MHz, V_S = 5V, R_{FIL} = 128Ω (Measured with Respect to DC Gain)	Test Frequency = 1MHz (0.1 • f_C) Test Frequency = 7.5MHz (0.75 • f_C) Test Frequency = 10MHz (1 • f_C) Test Frequency = 20MHz (2 • f_C) Test Frequency = 40MHz (4 • f_C)	● ● ● ● 	–0.1 –1.5 –3.5 –14.2 	0.02 –1.0 –3.0 –13.2 –27.5	0.25 –0.50 –2.40 –12.2 	dB dB dB dB dB
	Filter Gain Mismatch ($\lvert V_{OUTA}\rvert - \lvert V_{OUTB}\rvert$)	f_C = 1MHz, $f_{IN} = f_C$ f_C = 10MHz, $f_{IN} = f_C$	● ●	–0.25 –0.30	±0.02 ±0.02	0.25 0.30	dB dB
	Wideband Output Noise	f_C = 1MHz, R_{FIL} = 1.28k, BW = 2MHz f_C = 10MHz, R_{FIL} = 128Ω, BW = 20MHz			18 34		μV_{RMS} μV_{RMS}
THD	Total Harmonic Distortion	f_C = 1MHz, R_{FIL} = 1.28k, f_{IN} = 200kHz, $V_{IN} = 1V_{P-P}$			–84		dB
		f_C = 10MHz, R_{FIL} = 128Ω, f_{IN} = 2MHz, $V_{IN} = 1V_{P-P}$			–69		dB

Specifications are for the *$\overline{OUTA}$ or $\overline{OUTB}$ of a single 2nd order section* (A or B) with respect to $V_{GND} = V_{GNDA} = V_{GNDB}$, gain = 1, $R_{FIL} = R11 = R21 = R31 = R12 = R22 = R32$, (see Block Diagram) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications and typical values are at $T_A = 25°C$. V_S = single 5V, $\overline{EN}$ pin to logic "low," $R_L = 400\Omega$ connected to midsupply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ADC	DC Gain		●	0.99	1	1.01	V/V
$V_{OS(OUT)}$	DC Offset Voltage ($V_{\overline{OUTA}} - V_{GNDA}$) or ($V_{\overline{OUTB}} - V_{GNDB}$)	V_S = 3V, f_C = 1MHz, R_{FIL} = 1.28k V_S = 5V, V_S = ±5V, f_C = 1MHz, R_{FIL} = 1.28k	● ●	–9 –10	–2 –1	5 10	mV mV
$\Delta V_{OS(OUT)}$	DC Offset Voltage Mismatch ($V_{\overline{OUTA}} - V_{GNDA}$) – ($V_{\overline{OUTB}} - V_{GNDB}$)	V_S = 3V, f_C = 1MHz, R_{FIL} = 1.28k V_S = 5V, V_S = ±5V, f_C = 1MHz, R_{FIL} = 1.28k	● ●	–8 –10	±2 ±2	8 10	mV mV
Transfer Function Characteristics for Each Section (A or B) to Single-Ended Output (OUTA or OUTB)							
f_C	Cutoff Frequency Range (Note 7)	V_S = 3V, V_S = 5V, V_S = ±5V	●	0.2		10	MHz
TC	Cutoff Frequency Temperature Coefficient		●		±1		ppm/°C
	Filter Gain, f_C = 1MHz, V_S = 5V, R_{FIL} = 1.28k (Measured with Respect to DC Gain)	Test Frequency = 300kHz (0.3 • f_C) Test Frequency = 750kHz (0.75 • f_C) Test Frequency = 1MHz (1 • f_C) Test Frequency = 2MHz (2 • f_C) Test Frequency = 4MHz (4 • f_C)	● ● ● ● 	–0.10 –1.40 –3.50 –13.7 	0.15 –1.00 –3.10 –13.0 –25.0	0.40 –0.65 –2.60 –12.5 	dB dB dB dB dB

FILTER ELECTRICAL CHARACTERISTICS

Specifications are for the *OUTA or OUTB of a single 2nd order section* (A or B) with respect to $V_{GND} = V_{GNDA} = V_{GNDB}$, gain = 1, $R_{FIL} = R11 = R21 = R31 = R12 = R22 = R32$, (see Block Diagram) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications and typcial values are at $T_A = 25°C$. V_S = single 5V, $\overline{EN}$ pin to logic "low," $R_L = 400\Omega$ connected to midsupply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Filter Gain, f_C = 10MHz, V_S = 5V, R_{FIL} = 128Ω (Measured with Respect to DC Gain)	Test Frequency = 1MHz (0.1 • f_C) Test Frequency = 7.5MHz (0.75 • f_C) Test Frequency = 10MHz (1 • f_C) Test Frequency = 20MHz (2 • f_C) Test Frequency = 40MHz (4 • f_C)	● ● ● ● 	–0.3 –1.2 –3.1 –12.2 	0.15 –0.50 –2.30 –11.2 –19.1	0.5 0.0 –1.5 –10.2 	dB dB dB dB dB
	Filter Gain Mismatch ($\lvert V_{\overline{OUTA}}\rvert - \lvert V_{\overline{OUTB}}\rvert$)	f_C = 1MHz, $f_{IN} = f_C$ f_C = 10MHz, $f_{IN} = f_C$	● ●	–0.4 –0.5	±0.02 ±0.02	0.4 0.5	dB dB
	Wideband Output Noise	f_C = 1MHz, R_{FIL} = 1.28k, BW = 2MHz f_C = 10MHz, R_{FIL} = 128Ω, BW = 20MHz			22 60		μV_{RMS} μV_{RMS}
THD	Total Harmonic Distortion	f_C = 1MHz, R_{FIL} = 1.28k, f_{IN} = 200kHz, V_{IN} = $1V_{P-P}$			–84		dB
		f_C = 10MHz, R_{FIL} = 128Ω, f_{IN} = 2MHz, V_{IN} = $1V_{P-P}$			–75		dB

Specifications are for the *differential output (OUTA – $\overline{OUTA}$ or OUTB – $\overline{OUTB}$) of a single 2nd order section* (A or B), gain = –2, $R_{FIL} = R11 = R21 = R31 = R12 = R22 = R32$. All voltages are with respect to $V_{GND} = V_{GNDA} = V_{GNDB}$. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications and typical values are at $T_A = 25°C$. V_S = single 5V, $\overline{EN}$ pin to logic "low," $R_{LDIFF} = 800\Omega$ connected at midsupply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ADC	DC Gain		●		–2		V/V
$V_{OS(OUT)}$	DC Offset Voltage (OUTA – $\overline{OUTA}$) or (OUTB – $\overline{OUTB}$)	V_S = 3V, f_C = 1MHz, R_{FIL} = 1.28k V_S = 5V, f_C = 1MHz, R_{FIL} = 1.28k V_S = ±5V, f_C = 1MHz, R_{FIL} = 1.28k	● ● ●	–4 –12 –20	6 2 –5	16 15 10	mV mV mV
$\Delta V_{OS(OUT)}$	DC Offset Voltage Mismatch (OUTA – $\overline{OUTA}$) – (OUTB – $\overline{OUTB}$)	V_S = 3V, f_C = 1MHz, R_{FIL} = 1.28k V_S = 5V, f_C = 1MHz, R_{FIL} = 1.28k V_S = ±5V, f_C = 1MHz, R_{FIL} = 1.28k	● ● ●	–8 –12 –15	2 –2 2	8 12 15	mV mV mV
Transfer Function Characteristics for Each Section (A or B) to Differential Output (OUTA – $\overline{OUTA}$ or OUTB – $\overline{OUTB}$)							
f_C	Cutoff Frequency Range (Note 7)	V_S = 3V, V_S = 5V, V_S = ±5V	●	0.2		10	MHz
TC	Cutoff Frequency Temperature Coefficient		●		±1		ppm/°C
	Filter Gain, f_C = 1MHz, V_S = 5V, R_{FIL} = 1.28k (Note 8) (Measured with Respect to DC Gain)	Test Frequency = 300kHz (0.3 • f_C) Test Frequency = 750kHz (0.75 • f_C) Test Frequency = 1MHz (1 • f_C) Test Frequency = 2MHz (2 • f_C) Test Frequency = 4MHz (4 • f_C)	● ● ● ● 	–0.05 –1.40 –3.60 –13.7 	0.10 –1.10 –3.20 –13.1 –25.0	0.25 –0.80 –2.70 –12.5 	dB dB dB dB dB
	Filter Gain, f_C = 10MHz, V_S = 5V, R_{FL} = 128Ω (Note 8) (Measured with Respect to DC Gain)	Test Frequency = 1MHz (0.1 • f_C) Test Frequency = 7.5MHz (0.75 • f_C) Test Frequency = 10MHz (1 • f_C) Test Frequency = 20MHz (2 • f_C) Test Frequency = 40MHz (4 • f_C)	● ● ● ● 	–0.20 –1.30 –3.30 –13.1 	0.1 –0.8 –2.6 –12.1 –24.3	0.30 –0.20 –1.90 –11.1 	dB dB dB dB dB

FILTER ELECTRICAL CHARACTERISTICS

Specifications are for the *differential output (OUTA – $\overline{OUTA}$ or OUTB – $\overline{OUTB}$) of a single 2nd order section* (A or B), gain = –2, R_{FIL} = R11 = R21 = R31 = R12 = R22 = R32. All voltages are with respect to V_{GND} = V_{GNDA} = V_{GNDB}. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications and typical values are at T_A = 25°C. V_S = single 5V, $\overline{EN}$ pin to logic "low," R_{LDIFF} = 800Ω connected to midsupply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Filter Gain Mismatch $\lvert(V_{OUTA} - V_{\overline{OUTA}})\rvert - \lvert(V_{OUTB} - V_{\overline{OUTB}})\rvert$	f_C = 1MHz, $f_{IN} = f_C$ f_C = 10MHz, $f_{IN} = f_C$	● ●	–0.3 –0.4	±0.10 ±0.15	0.3 0.4	dB dB
	Wideband Output Noise	f_C = 1MHz, R_{FIL} = 1.28k, BW = 2MHz f_C = 10MHz, R_{FIL} = 128Ω, BW = 20MHz			36 88		μV_{RMS} μV_{RMS}
THD	Total Harmonic Distortion	f_C = 1MHz, R_{FIL} = 1.28k, f_{IN} = 200kHz, V_{IN} = $1V_{P-P}$			–84		dB
		f_C = 10MHz, R_{FIL} = 128Ω, f_{IN} = 2MHz, V_{IN} = $1V_{P-P}$			–69		dB

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: The inputs of each op amp are protected by back-to-back diodes. If either differential input voltage exceeds 1.4V, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The inverter bandwidth is measured with the SA or SB output floating, and is defined as the frequency at which the phase shift from OUTA (OUTB) to $\overline{OUTA}$ ($\overline{OUTB}$) drops from 180° to 135°.

Note 5: Measured with the SA or SB output connected in the filter application circuit as shown in the Block Diagram.

Note 6: The common mode input voltage range is measured by shorting the filter input to the common mode reference (GNDA or GNDB) and applying a DC input voltage to search for the common mode voltage range that creates a ±2mV (V_S = 3V) or ±5mV (V_S = ±5V) change in the (OUTA or OUTB) voltage (measured with respect to GNDA or GNDB).

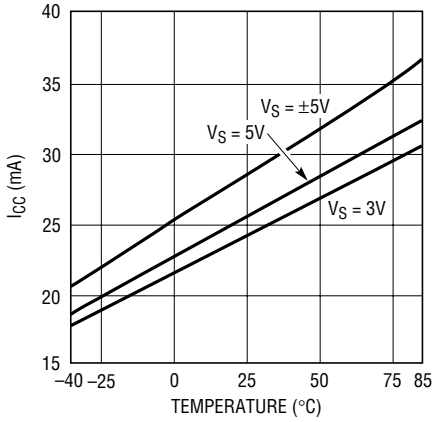
Note 7: The minimum cutoff frequency of the LT1568 is arbitrarily listed as 200kHz. The limit is arrived at by setting the maximum resistor value limit at 6.4k. Due to input bias current, the output DC offset through a single section can be as high as 25mV with resistors this large. The LT1568 can be used with even larger resistors if the large offset voltages can be tolerated. For cutoff frequencies below 200kHz, refer to the LTC1563-2, LTC1563-3.

Note 8: With equal-sized resistors, the differential DC gain through either a single section or cascaded sections is 6dB.

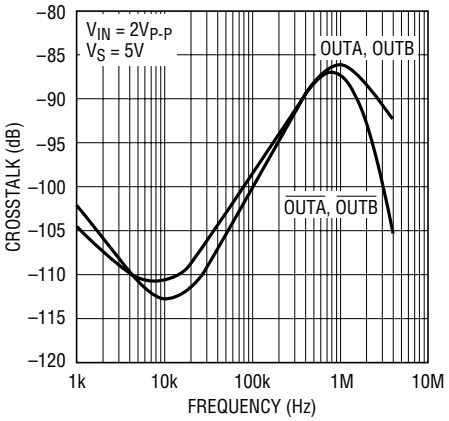
Note 9: The LT1568C is guaranteed to meet specified performance from 0°C to 70°C. The LT1568C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LT1568I is guaranteed to meet specified performance from –40°C to 85°C.

TYPICAL PERFORMANCE CHARACTERISTICS

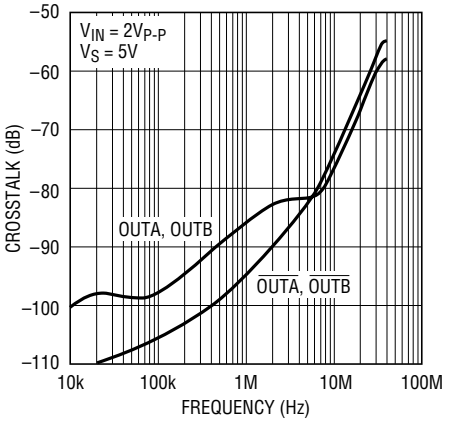
Supply Current vs Temperature



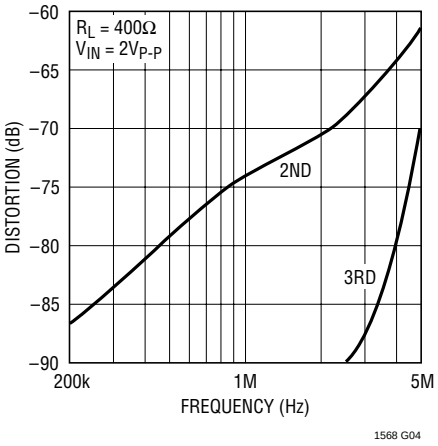
Crosstalk vs Frequency
f_{CUTOFF} = 1MHz



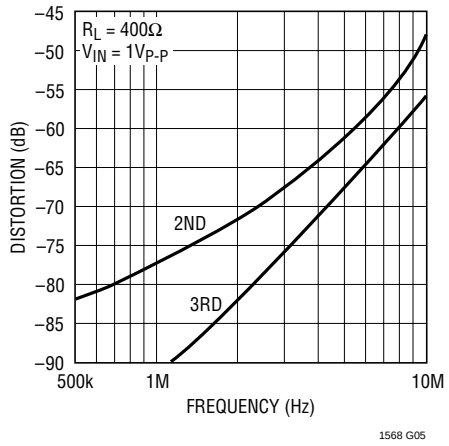
Crosstalk vs Frequency
f_{CUTOFF} = 10MHz



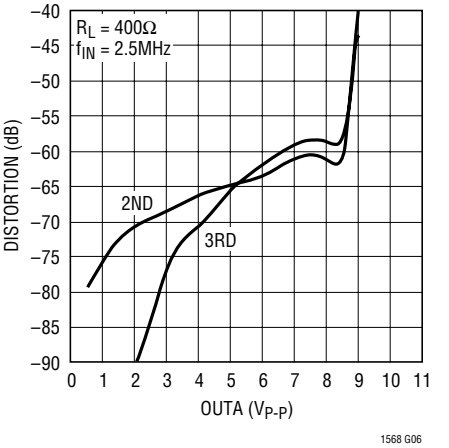
Distortion vs Frequency
V_S = ±5V, f_{CUTOFF} = 5MHz



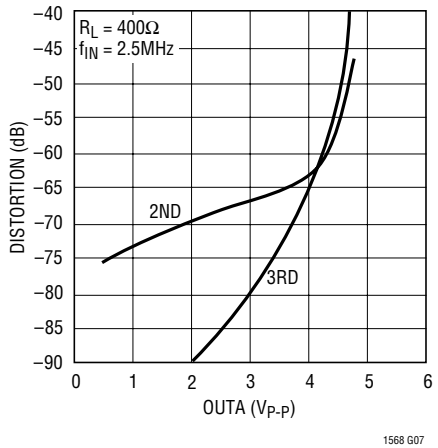
Distortion vs Frequency
V_S = ±5V, f_{CUTOFF} = 10MHz



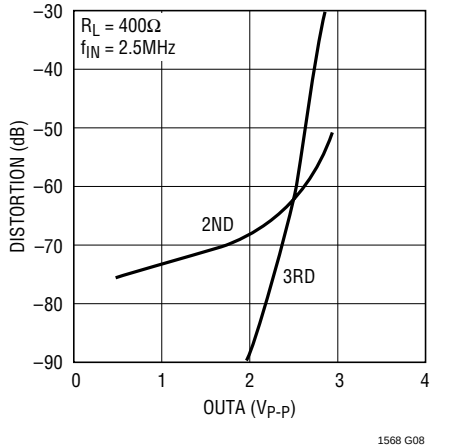
Distortion vs Output Voltage Swing
V_S = ±5V, f_{CUTOFF} = 5MHz



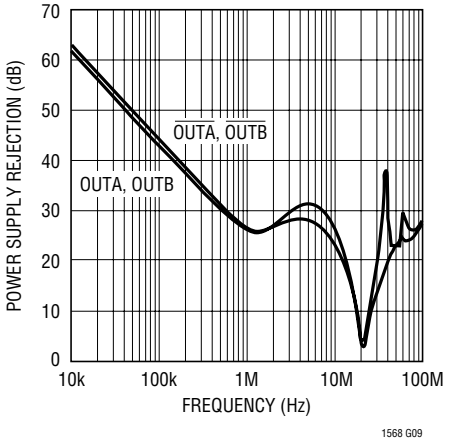
Distortion vs Output Voltage Swing
V_S = 5V, f_{CUTOFF} = 5MHz



Distortion vs Output Voltage Swing
V_S = 3V, f_{CUTOFF} = 5MHz



Power Supply Rejection vs Frequency



PIN FUNCTIONS

V^+ (Pins 1, 16): The V^+ positive supply voltage pins should be tied together and bypassed with a 0.1µF capacitor to an adequate analog ground plane using the shortest possible wiring.

INVA, INVB (Pins 2, 15): Inverting Input. Each of the INV pins is an inverting input of an op amp. Note that the INV pins are high impedance, and are susceptible to coupling of unintended signals. External parasitic capacitance on the INV nodes will also affect the frequency response of the filter sections. For these reasons, printed circuit connections to the INV pins must be kept as short as possible.

SA, SB (Pins 3, 14): Summing Pins. These pins are a summing junction for input signals. Stray capacitance on the SA or SB pins may cause "small" frequency errors of the frequency response near the cutoff frequency (or center frequency). The three external resistors for each section should be located as close as possible to the SA or SB pin to minimize stray capacitance (one picofarad of stray capacitance may add up to 0.1% frequency error).

OUTA, OUTB (Pins 4, 13): Lowpass Output. These pins are the rail-to-rail outputs of op amps. Each output is designed to drive a nominal net load of 400Ω and 30pF.

$\overline{\text{OUTA}}$, $\overline{\text{OUTB}}$ (Pins 5, 12): These pins are the inverted versions of the OUTA and OUTB outputs respectively. Each output is designed to drive a nominal load of 400Ω and 30pF.

GNDA (Pin 6): GNDA serves as the common mode reference voltage for section A. It should be tied to the analog ground plane in a dual supply system. In a single-supply system, an internal resistor divider can be used to establish a half-supply reference point. In that case, GNDA must be bypassed to V^- (Pins 8, 9) by a 0.1µF capacitor.

NC (Pin 7): This pin is not connected internally and can be connected to ground.

V^- (Pins 8, 9): The V^- negative supply voltage pins should be tied together and bypassed to GND by a 0.1µF capacitor in a dual-supply system. In a single-supply system, tie these pins to the ground plane.

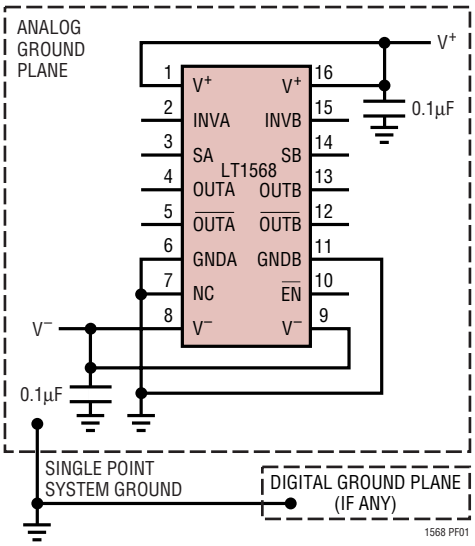
$\overline{\text{EN}}$ (Pin 10): ENABLE. When the $\overline{\text{EN}}$ input goes high or is open circuited, the LT1568 enters a shutdown state which reduces the supply current to approximately 0.5mA (V_S = 5V). The OUTA, OUTB, $\overline{\text{OUTA}}$ and $\overline{\text{OUTB}}$ pins assume high impedance states. GNDA will continue to be biased at half-supply. If an input signal is applied to a complete filter circuit while the LT1568 is in shutdown, some signal will normally flow to the output through passive components around the inactive IC.

$\overline{\text{EN}}$ is connected to V^+ through an internal pull-up resistor of approximately 40k. This defaults the LT1568 to the shutdown state if the $\overline{\text{EN}}$ pin is left floating. Therefore, the user must connect the $\overline{\text{EN}}$ pin to a voltage equal to or less than (V^+ – 2.1)V to enable the part for normal operation. (For example, if V^+ is 5V, then to enable the part the $\overline{\text{EN}}$ pin voltage should be 2.9V or less.)

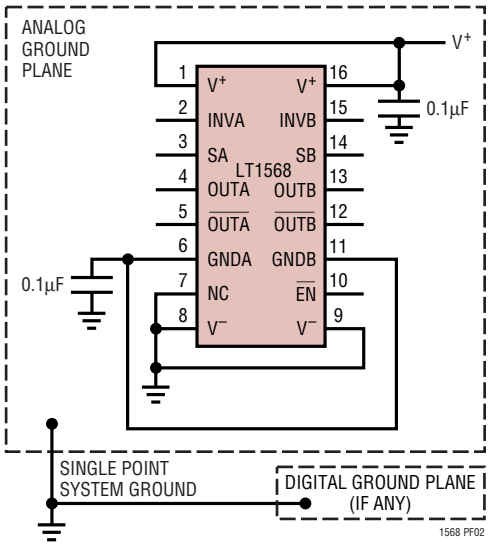
GNDB (Pin 11): GNDB serves as the common mode reference voltage for section B. It should be tied to the analog ground plane in a dual supply system. In a single-supply system, GNDB can be tied to GNDA to set the common mode voltage at half-supply. If it is tied to another reference voltage, GNDB should be bypassed to V^- (Pins 8, 9) by a 0.1µF capacitor.

PIN FUNCTIONS

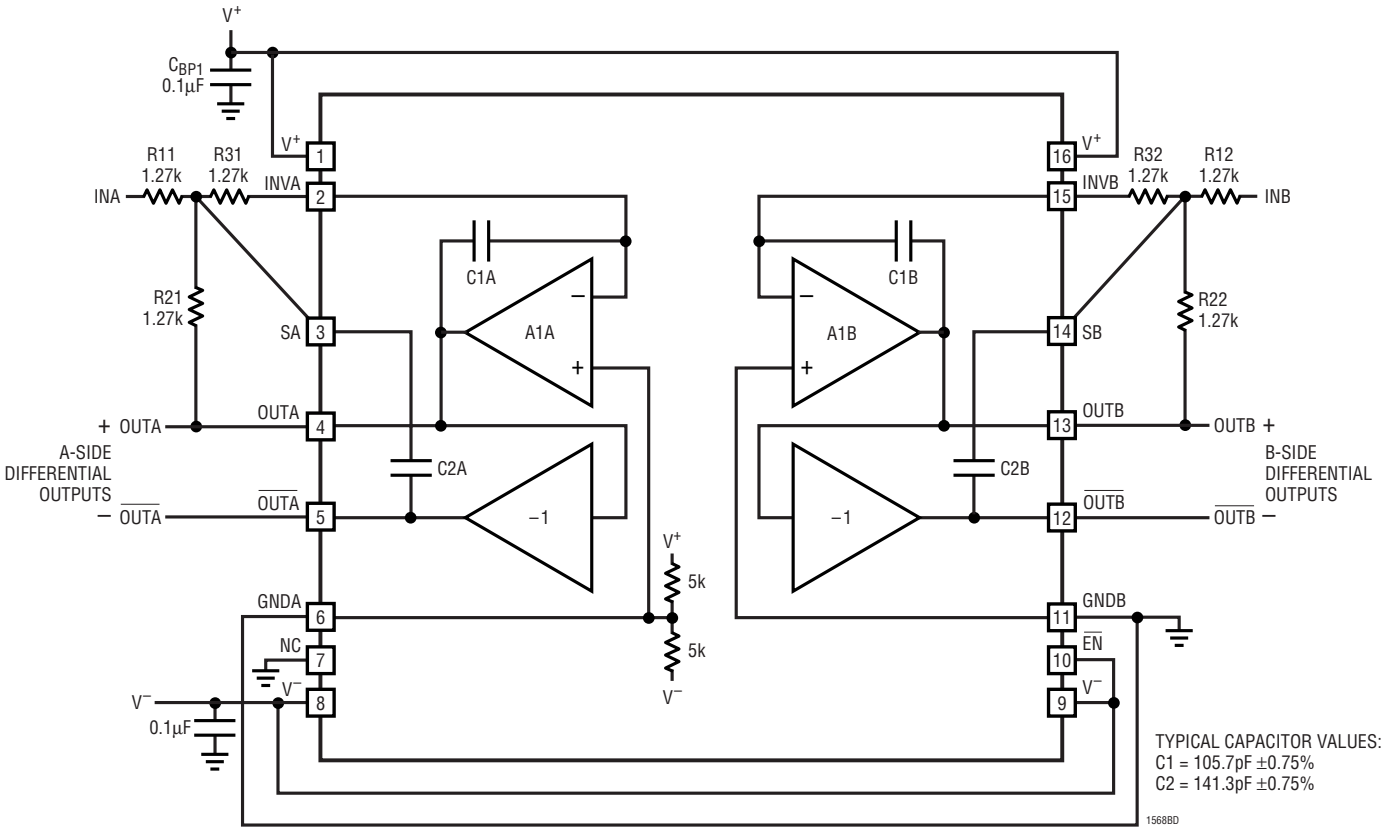
Dual Supply Power and Ground Connections



Single Supply Power and Ground Connections



BLOCK DIAGRAM AND TEST CIRCUIT



APPLICATIONS INFORMATION

The LT1568 has been designed to make the implementation of high frequency filtering functions very easy. Internal low noise amplifiers and capacitors are configured in a topology that requires only three external resistors to implement a 2nd order filter stage. The two 2nd order stages can be used independently or cascaded for simple 4th order filter functions. With two stages integrated on the same die, the matching of the independent sections is better than what can be achieved with separate amplifier components.

OPERATING WITH SINGLE OR DUAL SUPPLIES

Figure 1 shows the recommended connection of an analog ground plane with the LT1568 biased from either symmetrical dual (±V) power supplies or a single supply. Connection of the two GND pins is important to properly DC bias the internal amplifiers. The use of a ground plane helps to minimize noise and stray components to preserve signal integrity and maintain frequency response accuracy.

When biasing from a dual supply, it is recommended that a Schottky diode clamp (BAT54S) be added as shown. These diodes ensure that improper supply voltages, through either reverse polarity or power-up sequencing, do not damage the LT1568.

SIMPLE FILTER IMPLEMENTATIONS

The basic 2nd order filter block of the LT1568, with three external resistors connected as shown in the Block Diagram, has the following lowpass transfer function:

$$\frac{e_{OUT}}{e_{IN}} = -\frac{DC_{GAIN} \bullet (2\pi f_0)^2}{s^2 + \frac{2\pi f_0}{Q} s + (2\pi f_0)^2}$$

where e_{OUT} is either OUTA or OUTB,

$$DC_{GAIN} = \frac{R2}{R1},\ f_0 = \frac{1}{2\pi\sqrt{R2 \bullet R3 \bullet C1 \bullet C2}}$$

and

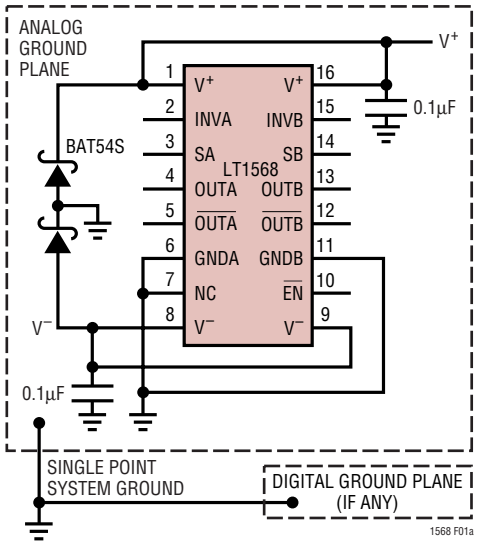
$$Q = \frac{2\pi \bullet C1 \bullet C2 \bullet R1 \bullet R2 \bullet R3 \bullet f_0}{C1 \bullet \left[R1 \bullet (R2 + R3) + R2 \bullet R3\right] - C2 \bullet R1 \bullet R2}$$

The typical values of the internal capacitors are:

C1= 105.7pF
C2 = 141.3pF

These filter functions assume ideal amplifiers.

Dual Supply Power and Ground Connections



Single Supply Power and Ground Connections

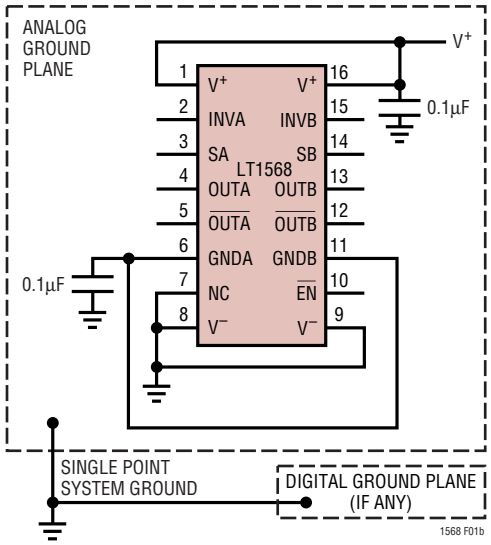


Figure 1. Dual and Single Supply and Ground Plane Connections

APPLICATIONS INFORMATION

The following filter examples are provided to make it easy to design a variety of filter stages. Both 2nd and 4th order filters are shown. For each filer, a table of external resistor values (standard 1% tolerance) is provided. These resistor values have been adjusted to compensate for the finite gain bandwidth product of the LT1568 amplifiers.

To implement a filter, simply connect the resistor values shown in the table for the cutoff frequency desired. If the desired cutoff frequency is not shown in the table of values, use interpolation as recommended in the next section.

DESIGNING FOR ANY CUTOFF FREQUENCY

To implement a lowpass filter with a cutoff frequency not included in the design table, resistor values can be interpolated in the following manner:

For a Cutoff Frequency, f_C, Less Than 1MHz

Start with the resistor values for f_C = 1MHz and then scale them up by the ratio of (1MHz/f_C).

Example: Implement a 2nd order lowpass Chebyshev filter with an f_C of 256kHz. From Table 2 the values for f_C of 1MHz are R11 = R21 = 976Ω and R31 825Ω.

Scaling for f_C = 256kHz:

R11 = R21 = 976Ω • (1MHz/256kHz) ≈ 3.83k

R31 = 825Ω • (1MHz/256kHz) ≈ 3.24k

For a Cutoff Frequency, f_C, Between Values Given in a Design Table

Start with the resistor values for the cutoff frequency closest to the desired one and scale the values up or down accordingly.

Example: Implement a 2nd order lowpass Chebyshev filter with an f_C of 3.2MHz. From Table 2 the closest values are for f_C of 3MHz and are R11 = R21 = 316Ω and R31 = 274Ω.

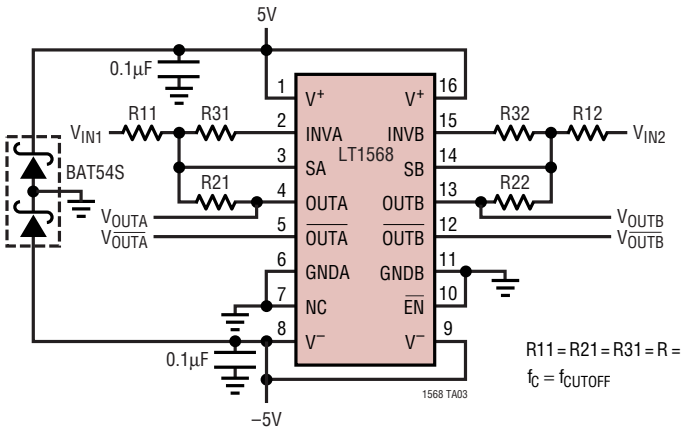
Scaling for f_C = 3.2MHz:

R11 = R21 = 316Ω • (3MHz/3.2MHz) ≈ 294Ω

R31 = 274Ω • (3MHz/3.2MHz) ≈ 255Ω

DUAL 2nd ORDER LOWPASS FILTER DESIGNS

Dual 2nd Order Lowpass Filter,
Dual Supply Operation



$$R11 = R21 = R31 = R = 128\Omega \bullet \frac{10MHz}{f_C}$$

$$f_C = f_{CUTOFF}$$

Dual 2nd Order Lowpass Filter,
Single Supply Operation

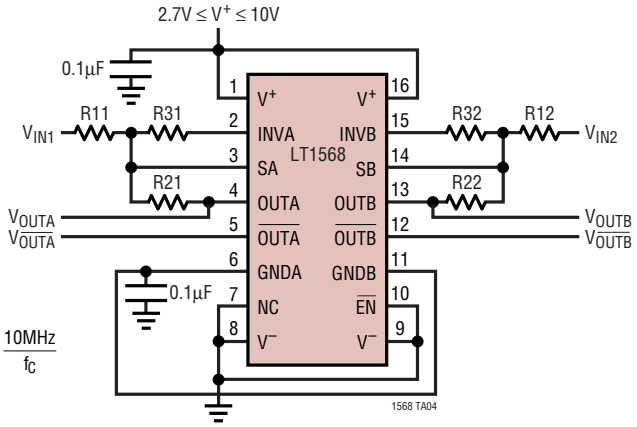
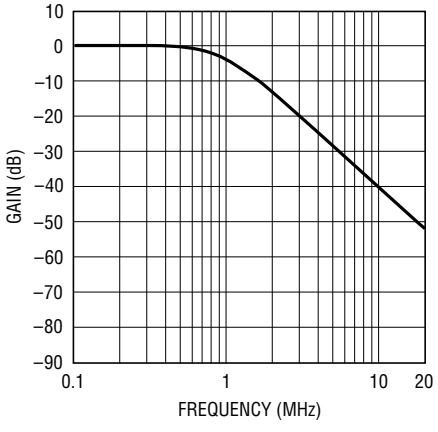


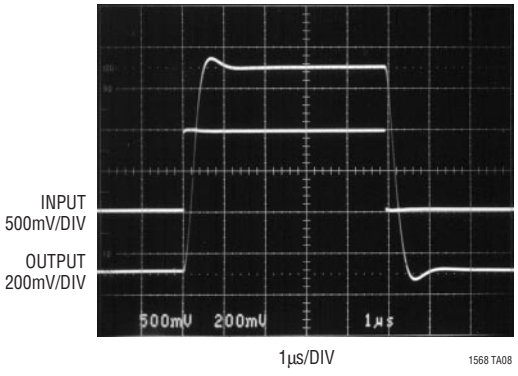
Table 1. Resistor Values in Ohms, Dual 2nd Order Butterworth, Gain = 1, R12 = R11, R22 = R21, R32 = R31

f_{CUTOFF} (MHz)	R11 = R21 = R31
0.2	6340Ω
0.5	2550Ω
1	1270Ω
2	634Ω
3	422Ω
4	324Ω
5	255Ω
6	210Ω
7	182Ω
8	162Ω
9	143Ω
10	127Ω

Amplitude Response
2nd Order Butterworth, f_{CUTOFF} = 1MHz



Transient Response
2nd Order Butterworth, f_{CUTOFF} = 1MHz

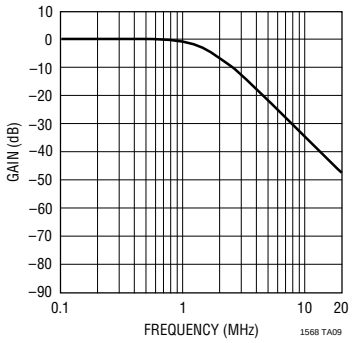


DUAL 2nd ORDER LOWPASS FILTER DESIGNS

Table 2. Resistor Values in Ohms, Dual 2nd Order Lowpass Chebyshev, ±0.25dB Passband Ripple, Gain = 1, R11 = R12, R21 = R22, R31 = R32

f_{CUTOFF} (MHz)	R11, R21	R31
1	976Ω	825Ω
2	475Ω	412Ω
3	316Ω	274Ω
4	226Ω	205Ω
5	178Ω	165Ω
6	143Ω	137Ω
7	121Ω	118Ω

Amplitude Response 2nd Order Lowpass Chebyshev, ±0.25dB Passband Ripple, f_{CUTOFF} = 1MHz



Transient Response 2nd Order Lowpass Chebyshev, ±0.25dB Passband Ripple, f_{CUTOFF} = 1MHz

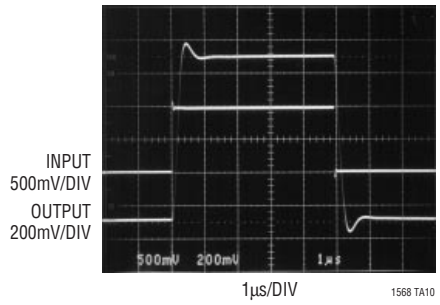
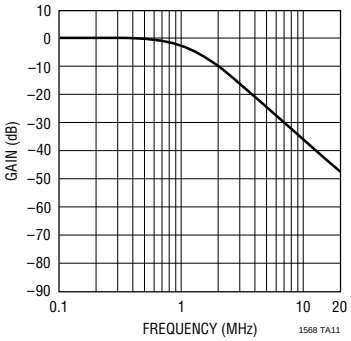


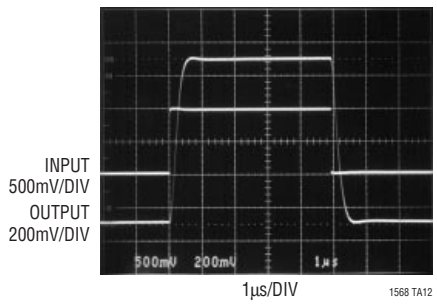
Table 3. Resistor Values in Ohms, Dual 2nd Order Lowpass Bessel, Gain = 1

f_{CUTOFF} (MHz)	R11, R21	R31
1	866Ω	1180Ω
2	422Ω	590Ω
3	280Ω	383Ω
4	210Ω	287Ω
5	165Ω	232Ω
6	137Ω	191Ω
7	115Ω	162Ω

Amplitude Response 2nd Order Lowpass Bessel, f_{CUTOFF} = 1MHz

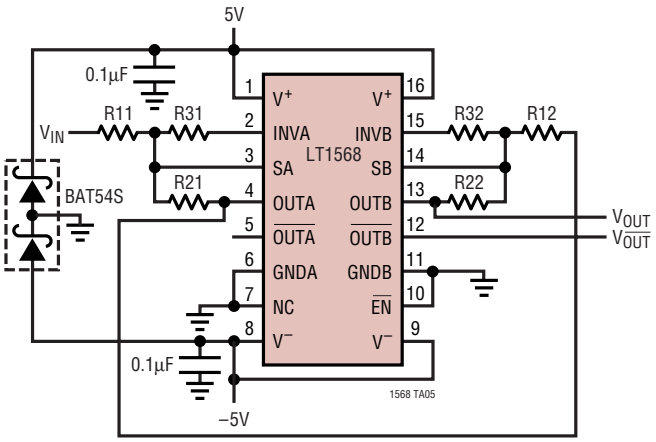


Transient Response 2nd Order Lowpass Bessel, f_{CUTOFF} = 1MHz



4th ORDER LOWPASS FILTER DESIGNS

4th Order Lowpass Filter,
Dual Supply Operation



4th Order Lowpass Filter,
Single Supply Operation

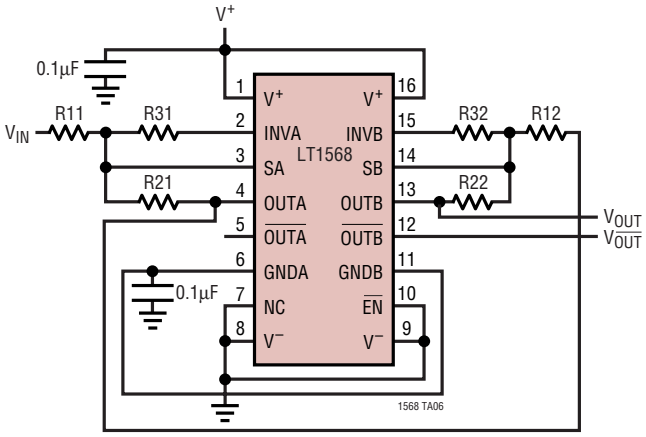
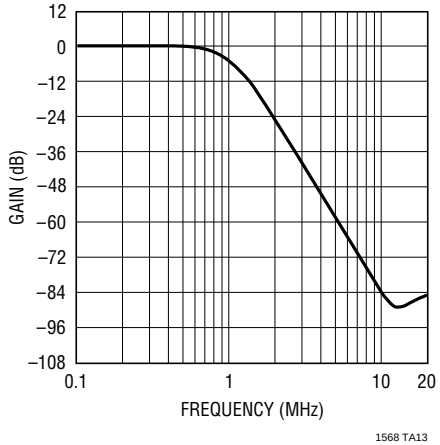


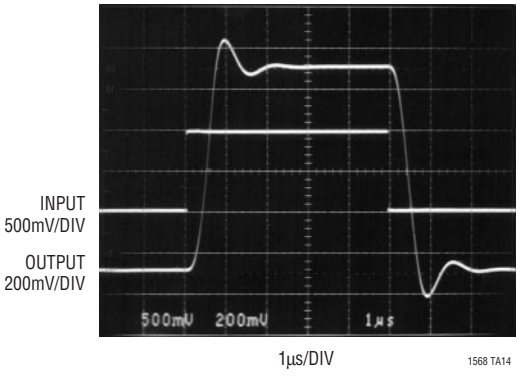
Table 4. Resistor Values in Ohms, 4th Order Lowpass Butterworth, Gain = 1

f_{CUTOFF} (MHz)	R11, R21	R31	R12, R22	R32
1	1.05k	1.58k	1.82k	887Ω
2	523Ω	787Ω	909Ω	432Ω
3	348Ω	523Ω	590Ω	294Ω
4	255Ω	383Ω	432Ω	215Ω
5	205Ω	309Ω	348Ω	174Ω
6	169Ω	255Ω	280Ω	143Ω
7	143Ω	221Ω	232Ω	124Ω
8	124Ω	196Ω	196Ω	107Ω
9	107Ω	174Ω	169Ω	97.6Ω
10	97.6Ω	158Ω	143Ω	88.7Ω

Amplitude Response
4th Order Lowpass Butterworth Lowpass, f_{CUTOFF} = 1MHz



Transient Response
4th Order Lowpass Butterworth Lowpass, f_{CUTOFF} = 1MHz

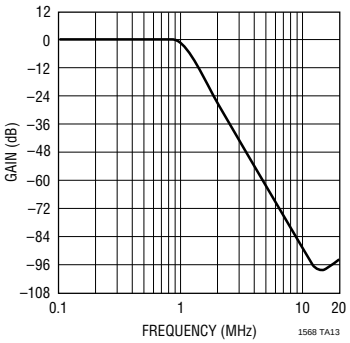


4th ORDER LOWPASS FILTER DESIGNS

Table 5. Resistor Values in Ohms, 4th Order Lowpass Chebyshev, ±0.25dB Passband Ripple, Gain = 1

f_{CUTOFF} (MHz)	R11, R21	R31	R12, R22	R32
1	1.87k	2.05k	2.21k	634Ω
2	931Ω	1.05k	1.10k	324Ω
3	604Ω	681Ω	698Ω	205Ω
4	453Ω	511Ω	499Ω	154Ω
5	357Ω	402Ω	383Ω	121Ω
6	287Ω	332Ω	309Ω	100Ω
7	243Ω	287Ω	255Ω	86.6Ω
8	205Ω	249Ω	215Ω	76.8Ω
9	178Ω	221Ω	182Ω	66.5Ω
10	154Ω	196Ω	158Ω	61.9Ω

Amplitude Response 4th Order Lowpass Chebyshev, ±0.25dB Passband Ripple, f_{CUTOFF} = 1MHz



Transient Response 4th Order Lowpass Chebyshev, ±0.25dB Passband Ripple, f_{CUTOFF} = 1MHz

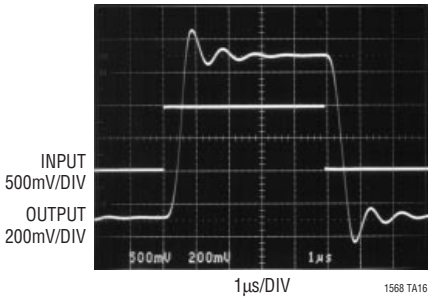
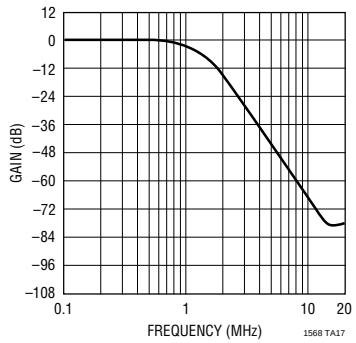


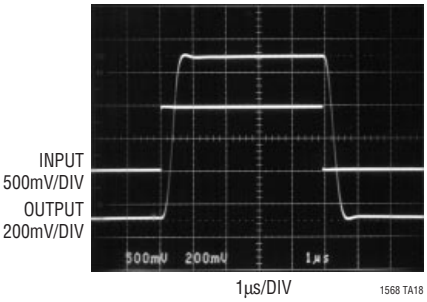
Table 6. Resistor Values in Ohms, 4th Order Lowpass Bessel, Gain = 1

f_{CUTOFF} (MHz)	R11, R21	R31	R12, R22	R32
1	715Ω	1.15k	1.91k	324Ω
2	357Ω	562Ω	432Ω	365Ω
3	237Ω	374Ω	280Ω	243Ω
4	174Ω	280Ω	205Ω	187Ω
5	137Ω	221Ω	162Ω	147Ω
6	115Ω	187Ω	130Ω	124Ω

Amplitude Response 4th Order Lowpass Bessel, f_{CUTOFF} = 1MHz

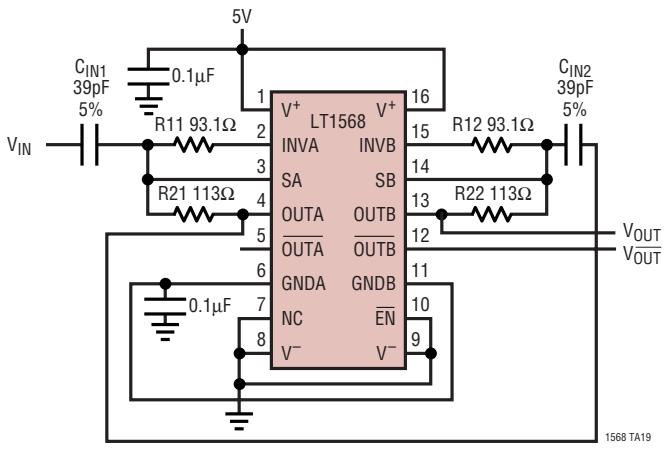


Transient Response 4th Order Lowpass Bessel, f_{CUTOFF} = 1MHz

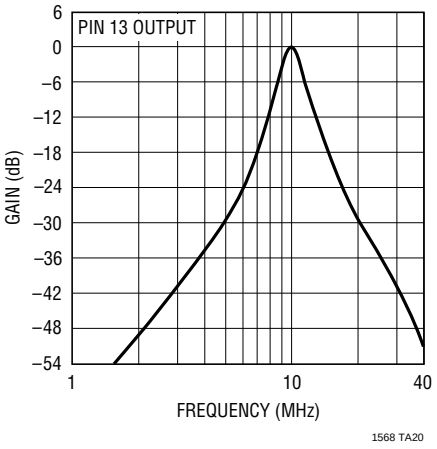


TYPICAL APPLICATIONS

4th Order Bandpass Filter
f_{CENTER} = 10MHz, –3dB Passband = f_{CENTER}/5.4

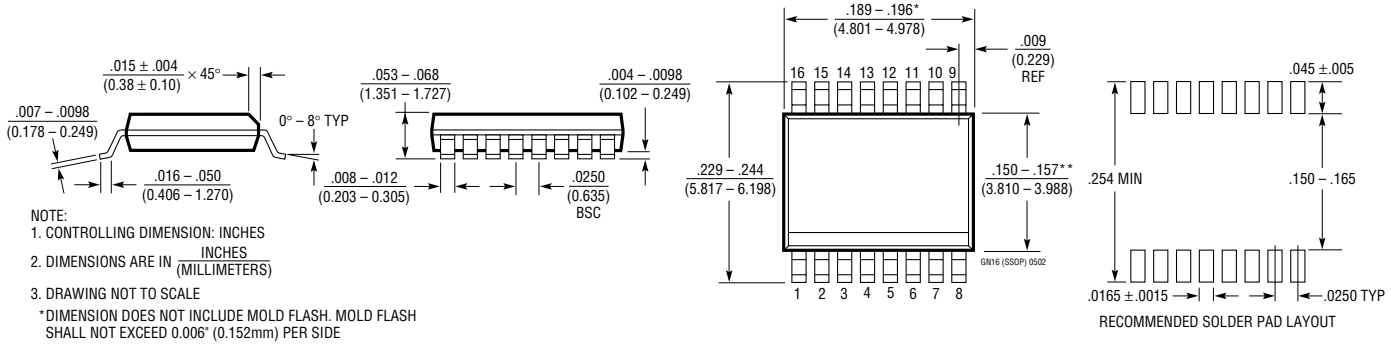


Amplitude Response
4th Order Bandpass Filter f_{CENTER} = 10MHz



PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC®1563	4th Order Filter Building Block	Lowpass or Bandpass Filter Designs, 256Hz to 256kHz
LTC1565-31	7th Order, Fully Differential 650kHz Lowpass Filter	SO-8, No External Components
LTC1566-1	7th Order, Fully Differential 2.3MHz Lowpass Filter	SO-8, No External Components
LT1567	Very Low Noise Op Amp and Inverter	1.4nV/√Hz Op Amp, MSOP Package, Differential Outputs
LT6600-10	Fully Differential 10MHz Lowpass Filter	55µV_{RMS} Noise 100kHz to 10MHz, Operates with 3V Supply
LT6600-20	Fully Differential 20MHz Lowpass Filter	86µV_{RMS} Noise 100kHz to 20MHz, Operates with Single 3V Supply

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