SUNTSU

Metal Half Size Dip CMOS VCXO

# SVCHSC Series

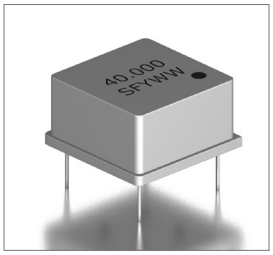
13.2mm x 13.2mm

## Features

- ±20ppm (Frequency Stability) Available
- Standard Half Size Package
- CMOS/TTL Compatible
- Fundamental or PLL (Phase Lock Loop) Available

## Applications

- Phase Locked Loops Circuit
- Synthesizers
- Base Stations




## Part Numbering Guide

**SVC HS C 3 A 48 A - 40.000M**

- **SUNTSU VCXO**
- **HALF SIZE**
- **CMOS**
- **SUPPLY VOLTAGE**
  - 3 : 3.3V±5%
  - 5 : 5.0V±5%
- **FREQUENCY STABILITY**
  - A : ±50ppm
  - B : ±30ppm
  - C : ±25ppm
  - D : ±20ppm
  - *E : ±15ppm
- **OPERATING TEMPERATURE RANGE**
  - 07 : 0°C - +70°C
  - 16 : -10°C - +60°C
  - 17 : -10°C - +70°C
  - 27 : -20°C - +70°C
  - 38 : -30°C - +85°C
  - 48 : -40°C - +85°C
- **PULLABILITY**
  - A : ±150ppm
  - B : ±100ppm
  - C : ±80ppm
  - D : ±50ppm
- **FREQUENCY**
  - MHz

RoHS COMPLIANT

Cage Code: 4GUT4

To customize your parameters contact a Suntsu representative.

* For frequency stability option E contact a Suntsu representative.

| Electrical Parameters | Units | Minimum | Typical | Maximum | Remarks |
|---|---|---|---|---|---|
| Frequency Range | MHz | 1 | | 160 | |
| Frequency Stability (Includes Initial Tolerance at 25°C, Frequency Stability over Operating Temperature, Output Load Change, Supply Voltage Change, and First Year Aging at 25°C.) | ppm | -20 | | +20 | See part numbering guide for options. |
| Operating Temperature | °C | -40 | | +85 | See part numbering guide for options. |
| Storage Temperature | °C | -55 | | +125 | |
| Supply Voltage ($V_{DD}$) 3.3V Option | V | 3.135 | 3.3 | 3.465 | |
| Supply Voltage ($V_{DD}$) 5.0V Option | V | 4.750 | 5.0 | 5.250 | |
| Current ($I_{DD}$) 3.3V Option | mA | | | 40 | |
| Current ($I_{DD}$) 5.0V Option | mA | | | 50 | |
| Current Voltage ($V_C$) 3.3V Option | V | 0.3 | | 3.0 | |
| Current Voltage ($V_C$) 5.0V Option | V | 0.5 | | 4.5 | |
| Pullability | ppm | ±50 | ±100 | ±150 | See part numbering guide for options. |
| Linearity | % | | | 10 | |
| Output Load (CMOS) | pF | | | 15 | |
| Output Load (TTL) | TTL | | | 10 | |
| CMOS Output Logic HIGH ($V_{OH}$) | V | 0.9*$V_{DD}$ | | | |
| CMOS Output Logic LOW ($V_{OL}$) | V | | | 0.1*$V_{DD}$ | |
| TTL Output Logic HIGH ($V_{OH}$) | V | 2.4 | | | |
| TTL Output Logic LOW ($V_{OL}$) | V | | | 0.4 | |
| Rise ($T_R$) And Fall ($T_F$) Time | ns | | | 5 | |
| Symmetry (Duty Cycle) | % | 45 | 50 | 55 | |
| Start-Up Time | ms | | | 10 | |
| Phase Jitter (12KHz ~ 20MHz) | ps | | | 1 | AT-Cut Fundamental |
| Phase Jitter (12KHz ~ 20MHz) | ps | | | 5 | PLL (Phase Lock Loop) |


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Specifications are subject to change without notice.

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**Call: +1-949-783-7300 | Fax: +1-949-783-7301**

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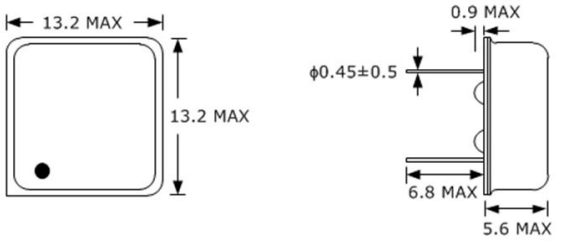
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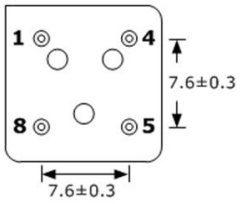
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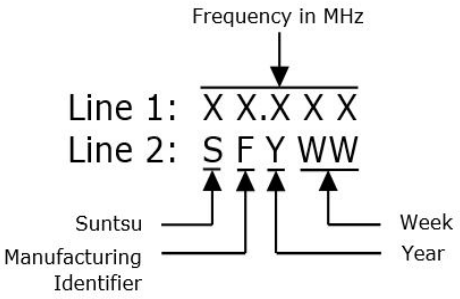
13.2mm x 13.2mm

## Outline Drawing & Part Marking

All dimensions are in millimeters (mm) unless otherwise noted. Drawings are not to scale.

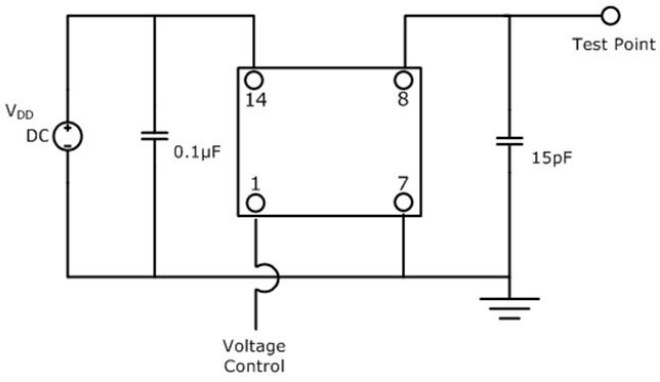


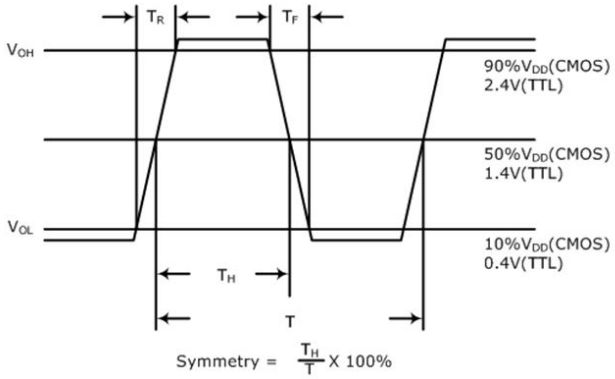




| PIN | FUNCTION |
|---|---|
| 1 | VOLTAGE CONTROL |
| 4 | GND |
| 5 | OUTPUT |
| 8 | $V_{DD}$ |

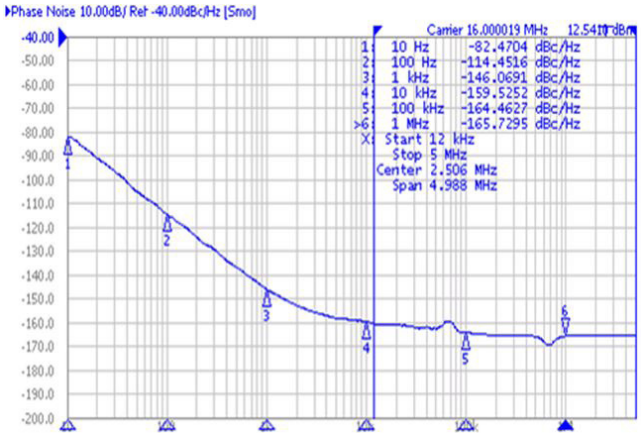
## Test Circuit (CMOS/TTL Compatible)



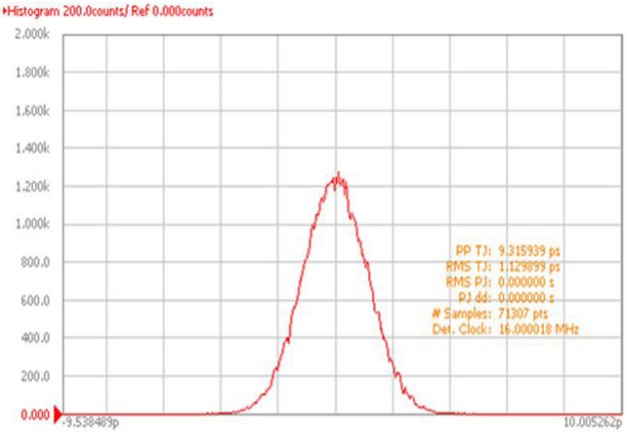

## Waveform (CMOS/TTL Compatible)




## Typical Phase Noise and Jitter Performance (Measured By Agilent E5052A)




Frequency - 16.000MHz




Frequency - 16.000MHz


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| Environmental Specifications | | Mechanical Specifications | |
|---|---|---|---|
| Temperature Cycling | MIL-STD-883, Method 1010, Condition B | Mechanical Shock | MIL-STD-202, Method 213, Condition B |
| Fine Leak Test | MIL-STD-883, Method 1014, Condition A | Vibration | MIL-STD-883, Method 2007, Condition A |
| Gross Leak Test | MIL-STD-883, Method 1014, Condition C | Moisture Resistance | MIL-STD-883, Method 1004 |
| Solderability | MIL-STD-883, Method 2003 | Resistance to Solvents | MIL-STD-202, Method 215 |
| Moisture Sensitivity | J-STD-020, MSL 1 | Resistance to Soldering Heat | MIL-STD-202, Method 210, Condition K |



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