Translation Loop, PLL, VCO Module

Data Sheet

ADF4401A

FEATURES

RF output frequency range: 62.5 MHz to 8000 MHz
VCO frequency range: 4 GHz to 8 GHz
9 fs rms jitter at 8 GHz output
17 dBm IF output power at 6 GHz RF output
90 dBc LO_IN to RF output
90 dBc spurious-free dynamic range
Low phase noise, voltage controlled oscillator
Programmable divide by 1, 2, 4, 8, 16, 32, or 64 output
3.3 V analog, digital, and mixer power supplies
5 V amplifier and VCO power supply
RF output mute function
18.00 mm × 18.00 mm, 80-terminal LGA_CAV
Supported in the ADIsimPLL design tool

APPLICATIONS

Instrumentation and measurement
Automated test equipment
Aerospace and defense

FUNCTIONAL BLOCK DIAGRAM

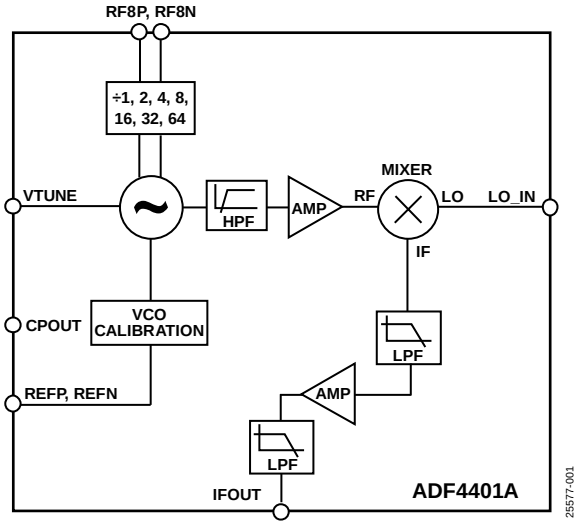


Figure 1.

GENERAL DESCRIPTION

The ADF4401A is a fully integrated, system in package (SiP) translation loop (also known as an offset loop) module that includes a voltage controlled oscillator (VCO) and calibration phase-locked loop (PLL) circuit. Designed for highly jitter sensitive applications, this solution reduces board space and complexity compared to traditional discrete translation loop solutions designed on a printed circuit board (PCB). The time to market is significantly reduced by taking advantage of this highly integrated solution with in package circuitry and enhanced isolation that attenuates spurious components. The ADF4401A provides a frequency synthesis solution for engineers designing highly competitive systems.

The ADF4401A requires an external phase detector or phase frequency detector (PFD) and an external local oscillator (LO) to form a frequency synthesis solution.

The ADF4401A implements an integrated downconversion mixing stage in the feedback loop that sets the loop gain to 1 and minimizes the in band phase noise. By combining the frequency downconversion stage and low noise, integrated, wideband, VCO technology from Analog Devices, Inc., the ADF4401A offers a wideband jitter performance of 9 fs rms at 8 GHz output. The output jitter performance is largely dependent on the performance of the external offset LO.

The ADF4401A module uses an internal PFD and VCO calibration circuitry to select the appropriate VCO band. The user can disable the calibration circuitry and close the loop using the external PFD. All on-chip registers are controlled via a serial port interface (SPI).

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REVISION HISTORY

12/2020—Revision 0: Initial Version

SPECIFICATIONS

Supply voltage (AV_{DD}) = VCC_PLL = VCC_CAL = VRF_INT = VRF_OUT = VCC_DIV = VCC_NDIV = VCC_REG = VCC_MIX = 3.3 V ± 5%, VCC_VCO = VCC_RF = VCC_IF1 = VCC_IF2 = 5 V ± 5%, GND = 0 V, dBm referred to 50 Ω, and T_A = −25°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RF OUTPUT CHARACTERISTICS					
RF Output Frequency	62.5		8000	MHz	
RF Output Power (RF_OUT_POWER = 11)		8		dBm	RF8N = 1 GHz, 3.3 nH inductor to VRF_OUT, single-ended
		1		dBm	RF8N = 8 GHz, 3.3 nH inductor to VRF_OUT, single-ended
RF Output Power Variation		±1		dB	RF8P or RF8N = 5 GHz
RF Output Power Variation (over Frequency)		±4		dB	RF8P or RF8N = 1 GHz to 8 GHz
Harmonic Content (RF8P and RF8N)					
Second Harmonic		−25		dBc	Fundamental VCO output
		−25		dBc	Divided VCO output
Third Harmonic		−12		dBc	Fundamental VCO output
		−15		dBc	Divided VCO output
LO_IN to RF Output		90		dBc	
Spurious-Free Dynamic Range		90		dBc	Within 100 MHz offset of carrier
		−90		dBc	>100 MHz offset of carrier, RF output (RF_{OUT}) > 1 GHz
EXTERNAL LO					
LO_IN Frequency (Doubler Disabled)	3.0		9.0	GHz	
LO_IN Frequency (Doubler Enabled)	1.5		4.5	GHz	
External LO Power (LO_IN)	−3	0	+3	dBm	
External LO Port Return Loss		8		dB	
VCO Frequency Feedthrough		−23		dBm	Measured at LO_IN
Other Spurious Feedthrough		−40		dBm	Measured at LO_IN
Input Power for 1 dB Output Compression (P1dB)		6		dBm	
INTERMEDIATE FREQUENCY (IF) OUTPUT					
IF Output Frequency (f_{IF})	50		1000	MHz	
IF Output Power		17		dBm	6 GHz RF output, internal RF setting = 1, LO power = 0 dBm, LO_IN = 6.6 GHz, f_{IF} = 600 MHz
		12		dBm	Internal RF setting = 0, LO power = 0 dBm, LO_IN = 6.6 GHz, f_{IF} = 600 MHz
LO_IN to IFOUT Isolation		−82		dBc	Internal RF setting = 0, LO_IN = 0 dBm,
Other Spurious Signals on IFOUT		−20		dBc	Main contributor is IFOUT harmonics
IF Output Return Loss		−9		dB	
Mismatch for Compliant Operation		−10		dB	≤900 MHz
		−2		dB	>900 MHz
LOGIC INPUTS					$\overline{CS}$, SDIO, SCLK, X2_EN, and CE are 3 V logic
Input High Voltage (V_{INH})	1.5			V	
Input Low Voltage (V_{INL})			0.4	V	
Input High Current (I_{INH}) and Input Low Current (I_{INL})			±1	μA	$\overline{CS}$, SDIO, SCLK, and CE
			±100	μA	X2_EN
Input Capacitance (C_{IN})		3.0		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS					
Output High Voltage (V_{OH})	AV_{DD} − 0.4			V	3.3 V output selected
	1.5	1.875		V	1.8 V output selected
Output High Current (I_{OH})			500	µA	
Output Low Voltage (V_{OL})			0.4	V	Output low current (I_{OL}) = 500 µA
POWER SUPPLIES					
AV_{DD} (Except VCO, Mixer, and Amplifier)	3.15	3.3	3.45	V	VCC_PLL, VCC_CAL, VRF_OUT, VRF_INT, VCC_DIV, VCC_NDIV, and VCC_REG are grouped as AV_{DD} and are at the same voltage
VCC_MIX	3.15	3.3	3.45	V	Must be equal to AV_{DD}
VCC_VCO	4.75	5	5.25	V	
VCC_RF	4.75	5	5.25	V	Voltages must equal VCC_VCO
VCC_IF1	4.75	5	5.25	V	
VCC_IF2	4.75	5	5.25	V	
Calibration PLL Supply Current (I_{PLL})					VCC_CAL, VCC_NDIV, VCC_PLL, and VCC_REG
		88		mA	Calibration mode
		26		mA	Translation loop mode
Output Divider Supply Current (I_{CC_DIV})		63		mA	RF output disabled, internal RF enabled
Divider = 1		75		mA	RF output and internal RF enabled
Divider = 2		89		mA	
Divider = 4		103		mA	
Divider = 8		112		mA	
Divider = 16		117		mA	
Divider = 32		121		mA	
Divider = 64		124		mA	
RF Output Supply Current (I_{RF_OUT})		4		mA	RF output disabled
		17		mA	RF_OUT_POWER = −4 dBm
		31		mA	RF_OUT_POWER = −1 dBm
		44		mA	RF_OUT_POWER = 2 dBm
		57		mA	RF_OUT_POWER = 5 dBm
Internal RF Supply Current (I_{RF_INT})		<1		µA	Internal RF disabled
		14		mA	POUT_AUX = low power for 0
		28		mA	POUT_AUX = high power for 1
VCO Supply Current (I_{CC_VCO})		140	200	mA	
RF Amplifier Current (I_{CC_RF})		76	90	mA	
I_{CC_IF1} Amplifier Current		76	90	mA	
I_{CC_IF2} Amplifier Current		76	90	mA	
Mixer Supply Current (I_{CC_MIX})					
LO Doubler Disabled		120	140	mA	
LO Doubler Enabled		136	160	mA	
3.3 V Total Current		386	473	mA	RF output enabled, RF output Setting 3, RF divider Setting 1, internal RF Setting 1, calibration PLL enabled, mixer LO doubler enabled
		308		mA	RF output enabled, RF output Setting 3, RF divider Setting 1, internal RF Setting 1, calibration PLL disabled, mixer LO doubler disabled
5 V Total Current		368	470	mA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CALIBRATION PLL SPECIFICATIONS					When used as internal PLL for frequency tuning, PLL and charge pump specifications do not apply when used as VCO only
REFP and REFN Characteristics					
Input Frequency	10		500	MHz	
Input Sensitivity					
Single-Ended Mode	0.4		AV_{DD}	V p-p	REFP biased at $AV_{DD}/2$, ac coupling ensures $AV_{DD}/2$ bias
Differential Mode	0.4		1.8	V p-p	Low voltage differential signal (LVDS) and low voltage positive emitter coupled logic (LVPECL) compatible, REFP and REFN biased at 2.1 V, ac coupling ensures 2.1 V bias
C_{IN}					
Single-Ended Mode		6.9		pF	
Differential Mode		1.4		pF	
Input Current			±150	µA	Single-ended reference programmed
			300	µA	Differential reference programmed
Phase Detector Frequency			125	MHz	
CHARGE PUMP (CALIBRATION ONLY)					
Charge Pump Current (I_{CP}), Sink and Source					
High Value		5.6		mA	
Low Value		0.35		mA	
VCO CHARACTERISTICS					
VCO Frequency	4		8	GHz	
Fundamental VCO Phase Noise Performance					VCO noise in open-loop conditions
		−117		dBc/Hz	100 kHz offset from 4.0 GHz carrier
		−139		dBc/Hz	1 MHz offset from 4.0 GHz carrier
		−156		dBc/Hz	10 MHz offset from 4.0 GHz carrier
		−162		dBc/Hz	100 MHz offset from 4.0 GHz carrier
		−112		dBc/Hz	100 kHz offset from 5.7 GHz carrier
		−136		dBc/Hz	1 MHz offset from 5.7 GHz carrier
		−153		dBc/Hz	10 MHz offset from 5.7 GHz carrier
		−161		dBc/Hz	100 MHz offset from 5.7 GHz carrier
		−109		dBc/Hz	100 kHz offset from 8.0 GHz carrier
		−133		dBc/Hz	1 MHz offset from 8.0 GHz carrier
		−152		dBc/Hz	10 MHz offset from 8.0 GHz carrier
		−162		dBc/Hz	100 MHz offset from 8.0 GHz carrier
VTUNE Input Range	1.2		2.75	V	
VCO 3 dB Tuning Port Bandwidth		100		MHz	
INTEGRATED RMS JITTER (100 Hz to 100 MHz)[1]		9		fs	8 GHz output, includes LO_IN and REF_PFD noise

[1] RF8N = 6.5 GHz, LO_IN = 6 GHz, and the reference to external PFD (REF_PFD) = 500 MHz. SMA100B is used as both the LO_IN signal and the REF_PFD signal.

TIMING CHARACTERISTICS

See Figure 2, Figure 3, and Figure 4.

Table 2. SPI Timing

Parameter	Min	Typ	Max	Unit	Description
f_{SCLK}			50	MHz	SCLK frequency
t_{SCLK}	20			ns	SCLK period
t_{HIGH}	10			ns	SCLK pulse width high
t_{LOW}	10			ns	SCLK pulse width low
t_{DS}	5			ns	SDIO setup time
t_{DH}	5			ns	SDIO hold time
t_{ACCESS}	10			ns	SCLK falling edge to SDIO valid propagation delay
t_Z	10			ns	$\overline{CS}$ rising edge to SDIO high-z
t_S	5			ns	$\overline{CS}$ falling edge to SCLK rising edge setup time
t_H	5			ns	SCLK rising edge to $\overline{CS}$ rising edge hold time

Timing Diagrams

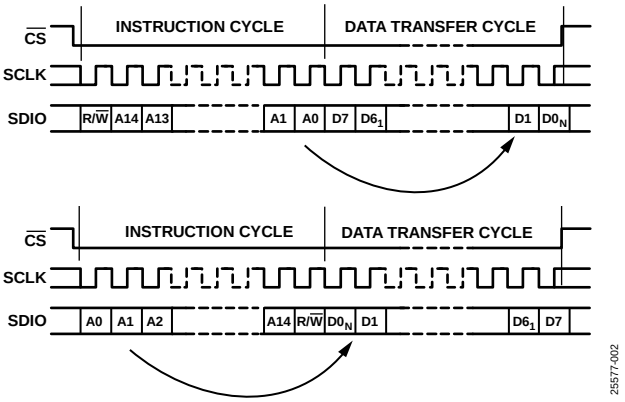


Figure 2. SPI Timing, MSB First (Upper) and LSB First (Lower)

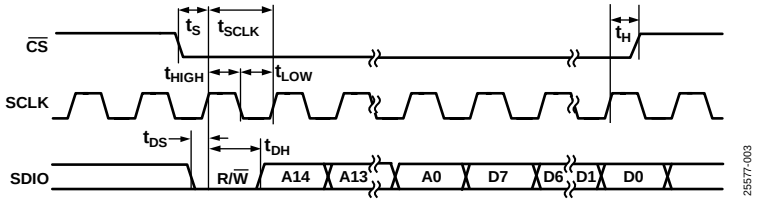


Figure 3. SPI Write Operation Timing

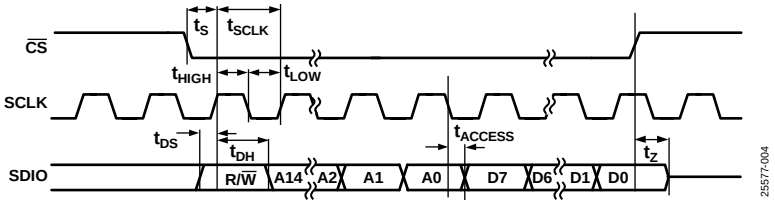


Figure 4. SPI Read Operation Timing

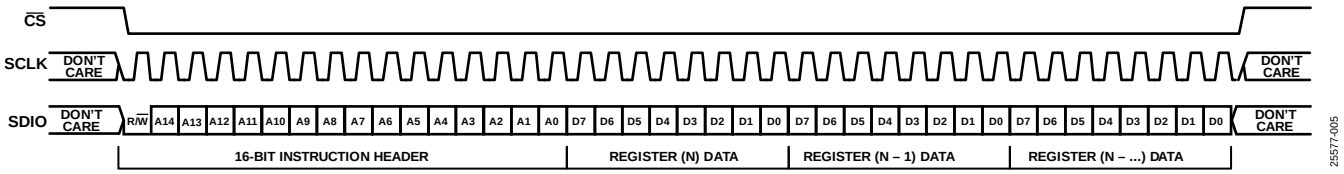


Figure 5. 3-Wire, MSB First, Descending Data, Streaming

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} Rails to GND[1]	−0.3 V to +3.6 V
AV_{DD} Rails to Each Other	−0.3 V to +0.3 V
VCC_VCO to AV_{DD}	−0.3 V to AV_{DD} + 2.8 V
VCC_RF, VCC_IF1, VCC_IF2, and VCC_VCO to GND[1]	−0.3 V to +5.5 V
VCC_MIX to AV_{DD}	−0.3 V to VCC_MIX + 0.3 V
VCC_MIX to GND[1]	−0.3 V to +3.6 V
CPOUT to GND[1]	−0.3 V to AV_{DD} + 0.3 V
VTUNE to GND[1]	−0.3 V to AV_{DD} + 0.3 V
Digital Input and Output Voltage to GND[1]	−0.3 V to AV_{DD} + 0.3 V
Analog Input and Output Voltage to GND[1]	−0.3 V to AV_{DD} + 0.3 V
REFP and REFN to GND[1]	−0.3 V to AV_{DD} + 0.3 V
REFP to REFN	±2.1 V
Temperature	
Operating Range	−25°C to +85°C
Storage Range	−65°C to +125°C
Maximum Junction	125 °C
Reflow Soldering	
Peak	260 °C
Time at Peak	30 sec
Transistor Count	
CMOS	152000
Bipolar	8000

[1] GND = 0 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CE-80-1[1]	27.9	12.1	°C/W

[1] Test Condition 1: thermal impedance simulated values are based on use of a 4-layer PCB with the thermal impedance paddle soldered to a ground plane.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.
Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADF4401A

Table 5. ADF4401A, 80-Terminal LGA_CAV

ESD Model	Withstand Threshold (V)	Class
HBM	±500[1]	1B
CDM	±125[2]	C0B

[1] All pins except IFOUT rated at ±2500 V HBM classification test level (Class 2).
[2] All pins except IFOUT, LO_IN, RF8P, and RF8N rated at ±500 V CDM classification test level (Class C2A). RF8P pin and RF8N pin rated at ±250 V CDM classification test level (Class C1).

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

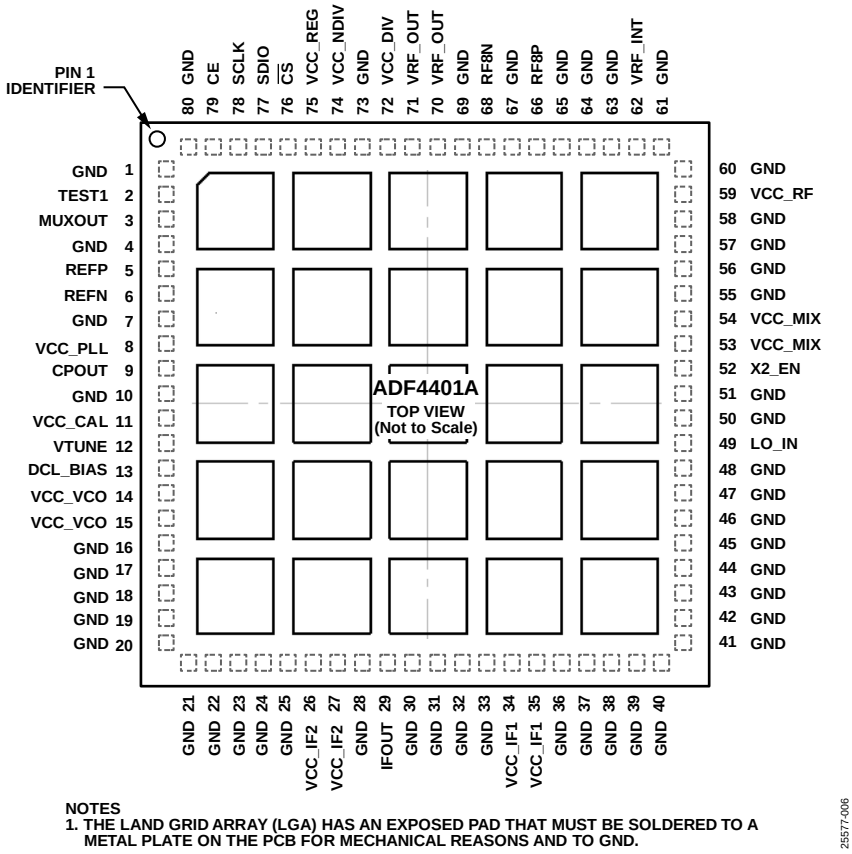


Figure 6. Pin Configuration, Top View

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 7, 10, 16 to 25, 28, 30 to 33, 36 to 48, 50, 51, 55 to 58, 60, 61, 63, 64, 65, 67, 69, 73, 80	GND	Ground. Tie all ground pins together.
2	TEST1	Internal Test Pin. Tie to GND.
3	MUXOUT	Multiplexer Output. The MUXOUT pin allows the digital lock detect for the calibration PLL and scaled RF to be externally accessible. The MUXOUT pin can be programmed to output the register settings in 4-wire SPI mode.
5	REFP	Reference Input. The signal at REFP is used as a reference for the calibration PLL.
6	REFN	Complementary Reference Input. If unused, ac couple the REFN pin to GND.
8	VCC_PLL	Analog Power Supply. The VCC_PLL pin ranges from 3.15 V to 3.45 V.
9	CPOUT	Charge Pump Output. When enabled, this output provides $\pm I_{CP}$ to the external loop filter. The output of the loop filter is connected to VTUNE to drive the internal VCO.
11	VCC_CAL	Power Supply for Internal Calibration Monitor Circuit. The voltage on the VCC_CAL pin ranges from 3.15 V to 3.45 V. VCC_CAL must have the same value as AV_{DD}, nominally 3.3 V.
12	VTUNE	Control Input to the VCO. This voltage determines the output frequency and is derived from filtering the CPOUT output voltage.
13	DCL_BIAS	Internal Compensation Node for VCO Noise Roll-Off. Internally, the DCL_BIAS pin is connected with 100 nF to GND, but larger capacitors to GND can be added if required.
14, 15	VCC_VCO	Power Supply for the VCO. The voltage on the VCC_VCO pin ranges from 4.75 V to 5.25 V. Place decoupling capacitors to the analog ground plane as close to the VCC_VCO pin as possible. For optimal performance, this supply must be clean and have low noise.
26, 27	VCC_IF2	5 V Supply to the IF Amplifier Connected to the IFOUT Pin.

Pin No.	Mnemonic	Description
29	IFOUT	Amplified Downconverted Output from the Mixer. Connect the IFOUT pin to an external phase detector or PFD.
34, 35	VCC_IF1	5 V Supply to the IF Amplifier Connected to the Mixer IF Output.
49	LO_IN	External RF Input to the Downconversion Mixer. Power can range from −3 dBm to +3 dBm. Take care to isolate LO_IN from the VCO circuitry and RF output. The LO_IN pin is matched internally to 50 Ω and must be ac-coupled.
52	X2_EN	Mixer Doubler Enable. A logic high to X2_EN doubles the LO_IN frequency to the downconversion mixer.
53, 54	VCC_MIX	Power Supply for Downconversion Mixer. The voltage on the VCC_MIX pin ranges from 3.15 V to 3.45 V. VCC_MIX must have the same value as AV_{DD}, nominally 3.3 V.
59	VCC_RF	5 V Supply to the RF Amplifier Connected to the Mixer RF Input.
62	VRF_INT	Power Supply for PLL and VCO Auxiliary RF Output Driving the Mixer. The voltage on the VRF_INT pin ranges from 3.15 V to 3.45 V. VRF_INT must have the same value as AV_{DD}, nominally 3.3 V.
66	RF8P	RF Output. The output level is programmable. The VCO fundamental output or a divided down version is available. Pull-up inductors to VRF_OUT increase the output power level.
68	RF8N	Complementary RF Output. The output level is programmable. The VCO fundamental output or a divided down version is available. Pull-up inductors to VRF_OUT increase the output power level.
70, 71	VRF_OUT	Power Supply for PLL and VCO Main RF Output. The voltage on the VRF_OUT pin ranges from 3.15 V to 3.45 V. VRF_OUT must have the same value as AV_{DD}, nominally 3.3 V.
72	VCC_DIV	Power Supply for the VCO Output Stage and Divider. The voltage on the VCC_DIV pin must have the same value as AV_{DD}, nominally 3.3 V.
74	VCC_NDIV	N Divider Power Supply. The voltage on the VCC_NDIV pin must have the same value as AV_{DD}, nominally 3.3 V.
75	VCC_REG	Regulator Input for 1.8 V Digital Logic. The voltage on the VCC_REG pin must have the same value as AV_{DD}, nominally 3.3 V.
76	$\overline{CS}$	Chip Select, CMOS Input. When $\overline{CS}$ goes high, the data stored in the shift register is loaded into the register that is selected by the address bits.
77	SDIO	Serial Data Input Output. This input is a high impedance CMOS input.
78	SCLK	Serial Clock Input. Data is clocked into the 24-bit shift register on the clock rising edge. This input is a high impedance CMOS input.
79	CE	Chip Enable. Connect to 3.3 V or AV_{DD}. A logic low on the CE pin shuts down the PLL and VCO circuitry.
	EPAD	Exposed Pad. The land grid array (LGA) has an exposed pad that must be soldered to a metal plate on the PCB for mechanical reasons and to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

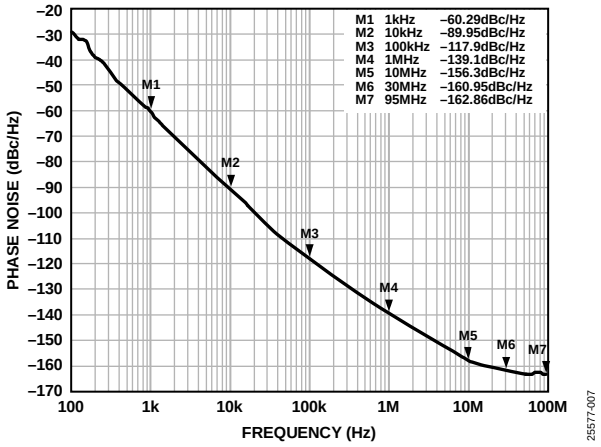


Figure 7. Open-Loop VCO Phase Noise, 4.0 GHz, VCC_VCO = 5 V

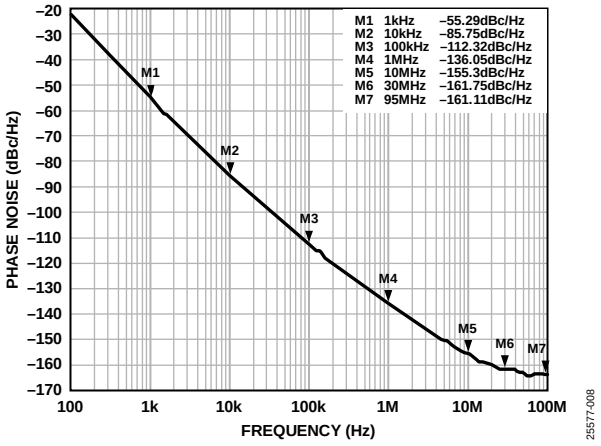


Figure 8. Open-Loop VCO Phase Noise, 5.7 GHz, VCC_VCO = 5 V

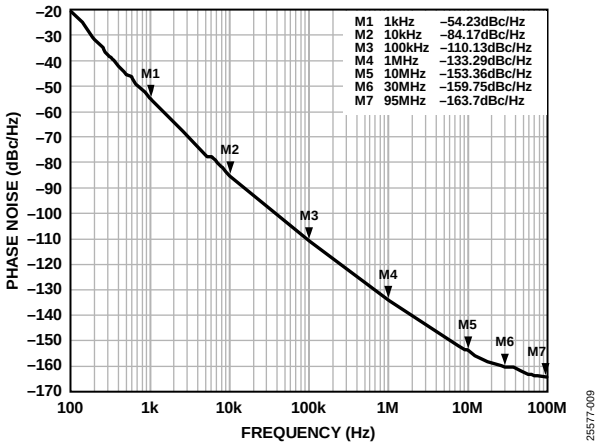


Figure 9. Open-Loop VCO Phase Noise, 8.0 GHz, VCC_VCO = 5 V

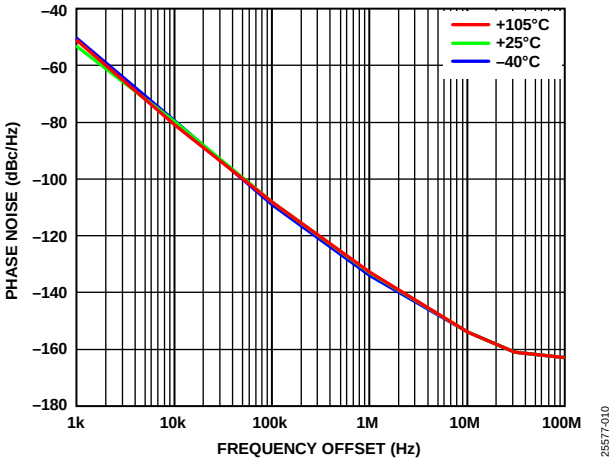


Figure 10. Open-Loop VCO Phase Noise over Temperature, 8.0 GHz, VCC_VCO = 5 V

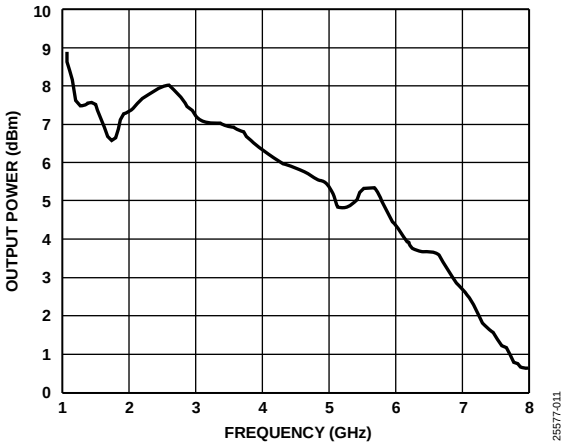


Figure 11. RF8N Single-Ended Output Power, De-Embedded Board and Cable Measurement, (3.3 nH Inductors, 10 pF AC Coupling Capacitors Limit Power at Low Frequencies), Maximum Power Setting

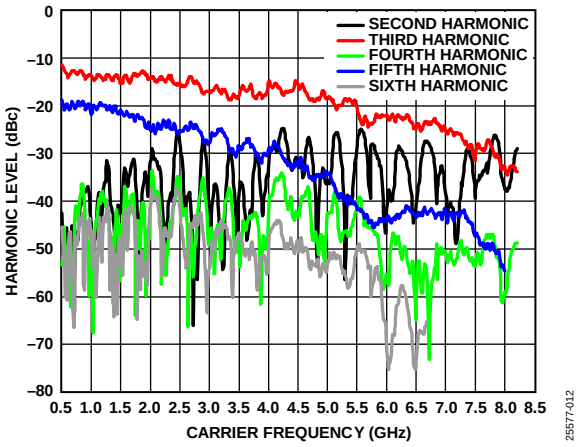


Figure 12. RF8P and RF8N Output Harmonics, De-Embedded Board and Cable Measurement, Combined Using Balun

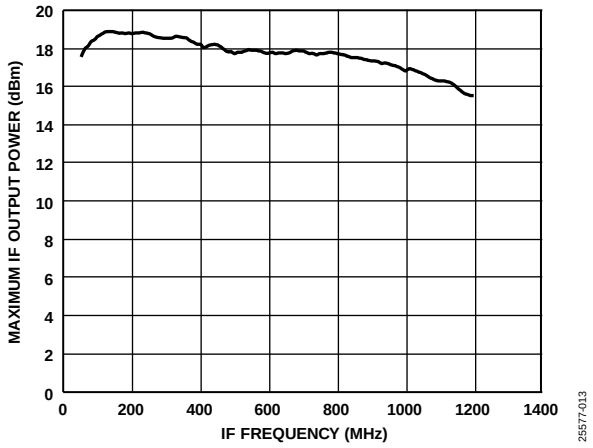


Figure 13. Maximum IF Output Power vs. IF Frequency

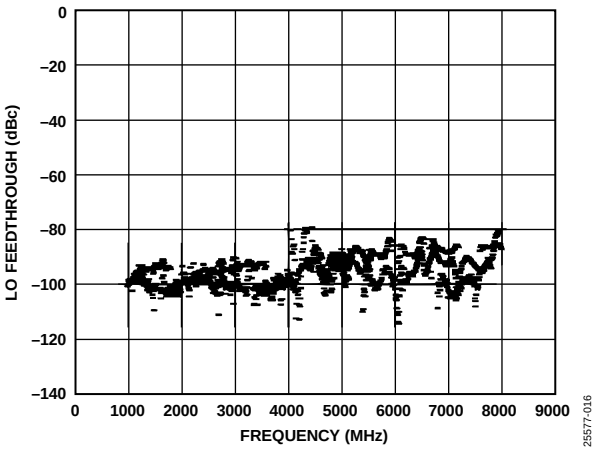


Figure 16. LO_IN to RF8N Feedthrough

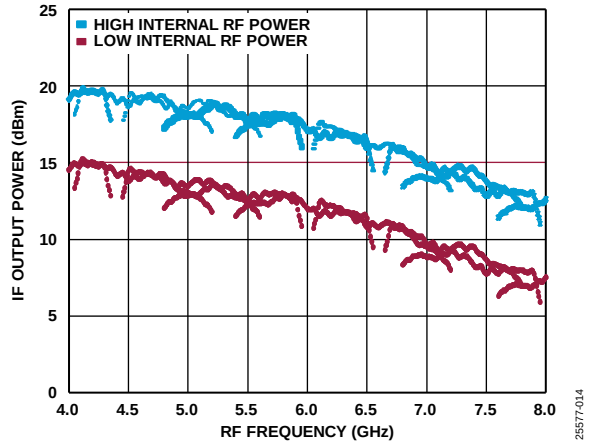


Figure 14. IF Output Power vs. RF Frequency for Different LO_IN Frequencies

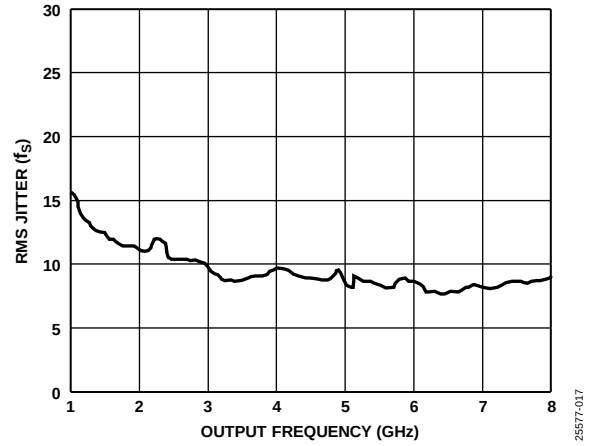


Figure 17. RMS Jitter vs. Output Frequency

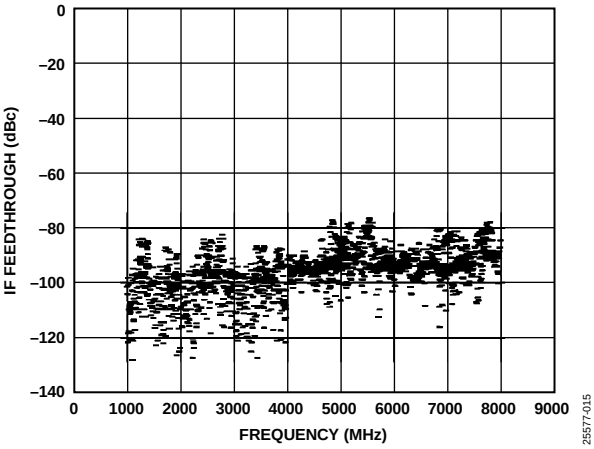


Figure 15. IFOUT to RF8N Feedthrough

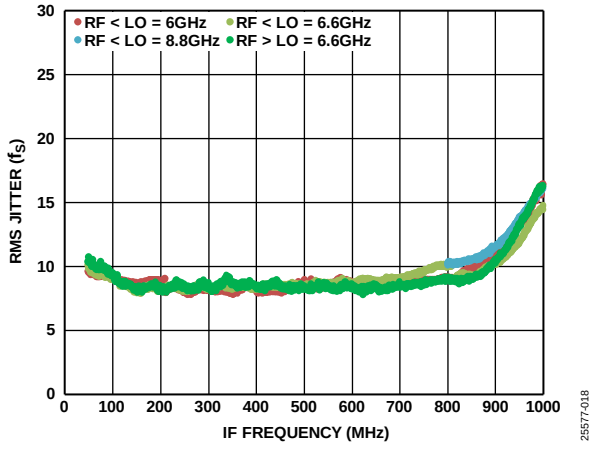


Figure 18. RMS Jitter vs. IF Frequency

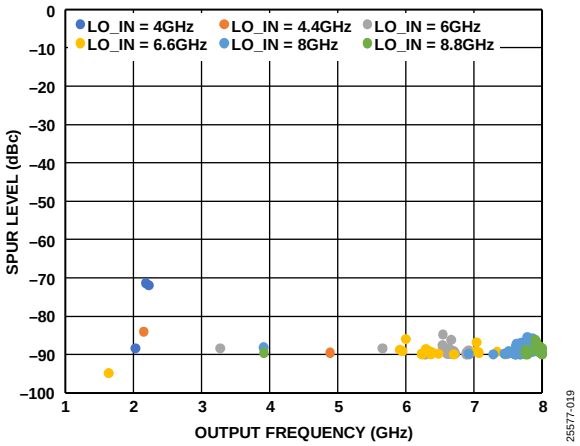


Figure 19. Spurious Signals on RF Output Within ±100 MHz Offset from Carrier

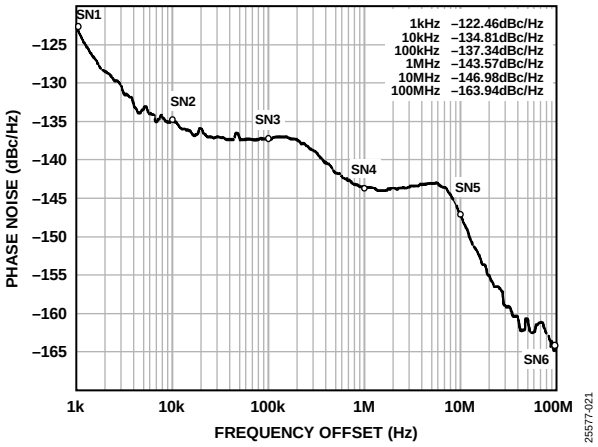


Figure 21. Closed-Loop Phase Noise at 6.45 GHz Output, LO_IN = 6 GHz, SMA100B Used as External LO and Reference to External Phase Detector

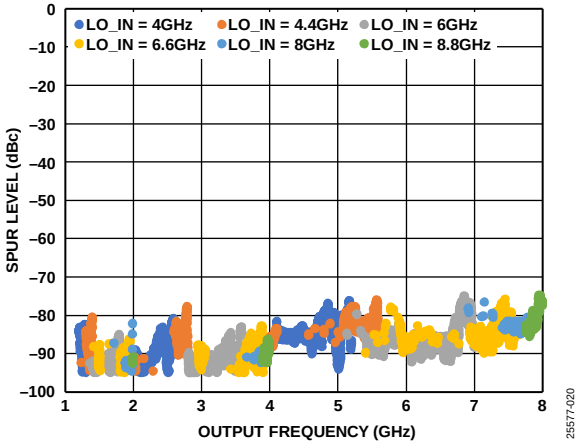


Figure 20. Spurious Signals on RF Output Outside of ±100 MHz Offset from Carrier

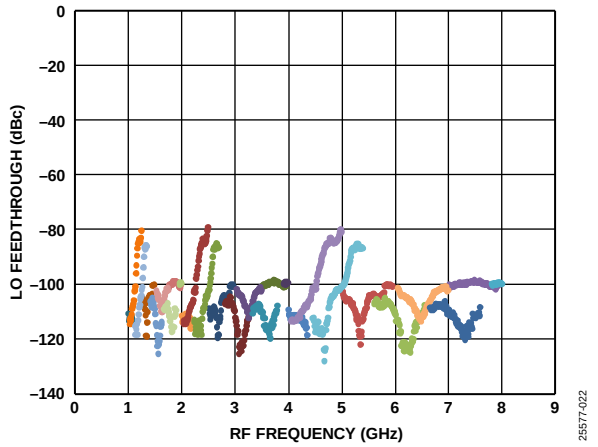


Figure 22. LO_IN to IFOUT Feedthrough for Different LO_IN Frequencies

THEORY OF OPERATION

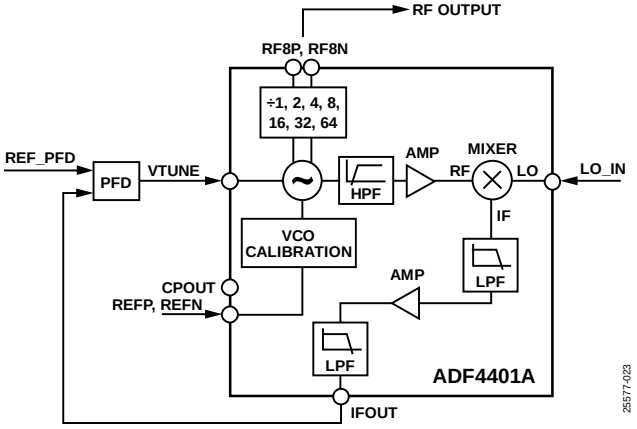


Figure 23. ADF4401A Translation Loop Block Diagram

The ADF4401A is an SiP translation loop (offset loop) module that includes the VCO and calibration PLL circuit, a downconversion mixer, and RF and IF amplifiers. This SiP translates the lower REF_PFD frequency of the external PFD up to a higher frequency range of 4 GHz to 8 GHz, as determined by the LO_IN pin.

The phase noise in a PLL circuit can be described as having two components: a flat noise component known as the PLL noise floor and a 1/f noise profile component known as the PLL 1/f noise.

A PLL circuit with a low N divider value allows the user to design a frequency synthesizer with correspondingly low phase noise performance. See the RF N Divider section for more information.

The translation loop synthesizer decouples the required channel spacing from the N divider value to optimize the phase noise of the PLL. In this translation loop synthesizer circuit, N = 1 is used.

As shown in Figure 23, the ADF4401A locks the higher RF output frequency range of 4 GHz to 8 GHz to the REF_PFD frequency of the external PFD. The integrated mixer and the LO_IN pin perform the divider function of this PLL circuit. The integrated RF amplifiers provide the required LO isolation, and the IF amplifiers provide the required external IFOUT levels.

With the LO in the feedback loop, the equation at the external PFD is as follows for high-side injection (IF = LO − RF):

$$REF_PFD/R = (LO_IN - RF8x)/N$$

where:
R is the R divider.
N is the N divider.

For low-side injection (IF = RF − LO),

$$REF_PFD/R = (RF8x - LO_IN)/N$$

In this circuit, R and N = 1. Thus, the output frequency is RF8x = LO_IN ± REF_PFD.

CIRCUIT DESCRIPTION

RF AMPLIFIER

The ADF4401A integrates an RF amplification stage between the VCO output stage and the RF input of the mixer (see Figure 24). The primary function of the RF amplifiers is to provide the required drive level for the mixer and increase the effective isolation of the LO on the RF output. A high-pass filter (HPF) helps ensure spectral purity at the RF output and minimizes the IF feedthrough to the RF output of the ADF4401A.

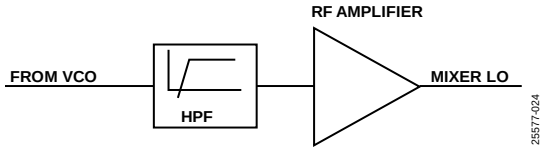


Figure 24. RF Amplifiers

DOWNCONVERSION MIXER

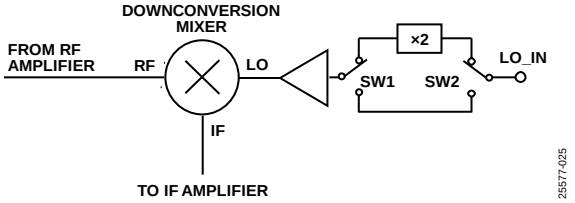


Figure 25. Downconversion Mixer

The mixer selected for the translation loop meets the following requirements:

- Operates in the required frequency range
- High RF to LO isolation
- Low noise figure

The LO_IN pin is connected to the mixer LO input. An optional doubler on the LO path allows the user to select either the LO_IN frequency or 2× LO_IN frequency to drive the downconversion mixer. This doubler reduces the requirement for external LO frequencies considerably.

IF AMPLIFIER

The ADF4401A integrates an IF amplification stage between the output of the mixer and the IFOUT pin (see Figure 26). The IF amplifier increases the LO to IF isolation of the mixer and provides the required 15 dBm IFOUT drive level. Low-pass filters (LPFs) placed before and after the IF amplifier remove unwanted high frequency products from the mixer.

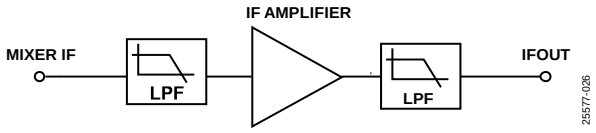


Figure 26. IF Amplifiers

CALIBRATION REFERENCE INPUT

Figure 27 shows the reference input stage of the calibration PLL. This reference input assists the VCO in selecting the most appropriate VCO band for optimal performance. When the appropriate band is selected, the reference input can be shut down, and the VCO can be locked with an external PFD circuit.

The reference input can accept both single-ended and differential signals. Use the reference mode bit (REG0022, Bit 6) to select the input mode. To use a differential signal on the reference input, program REG0022, Bit 6 to 1. When using a differential signal, SW1 and SW2 are open, SW3 and SW4 are closed, and the current source that drives the differential pair of transistors switches on. The differential signal is buffered and provided to an emitter coupled logic (ECL) to the CMOS converter.

When a single-ended signal is used as the reference, connect the reference signal to REFP and program REG0022, Bit 6 to 0. When using a single-ended signal, SW1 and SW2 are closed, SW3 and SW4 are open, and the current source that drives the differential pair of transistors switches off.

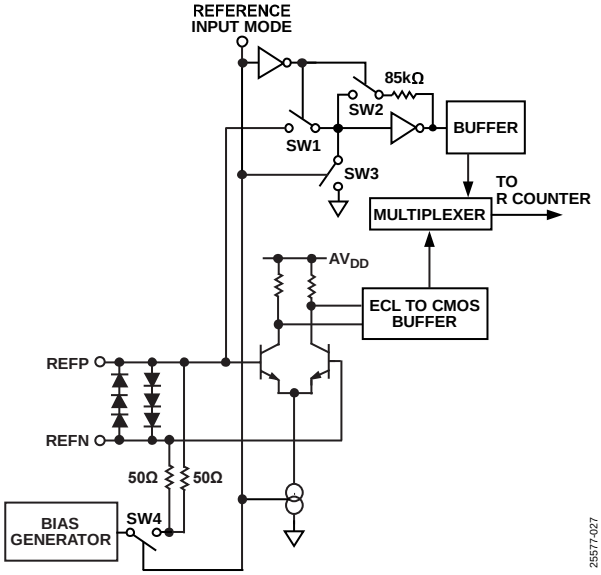


Figure 27. Reference Input Stage, Differential Mode

RF N DIVIDER

The RF N divider allows a division ratio in the calibration PLL feedback path. Determine the division ratio by the integer value of N (INT), main fractional value (FRAC1), auxiliary fractional value (FRAC2), and auxiliary modulus value (MOD2) that the RF N divider comprises.

INT, FRAC1, FRAC2, MOD1, MOD2, and R Counter Relationship

The INT, FRAC1, FRAC2, MOD1, and MOD2 values, in conjunction with the R counter, make it possible to generate output frequencies that are spaced by fractions of the PDF frequency (f_{PFD}). For more information, see the VCO Calibration, a Worked Example section.

Calculate the VCO output frequency (f_{VCO_OUT}) using the following equation:

$$f_{VCO_OUT} = f_{PFD} \times N \quad (1)$$

Calculate f_{PFD} using the following equation:

$$f_{PFD} = REF_{IN} \times \frac{1}{R \times (1+T)} \quad (2)$$

where:
REF_{IN} is the reference frequency input.
R is the preset divide ratio of the binary 5-bit programmable reference counter (1 to 32).
T is the REF_{IN} divide by 2 bit (0 or 1).

Calculate the desired value of the feedback N counter using the following equation:

$$N = INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1} \quad (3)$$

where:
INT is the 16-bit integer value. In integer mode, INT = 16 to 32,767 for the 4/5 prescaler, and 64 to 65,535 for the 8/9 prescaler. In fractional mode, INT = 23 to 32,767 for the 4/5 prescaler, and 75 to 65,535 for the 8/9 prescaler.
FRAC1 is the numerator of the primary modulus (0 to 33,554,431).
FRAC2 is the numerator of the 14-bit auxiliary modulus (0 to 16,383).
MOD2 is the programmable, 14-bit auxiliary fractional modulus (2 to 16,383).
MOD1 is a 25-bit primary modulus with a fixed value of 2^{25} = 33,554,432.

Equation 1, Equation 2, and Equation 3 result in a low frequency resolution with no residual frequency error.

To apply Equation 3, perform the following steps:

1. Calculate N by dividing f_{VCO_OUT}/f_{PFD}. The integer value of this number forms INT.
2. Subtract INT from the full N value.
3. Multiply the remainder by 2^{25}. The integer value of this number forms FRAC1.
4. Calculate MOD2 based on the channel spacing frequency (f_{CHSP}) using the following equation:

$$MOD2 = f_{PFD}/\text{GCD}(f_{PFD}, f_{CHSP}) \quad (4)$$

where:
f_{CHSP} is the desired channel spacing frequency.
$\text{GCD}(f_{PFD}, f_{CHSP})$ is the greatest common divisor of the PFD frequency and the channel spacing frequency.

5. Calculate FRAC2 using the following equation:

$$FRAC2 = ((N - INT) \times 2^{25} - FRAC1) \times MOD2 \quad (5)$$

The FRAC2 fraction and MOD2 fraction result in outputs with zero frequency error for channel spacing when

$$f_{PFD}/\text{GCD}(f_{PFD}, f_{CHSP}) = MOD2 < 16{,}383 \quad (6)$$

If zero frequency error is not required, the MOD1 and MOD2 denominators operate together to create a 39-bit resolution modulus.

R Counter

The 5-bit R counter allows the input reference frequency (input to REFP and REFN) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 32 are allowed.

PFD AND CHARGE PUMP

The calibration PFD takes inputs from the internal R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 28 is a simplified schematic of the PFD. The PFD includes a fixed delay element that sets the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and provides a consistent reference spur level. Set the phase detector polarity to positive on this device because of the positive tuning of the VCO.

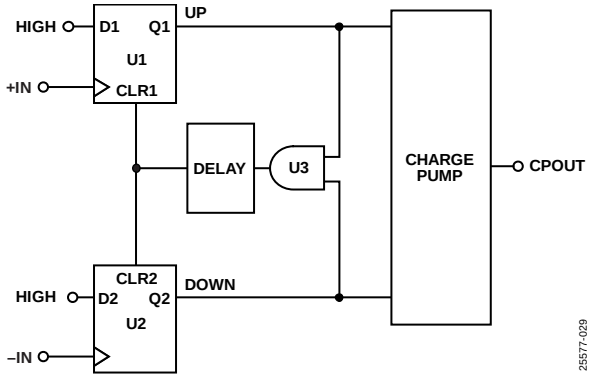


Figure 28. PFD Simplified Schematic

MUXOUT AND VCO CALIBRATION LOCK DETECT

The output multiplexer on the ADF4401A allows the user to access various internal points on the chip. Figure 29 shows the MUXOUT section in block diagram form. The lock detect indicator is only for the calibration PLL.

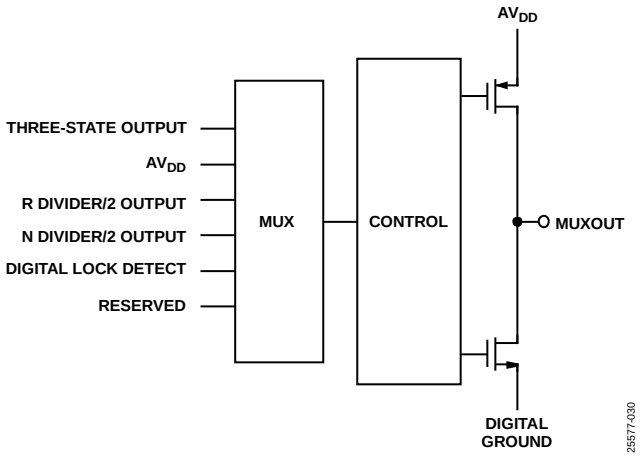


Figure 29. MUXOUT Schematic

DOUBLE BUFFERS

The FRAC1 value, FRAC2 value, MOD2 value, reference doubler, reference divide by 2 (RDIV2), R counter value, and charge pump current setting are double buffered in the ADF4401A. Two events must occur before the ADF4401A uses a new value for any of the double buffered settings. First, the new value must latch into the device by writing to the appropriate register, and second, a new write to the REG0010 register must be performed.

For example, to ensure that the MOD2 value loads correctly, the REG0010 register must be written to every time the MOD2 value updates.

VCO

The VCO core in the ADF4401A consists of four separate VCO cores: Core A, Core B, Core C, and Core D. Each core uses 256 overlapping bands, which allows the device to cover a wide frequency range with small VCO sensitivity (K_V) and optimal phase noise and spurious performance.

The proper VCO and band are chosen automatically by the VCO and band select logic whenever the REG0010 register is updated and automatic calibration is enabled. The VTUNE pin is disconnected from the output of the loop filter and is connected to an internal reference voltage.

The R counter output is used as the clock for the band select logic. After band selection, normal PLL action resumes. The nominal value of K_V along with an average value are shown in Figure 30 when the N divider is driven from the VCO output, or the K_V value is divided by D. D is the output divider value if the N divider is driven from the RF output divider.

The VCO shows the variation of K_V as the tuning voltage, VTUNE, varies both within the band and from band to band. For wideband applications covering a wide frequency range (and changing output dividers), a value of 80 MHz/V provides the most accurate K_V, because this value is closest to the average value.

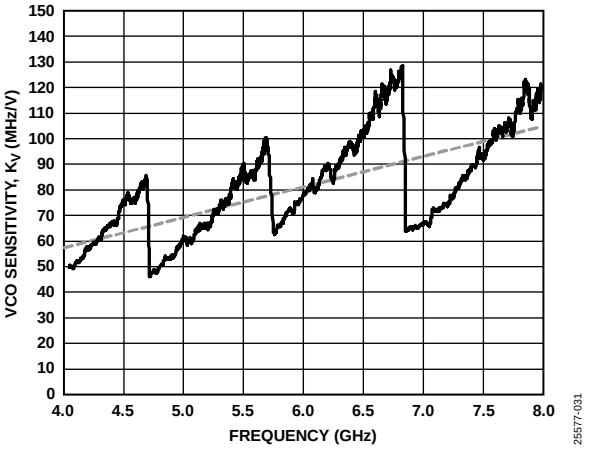


Figure 30. VCO Sensitivity, K_V vs. Frequency

OUTPUT STAGE

The RF8P and RF8N pins of the ADF4401A connect to the collectors of a bipolar negative positive negative (NPN) differential pair driven by buffered outputs of the VCO, as shown in Figure 31. The ADF4401A contains internal 50 Ω resistors connected to the VRF_OUT pins. To optimize the power dissipation vs. the output power requirements, the tail current of the differential pair is programmable using REG0025, Bits[1:0]. Four current levels can be set. These levels provide approximate output power levels of −4 dBm, −1 dBm, 2 dBm, and 5 dBm. Levels of −4 dBm and −1 dBm can be achieved by ac coupling into a 50 Ω load. The 2 dBm and 5 dBm levels must be used with an external shunt inductor to VRF_OUT, or else the output stage may compress. An inductor has a narrower operating frequency than a 50 Ω resistor. For accurate power levels, refer to the Typical Performance Characteristics section. Add an external shunt inductor to provide higher power levels, which is less wideband than the internal bias only. Terminate the unused complementary output with a circuit similar to the used output.

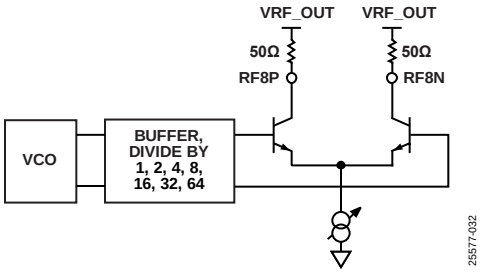


Figure 31. Output Stage

SPI

The SPI of the ADF4401A allows the user to configure the device as required via a 3-wire or 4-wire SPI port. This interface provides users with added flexibility and customization. The SPI consists of four control lines: SCLK, SDIO, $\overline{CS}$, and MUXOUT. MUXOUT is the serial data output in 4-wire SPI mode. The timing requirements for the SPI port are detailed in Table 2.

The SPI protocol consists of a read and write bit and 15 register address bits, followed by eight data bits. Both the address and data fields are organized with the MSB first and end with the LSB by default. Figure 3 and Figure 4 show the timing diagrams for SPI writes and reads, respectively. The significant bit order can be changed via the REG0000 register, Bit 1 (LSB_FIRST) setting, and the related timing diagram is shown in Figure 2.

The ADF4401A input logic level for the write cycle is compatible with a 1.8 V logic level. On a read cycle, both the SDIO and MUXOUT pins are configurable for 1.8 V (default) or 3.3 V output levels by the LEV_SEL bit setting.

SPI Stream Mode

The ADF4401A supports stream mode, where data bits are loaded to or read from registers serially without writing the register address (instruction word). Stream mode is useful in time critical applications when a large amount of data must be transferred or when some registers must be updated repeatedly.

The slave device starts reading or writing data to this address and continues as long as $\overline{CS}$ is asserted and single-byte writes are not enabled (Bit 7 in the REG0001 register). The slave device automatically increments or decrements the address depending on the setting of the address ascension bit (Bit 2 in the REG0000 register).

The instruction header starts with a Logic 0 to indicate a write sequence and addresses the register. Then, the data for registers (N, N − 1, and N − 2) are loaded consecutively without any assertion in $\overline{CS}$.

The registers are organized into eight bits, and if a register requires more than eight bits, sequential register addresses are used. This organization enables using stream mode and simplifies loading. For example, FRAC1WORD is stored in the REG0017, REG0016, REG0015, and REG0014 registers (MSB to LSB). These registers can be loaded by using the REG0016 register and sending the whole 24-bit data afterward, as shown in Figure 5.

APPLICATIONS INFORMATION

DEVICE SETUP

The recommended sequence of steps to set up the ADF4401A are as follows:

1. Set up the SPI.
2. Perform the initialization sequence.
3. Perform the frequency update sequence for the internal PLL.
4. Change the mode from internal PLL to external PFD.
5. Perform the frequency update sequence for the translation loop.

Step 1: Set Up the SPI

Initialize the SPI. Write the values in Table 7 to the REG0000 register and REG0001 register.

Table 7. SPI Setup

Address	Setting	Notes
0x00	0x18	4-wire SPI
0x01	0x00	Stalling, master readback control

Step 2: Initialization Sequence

Write to each register in reverse order from Address 0x7C to Address 0x10. Select the appropriate values to generate the desired frequency. The frequency update sequence follows to generate the desired output frequency.

Step 3: Frequency Update Sequence (Internal PLL)

Frequency updates require updating MOD2, FRAC1, FRAC2, and INT. Therefore, the update sequence must be as follows:

1. REG001A (new MOD2WORD[13:8])
2. REG0019 (new MOD2WORD[7:0])
3. REG0018 (new FRAC2WORD[13:7])
4. REG0017 (new FRAC2WORD[6:0])
5. REG0016 (new FRAC1WORD[23:16])
6. REG0015 (new FRAC1WORD[15:8])
7. REG0014 (new FRAC1WORD[7:0])
8. REG0011 (new BIT_INTEGER_WORD[15:8])
9. REG0010 (new BIT_INTEGER_WORD[7:0])

The frequency change occurs on the write to the REG0010 register.

The unchanged registers do not need to be updated. For example, for an integer N PLL configuration (fractional parts are not used), skip Step 1 to Step 7. In this case, the only required updates are the REG0011 register and REG0010 register.

Step 4: External PFD Operation

The VTUNE input is switched to the external PFD and the VCO locks using the translation loop module.

To improve performance, it is recommended to power off the internal PLL synthesizer by setting REG001E, Bit 2 = 1.

Alternatively, if the switching speed between frequencies is to be minimized, leave the internal PLL powered up and take the following steps:

1. Place the internal PLL charge pump in tristate. REG003E, Bits[3:2] = 0.
2. Disable the fractional-N Σ-Δ engine, REG002B, Bit 0 = 1.
3. Set the R divider to 0. REG001F, Bits[4:0] = 0.
4. Set the N divider to the maximum value, 65535. REG0010, Bits[7:0] = 255 and REG0011, Bits[7:0] = 255.

Step 5: Frequency Update Sequence (Translation Loop)

Change the external PFD frequency and external LO frequency, if required. Frequency updates require reenabling the internal PFD, switching VTUNE to use the internal PFD, and locking the VCO with the new frequency. Then, the VTUNE input is switched to the external PFD, and the VCO locks to the new frequency using the translation loop module.

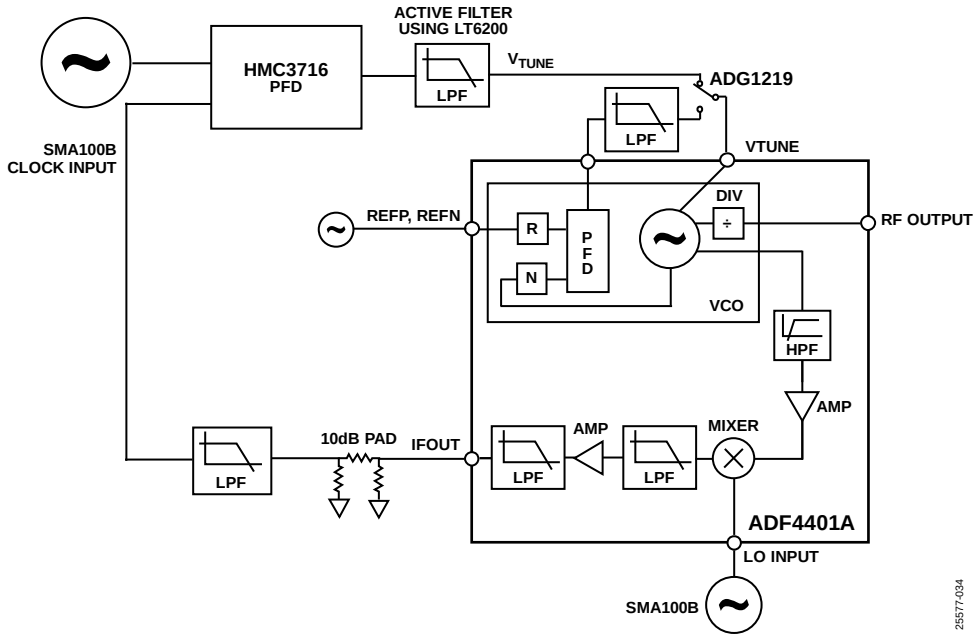


Figure 32. ADF4401A Evaluation Setup Block Diagram

VCO CALIBRATION, A WORKED EXAMPLE

Internal PLL blocks (internal PFD and internal N and R dividers) are used for VCO calibration. All parameters are referred to as internal PLL in this section. Use the following equations to program the ADF4401A synthesizer:

$$f_{RFOUT} = \left(INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1} \right) \times \frac{f_{PFD}}{RF\ Divider} \quad (7)$$

where:
f_{RFOUT} is the RF output frequency.
INT is the integer division factor.
FRAC1 is the fractionality.
FRAC2 is the auxiliary fractionality.
MOD1 is the fixed 25-bit modulus.
MOD2 is the auxiliary modulus.
RF Divider is the output divider that divides down the VCO frequency.

$$f_{PFD} = REF_{IN} \times (1/(R \times (1 + T))) \quad (8)$$

where:
REF_{IN} is the reference frequency input.
R is the reference division factor.
T is the reference divide by 2 bit (0 or 1).

For example, in a universal mobile telecommunication system (UMTS), where a 2112.8 MHz f_{RFOUT} is required, a 122.88 MHz REF_{IN} is available. The ADF4401A VCO operates in the frequency range of 4 GHz to 8 GHz. Therefore, the RF divider of 2 must be used (VCO frequency = 4225.6 MHz, RF_{OUT} = VCO frequency/RF divider = 4225.6 MHz/2 = 2112.8 MHz).

The feedback path is also important. In this example, the VCO output is fed back before the output divider (see Figure 33).

In this example, the 122.88 MHz reference signal is divided by 2 to generate a f_{PFD} of 61.44 MHz. The desired channel spacing frequency is 200 kHz.

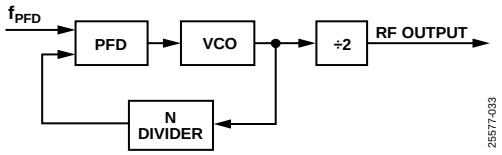


Figure 33. Loop Closed Before Output Divider

The values used in this worked example are as follows:

$$N = f_{VCO_OUT}/f_{PFD} = 4225.6\ MHz/61.44\ MHz = 68.7760416666666667 \quad (9)$$

where:
N is the desired value of the feedback counter, N.
f_{VCO_OUT} is the output frequency of the VCO without using the output divider.
f_{PFD} is the frequency of the phase frequency detector.

$$INT = INT(VCO\ frequency/f_{PFD}) = 68 \quad (10)$$

$$FRAC = 0.7760416666666667 \quad (11)$$

where *FRAC* is the fractional part of the N.

$$MOD1 = 33{,}554{,}432 \quad (12)$$

$$FRAC1 = INT(MOD1 \times FRAC) = 26{,}039{,}637 \quad (13)$$

$$\text{Remainder} = 0.3333333333 \text{ or } 1/3 \quad (14)$$

$$MOD2 = f_{PFD}/\text{GCD}(f_{PFD}, f_{CHSP}) = 61.44\ MHz/\text{GCD}(61.44\ MHz, 200\ kHz) = 1536 \quad (15)$$

where GCD is the greatest common divider operant.

$$FRAC2 = \text{Remainder} \times 1536 = 512 \quad (16)$$

From Equation 8,

$$f_{PFD} = (122.88\ \text{MHz} \times (1/2) = 61.44\ \text{MHz} \quad (17)$$

$$2112.8\ \text{MHz} = 61.44\ \text{MHz} \times ((INT + (FRAC1 + FRAC2/MOD2)/2^{25}))/2 \quad (18)$$

where:
INT = 68.
FRAC1 = 26,039,637.
MOD2 = 1536.
FRAC2 = 512.
RF Divider = 2.

VCO CALIBRATION TIME

The VCO calibration settling time divides into a number of settings. The total lock time for changing frequencies is the sum of the four separate times: synthesizer lock, VCO band selection, automatic level calibration (ALC), and calibration PLL settling time.

Synthesizer Lock

The synthesizer lock timeout ensures that the VCO calibration DAC, which forces the VCO tune voltage (VTUNE), has settled to a steady value for the band select circuitry. SYNTH_LOCK_TIMEOUT and timeout select the length of time the DAC is allowed to settle to the final voltage before the VCO calibration process continues to the next phase (VCO band selection).

The PFD frequency is the clock for this logic, and the duration is set using the following equation:

$$\frac{SYNTH_LOCK_TIMEOUT \times 1024 + timeout}{f_{PFD}} \quad (19)$$

where:
SYNTH_LOCK_TIMEOUT is programmed in REG0033.
Timeout is programmed in REG0031 and REG0032.

The calculated time must be greater than or equal to 20 µs.

For the SYNTH_LOCK_TIMEOUT bit, the minimum value is 2 and the maximum value is 31. For the timeout bit, the minimum value is 2 and the maximum value is 1023.

VCO Band Selection

VCO_BAND_DIV (programmed in the REG0030 register) and the f_{PFD} are used to generate the VCO band selection clock as follows:

$$f_{BSC} = \frac{f_{PFD}}{VCO_BAND_DIV} \quad (20)$$

where f_{BSC} is the band select clock frequency.

The calculated frequency must be less than 2.4 MHz.

16 clock cycles are required for one VCO core and band calibration step, and the total band selection process takes 11 steps, resulting in the following equation:

$$11 \times \frac{16 \times VCO_BAND_DIV}{f_{PFD}} \quad (21)$$

The minimum value for VCO_BAND_DIV is 1 and the maximum value is 255.

Automatic Level Calibration

Use the ALC function to choose the correct bias current in the ADF4401A VCO core. The duration required for the VCO bias voltage to settle for each step is set by the following equation:

$$\frac{VCO_ALC_TIMEOUT \times 1024 + timeout}{f_{PFD}} \quad (22)$$

where
VCO_ALC_TIMEOUT and *timeout* are programmed in the REG0034, REG0032, and REG0031 registers.

The calculated time must be greater than or equal to 50 µs.

The total ALC takes 63 steps, as shown in the following equation:

$$63 \times \frac{VCO_ALC_TIMEOUT \times 1024 + timeout}{f_{PFD}} \quad (23)$$

The minimum value for VCO_ALC_TIMEOUT is 2, and the maximum value is 31.

Calibration PLL Settling Time

The time taken for the loop to settle is inversely proportional to the low-pass filter bandwidth. The settling time is accurately modeled in the ADIsimPLL design tool.

Calibration Lock Time, a Worked Example

Assume that f_{PFD} = 61.44 MHz,

$$VCO_BAND_DIV = \text{Ceiling}(f_{PFD}/2{,}400{,}000) = 26 \quad (24)$$

where Ceiling*()* rounds up to the nearest integer.

$$SYNTH_LOCK_TIMEOUT \times 1024 + timeout > 1228.8 \quad (25)$$

$$VCO_ALC_TIMEOUT \times 1024 + timeout > 3072 \quad (26)$$

There are several suitable values that meet these criteria. By considering the minimum specifications, the following values are the most suitable:

- SYNTH_LOCK_TIMEOUT = 2 (minimum value)
- VCO_ALC_TIMEOUT = 3
- Timeout = 2

Much faster lock times than those detailed in this data sheet are possible by bypassing the calibration processes. See the AN-2005 Application Note for more information.

LOCAL OSCILLATOR (LO_IN)

The selection of an external LO to the ADF4401A is of critical importance. Because the divider function has been replaced by a mixer, the phase noise of the external LO modulates the carrier frequency inside the PLL loop bandwidth and dominates the measured phase noise. For this reason, only the highest performance LO sources, such as voltage controlled surface acoustic wave (SAW) oscillators (VCSOs), comb generators, and dielectric resonator oscillators (DROs), are recommended.

EXTERNAL PHASE DETECTOR

To take advantage of the ability of the architecture of offset loop PLLs to generate extremely low noise carrier frequencies, it is important to use a phase detector or PFD that can operate at high frequencies, minimizing the need for any dividers that can degrade the in band noise response.

The 1.3 GHz phase comparison frequency of the HMC3716 makes it ideal for use with the IF range of the ADF4401A. The ability of such a circuit to compare both frequency and phase means no additional circuitry is required to steer the frequency to the intended output frequency.

Mixers can also be used as phase detectors, but these require additional circuitry to steer the frequency within the capture range of the mixer (the intended frequency ± the external loop bandwidth).

PHASE DETECTOR REFERENCE

In addition to choosing a low noise LO source and high frequency low noise phase detector, the reference frequency to the external phase detector is also of critical importance. For most applications, the external phase detector reference must have fast switching and high resolution. For this reason, direct digital synthesizers (DDSs) are highly recommended. A devices like the AD9162 is suitable and cover the IF range of the ADF4401A.

POWER SUPPLIES

To ensure optimal performance, connect a low noise regulator, such as the ADM7150, to all supply pins.

PCB DESIGN GUIDELINES

Connect all of the GND pins to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the ADF4401A.

For optimal heatsinking, use vias to connect the GND copper area to the internal ground planes of the PCB. Liberally distribute these GND vias to provide both an optimal ground connection and thermal path to the internal planes of the PCB. Pay attention to the location and density of the thermal vias.

The ADF4401A can benefit from the heatsinking afforded by vias that connect to internal GND planes at these locations due to their proximity to internal power handling components. The optimum number of thermal vias depends on the PCB design. For example, a PCB may use small via holes and therefore must employ more thermal vias than a board that uses larger holes.

For a microwave PLL and VCO synthesizer, such as the ADF4401A, care must be taken with the board stackup and layout. Do not use FR4 material because it can cause signal power loss above 3 GHz. Instead, the Rogers 4350, Rogers 4003, or Rogers 3003 dielectric material is suitable.

Care must be taken with the RF output traces to minimize discontinuities and ensure optimal signal integrity. Via placement and grounding are critical.

OUTPUT MATCHING

The RF8P and RF8N pins can be ac-coupled to the next circuit, if desired. However, if higher output power is required, use a pull-up inductor to VRF_OUT to increase the output power level as shown in Figure 34.

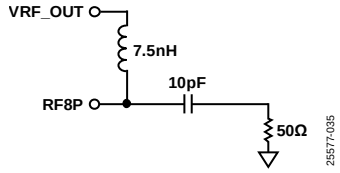


Figure 34. Optimum Output Stage

When differential outputs are not needed, terminate the unused output or combine the outputs using a balun.

For frequencies below 2 GHz, use a 100 nH inductor instead of a 7.5 nH inductor on the RF8P and RF8N pins.

The RF8P and RF8N pins are a differential circuit. Provide each output with the same (or similar) components where possible, such as a similar shunt inductor value, bypass capacitor, and termination.

REGISTER SUMMARY

Table 8. ADF4401A Register Summary

Reg	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	RW
0x00	[7:0]	SOFT_RESET_R	LSB_FIRST_R	ADDRESS_ ASCENSION_R	SDO_ACTIVE_R	SDO_ACTIVE	ADDRESS_ ASCENSION	LSB_FIRST	SOFT_RESET	0x18	R/W
0x01	[7:0]	SINGLE_ INSTRUCTION	STALLING	MASTER_ READBACK_ CONTROL	RESERVED					0x00	R/W
0x10	[7:0]	BIT_INTEGER_WORD[7:0]								0x32	R/W
0x11	[7:0]	BIT_INTEGER_WORD[15:8]								0x00	R/W
0x12	[7:0]	RESERVED	EN_AUTOCAL	PRE_SEL	RESERVED					0x40	R/W
0x14	[7:0]	FRAC1WORD[7:0]								0x00	R/W
0x15	[7:0]	FRAC1WORD[15:8]								0x00	R/W
0x16	[7:0]	FRAC1WORD[23:16]								0x00	R/W
0x17	[7:0]	FRAC2WORD[6:0]							FRAC1WORD [24]	0x00	R/W
0x18	[7:0]	RESERVED	FRAC2WORD[13:7]							0x00	R/W
0x19	[7:0]	MOD2WORD[7:0]								0xE8	R/W
0x1A	[7:0]	RESERVED		MOD2WORD[13:8]						0x03	R/W
0x1E	[7:0]	CP_CURRENT				PD_POL	PD	RESERVED	CNTR_RESET	0x48	R/W
0x1F	[7:0]	RESERVED			R_WORD					0x01	R/W
0x20	[7:0]	MUXOUT				MUXOUT_EN	LEV_SEL	RESERVED		0x14	R/W
0x22	[7:0]	RESERVED	REFIN_MODE	RESERVED	RDIV2	RESERVED				0x00	R/W
0x24	[7:0]	FB_SEL	DIV_SEL			RESERVED				0x80	R/W
0x25	[7:0]	RESERVED		RF_DIVSEL_ DB	RESERVED		RF_EN	RF_OUT_POWER		0x07	R/W
0x27	[7:0]	LD_BIAS		LDP	RESERVED					0xC5	R/W
0x28	[7:0]	DOUBLE_BUFF	RESERVED				LD_COUNT		LOL_EN	0x03	R/W
0x2B	[7:0]	RESERVED		LSB_P1	VAR_MOD_EN	RESERVED	SD_LOAD_ ENB	RESERVED	SD_EN_ FRAC0	0x01	R/W
0x2C	[7:0]	RESERVED	ALC_RECT_ SELECT_ VCO1	ALC_REF_ DAC_LO_ VCO1	ALC_REF_DAC_NOM_VCO1			VTUNE_ CALSET_EN	DISABLE_ALC	0x44	R/W
0x2D	[7:0]	RESERVED			ALC_RECT_ SELECT_VCO2	ALC_REF_DAC_ LO_VCO2	ALC_REF_DAC_NOM_VCO2			0x11	R/W
0x2E	[7:0]	RESERVED			ALC_RECT_ SELECT_VCO3	ALC_REF_DAC_ LO_VCO3	ALC_REF_DAC_NOM_VCO3			0x12	R/W
0x2F	[7:0]	RESERVED			ALC_RECT_ SELECT_VCO4	ALC_REF_DAC_L O_VCO4	ALC_REF_DAC_NOM_VCO4			0x94	R/W
0x30	[7:0]	VCO_BAND_DIV								0x3F	R/W
0x31	[7:0]	TIMEOUT[7:0]								0xA7	R/W
0x32	[7:0]	ADC_MUX_ SEL	RESERVED	ADC_FAST_ CONV	ADC_CTS_ CONV	ADC_ CONVERSION	ADC_ ENABLE	TIMEOUT[9:8]		0x04	R/W
0x33	[7:0]	RESERVED			SYNTH_LOCK_TIMEOUT					0x0C	R/W
0x34	[7:0]	VCO_FSM_TEST_MODES			VCO_ALC_TIMEOUT					0x9E	R/W
0x35	[7:0]	ADC_CLK_DIVIDER								0x4C	R/W
0x36	[7:0]	ICP_ADJUST_OFFSET								0x30	R/W
0x37	[7:0]	SI_BAND_SEL								0x00	R/W
0x38	[7:0]	SI_VCO_SEL				SI_VCO_BIAS_CODE				0x00	R/W
0x39	[7:0]	RESERVED	VCO_FSM_TEST_MUX_SEL			SI_VTUNE_CAL_SET				0x07	R/W
0x3A	[7:0]	ADC_OFFSET								0x55	R/W
0x3E	[7:0]	RESERVED				CP_TMODE		RESERVED		0x0C	R/W
0x3F	[7:0]	RESERVED								0x80	R/W
0x40	[7:0]	RESERVED								0x50	R/W
0x41	[7:0]	RESERVED								0x28	R/W
0x47	[7:0]	RESERVED								0xC0	R/W
0x52	[7:0]	RESERVED								0xF4	R/W
0x6E	[7:0]	VCO_DATA_READBACK[7:0]								0x00	R
0x6F	[7:0]	VCO_DATA_READBACK[15:8]								0x00	R
0x72	[7:0]	RESERVED	AUX_FREQ_ SEL	POUT_AUX		PDB_AUX	RESERVED			0x32	R/W
0x73	[7:0]	RESERVED					ADC_CLK_ DISABLE	PD_NDIV	LD_DIV	0x00	R/W
0x7C	[7:0]	RESERVED							LOCK_DETECT _READBACK	0x00	R

REGISTER DETAILS

Address: 0x00, Default: 0x18, Name: REG0000

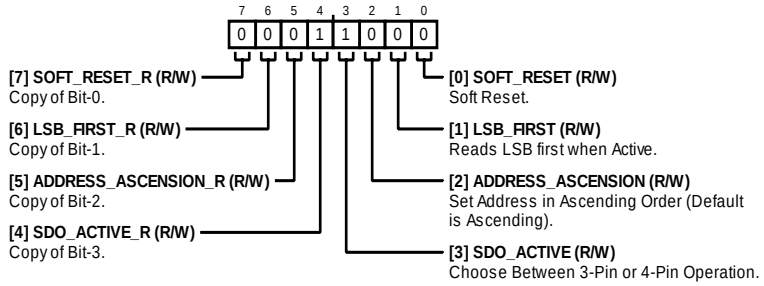


Table 9. Bit Descriptions for REG0000

Bit(s)	Bit Name	Description	Default	Access
7	SOFT_RESET_R	Copy of Bit 0.	0x0	R/W
6	LSB_FIRST_R	Copy of Bit 1.	0x0	R/W
5	ADDRESS_ASCENSION_R	Copy of Bit 2.	0x0	R/W
4	SDO_ACTIVE_R	Copy of Bit 3.	0x1	R/W
3	SDO_ACTIVE	Choose between 3-pin or 4-pin operation. 0: 3-pin. 1: 4-pin. Enables the SDIO pin and the SDIO pin becomes an input only.	0x1	R/W
2	ADDRESS_ASCENSION	Set Address in Ascending Order (Default Is Ascending). 0: descending. 1: ascending.	0x0	R/W
1	LSB_FIRST	Reads LSB First when Active.	0x0	R/W
0	SOFT_RESET	Soft Reset. 0: normal operation. 1: soft reset.	0x0	R/W

Address: 0x01, Default: 0x00, Name: REG0001

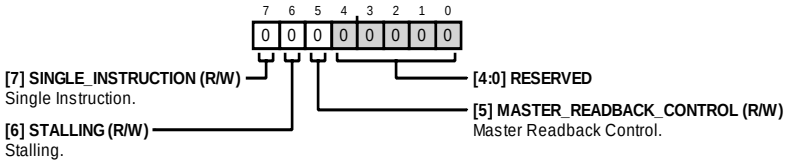


Table 10. Bit Descriptions for REG0001

Bit(s)	Bit Name	Description	Default	Access
7	SINGLE_INSTRUCTION	Single Instruction. SPI stream mode is disabled if the SINGLE_INSTRUCTION bit is set to 1.	0x0	R/W
6	STALLING	Stalling.	0x0	R/W
5	MASTER_READBACK_CONTROL	Master Readback Control.	0x0	R/W
[4:0]	RESERVED	Reserved.	0x0	R

Address: 0x10, Default: 0x32, Name: REG0010

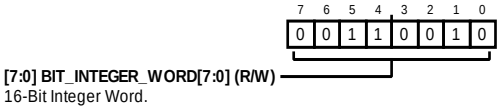


Table 11. Bit Descriptions for REG0010

Bit(s)	Bit Name	Description	Default	Access
[7:0]	BIT_INTEGER_WORD[7:0]	16-Bit Integer Word. Sets the integer value of N (for the internal PLL). Updates to the PLL N counter, including FRAC1, FRAC2, and MOD2, are double buffered by this bit field.	0x32	R/W

Address: 0x11, Default: 0x00, Name: REG0011

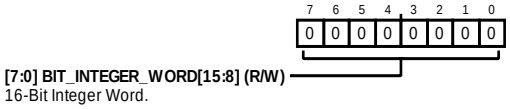


Table 12. Bit Descriptions for REG0011

Bit(s)	Bit Name	Description	Default	Access
[7:0]	BIT_INTEGER_WORD[15:8]	16-Bit Integer Word. Sets the integer value of N.	0x0	R/W

Address: 0x12, Default: 0x40, Name: REG0012

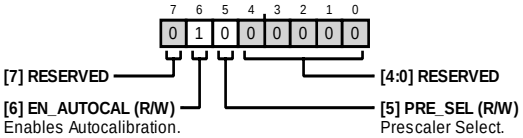


Table 13. Bit Descriptions for REG0012

Bit(s)	Bit Name	Description	Default	Access
7	RESERVED	Reserved.	0x0	R
6	EN_AUTOCAL	Enables Autocalibration. 0: VCO autocalibration disabled. 1: VCO autocalibration enabled.	0x1	R/W
5	PRE_SEL	Prescaler Select. The dual modulus prescaler for the calibration PLL is set by the PRE_SEL bit. The prescaler, at the input to the N divider, divides down the VCO signal so the N divider can handle it. The prescaler setting affects the RF frequency and the minimum and maximum INT values. 0: 4/5 prescaler. 1: 8/9 prescaler.	0x0	R/W
[4:0]	RESERVED	Reserved.	0x0	R

Address: 0x14, Default: 0x00, Name: REG0014

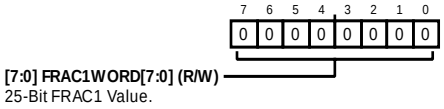


Table 14. Bit Descriptions for REG0014

Bit(s)	Bit Name	Description	Default	Access
[7:0]	FRAC1WORD[7:0]	25-Bit FRAC1 Value. Sets the FRAC1 value.	0x0	R/W

Address: 0x15, Default: 0x00, Name: REG0015

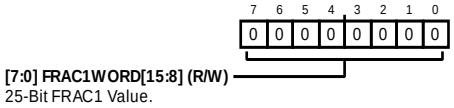


Table 15. Bit Descriptions for REG0015

Bit(s)	Bit Name	Description	Default	Access
[7:0]	FRAC1WORD[15:8]	25-Bit FRAC1 Value. Sets the FRAC1 value.	0x0	R/W

Address: 0x16, Default: 0x00, Name: REG0016

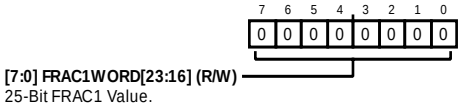


Table 16. Bit Descriptions for REG0016

Bit(s)	Bit Name	Description	Default	Access
[7:0]	FRAC1WORD[23:16]	25-Bit FRAC1 Value. Sets the FRAC1 value.	0x0	R/W

Address: 0x17, Default: 0x00, Name: REG0017

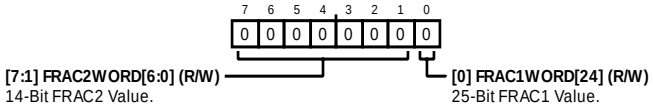


Table 17. Bit Descriptions for REG0017

Bit(s)	Bit Name	Description	Default	Access
[7:1]	FRAC2WORD[6:0]	14-Bit FRAC2 Value. Sets the FRAC2 value.	0x0	R/W
0	FRAC1WORD[24]	25-Bit FRAC1 Value. Sets the FRAC1 value.	0x0	R/W

Address: 0x18, Default: 0x00, Name: REG0018

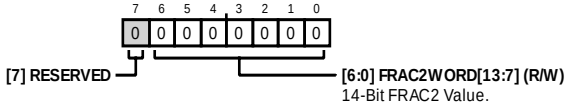


Table 18. Bit Descriptions for REG0018

Bit(s)	Bit Name	Description	Default	Access
7	RESERVED	Reserved.	0x0	R
[6:0]	FRAC2WORD[13:7]	14-Bit FRAC2 Value. Sets the FRAC2 value.	0x0	R/W

Address: 0x19, Default: 0xE8, Name: REG0019

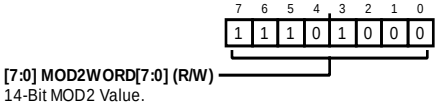


Table 19. Bit Descriptions for REG0019

Bit(s)	Bit Name	Description	Default	Access
[7:0]	MOD2WORD[7:0]	14-Bit MOD2 Value. Sets the MOD2 value.	0xE8	R/W

Address: 0x1A, Default: 0x03, Name: REG001A

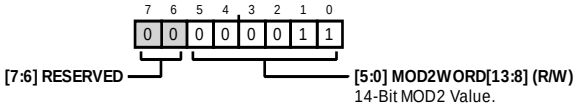


Table 20. Bit Descriptions for REG001A

Bit(s)	Bit Name	Description	Default	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	MOD2WORD[13:8]	14-Bit MOD2 Value. Sets the MOD2 value.	0x3	R/W

Address: 0x1E, Default: 0x48, Name: REG001E

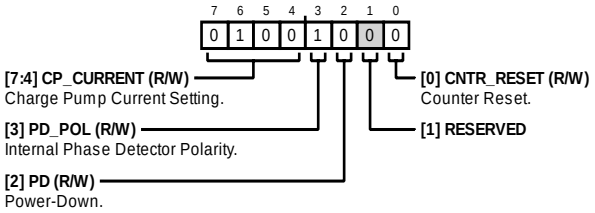


Table 21. Bit Descriptions for REG001E

Bit(s)	Bit Name	Description	Default	Access
[7:4]	CP_CURRENT	Charge Pump Current Setting. Sets the charge pump current. Set the CP_CURRENT bits to the charge pump current that the loop filter is designed for. 0: 0.35 mA. 1: 0.70 mA. 10: 1.05 mA. 11: 1.4 mA. 100: 1.75 mA. 101: 2.1 mA. 110: 2.45 mA. 111: 2.8 mA. 1000: 3.15 mA. 1001: 3.5 mA. 1010: 3.85 mA. 1011: 4.2 mA. 1100: 4.55 mA. 1101: 4.9 mA. 1110: 5.25 mA. 1111: 5.6 mA.	0x4	R/W
3	PD_POL	Internal Phase Detector Polarity. If using a noninverting loop filter, set phase detector polarity to positive. If using an inverting loop filter, set phase detector polarity to negative. 0: negative phase detector polarity. 1: positive phase detector polarity.	0x1	R/W
2	PD	Power-Down. Setting to 1 powers down all internal PLL blocks of the VCO/PLL. The VCO and multipliers remain powered up. The registers do not lose their values. After bringing the ADF4401A back to calibration mode (setting to 0) a write to REG0010 is required to relock the calibration loop. 0: calibration mode. 1: translation loop mode.	0x0	R/W
1	RESERVED	Reserved.	0x0	R
0	CNTR_RESET	Counter Reset. Setting to 1 holds the N divider and R counter in reset. There are no signals entering the PFD. 0: normal operation. 1: counter reset.	0x0	R/W

Address: 0x1F, Default: 0x01, Name: REG001F

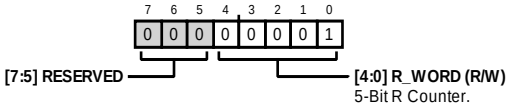


Table 22. Bit Descriptions for REG001F

Bit(s)	Bit Name	Description	Default	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	R_WORD	5-Bit R Counter.	0x1	R/W

Address: 0x20, Default: 0x14, Name: REG0020

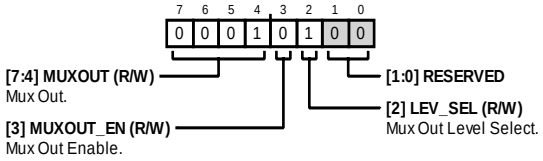


Table 23. Bit Descriptions for REG0020

Bit(s)	Bit Name	Description	Default	Access
[7:4]	MUXOUT	Mux Out. Is used to set the mux out signal when MUXOUT_EN = 1. 0: tristate, high impedance output (only works when MUXOUT_EN = 0). 1: digital lock detect for calibration PLL. 10: charge pump up. 11: charge pump down. 100: R divider output/2. 101: N divider output/2. 110: VCO test modes. 111: reserved. 1000: high. 1001: VCO calibration R band/2. 1010: VCO calibration N band/2.	0x1	R/W
3	MUXOUT_EN	Mux Out Enable. Set to 0 if using 4-wire SPI. 0: MUXOUT pin is configured as serial data output for 4-wire SPI. Mux out functionality is disabled. 1: MUXOUT pin is configured for mux out functionality.	0x0	R/W
2	LEV_SEL	Mux Out Level Select. Select the voltage level of the logic at the mux out. 0: 1.8 V logic. 1: 3.3 V logic.	0x1	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x22, Default: 0x00, Name: REG0022

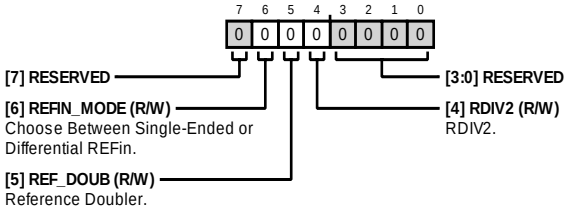


Table 24. Bit Descriptions for REG0022

Bit(s)	Bit Name	Description	Default	Access
7	RESERVED	Reserved.	0x0	R
6	REFIN_MODE	Choose Between Single-Ended or Differential REF_{IN}. 0: single-ended REF_{IN}. 1: differential REF_{IN}.	0x0	R/W
5	REF_DOUB	Reserved.	0x0	R/W
4	RDIV2	RDIV2. Controls the reference divide by 2 clock. This feature can be used to provide a 50% duty cycle signal to the PFD. 0: RDIV2 disabled. 1: RDIV2 enabled.	0x0	R/W
[3:0]	RESERVED	Reserved.	0x0	R

Address: 0x24, Default: 0x80, Name: REG0024

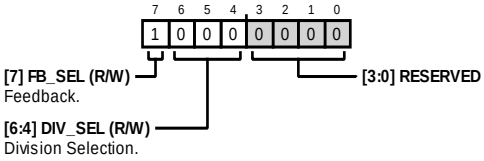


Table 25. Bit Descriptions for REG0024

Bit(s)	Bit Name	Description	Default	Access
7	FB_SEL	Feedback. 0: divider feedback to N counter. 1: fundamental feedback to N counter.	0x1	R/W
[6:4]	DIV_SEL	Division Selection. 0: divide 1. 1: divide 2. 10: divide 4. 11: divide 8. 100: divide 16. 101: divide 32. 110: divide 64. 111: reserved.	0x0	R/W
[3:0]	RESERVED	Reserved.	0x0	R

Address: 0x25, Default: 0x07, Name: REG0025

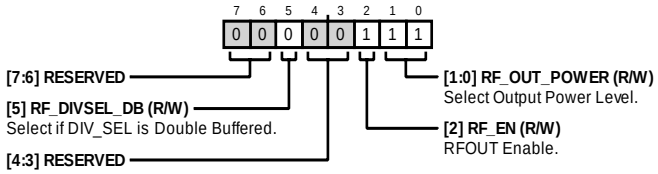


Table 26. Bit Descriptions for REG0025

Bit(s)	Bit Name	Description	Default	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	RF_DIVSEL_DB	Select if DIV_SEL is Double Buffered.	0x0	R/W
[4:3]	RESERVED	Reserved.	0x0	R/W
2	RF_EN	RF_{OUT} Enable. 0: RF_{OUT} disabled. 1: RF_{OUT} enabled.	0x1	R/W
[1:0]	RF_OUT_POWER	Select Output Power Level. 0: −4 dBm. 1: −1 dBm. 10: 2 dBm. 11: 5 dBm.	0x3	R/W

Address: 0x27, Default: 0xC5, Name: REG0027

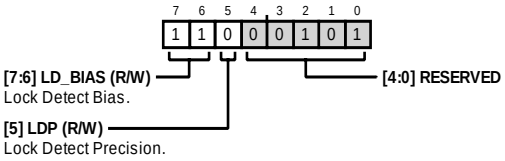


Table 27. Bit Descriptions for REG0027

Bit(s)	Bit Name	Description	Default	Access
[7:6]	LD_BIAS	Lock Detect Bias. The lock detector window size is set by adjusting the lock detector bias in conjunction with the lock detector precision. 0: 5 ns lock detect delay if LDP = 0. 1: 6 ns. 10: 8 ns. 11: 12 ns lock detect delay (for large values of bleed)	0x3	R/W
5	LDP	Lock Detect Precision. Controls the sensitivity of the digital lock detector, depending on INT or FRAC operation selected. 0: FRAC mode (5 ns). 1: INT mode (2.4 ns).	0x0	R/W
[4:0]	RESERVED	Reserved.	0x5	R/W

Address: 0x28, Default: 0x03, Name: REG0028

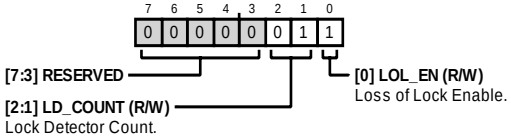


Table 28. Bit Descriptions for REG0028

Bit(s)	Bit Name	Description	Default	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:1]	LD_COUNT	Lock Detector Count. Initial value of the lock detector. This field sets the number of counts of PFD within lock window before asserting digital lock detect high. 0: 1024 cycles. 1: 2048 cycles. 10: 4096 cycles. 11: 8192 cycles.	0x1	R/W
0	LOL_EN	Loss of Lock Enable. When loss of lock is enabled, if the digital lock detect is asserted, and the reference signal is removed, digital lock detect goes low. It is recommended to set to 1 to enable loss of lock. 0: disabled. 1: loss of lock enabled.	0x1	R/W

Address: 0x2B, Default: 0x01, Name: REG002B

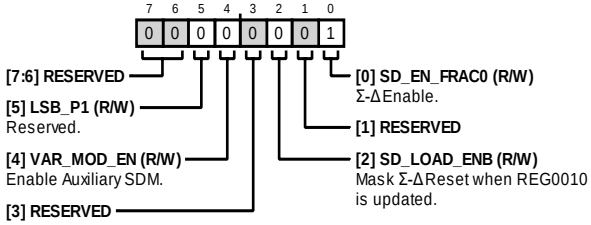


Table 29. Bit Descriptions for REG002B

Bit(s)	Bit Name	Description	Default	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	LSB_P1	Reserved.	0x0	R/W
4	VAR_MOD_EN	Enable Auxiliary SDM. Set to 0 for normal operation.	0x0	R/W
3	RESERVED	Reserved.	0x0	R
2	SD_LOAD_ENB	Mask Σ-Δ Reset when REG0010 is updated.	0x0	R/W
1	RESERVED	Reserved.	0x0	R
0	SD_EN_FRAC0	Σ-Δ Enable. Set to 1 when in INT mode (when FRAC1 = FRAC2 = 0), and set to 0 when in FRAC mode. 0: Σ-Δ enabled (for fractional mode). 1: Σ-Δ disabled (for integer mode).	0x1	R/W

Address: 0x2C, Default: 0x44, Name: REG002C

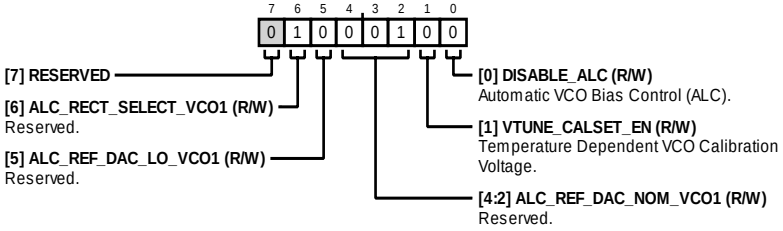


Table 30. Bit Descriptions for REG002C

Bit(s)	Bit Name	Description	Default	Access
7	RESERVED	Reserved.	0x0	R
6	ALC_RECT_SELECT_VCO1	Reserved.	0x1	R/W
5	ALC_REF_DAC_LO_VCO1	Reserved.	0x0	R/W
[4:2]	ALC_REF_DAC_NOM_VCO1	Reserved.	0x1	R/W
1	VTUNE_CALSET_EN	Temperature Dependent VCO Calibration Voltage. 0: disable temperature dependent VCO calibration voltage. 1: enable temperature dependent VCO calibration voltage.	0x0	R/W
0	DISABLE_ALC	Automatic VCO Bias Control (ALC). 0: ALC enabled. 1: ALC disabled.	0x0	R/W

Address: 0x2D, Default: 0x11, Name: REG002D

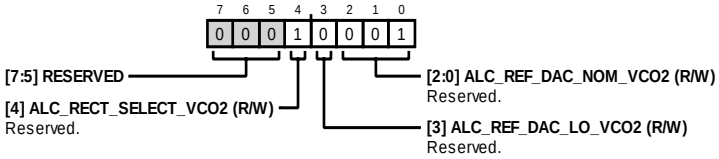


Table 31. Bit Descriptions for REG002D

Bit(s)	Bit Name	Description	Default	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	ALC_RECT_SELECT_VCO2	Reserved.	0x1	R/W
3	ALC_REF_DAC_LO_VCO2	Reserved.	0x0	R/W
[2:0]	ALC_REF_DAC_NOM_VCO2	Reserved.	0x1	R/W

Address: 0x2E, Default: 0x10, Name: REG002E

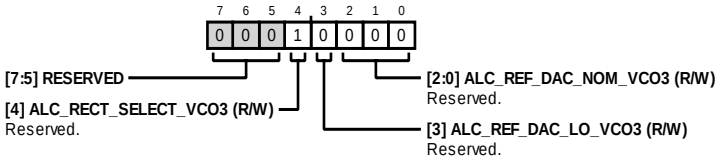


Table 32. Bit Descriptions for REG002E

Bit(s)	Bit Name	Description	Default	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	ALC_RECT_SELECT_VCO3	Reserved.	0x1	R/W
3	ALC_REF_DAC_LO_VCO3	Reserved.	0x0	R/W
[2:0]	ALC_REF_DAC_NOM_VCO3	Reserved.	0x0	R/W

Address: 0x2F, Default: 0x92, Name: REG002F

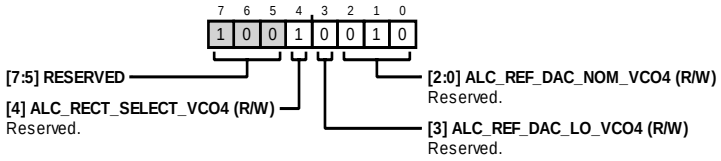


Table 33. Bit Descriptions for REG002F

Bit(s)	Bit Name	Description	Default	Access
[7:5]	RESERVED	Reserved. Set to 0x4 for normal operation.	0x4	R/W
4	ALC_RECT_SELECT_VCO4	Reserved.	0x1	R/W
3	ALC_REF_DAC_LO_VCO4	Reserved.	0x0	R/W
[2:0]	ALC_REF_DAC_NOM_VCO4	Reserved.	0x2	R/W

Address: 0x30, Default: 0x3F, Name: REG0030

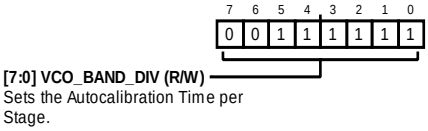


Table 34. Bit Descriptions for REG0030

Bit(s)	Bit Name	Description	Default	Access
[7:0]	VCO_BAND_DIV	Sets the Autocalibration Time per Stage. See the VCO Calibration Time section for details.	0x3F	R/W

Address: 0x31, Default: 0xA7, Name: REG0031

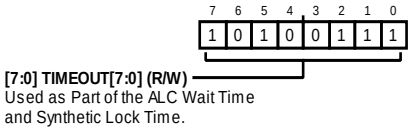


Table 35. Bit Descriptions for REG0031

Bit(s)	Bit Name	Description	Default	Access
[7:0]	TIMEOUT[7:0]	Used as Part of the ALC Wait Time and Synthetic Lock Time. See the VCO Calibration Time section for details.	0xA7	R/W

Address: 0x32, Default: 0x04, Name: REG0032

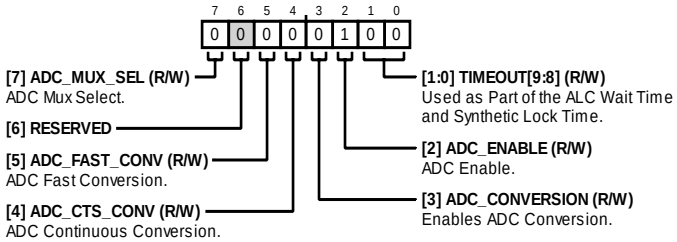


Table 36. Bit Descriptions for REG0032

Bit(s)	Bit Name	Description	Default	Access
7	ADC_MUX_SEL	ADC Mux Select. 0: proportional to absolute temperature (PTAT) voltage muxed to ADC input. 1: scaled VTUNE voltage muxed to ADC input.	0x0	R/W
6	RESERVED	Reserved.	0x0	R

Bit(s)	Bit Name	Description	Default	Access
5	ADC_FAST_CONV	ADC Fast Conversion. 0: disabled. 1: enabled.	0x0	R/W
4	ADC_CTS_CONV	ADC Continuous Conversion. 0: disabled. 1: enabled.	0x0	R/W
3	ADC_CONVERSION	Enables ADC Conversion. 0: no ADC conversion. 1: perform ADC conversion on REG0000 write if ADC is enabled.	0x0	R/W
2	ADC_ENABLE	ADC Enable. 0: disabled. 1: enabled.	0x1	R/W
[1:0]	TIMEOUT[9:8]	Used as Part of the ALC Wait Time and Synthetic Lock Time. See the VCO Calibration Time section for details.	0x0	R/W

Address: 0x33, Default: 0x0C, Name: REG0033

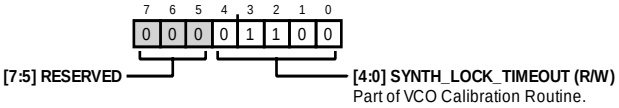


Table 37. Bit Descriptions for REG0033

Bit(s)	Bit Name	Description	Default	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	SYNTH_LOCK_TIMEOUT	Part of VCO Calibration Routine. See the VCO Calibration Time section for details.	0xC	R/W

Address: 0x34, Default: 0x9E, Name: REG0034

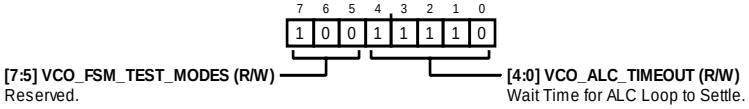


Table 38. Bit Descriptions for REG0034

Bit(s)	Bit Name	Description	Default	Access
[7:5]	VCO_FSM_TEST_MODES	Reserved.	0x4	R/W
[4:0]	VCO_ALC_TIMEOUT	Wait Time for ALC Loop to Settle. See the VCO Calibration Time section for details.	0x1E	R/W

Address: 0x35, Default: 0x4C, Name: REG0035

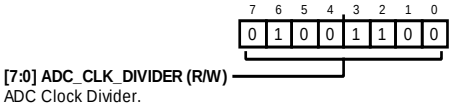


Table 39. Bit Descriptions for REG0035

Bit(s)	Bit Name	Description	Default	Access
[7:0]	ADC_CLK_DIVIDER	ADC Clock Divider. ADC clock = f_{PFD}/((ADC_CLK_DIVIDER × 4) + 2). Target 100 kHz for ADC clock Refer to AN-2005 for more details.	0x4C	R/W

Address: 0x36, Default: 0x30, Name: REG0036

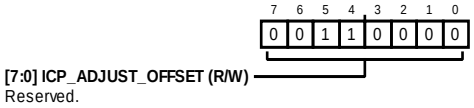


Table 40. Bit Descriptions for REG0036

Bit(s)	Bit Name	Description	Default	Access
[7:0]	ICP_ADJUST_OFFSET	Reserved.	0x30	R/W

Address: 0x37, Default: 0x00, Name: REG0037

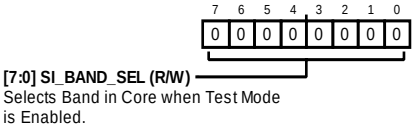


Table 41. Bit Descriptions for REG0037

Bit(s)	Bit Name	Description	Default	Access
[7:0]	SI_BAND_SEL	Selects Band in Core when Test Mode is Enabled.	0x0	R/W

Address: 0x38, Default: 0x00, Name: REG0038

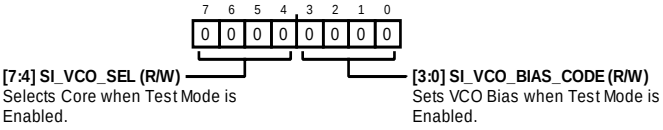


Table 42. Bit Descriptions for REG0038

Bit(s)	Bit Name	Description	Default	Access
[7:4]	SI_VCO_SEL	Selects Core when Test Mode is Enabled. 0: all cores off. 1: VCO Core D. 10: VCO Core C. 100: VCO Core B. 1000: VCO Core A.	0x0	R/W
[3:0]	SI_VCO_BIAS_CODE	Sets VCO Bias when Test Mode is Enabled. 0000: maximum VCO bias (approximately 3.2 V). 1111: minimum VCO bias (approximately 1.8 V).	0x0	R/W

Address: 0x39, Default: 0x07, Name: REG0039

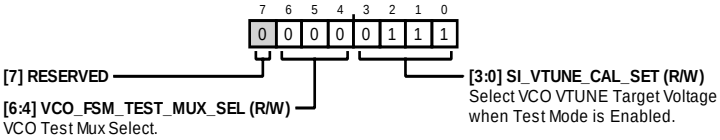


Table 43. Bit Descriptions for REG0039

Bit(s)	Bit Name	Description	Default	Access
7	RESERVED	Reserved.	0x0	R
[6:4]	VCO_FSM_TEST_MUX_SEL	VCO Test Mux Select. 0: busy. 1: N band. 10: R band. 11: reserved. 100: timeout clock.	0x0	R/W

Bit(s)	Bit Name	Description	Default	Access
		101: bias minimum. 110: ADC busy. 111: logic low.		
[3:0]	SI_VTUNE_CAL_SET	Select VCO VTUNE Target Voltage when Test Mode is Enabled. 0: 0.58 V. 1: 0.73 V. 10: 0.88 V. 11: 1.03 V. 100: 1.18 V. 101: 1.33 V. 110: 1.48 V. 111: 1.63 V. 1000: 1.78 V. 1001: 1.93 V. 1010: 2.08 V. 1011: 2.23 V. 1100: 2.38 V. 1101: 2.53 V. 1110: 2.68 V. 1111: 2.83 V.	0x7	R/W

Address: 0x3A, Default: 0x55, Name: REG003A

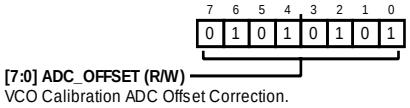


Table 44. Bit Descriptions for REG003A

Bit(s)	Bit Name	Description	Default	Access
[7:0]	ADC_OFFSET	VCO Calibration ADC Offset Correction.	0x55	R/W

Address: 0x3E, Default: 0x0C, Name: REG003E

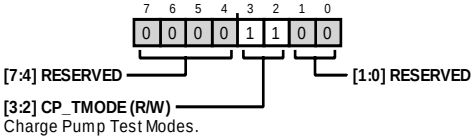


Table 45. Bit Descriptions for REG003E

Bit(s)	Bit Name	Description	Default	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:2]	CP_TMODE	Charge Pump Test Modes 0: CP tristate 11: normal operation	0x3	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x3F, Default: 0x80, Name: REG003F

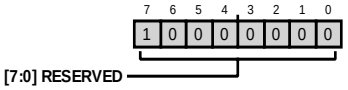


Table 46. Bit Descriptions for REG003F

Bit(s)	Bit Name	Description	Default	Access
[7:0]	RESERVED	Reserved.	0x80	R/W

Address: 0x40, Default: 0x50, Name: REG0040

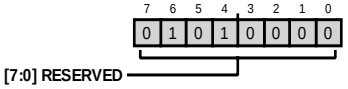


Table 47. Bit Descriptions for REG0040

Bit(s)	Bit Name	Description	Default	Access
[7:5]	RESERVED	Reserved.	0x50	R

Address: 0x41, Default: 0x28, Name: REG0041

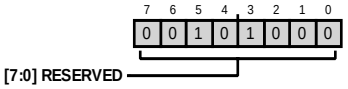


Table 48. Bit Descriptions for REG0041

Bit(s)	Bit Name	Description	Default	Access
[7:0]	RESERVED	Reserved.	0x28	R/W

Address: 0x47, Default: 0xC0, Name: REG0047

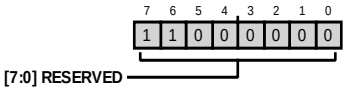


Table 49. Bit Descriptions for REG0047

Bit(s)	Bit Name	Description	Default	Access
[7:0]	RESERVED	Reserved.	0xC0	R

Address: 0x52, Default: 0xF4, Name: REG0052

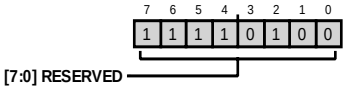


Table 50. Bit Descriptions for REG0052

Bit(s)	Bit Name	Description	Default	Access
[7:0]	RESERVED	Reserved.	0xF4	R

Address: 0x6E, Default: 0x00, Name: REG006E

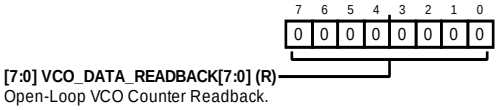


Table 51. Bit Descriptions for REG006E

Bit(s)	Bit Name	Description	Default	Access
[7:0]	VCO_DATA_READBACK[7:0]	Open-Loop VCO Counter Readback.	0x0	R

Address: 0x6F, Default: 0x00, Name: REG006F

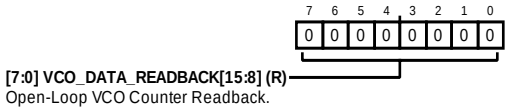


Table 52. Bit Descriptions for REG006F

Bit(s)	Bit Name	Description	Default	Access
[7:0]	VCO_DATA_READBACK[15:8]	Open-Loop VCO Counter Readback.	0x0	R

Address: 0x72, Default: 0x32, Name: REG0072

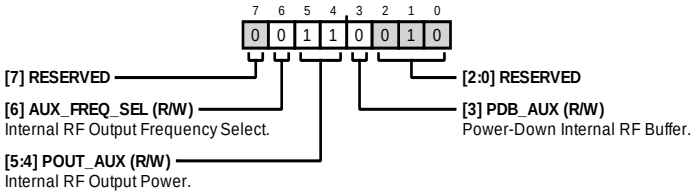


Table 53. Bit Descriptions for REG0072

Bit(s)	Bit Name	Description	Default	Access
7	RESERVED	Reserved.	0x0	R
6	AUX_FREQ_SEL	Internal RF Output Frequency Select. This selects the VCO fundamental or divided frequency to the downconversion mixer. 0: divided output. 1: VCO output.	0x0	R/W
[5:4]	POUT_AUX	Internal RF Output Power. Sets the power at the auxiliary RF port, which drives the mixer path. 0: low power. 1: high power.	0x1	R/W
3	PDB_AUX	Power-Down Internal RF Buffer. This must be set to 1 for normal operation.	0x1	R/W
[2:0]	RESERVED	Reserved.	0x2	R

Address: 0x73, Default: 0x00, Name: REG0073

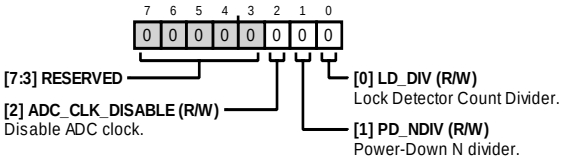


Table 54. Bit Descriptions for REG0073

Bits	Bit Name	Description	Default	Access
[7:3]	RESERVED	Reserved.	0x0	R
2	ADC_CLK_DISABLE	Disable ADC Clock. ADC_ENABLE setting overwrites this bit.	0x0	R/W
1	PD_NDIV	Power-Down N Divider.	0x0	R/W
0	LD_DIV	Lock Detector Count Divider. Divides the lock detector count cycles by 32 so that the LD_COUNT bits in the REG0028 register can be selected as 32, 64, 128, and 256.	0x0	R/W

Address: 0x7C, Default: 0x00, Name: REG007C

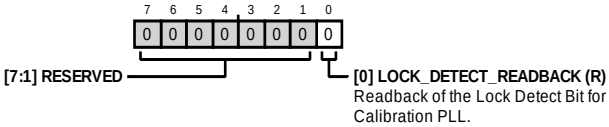


Table 55. Bit Descriptions for REG007C

Bit(s)	Bit Name	Description	Default	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	LOCK_DETECT_READBACK	Readback of the Lock Detect Bit for Calibration PLL.	0x0	R

OUTLINE DIMENSIONS

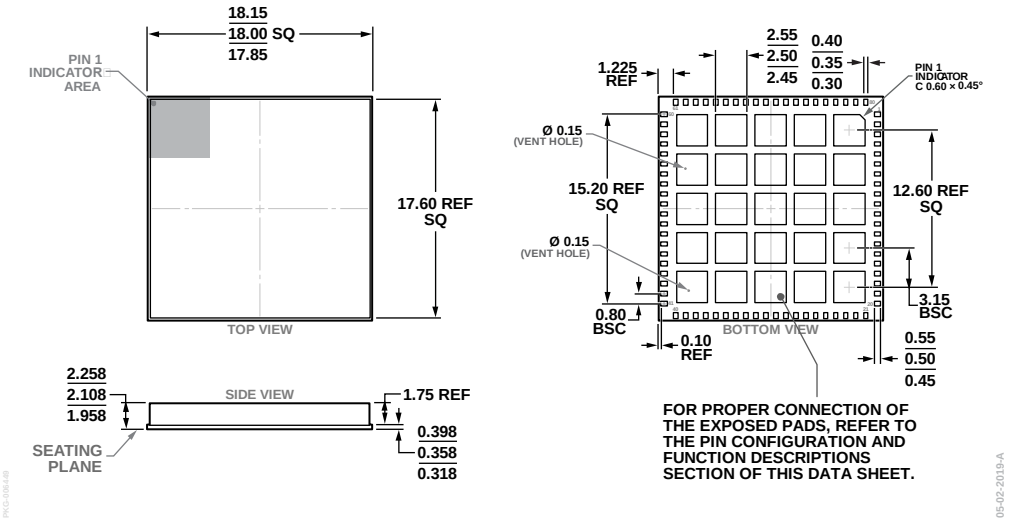


Figure 35. 80-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]
18.00 mm × 18.00 mm Body and 2.108 mm Package Height
(CE-80-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF4401ABCEZ	−25°C to +85°C	80-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]	CE-80-1
EV-ADF4401ASD2Z		Evaluation Board	

[1] Z = RoHS Compliant Part.

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