DS2465

DeepCover Secure Authenticator with SHA-256 Coprocessor and 1-Wire Master Function

General Description

DeepCover® embedded security solutions cloak sensitive data under multiple layers of advanced physical security to provide the most secure key storage possible.

The DeepCover Secure Authenticator (DS2465) is a SHA-256 coprocessor with built-in 1-Wire® master that provides the SHA-256 and memory functionality required by a host system to communicate with and operate a 1-Wire SHA-256 slave. In addition, it performs protocol conversion between the I²C master and any attached 1-Wire SHA-256 slaves. For 1-Wire line driving, internal user-adjustable timers relieve the system host processor from generating time-critical 1-Wire waveforms, supporting both standard and overdrive 1-Wire communication speeds. The 1-Wire line can be powered down under software control. Strong pullup features support 1-Wire power delivery to 1-Wire devices such as EEPROMs. When not in use, the DS2465 can be put in sleep mode where power consumption is minimal.

Ordering Information appears at end of data sheet.

Features

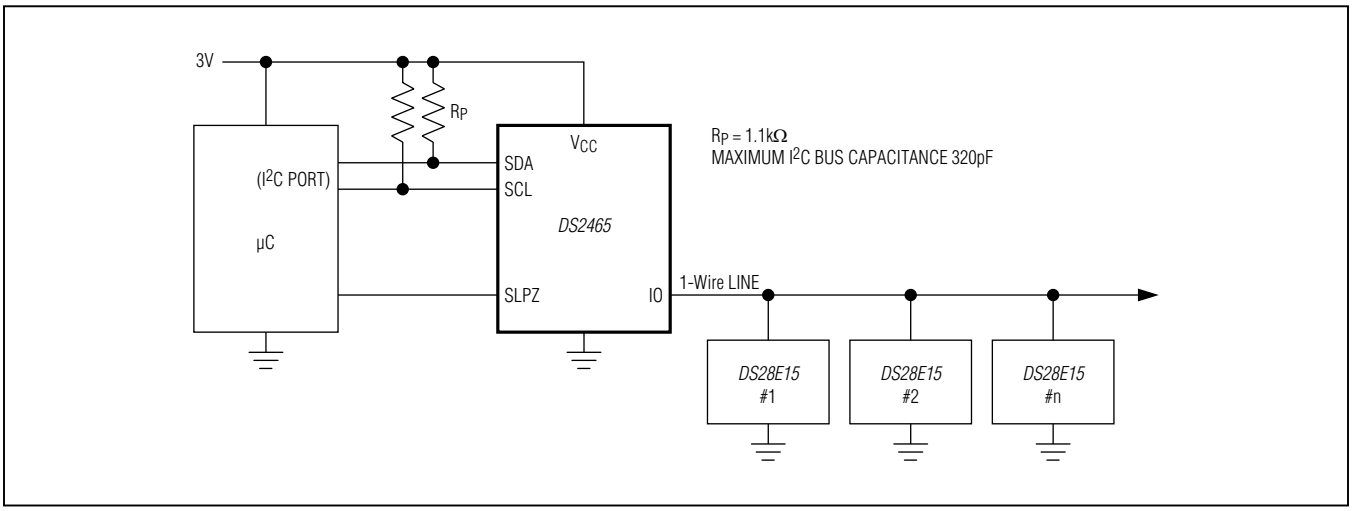
- **SHA-256 Engine to Operate a Symmetric-Key-Based Bidirectional Secure Authentication Model**
- **Two 32-Byte Pages of User EEPROM with Multiple Programmable Protection Options**
- **1-Wire Master Port with Selectable Active or Passive 1-Wire Pullup**
- **Strong 1-Wire Pullup Provided by an Internal Low-Impedance Signal Path**
- **1-Wire Port Can Be Powered Down Under Software Control**
- **I²C Operating (Pullup) Voltage: 3.3V ±10%**
- **±8kV ESD Protection on IO to GND (JESD22-A114 HBM, Typical)**
- **Operating Range: 3.3V ±10%, -40°C to +85°C**
- **6-Pin TSOC Package**

Applications

Authentication of Consumables

Secure Feature Control

Typical Application Circuit



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For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

219-0017; Rev 3; 9/13

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to GND .....-0.5V to +4.0V
Maximum Current into Any Pin.....20mA
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.97	3.3	3.63	V
Supply Current	I_{CC}	(Note 2)			750	µA
		Sleep mode (SLPZ pin low), V_{CC} = 3.63V		0.5	1.0	
Power-On Reset Trip Point	V_{POR}	(Note 3)		1.0	1.4	V
1-Wire Input High	V_{IH1}		0.6 x V_{CC}			V
1-Wire Input Low	V_{IL1}				0.2 x V_{CC}	V
1-Wire Weak Pullup Resistor (Notes 3, 4)	R_{WPU}	Low range	375	500	750	Ω
		High range	750	1000	1350	
1-Wire Output Low	V_{OL1}	V_{CC} = 2.97V, 8mA sink current			0.25	
Active Pullup On Threshold	V_{IAPO}	(Note 3)		0.95	1.2	V
Active Pullup On Time (Notes 3, 5)	t_{APU}	1-Wire time slot	Equal to t_{REC0}			µs
		1-Wire reset standard speed	2.375	2.5	2.625	
		1-Wire reset overdrive speed	0.475	0.5	0.525	
Active Pullup Impedance	R_{APU}	V_{CC} = 2.97V, 4mA load (Note 3)			60	Ω
1-Wire Output Fall Time (Note 3)	t_F	Standard	0.25		1	µs
		Overdrive	0.05		0.2	
IO PIN: 1-Wire TIMING (Note 6)						
Reset Low Time	t_{RSTL}	Standard	-5%	See Table 6	+9%	µs
		Overdrive				
Reset High Time	t_{RSTH}	Standard and overdrive	Equal to t_{RSTL}			µs
Presence-Detect Sample Time	t_{MSP}	Standard	-5%	See Table 6	+9%	µs
		Overdrive				
Sampling for Short and Interrupt	t_{SI}	Standard	7.6	8	8.72	µs
		Overdrive	1.9	2	2.18	
Write-1/Read Low Time	t_{W1L}	Standard	7.6	8	8.72	µs
		Overdrive	-5%	See Table 6	+9%	

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ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Read Sample Time	t_{MSR}	Standard	11.4	12	13.1	µs
		Overdrive	1.4	1.5	1.64	
Write-0 Low Time	t_{W0L}	Standard	-5%	See Table 6	+9%	µs
		Overdrive				
Write-0 Recovery Time	t_{REC0}	Standard and overdrive	-5%	See Table 6	+9%	µs
1-Wire Time Slot	t_{slot}	Standard and overdrive	Equal to t_{W0L} + t_{REC0}			µs
SHA-256 ENGINE						
Computation Current	I_{CSHA}	**Refer to the full data sheet.**				mA
Computation Time	t_{CSHA}					ms
EEPROM						
Programming Current	I_{PROG}	(Notes 3, 7)			2	mA
Programming Time for a 32-Bit Segment	t_{PROG}				10	ms
Write/Erase Cycling Endurance	N_{CY}	T_A = +85°C (Notes 8, 9)	100k			—
Data Retention	t_{DR}	T_A = +85°C (Notes 10, 11)	10			Years
SLPZ PIN						
Low Level Input Voltage	V_{IL}		-0.5		0.3 x V_{CC}	V
High Level Input Voltage	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.5V	V
Input Leakage Current	I_I	Pin at 3.63V (Note 3)			0.1	µA
Wake-Up Time from Sleep Mode	t_{SWUP}	(Note 12)			200	µs
I²C SCL AND SDA PINS (Note 13)						
Low Level Input Voltage	V_{IL}		-0.5		0.3 x V_{CC}	V
High Level Input Voltage	V_{IH}		0.7 x V_{CC}		$V_{CC(MAX)}$ + 0.5V	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	(Note 3)	0.05 x V_{CC}			V
Low Level Output Voltage at 3mA Sink Current	V_{OL}				0.4	V
Output Fall Time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$ with a Bus Capacitance from 10pF to 400pF	t_{OF}	(Note 3)	60		250	ns
Pulse Width of Spikes That Are Suppressed by the Input Filter	t_{SP}	(Note 3)			50	ns
Input Current with an Input Voltage Between 0.1$V_{CC(MAX)}$ and 0.9$V_{CC(MAX)}$	I_I	(Notes 3, 14)	-10		+10	µA

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ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	(Note 3)			10	pF
SCL Clock Frequency	f_{SCL}		0		400	kHz
Hold Time (Repeated) START Condition; After this Period, the First Clock Pulse is Generated	$t_{HD:STA}$	(Note 3)	0.6			µs
Low Period of the SCL Clock	t_{LOW}	(Note 3)	1.3			µs
High Period of the SCL Clock	t_{HIGH}	(Note 3)	0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$	(Note 3)	0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Notes 3, 15, 16)			0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Notes 3, 17)	250			ns
Setup Time for STOP Condition	$t_{SU:STO}$	(Note 3)	0.6			µs
Bus Free Time Between a STOP and START Condition	t_{BUF}	(Note 3)	1.3			µs
Capacitive Load for Each Bus Line	C_B	(Notes 3, 18)			400	pF
Oscillator Warmup Time	t_{OSCWUP}	(Note 12)			200	µs

Note 1: Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.

Note 2: Operating current with 1-Wire write byte sequence followed by continuous read of 1-Wire Master Status register at 400kHz in overdrive.

Note 3: Guaranteed by design and/or characterization only. Not production tested.

Note 4: Active pullup or resistive pullup and range are configurable.

Note 5: The active pullup does not apply to the rising edge of a presence pulse outside of a 1-Wire Reset Pulse command or during the recovery after a short on the 1-Wire line.

Note 6: All 1-Wire timing specifications are derived from the same timing circuit.

Note 7: Current drawn from V_{CC} during the EEPROM programming interval or SHA-256 computation.

Note 8: Write-cycle endurance is tested in compliance with JESD47G.

Note 9: Not 100% production tested; guaranteed by reliability monitor sampling.

Note 10: Data retention is tested in compliance with JESD47G.

Note 11: Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to the data sheet limit at operating temperature range is established by reliability testing.

Note 12: I^2C communication should not take place for the max t_{OSCWUP} or t_{SWUP} time following a power-on reset or a wake-up from sleep mode.

Note 13: All I^2C timing values are referred to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

Note 14: I/O pins of the DS2465 do not obstruct the SDA and SCL lines if V_{CC} is switched off.

Note 15: The DS2465 provides a hold time of at least 300ns for the SDA signal (referenced to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 16: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the setup time before it releases the clock (I^2C bus specification Rev. 03, 19 June 2007).

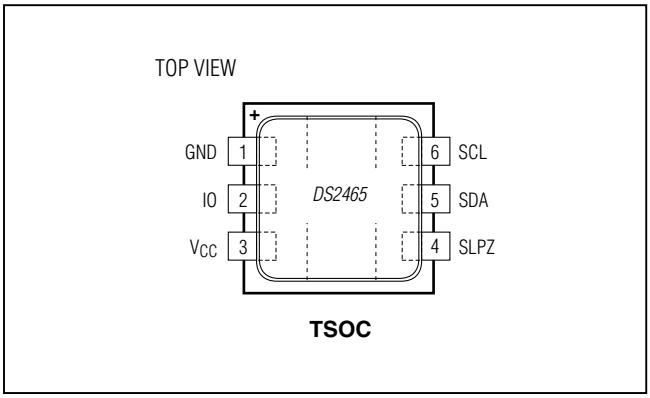
Note 17: A fast-mode I^2C bus device can be used in a standard-mode I^2C-bus system, but the requirement $t_{SU:DAT} \geq 250ns$ must then be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{R(MAX)} + t_{SU:DAT} = 1000 + 250 = 1250ns$ (according to the standard-mode I^2C bus specification) before the SCL line is released. Also the acknowledge timing must meet this setup time (I^2C bus specification Rev. 03, 19 June 2007).

Note 18: C_B = Total capacitance of one bus line in pF. The maximum bus capacitance allowable may vary from this value depending on the actual operating voltage and frequency of the application (I^2C bus specification Rev. 03, 19 June 2007).

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Pin Configuration



TSOC

Pin Description

PIN	NAME	FUNCTION
1	GND	Ground Reference
2	IO	I/O Driver for 1-Wire Line
3	V_{CC}	Power-Supply Input
4	SLPZ	Active-Low Control Input. Activates the low-power sleep mode and issues a device reset of the SHA-coprocessor and the 1-Wire master (equivalent to the 1-Wire Master Reset command).
5	SDA	I^2C Serial-Data Input/Output. Must be connected to V_{CC} through a pullup resistor.
6	SCL	I^2C Serial-Clock Input. Must be connected to V_{CC} through a pullup resistor.

Detailed Description

The DS2465 is a SHA-256 coprocessor with built-in 1-Wire master and two pages of user memory.

Refer to the full data sheet for this information.

The self-timed 1-Wire master function supports advanced 1-Wire waveform features including standard and overdrive speeds, active pullup, and strong pullup for power delivery. The active pullup affects rising edges on the 1-Wire side. The strong pullup function uses the same pullup transistor as the active pullup, but with a different control algorithm. Once supplied with command and data, the input/output controller of the DS2465 performs time-critical 1-Wire communication functions such as reset/presence-detect cycle, read-byte, write-byte, single-bit R/W, and triplet for ROM Search, without requiring interaction with the host processor. The host obtains feedback (completion of a 1-Wire function, presence pulse, 1-Wire short, and search direction taken) through the 1-Wire Master Status register and data through the 1-Wire Read Data register. All registers, the user memory and a scratchpad are located in a linear address space for direct access. The DS2465 communicates with a host processor through its I^2C bus interface in standard mode or in fast mode. See Figure 1 for a block diagram.

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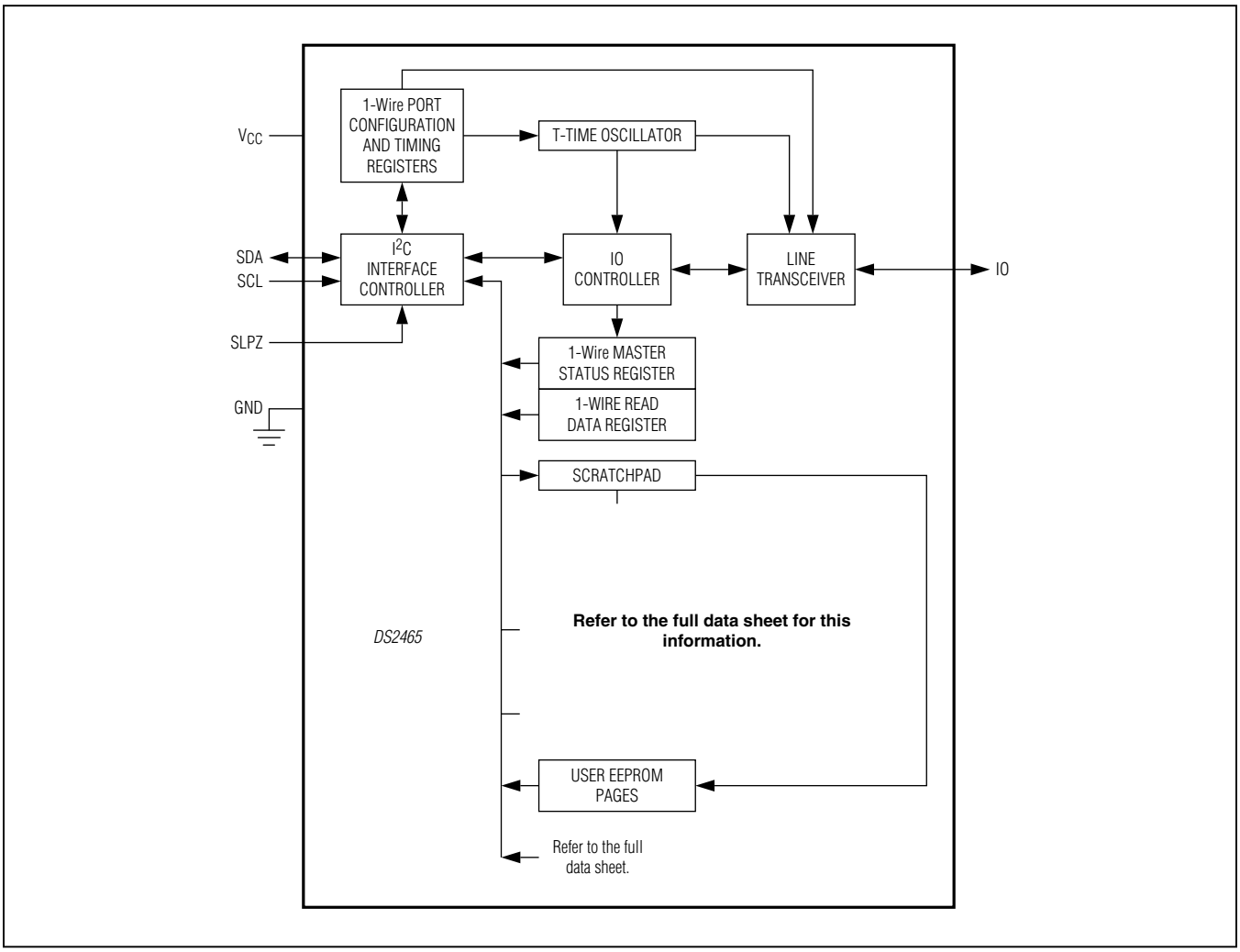


Figure 1. Block Diagram

Memory

Figure 2 shows the memory organization of the DS2465. The memory begins at address 00h with the input scratchpad. The register section follows at address 60h. Addresses 00 to 6F

are implemented as volatile SRAM. The 1-Wire port configuration settings have default values that are loaded automatically during power-on. The address range 70h and higher is non-volatile. It contains factory-programmed device identification data, a personality byte, and the user memory pages.

Refer to the full data sheet for this information.

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ADDRESS RANGE	TYPE	ACCESS	DESCRIPTION
00h to 4Bh	SRAM	R/W	Input scratchpad
4Ch to 5Fh	—	—	(Reserved)
60h	—	W	Command register
61h	SRAM	R	1-Wire Master Status register
62h	SRAM	R	1-Wire Read Data register
Refer to the full data sheet.			
66h	—	—	(Reserved)
67h	SRAM	R/W	1-Wire Master Configuration register
68h	SRAM	R/W	1-Wire Port Configuration t_{RSTL}
69h	SRAM	R/W	1-Wire Port Configuration t_{MSP}
6Ah	SRAM	R/W	1-Wire Port Configuration t_{W0L}
6Bh	SRAM	R/W	1-Wire Port Configuration t_{REC0}
6Ch	SRAM	R/W	1-Wire Port Configuration R_{WPU}
6Dh	SRAM	R/W	1-Wire Port Configuration Overdrive t_{W1L}
6Eh to 6Fh	—	—	(Reserved)
70h	ROM	R	Factory byte
Refer to the full data sheet.			
73h	ROM	R	Personality byte
74h to 7Fh	—	—	(Reserved)
80h to 9Fh	EEPROM	(R)/(W)	User memory page 0
A0h to BFh	EEPROM	(R)/(W)	User memory page 1
C0h to FFh	—	—	(Reserved)

Figure 2. Memory Map

Device Registers

The registers of the DS2465 fall into three categories: write-only, read-only and read/write. Write-only applies to the command register. Status registers, the 1-Wire read data register , are read-only. The configuration registers can be read and written; they also have defined power-on default settings. The factory byte, Manufacturer ID, and Personality byte are read-only.

Command Register (60h)

To execute a 1-Wire function, the DS2465 needs to receive a command from the I²C host. Commands are written one at a time to the Command register. Most commands consist of a command code and a parameter byte. The command code indicates the type of instruction and the position of the read pointer for the next I²C read-access. See section *Function Commands* for details.

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1-Wire Master Status Register (61h)

The 1-Wire Master Status register is the general means for the DS2465 to report bit-type data from the 1-Wire side, 1-Wire busy status, and its own reset status to the host processor (Table 1). All 1-Wire communication commands and the 1-Wire Master Reset command position the read pointer at the Status register for the host processor to read with minimal protocol overhead. Status information is updated during the execution of certain commands only. Details are given in the description of the various status bits that follow.

Table 1. 1-Wire Master Status Bit Assignment

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR	TSB	SBR	RST	LL	SD	PPD	1WB

Bit 7: Branch Direction Taken (DIR). Whenever a 1-Wire Triplet command is executed, this bit reports to the host processor the search direction that was chosen by the third bit of the triplet. The power-on default of DIR is 0. This bit is updated only with a 1-Wire Triplet command and has no function with other commands. For additional information, see the description of the 1-Wire Triplet command and Application Note 187: *1-Wire Search Algorithm*.

Bit 6: Triplet Second Bit (TSB). The TSB bit reports the logic state of the active 1-Wire line sampled at t_{MSR} of the second bit of a 1-Wire Triplet command. The power-on default of TSB is 0. This bit is updated only with a 1-Wire Triplet command and has no function with other commands.

Bit 5: Single Bit Result (SBR). The SBR bit reports the logic state of the active 1-Wire line sampled at t_{MSR} of a 1-Wire Single Bit command or the first bit of a 1-Wire Triplet command. The power-on default of SBR is 0. If the 1-Wire Single Bit command sends a 0 bit, SBR should be 0. With a 1-Wire Triplet command, SBR could be 0 as well as 1, depending on the response of the 1-Wire devices connected. The same result applies to a 1-Wire Single Bit command that sends a 1 bit.

Bit 4: Device Reset (RST). If the RST bit is 1, the DS2465 has performed an internal reset cycle, either caused by a power-on reset, a low pulse at SLPZ, or from executing the Device Reset command. The RST bit is cleared automatically when the 1-Wire Master Configuration register is updated by the host processor.

Bit 3: Logic Level (LL). The LL bit reports the logic state of the active 1-Wire line without initiating any 1-Wire communication. The 1-Wire line is sampled for this purpose every time the 1-Wire Master Status register is read. The sampling and updating of the LL bit takes place when the host processor has addressed the DS2465 in read mode (during the acknowledge cycle), provided that the read pointer is positioned at the 1-Wire Master Status register.

Bit 2: Short Detected (SD). The SD bit is updated with every 1-Wire Reset command. If the DS2465 detects a logic 0 on the 1-Wire line at t_{SI} during the presence-detect cycle, the SD bit is set to 1. This bit returns to its default 0 with a subsequent 1-Wire Reset command provided that the short has been removed.

Bit 1: Presence-Pulse Detect (PPD). The PPD bit is updated with every 1-Wire Reset command. If the DS2465 detects a presence pulse from a 1-Wire device at t_{MSP} during the presence-detect cycle, the PPD bit is set to 1. This bit returns to its default 0 if there is no presence pulse or if the 1-Wire line is shorted during a subsequent 1-Wire Reset command.

Bit 0: 1-Wire Busy (1WB). The 1WB bit reports to the host processor whether the 1-Wire line is busy. During 1-Wire communication 1WB is 1; once the command is completed, 1WB returns to its default 0. Details on when 1WB changes state and for how long it remains at 1 are found in the *Function Commands* section.

1-Wire Read Data Register (62h)

When the DS2465 completes a 1-Wire Read Byte command, it puts the data read from the 1-Wire slave into the 1-Wire Read Data register. While the command is being executed, the I^2C host checks the 1WB bit in the 1-Wire Master Status register. When the 1-Wire line is no longer busy, the I^2C host performs a dummy write to address 62h and then accesses the DS2465 in read mode to read the data byte.

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1-Wire Master Configuration Register (67h)

The DS2465 supports four 1-Wire features that are enabled or selected through the 1-Wire Master Configuration register (Table 3). These features are: Active Pullup (APU), 1-Wire Power-Down (PDN), Strong Pullup (SPU), 1-Wire Speed (1WS). APU, SPU and 1WS can be selected in any combination. While APU and 1WS maintain their state, SPU returns to its inactive state as soon as the strong pullup has ended.

After a device reset (power-up cycle, a low pulse at SLPZ, or initiated by the 1-Wire Master Reset command), the 1-Wire Master Configuration register reads 00h. When writing to the register, the new data is accepted only if the upper nibble (bits 7 to 4) is the one's complement of the lower nibble (bits 3 to 0). When read, the upper nibble is always 0h.

Table 3. 1-Wire Master Configuration Bit Assignment

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{1WS}$	$\overline{SPU}$	$\overline{PDN}$	$\overline{APU}$	1WS	SPU	PDN	APU

Bit 3: 1-Wire Speed (1WS). The 1WS bit determines the timing of any 1-Wire communication generated by the DS2465. Most 1-Wire slave devices support standard speed (1WS = 0). Many 1-Wire devices can also communicate at a higher data rate, called overdrive speed. Some 1-Wire devices, including the DeepCover SHA-256 family of slave devices, only support overdrive and 1WS should always be programmed high for these devices. To change from standard to overdrive speed, a 1-Wire device needs to receive an Overdrive-Skip ROM or Overdrive-Match ROM command, as explained in the 1-Wire device data sheets. The change in speed occurs immediately after the 1-Wire device has received the speed-changing command code. The DS2465 must take part in this speed change to stay synchronized. This is accomplished by writing to the 1-Wire Master Configuration register with the 1WS bit as 1 immediately after the 1-Wire Byte command that changes the speed of a 1-Wire device. Writing to the 1-Wire Master Configuration register with the 1WS bit as 0, followed by a 1-Wire Reset command, changes the DS2465 and any 1-Wire devices on the active 1-Wire line back to standard speed.

Bit 2: Strong Pullup (SPU). The SPU bit is used to activate the strong pullup function prior to a 1-Wire Write Byte, 1-Wire Read Byte, or 1-Wire Single Bit command. Strong pullup is commonly used with 1-Wire EEPROM devices when copying scratchpad data to the main memory or when performing a SHA computation. The respective device data sheets specify the location in the communications protocol after which the strong pullup should be applied. The SPU bit must be set immediately prior to issuing the command that puts the 1-Wire device into the state where it needs the extra power. The strong pullup uses the same internal pullup transistor as the active pullup feature. See the R_{APU} parameter in the *Electrical Characteristics* to determine whether the voltage drop is low enough to maintain the required 1-Wire voltage at a given load current and supply voltage.

If SPU is 1, the DS2465 treats the rising edge of the time slot in which the strong pullup starts as if the active pullup was activated. However, in contrast to the active pullup, the strong pullup, i.e., the internal pullup transistor, remains conducting, as shown in Figure 3, until one of four events occurs: the DS2465 receives a command that generates 1-Wire communication (the typical case); the SPU bit in the 1-Wire Master Configuration register is written to 0; the PDN bit in the 1-Wire Master Configuration register is written to 1; or the DS2465 receives the 1-Wire Master Reset command. When the strong pullup ends, the SPU bit is automatically reset to 0. Using the strong pullup feature does not change the state of the APU bit in the 1-Wire Master Configuration register.

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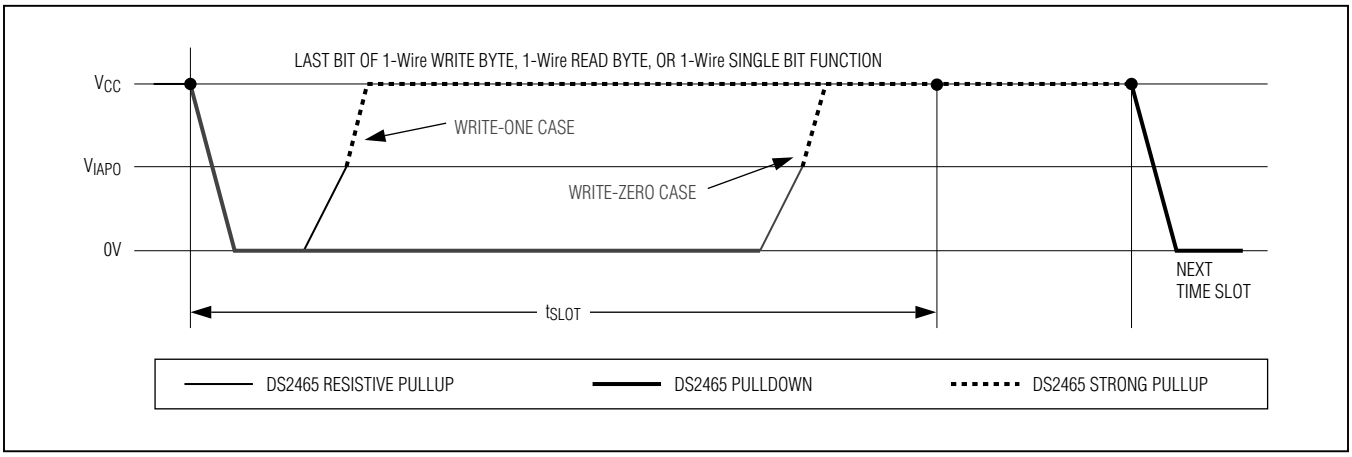


Figure 3. Low-Impedance Pullup Timing

Bit 1: 1-Wire Power-Down (PDN). The PDN bit is used to remove power from the 1-Wire port, e.g., to force a 1-Wire slave to perform a power-on reset. PDN interacts with the sleep mode, which is controlled by the SLPZ pin (Table 4). The default state of PDN is 0, enabling normal operation. When PDN is changed to 1, no 1-Wire communication is possible. To end the 1-Wire power-down state, the PDN bit needs to be changed to 0. To exit the DS2465 from sleep mode, change the SLPZ pin state from 0 to 1. This forces the DS2465 to perform a power-on reset and clears PDN to 0 for normal operation.

Table 4. Interaction of PDN and SLPZ

	SLPZ PIN IS AT LOGIC 0	SLPZ PIN IS AT LOGIC 1
PDN is 0	• R_{WPU} is disconnected; IO is at 0V, causing the slaves to lose power. • The DS2465 is powered down (sleep mode).	• R_{WPU} is connected; IO is at V_{CC}, keeping the slaves powered. • The DS2465 is powered up (normal operation).
PDN is 1		• R_{WPU} is disconnected; IO is at 0V, causing the slaves to lose power. • The DS2465 is powered up.

Bit 0: Active Pullup (APU). The APU bit controls whether an active pullup (low impedance transistor) or a passive pullup (R_{WPU} resistor) is used to drive a 1-Wire line from low to high. When APU = 0, active pullup is disabled (resistor mode). Enabling active pullup is generally recommended for best 1-Wire performance. The active pullup does not apply to the rising edge of a recovery after a short on the 1-Wire line. If enabled, a fixed-duration active pullup (nominally 2.5µs standard speed, 0.5µs overdrive speed) also applies in a reset/presence detect cycle on the rising edges after t_{RSTL} and after t_{PDL}.

The circuit that controls rising edges (Figure 4) operates as follows: At t_1, the pulldown (from DS2465 or 1-Wire slave) ends. From this point on the 1-Wire line is pulled high through R_{WPU} internal to the DS2465. V_{CC} and the capacitive load of the 1-Wire line determine the slope. In case that active pullup is disabled (APU = 0), the resistive pullup continues, as represented by the solid line. With active pullup enabled (APU = 1), and when at t_2 the voltage has reached the V_{IAPO} threshold, the DS2465 activates a low-impedance pullup transistor, as represented by the dashed line. The active pullup remains active until the end of the time slot (t_3), after which the resistive pullup continues. The shortest duration of the active pullup is t_{REC0} in a write-zero time slot and the longest duration is $t_{W0L} + t_{REC0} - t_{W1L}$ in a write-one time slot. In a read data time slot, the active pullup duration is slave dependent. See the strong pullup (SPU) section for a way to keep the pullup transistor conducting beyond t_3.

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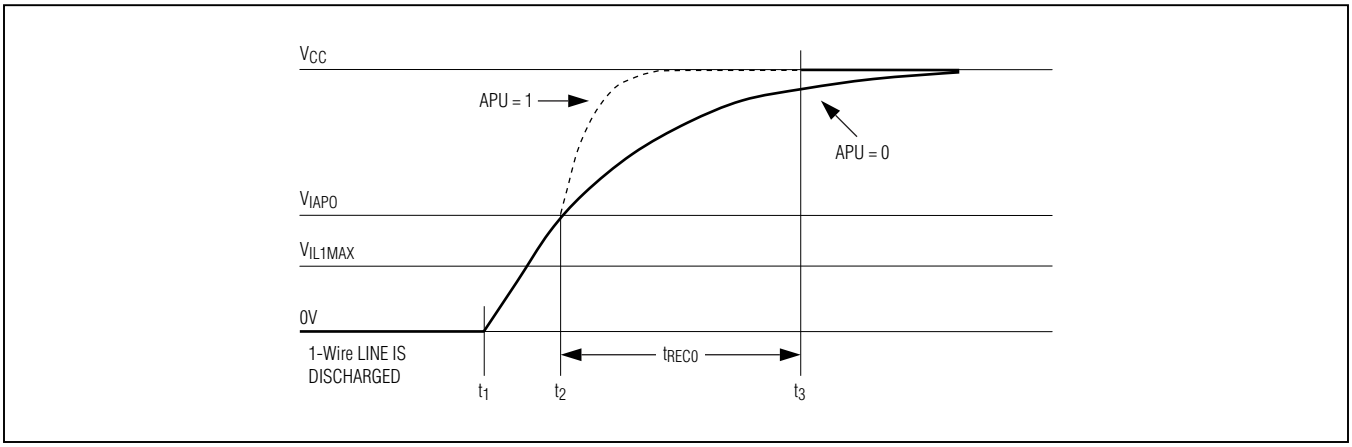


Figure 4. Rising Edge Pullup During a Time Slot

1-Wire Port Configurations

The DS2465 allows adapting several timing parameters and the pullup resistor to the application's needs. Each of these parameters has its own 1-Wire Port Configuration register, located in the address range from 68h to 6Dh (Table 5). For t_{RSTL}, t_{MSP} and t_{W0L} the values for standard and overdrive speed can be adjusted independently. The lower nibble applies to standard speed, the upper nibble to overdrive speed. The t_{REC0} and R_{WPU} settings apply at both 1-Wire speeds. The parameter t_{W1L} can be adjusted for overdrive speed only; the standard speed value us fixed. For t_{REC0}, R_{WPU} and t_{W1L} the upper nibble has no function. See Table 6 for the conversion between binary code and parameter value.

After a device reset (power-up cycle, a low pulse at SLPZ, or initiated by the 1-Wire Master Reset command), the 1-Wire Port Configuration registers are initialized to their default values. To change a port configuration, access the respective register in I^2C write mode and provide the new code as data byte. Starting at address 68h all port configurations can be adjusted in a single write access. The new setting applies on the rising SCL edge of the data byte acknowledge bit, provided that the 1-Wire line is not busy (1WB = 0). The upper 4 bits of the registers at 6Bh to 6Dh are not used. They can be written, byte their value has no effect on the device operation.

Table 5. 1-Wire Port Configuration Address Details

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
68h	t_{RSTL} Overdrive Speed (OD)				t_{RSTL} Standard Speed (STD)			
69h	t_{MSP} Overdrive Speed (OD)				t_{MSP} Standard Speed (STD)			
6Ah	t_{W0L} Overdrive Speed (OD)				t_{W0L} Standard Speed (STD)			
6Bh	(not used, default 0000b)				t_{REC0} (speed independent)			
6Ch	(not used, default 0000b)				R_{WPU} (speed independent)			
6Dh	(not used, default 0000b)				t_{W1L} Overdrive Speed (OD)			

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Table 6. Conversion between parameter value code and typical parameter value

PARAMETER VALUE CODE	t_{RSTL} VALUE IN µs		t_{MSP} VALUE IN µs		t_{W0L} VALUE IN µs		t_{REC0} VALUE IN µs	R_{WPU} VALUE IN Ω	t_{W1L} VALUE IN µs
	STD	OD	STD	OD	STD	OD	STD, OD	STD, OD	OD
0000b	440	44	58	5.5	52	5.0	2.5	500	do not use
0001b	460	46	58	5.5	54	5.5	2.5	500	0.25
0010b	480	48	60	6.0	56	6.0	2.5	500	0.50
0011b	500	50	62	6.5	58	6.5	2.5	500	0.75
0100b	520	52	64	7.0	60	7.0	2.5	500	**1.00**
0101b	540	54	66	7.5	62	7.5	2.5	500	1.25
0110b	**560**	**56**	**68**	**8.0**	**64**	**8.0**	**5.0**	**1000**	1.50
0111b	580	58	70	8.5	66	8.5	7.5	1000	1.75
1000b	600	60	72	9.0	68	9.0	10.0	1000	2.00
1001b	620	62	74	9.5	70	9.5	12.5	1000	2.25
1010b	640	64	76	10.0	70	10	15.0	1000	2.50
1011b	660	66	76	10.5	70	10	17.5	1000	2.75
1100b	680	68	76	11.0	70	10	20.0	1000	3.00
1101b	700	70	76	11.0	70	10	22.5	1000	3.25
1110b	720	72	76	11.0	70	10	25.0	1000	3.50
1111b	740	74	76	11.0	70	10	25.0	1000	3.75

Note: *The power-on default values are* ***bold****.*

Factory Byte (70h)

This byte reads 55h.

Refer to the full data sheet for this information.

Personality Byte (73h)

This byte reads 00h.

Function Commands

The DS2465 understands

function commands. The feedback path to the host is controlled by a read pointer, which is set automatically by each function command for the host to efficiently access relevant information. The host processor sends these commands and applicable parameters as strings of one or two bytes using the I²C interface. The I²C protocol requires that each byte be acknowledged by the receiving party to confirm acceptance or not be acknowledged to indicate an error condition (invalid code or parameter) or to end the communication. See the *I²C Interface* section for details of the I²C protocol including acknowledge. The function commands are as follows:

Refer to the full data sheet for this information.

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Refer to the full data sheet for this information.

The subsequent pages describe the function commands in a concise, table-like fashion.

Copy Scratchpad	
Command Code	5Ah
Parameter Byte	Data destination, segment number (Table 7)
Usage	Transferring scratchpad data to user EEPROM pages;
Other Notes	If the target memory is write-protected, this command cannot not complete successfully. Data is taken from the scratchpad location that corresponds to the segment number. Example: segment 0 corresponds to SP+0 to SP+3, addresses 00h to 03h.
Command Restrictions	The data must first be written to the scratchpad. The target memory must not be write-protected (locked).
Error Conditions (Error Response)	If the target memory is write protected, the memory write cycles do not take place. In that case the device is not busy and acknowledges its I^2C address immediately when accessed.
MAC Notes	**Refer to the full data sheet.**
I^2C Busy Duration	For 1 x t_{PROG} or 8 x t_{PROG} depending on the parameter byte, counted from the rising SCL edge of the parameter byte acknowledge bit.
Command Duration	I^2C busy duration + 1.09µs
1-Wire Activity	None
Read Pointer Position	1-Wire Master Status register
Master Status Bits Affected	None
Master Configurations Affected	None
1-Wire Port Configurations Affected	None

Table 7. Parameter Byte Bitmap

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
S/U	X	TT		F/S	SEG#		

X = Don't care

Refer to the full data sheet for this information.

Bits 5:4: Target (TT). These bits specify the user memory page number (S/U = 1) to which the scratchpad data is to be copied.

For S/U = 1, the assignments are:

00 User page 0

01 User page 1

10 (reserved)

11 (reserved)

Bit 3: Full or segment copy (F/S). This bit is relevant only is S/U = 1. It specifies whether the entire page is programmed or only the segment selected by SEG#. If F/S = 0, the entire page is programmed. If F/S = 1, only the selected segment is programmed. If one block of a targeted page is write protected then the F/S bit is forced to 1.

Bits 2:0: Segment Number (SEG#). These bits are relevant only if (S/U = 1) and (F/S = 1). They specify the segment of the selected user memory page to be programmed with scratchpad data. All codes are valid. The code 000b refers to the first four bytes of the page, etc.

1-Wire Master Reset	
Command Code	F0h
Parameter Byte	N/A
Usage	Device initialization after power-up; re-initialization (reset) as desired.
Other Notes	Performs a global reset of device state machine logic. Terminates any ongoing 1-Wire communication.
Command Restrictions	The command must be followed by a 1-Wire Reset Pulse command.
Error Conditions (Error Response)	None
MAC Notes	N/A
I^2C Busy Duration	None
Command Duration	Maximum 1.635µs. Counted from rising SCL edge of the command code acknowledge bit.
1-Wire Activity	Ends maximum 1.09µs after the rising SCL edge of the command code acknowledge bit.
Read Pointer Position	(N/A)
Master Status Bits Affected	RST set to 1; 1WB, PPD, SD, SBR, TSB, DIR set to 0.
Master Configurations Affected	1WS, APU, PDN, SPU set to 0.
1-Wire Port Configurations Affected	t_{RSTL}, t_{MSP}, t_{W0L}, t_{W1L}, t_{REC0}, and R_{WPU} are reset to their default values.

1-Wire Reset Pulse	
Command Code	B4h
Parameter Byte	N/A
Usage	To initiate or end any 1-Wire communication sequence. To finish a 1-Wire Master Reset command.
Other Notes	Generates a 1-Wire reset/presence-detect cycle (Figure 5) at the 1-Wire line. The state of the 1-Wire line is sampled at t_{SI} and t_{MSP} and the result is reported to the host processor through the 1-Wire Master Status Register, bits PPD and SD.
Command Restrictions	1-Wire activity must have ended before the DS2465 can process this command.
Error Conditions (Error Response)	Command code is not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
MAC Notes	N/A
I^2C Busy Duration	None
Command Duration	2 x t_{RSTL} + maximum 1.09µs, counted from the rising SCL edge of the command code acknowledge bit.
1-Wire Activity	Begins maximum 1.09µs after the rising SCL edge of the command code acknowledge bit.
Read Pointer Position	1-Wire Master Status register (for busy polling).
Master Status Bits Affected	1WB (set to 1 for 2 x t_{RSTL}), PPD is updated at t_{RSTL} + t_{MSP}, SD is updated at t_{RSTL} + t_{SI}.
Master Configurations Affected	1WS and APU apply.
1-Wire Port Configurations Affected	t_{RSTL}, t_{MSP}, and R_{WPU} current values apply.

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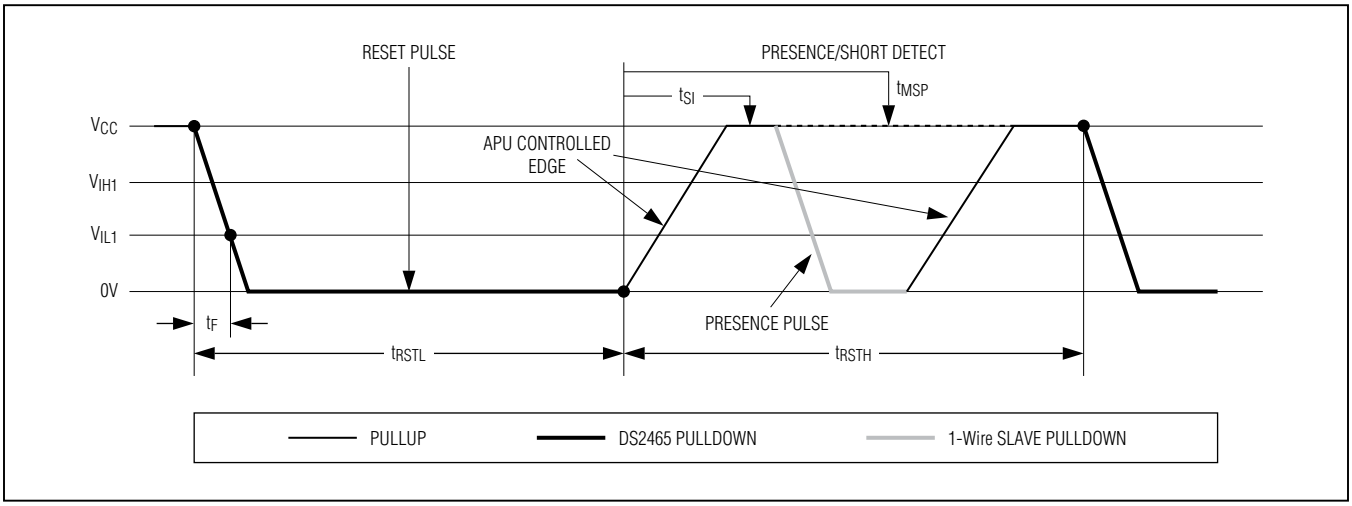


Figure 5. 1-Wire Reset/Presence-Detect Cycle

1-Wire Single Bit	
Command Code	87h
Parameter Byte	Type of time slot (Table 21)
Usage	To perform single-bit writes or reads at the 1-Wire line when single bit communication is necessary (the exception).
Other Notes	Generates a single 1-Wire time slot as specified by the parameter byte at the 1-Wire line; reads the logic level at the 1-Wire line at t_{MSR} and updates SBR accordingly.
Command Restrictions	1-Wire activity must have ended before the DS2465 can process this command.
Error Conditions (Error Response)	Command code is not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
MAC Notes	N/A
I^2C Busy Duration	None
Command Duration	t_{SLOT} + maximum 1.09µs, counted from the rising SCL edge of the parameter byte acknowledge bit.
1-Wire Activity	Begins maximum 1.09µs after the rising SCL edge of the parameter byte acknowledge bit.
Read Pointer Position	1-Wire Master Status register (for busy polling and data reading).
Master Status Bits Affected	1WB (set to 1 for t_{SLOT}), SBR is updated at t_{MSR}, DIR (may change its state).
Master Configurations Affected	1WS, APU, SPU apply.
1-Wire Port Configurations Affected	t_{W0L}, t_{W1L}, t_{REC0}, and R_{WPU} current values apply.

Table 21. Parameter Byte Bitmap

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
V	X	X	X	X	X	X	X

X = Don't care

Bit 7: Bit value (V). This bit specifies the type of time slot to be generated. If V = 0, a write-zero time slot (Figure 6) is generated. If V = 1, a write-one time slot (Figure 7) is generated, which also functions as a read-data time slot.

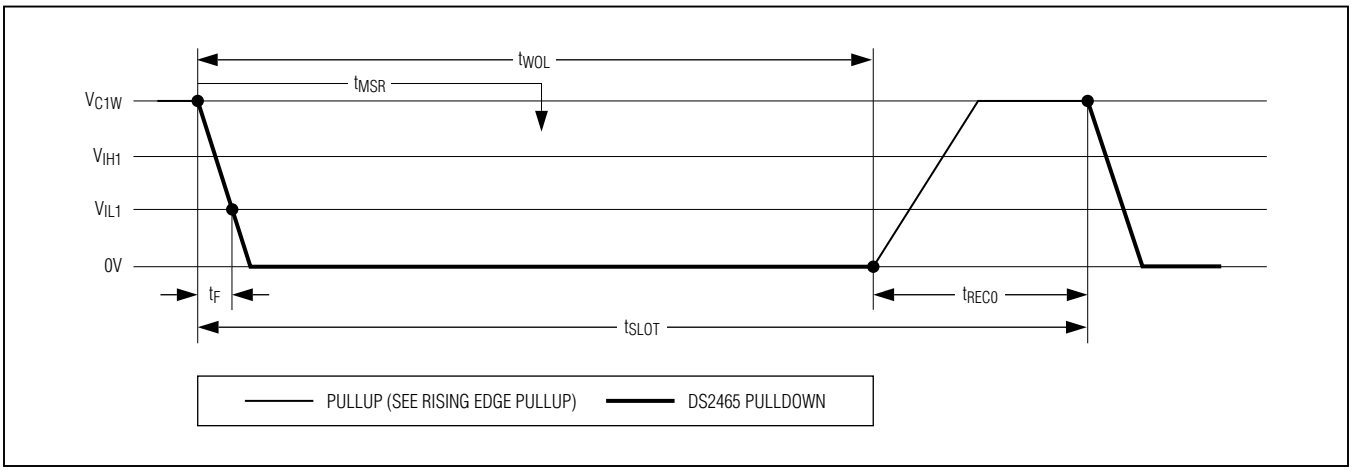
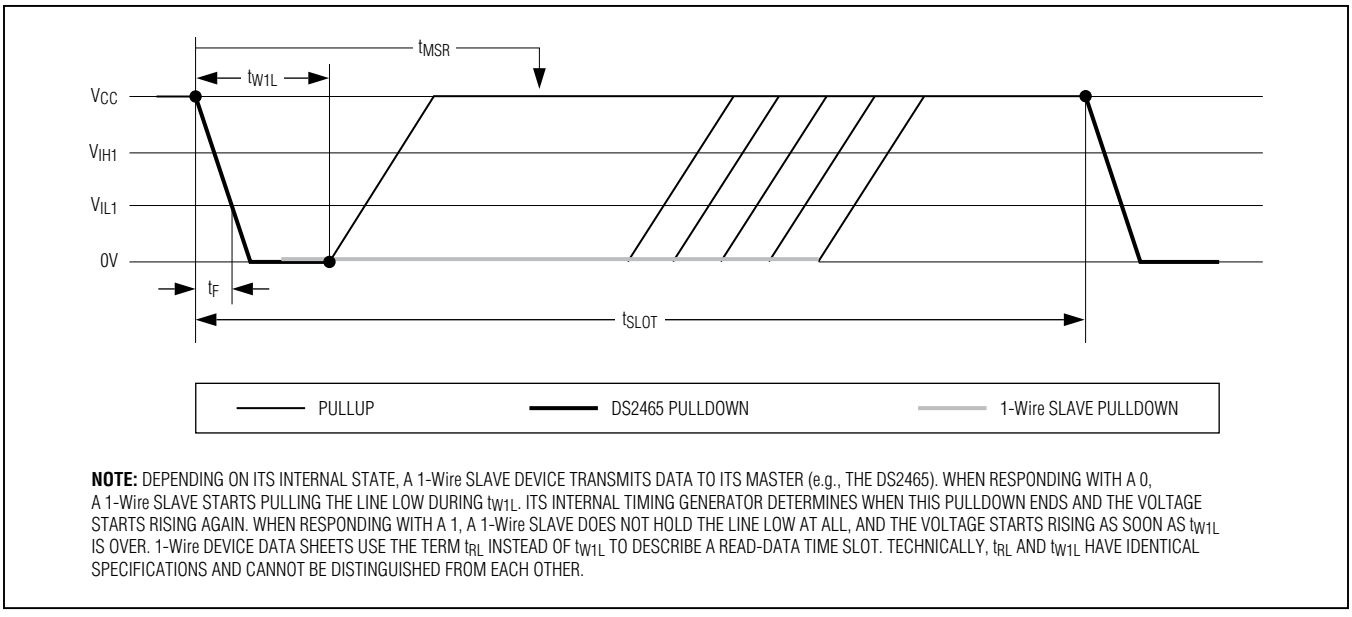


Figure 6. Write-Zero Time Slot



NOTE: DEPENDING ON ITS INTERNAL STATE, A 1-Wire SLAVE DEVICE TRANSMITS DATA TO ITS MASTER (e.g., THE DS2465). WHEN RESPONDING WITH A 0, A 1-Wire SLAVE STARTS PULLING THE LINE LOW DURING t_{W1L}. ITS INTERNAL TIMING GENERATOR DETERMINES WHEN THIS PULLDOWN ENDS AND THE VOLTAGE STARTS RISING AGAIN. WHEN RESPONDING WITH A 1, A 1-Wire SLAVE DOES NOT HOLD THE LINE LOW AT ALL, AND THE VOLTAGE STARTS RISING AS SOON AS t_{W1L} IS OVER. 1-Wire DEVICE DATA SHEETS USE THE TERM t_{RL} INSTEAD OF t_{W1L} TO DESCRIBE A READ-DATA TIME SLOT. TECHNICALLY, t_{RL} AND t_{W1L} HAVE IDENTICAL SPECIFICATIONS AND CANNOT BE DISTINGUISHED FROM EACH OTHER.

Figure 7. Write-One and Read-Data Time Slot

1-Wire Write Byte	
Command Code	A5h
Parameter Byte	Data byte (Table 22)
Usage	To write commands or data to the 1-Wire line. Equivalent to executing eight 1-Wire Single Bit commands, but faster due to less I^2C traffic.
Other Notes	Writes a single data byte to the 1-Wire line.
Command Restrictions	1-Wire activity must have ended before the DS2465 can process this command.
Error Conditions (Error Response)	Command code is not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
MAC Notes	N/A
I^2C Busy Duration	None
Command Duration	8 x t_{SLOT} + maximum 1.09µs, counted from the rising SCL edge of the parameter byte acknowledge bit.
1-Wire Activity	Begins maximum 1.09µs after the rising SCL edge of the parameter byte acknowledge bit. **Note:** The bit order on the I^2C bus and the 1-Wire line is different (1-Wire: LSB first; I^2C: MSB first). Therefore, 1-Wire activity cannot begin before the DS2465 has received the full data byte.
Read Pointer Position	1-Wire Master Status register (for busy polling).
Master Status Bits Affected	1WB (set to 1 for 8 x t_{SLOT}).
Master Configurations Affected	1WS, APU, SPU apply.
1-Wire Port Configurations Affected	t_{W0L}, t_{W1L}, t_{REC0}, and R_{WPU} current values apply.

Table 22. Parameter Byte Bitmap

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DATA							

Bit 7:0: Data Byte (DATA). These bits specify the data to be written to the 1-Wire line. The time slot for bit 0 is generated first.

1-Wire Read Byte	
Command Code	96h
Parameter Byte	N/A
Usage	To read data from the 1-Wire line. Equivalent to executing eight 1-Wire Single Bit commands with V = 1 (write-one time slot), but faster due to less I^2C traffic.
Other Notes	Generates eight read-data time slots on the 1-Wire line and stores result in the 1-Wire Read Data Register.
Command Restrictions	1-Wire activity must have ended before the DS2465 can process this command.
Error Conditions (Error Response)	Command code is not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
MAC Notes	N/A
I^2C Busy Duration	None
Command Duration	8 x t_{SLOT} + maximum 1.09µs, counted from the rising SCL edge of the command code acknowledge bit.
1-Wire Activity	Begins maximum 1.09µs after the rising SCL edge of the command code acknowledge bit.
Read Pointer Position	1-Wire Master Status register (for busy polling). **Note:** To read the data byte received from the 1-Wire line, issue a dummy write to memory address of the 1-Wire Read Data register. Then access the DS2465 in read mode.
Master Status Bits Affected	1WB (set to 1 for 8 x t_{SLOT}).
Master Configurations Affected	1WS, APU, SPU apply.
1-Wire Port Configurations Affected	t_{REC0}, t_{W1L}, and R_{WPU} current values apply.

1-Wire Triplet	
Command Code	78h
Parameter Byte	Branch Direction (Table 23)
Usage	To perform a 1-Wire Search ROM sequence; a full sequence requires this command to be executed 64 times to identify and address one device.
Other Notes	Generates three time slots: two read time slots and one write time slot at the 1-Wire line. The type of write time slot depends on the result of the read time slots and the direction byte. • If the read time slots are 0 and 1, they are followed by a write-zero time slot. • If the read time slots are 1 and 0, they are followed by a write-one time slot. • If the read time slots are both 1 (error case), the subsequent write time slot is a write-one. • If the read time slots are both 0, the parameter byte determines the type of the subsequent write time slot.
Command Restrictions	1-Wire activity must have ended before the DS2465 can process this command.
Error Conditions (Error Response)	Command code is not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
MAC Notes	N/A
I^2C Busy Duration	None
Command Duration	3 x t_{SLOT} + maximum 1.09µs, counted from the rising SCL edge of the parameter byte acknowledge bit.
1-Wire Activity	Begins maximum 1.09µs after the rising SCL edge of the parameter byte acknowledge bit.
Read Pointer Position	1-Wire Master Status register (for busy polling and data reading).
Master Status Bits Affected	1WB (set to 1 for 3 x t_{SLOT}), SBR is updated at the first t_{MSR}, TSB and DIR are updated at the second t_{MSR} (i.e., at t_{SLOT} + t_{MSR}).
Master Configurations Affected	1WS, APU apply.
1-Wire Port Configurations Affected	t_{W0L}, t_{W1L}, t_{REC0}, and R_{WPU} current values apply.

Table 23. Parameter Byte Bitmap

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
V	X	X	X	X	X	X	X

X = Don't care

Bit 7: Bit value (V). This bit specifies the branch direction to be taken if both, the first and the second read time slot read a 0. If V = 0, a write-zero time slot is generated. If V = 1, a write-one time slot is generated.

1-Wire Receive Block	
Command Code	E1h
Parameter Byte	Block size (Table 25)
Usage	To read memory data from a secure 1-Wire memory device.
Other Notes	Reads 1 to 63 bytes from the 1-Wire line and makes them accessible from the scratchpad.
Command Restrictions	1-Wire activity must have ended before this command can be processed.
Error Conditions (Error Response)	Command code is not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
MAC Notes	None
I^2C Busy Duration	None
Command Duration	(1 to 63) x 8 x t_{SLOT} + maximum 1.09µs, counted from rising SCL edge of the parameter byte acknowledge bit.
1-Wire Activity	Begins maximum 1.09µs after the rising SCL edge of the parameter byte acknowledge bit.
Read Pointer Position	1-Wire Master Status register (for busy polling).
Master Status Bits Affected	1WB (set to 1 for 8 x BS x t_{SLOT}).
Master Configurations Affected	1WS, APU apply
1-Wire Port Configurations Affected	t_{REC0}, t_{W1L}, and R_{WPU} current values apply.

Table 25. Parameter Byte Bitmap

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	BS					

X = Don't care

Bits 5:0: Block Size (BS). These bits specify the number of bytes to be received and written to the Input Scratchpad starting at location 00h. If BS = 000000b, one byte is received.

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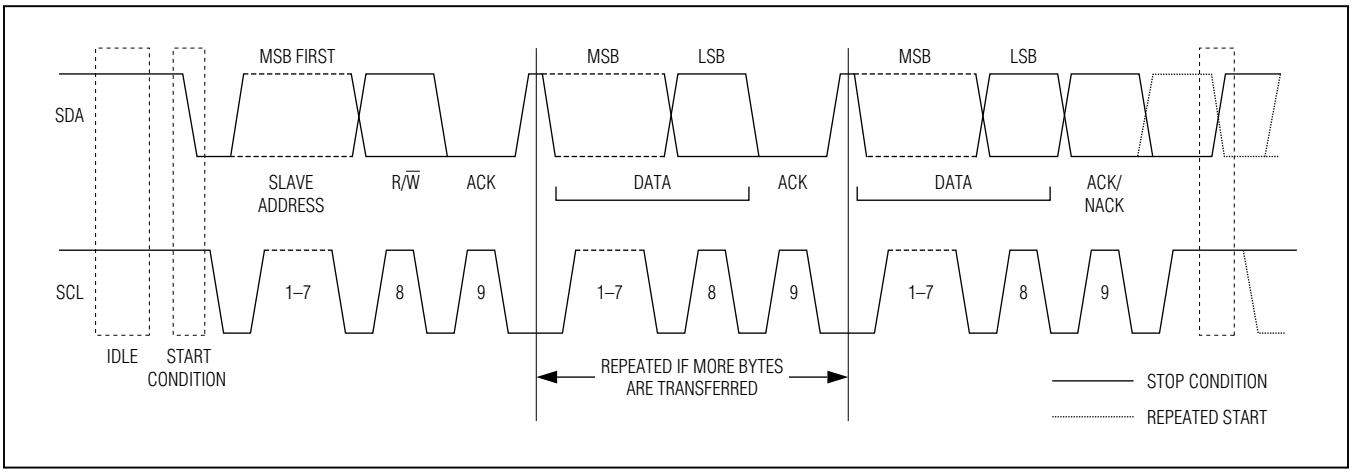


Figure 8. I²C Protocol Overview

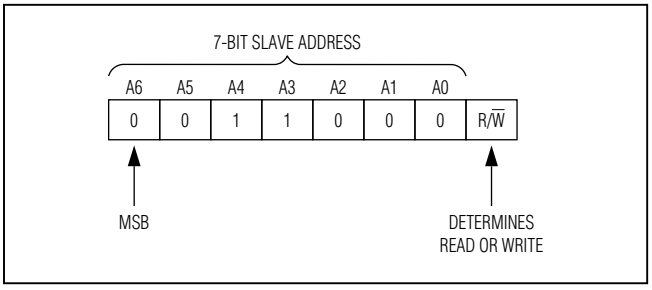


Figure 9. DS2465 Slave Address

I²C Interface

General Characteristics

The I²C bus uses a data line (SDA) plus a clock signal (SCL) for communication. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage through a pullup resistor. When there is no communication, both lines are high. The output stages of devices connected to the bus must have an open drain or open collector to perform the wired-AND function. Data on the I²C bus can be transferred at rates of up to 100kbps in standard mode and up to 400kbps in fast mode. The DS2465 works in both modes.

A device that sends data on the bus is defined as a transmitter, and a device receiving data is defined as a receiver. The device that controls the communication is called a master. The devices that are controlled by the master are slaves. To be individually accessed, each device must have a slave address that does not conflict with other devices on the bus.

Data transfers can be initiated only when the bus is not busy. The master generates the serial clock (SCL), controls the bus access, generates the START and STOP conditions, and determines the number of data bytes transferred between START and STOP (Figure 8). Data is transferred in bytes with the most significant bit being transmitted first. After each byte follows an acknowledge bit to allow synchronization between master and slave.

Slave Address

The slave address to which the DS2465 responds is shown in Figure 9. The slave address is part of the slave address/control byte. The last bit of the slave address/control byte (R/$\overline{W}$) defines the data direction. When set to 0, subsequent data flows from master to slave (write access); when set to 1, data flows from slave to master (read access).

I²C Definitions

The following terminology is commonly used to describe I²C data transfers. The timing references are defined in Figure 10.

Bus Idle or Not Busy: Both SDA and SCL are inactive and in their logic-high states.

START Condition: To initiate communication with a slave, the master must generate a START condition. A START condition is defined as a change in state of SDA from high to low while SCL remains high.

STOP Condition: To end communication with a slave, the master must generate a STOP condition. A STOP condition is defined as a change in state of SDA from low to high while SCL remains high.

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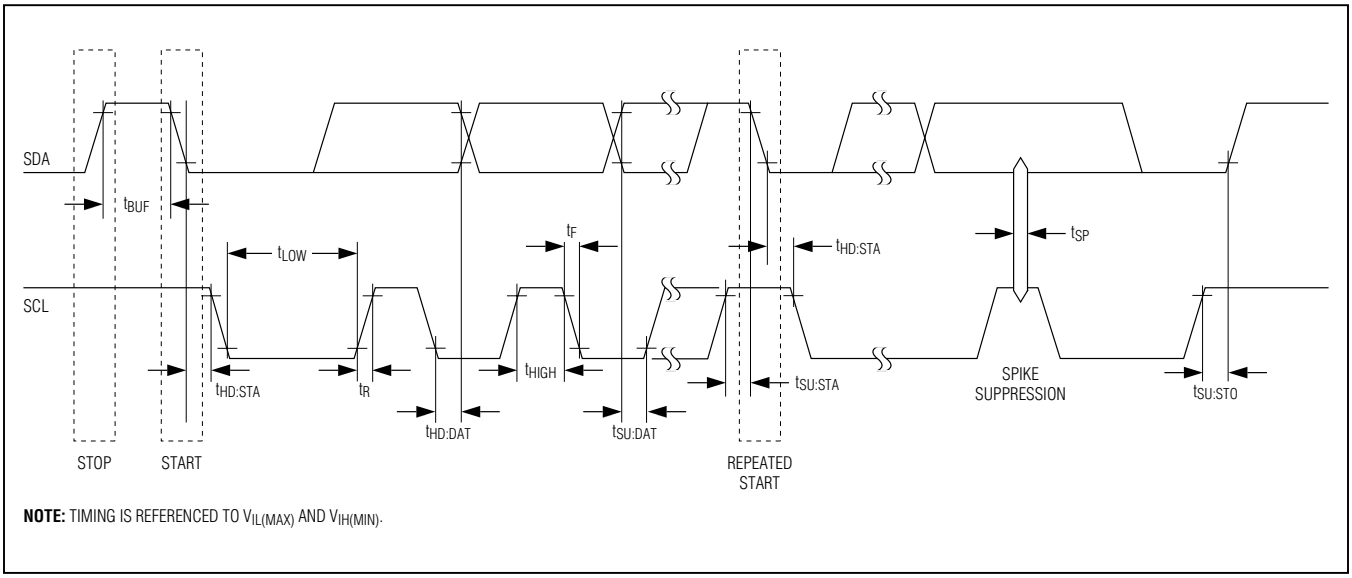


Figure 10. I²C Timing Diagram

Repeated START Condition: Repeated STARTs are commonly used for read accesses after having specified a memory address to read from in a preceding write access. The master can use a repeated START condition at the end of a data transfer to immediately initiate a new data transfer following the current one. A repeated START condition is generated the same way as a normal START condition, but without leaving the bus idle after a STOP condition.

Data Valid: With the exception of the START and STOP condition, transitions of SDA can occur only during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the required setup and hold time ($t_{HD:DAT}$ after the falling edge of SCL and $t_{SU:DAT}$ before the rising edge of SCL; see Figure 10). There is one clock pulse per bit of data. Data is shifted into the receiving device during the rising edge of the SCL pulse.

When finished with writing, the master must release the SDA line for a sufficient amount of setup time (minimum $t_{SU:DAT}$ + t_R in Figure 10) before the next rising edge of SCL to start reading. The slave shifts out each data bit on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. The master generates all SCL clock pulses, including those needed to read from a slave.

Acknowledged by Slave: A slave device, when addressed, is usually obliged to generate an acknowledge after the receipt of each byte. The master must generate the clock pulse for each acknowledge bit. A slave that acknowledges must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse. Setup and hold times $t_{SU:DAT}$ and $t_{HD:DAT}$ must be taken into account.

Acknowledged by Master: To continue reading from a slave, the master is obliged to generate an acknowledge after the receipt of each byte. The master must generate the clock pulse for each acknowledge bit. A master that acknowledges must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse. Setup and hold times $t_{SU:DAT}$ before the rising edge of SCL and $t_{HD:DAT}$ after the falling edge of SCL must be taken into account.

Not Acknowledged by Slave: A slave device may be unable to receive or transmit data, for example, because it is busy performing a real-time function such as MAC computation or EEPROM write cycle or is in sleep mode. In this case, the slave does not acknowledge its slave address and leaves the SDA line high. A slave that is ready to communicate acknowledges at least its slave address. However, some time later the

slave may refuse to accept data, possibly because of an invalid command code or unexpected data. In this case, the slave device does not acknowledge any of the bytes that it refuses and leaves SDA high. In either case, after a slave has failed to acknowledge, the master first should generate a repeated START condition or a STOP condition followed by a START condition to begin a new data transfer.

Not Acknowledged by Master: At some time when receiving data, the master must signal an end of data to the slave. To achieve this, the master does not acknowledge the last byte that it has received from the slave. In response, the slave releases SDA, allowing the master to generate the STOP condition.

Read and Write

To write to the DS2465, the master must access the device in write access mode, i.e., the slave address must be sent with the direction bit set to 0. The next byte to be sent in write access mode is an address byte to select the register or memory address to be written to or to set the address for a subsequent read access (dummy write).

To read from the DS2465, the master must access the device in read access mode, i.e., the slave address must be sent with the direction bit set to 1. The read address is determined either from a preceding write access or implied from a function command.

The DS2465 has different types of memory. Some areas allow unrestricted read/write access [R/W], others are write-only [W], read-only [R] or have user-programmable access restrictions [(R)/(W)].

As a consequence, the read and write behavior is address dependent. Figure 11 shows details.

Type 1 Behavior

The common I²C random access read/write protocol with data acknowledge and address auto-increment applies.

Type 2 Behavior

This behavior applies to the command register, the address to which commands and parameter bytes are written, e.g., to activate the SHA engine or to start any activity on the 1-Wire port. When accessed in write mode, the address does not increment. The subsequent read position is implied by the command code that the master writes. When accessed in read mode coming from a lower address, the data read is indeterminate, but the address increments.

ADDRESS RANGE	ACCESS	READ/WRITE BEHAVIOR	NOTES
00h to 4Bh	R/W	Type 1	Scratchpad.
4Ch to 5Fh	—	Type 1	Reserved. Data written is not stored. Data read is indeterminate.
60h	W	Type 2	Command register.
61h	R	Type 3	1-Wire Master Status.
62h	R	Type 4	1-Wire Read Data.
Refer to the full data sheet.			
66h	—	Type 1	Reserved
67h to 6Dh	R/W	Type 1	1-Wire Configuration.
6Eh to 6Fh	—	Type 1	Reserved. Data written is not stored. Data read is indeterminate.
70h to 73h	R	Type 4	Factory-programmed data.
74h to 7Fh	—	Type 4	Reserved. Data read is indeterminate.
80h to BFh	(R)/(W)	Type 4	User memory.
C0h to FFh	—	Type 4	Reserved. Data written is not stored. Data read is indeterminate.

Figure 11. Address-Specific Read and Write Behavior

Type 3 Behavior

This behavior applies to the

1-Wire Master Status register. Write mode access is used to set the address for a subsequent read access (dummy write); data bytes are not acknowledged. When accessed in read mode, the address does not increment.

Type 4 Behavior

This behavior is similar to type 1, but data bytes are discarded. It applies to EEPROM locations and some read-only addresses. Write mode access is used to set the address for a subsequent read access (dummy write); the address increments after a data byte has been acknowledged. When accessed in read mode, the address increments after a byte is transmitted.

I²C Communication Examples

See Table 26 and Table 27 for the I²C communication legend and data direction codes.

Table 26. I²C Communication—Legend

SYMBOL	DESCRIPTION
S	START Condition
AD, 0	Select DS2465 for Write Access
AD, 1	Select DS2465 for Read Access
Sr	Repeated START Condition
P	STOP Condition
A	Acknowledged
A\	Not Acknowledged
(Idle)	Bus Not Busy
<byte>	Transfer of One Byte
CPS	Command “Copy Scratchpad”, 5Ah
Refer to the full data sheet.	
1WMR	Command “1-Wire Master Reset”, F0h
1WRS	Command “1-Wire Reset Pulse”, B4h
1WSB	Command “1-Wire Single Bit”, 87h
1WWB	Command “1-Wire Write Byte”, A5h
1WRB	Command “1-Wire Read Byte”, 96h
1WT	Command “1-Wire Triplet”, 78h
Refer to the full data sheet.	
1WRB	Command “1-Wire Receive Block”, E1h

Table 27. Data Direction Codes

Master-to-Slave	Slave-to-Master	(DS2465 busy)

I²C Communication Examples (continued)

Copy Scratchpad, e.g., to Write Data to the User Memory

S	AD,0	A	60h	A	CPS	A	<byte>	A	P	Programming

The parameter byte is always acknowledged, regardless of its value (is always valid).

Refer to the full data sheet for this information.

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I²C Communication Examples (continued)

Refer to the full data sheet for this information.

1-Wire Master Reset, e.g., After Power-Up

S	AD,0	A	60h	A	1WMR	A	Sr	AD,0	A	60h	A	1WRS	A	P

The 1-Wire Master Reset must be followed by a 1-Wire Reset Pulse command.

1-Wire Reset Pulse, e.g., to Begin or End 1-Wire Communication

Case A: 1-Wire Idle (1WB = 0), No Busy Polling to Read the Result

S	AD,0	A	60h	A	1WRS	A	P	(Idle)	S	AD,1	A	<byte>	A\	P

In the first cycle, the master sends the command; then the master waits (Idle) for the 1-Wire Reset to complete. In the second cycle the DS2465 is accessed to read the result of the 1-Wire Reset from the 1-Wire Master Status register.

Case B: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed, then Read the Result

S	AD,0	A	60h	A	1WRS	A	Sr	AD,1	A	<byte>	A	<byte>	A\	P

Repeat until the 1WB bit has changed to 0.

Case C: 1-Wire Busy (1WB = 1)

S	AD,0	A	60h	A	1WRS	A\	P

The master should stop and restart as soon as the DS2465 does not acknowledge the command code.

1-Wire Single Bit, e.g., to Generate a Single Time Slot on the 1-Wire Line

Case A: 1-Wire Idle (1WB = 0), No Busy Polling

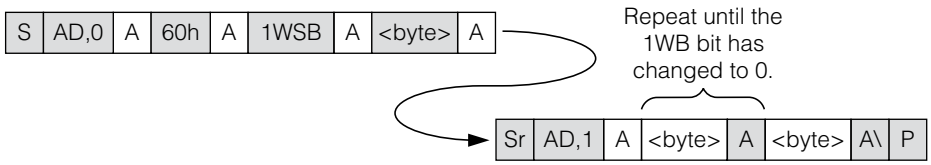
S	AD,0	A	60h	A	1WSB	A	<byte>	A	P	(Idle)

S	AD,1	A	<byte>	A\	P

The idle time is needed for the 1-Wire function to complete. Then access the device in read mode to get the result from the 1-Wire single-bit command.

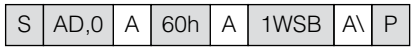
I^2C Communication Examples (continued)

Case B: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed



When 1WB has changed from 1 to 0, the 1-Wire Master Status register holds the valid result of the 1-Wire Single Bit command.

Case C: 1-Wire Busy (1WB = 1)



The master should stop and restart as soon as the DS2465 does not acknowledge the command code.

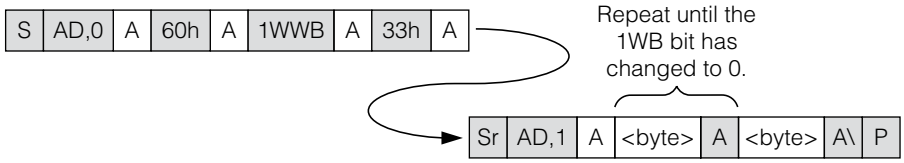
1-Wire Write Byte, e.g., to Send a Command Code to the 1-Wire Line

Case A: 1-Wire idle (1WB = 0), No Busy Polling



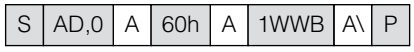
33h is the valid 1-Wire ROM function command for Read ROM. The idle time is needed for the 1-Wire function to complete. There is no data read back from the 1-Wire line with this command.

Case B: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed.



When 1WB has changed from 1 to 0, the 1-Wire Write Byte command is completed.

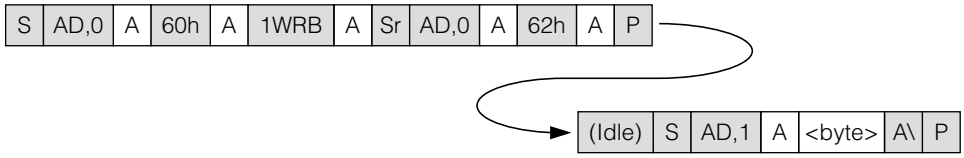
Case C: 1-Wire Busy (1WB = 1)



The master should stop and restart as soon as the DS2465 does not acknowledge the command code.

1-Wire Read Byte, e.g., to Read a Byte from the 1-Wire Line

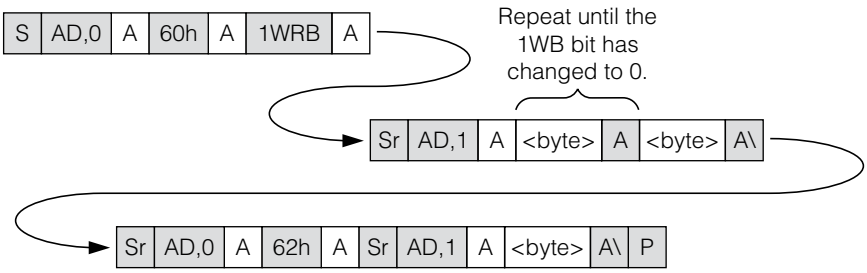
Case A: 1-Wire Idle (1WB = 0), No Busy Polling, Set read address before Idle Time



The read address is set to the 1-Wire Read Data register while the 1-Wire Read Byte command is still in progress. Then, after the 1-Wire function is completed, the device is accessed to read the data byte that was obtained from the 1-Wire line.

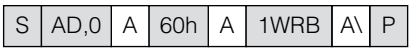
I^2C Communication Examples (continued)

Case B: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed



Poll the Status register until the 1WB bit has changed from 1 to 0. Then set the read address to the 1-Wire Read Data register and access the device again to read the data byte that was obtained from the 1-Wire line.

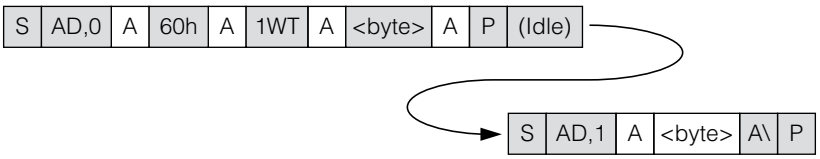
Case C: 1-Wire Busy (1WB = 1)



The master should stop and restart as soon as the DS2465 does not acknowledge the command code.

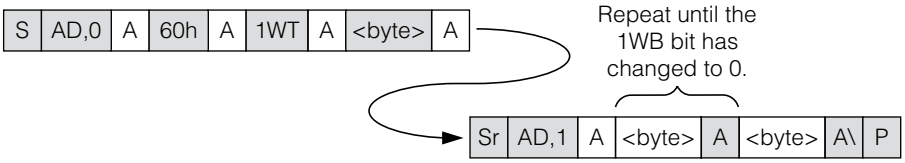
1-Wire Triplet, e.g., to Perform a Search ROM Function on the 1-Wire Line

Case A: 1-Wire Idle (1WB = 0), No Busy Polling



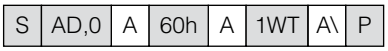
The idle time is needed for the 1-Wire function to complete. Then access the device in read mode to get the result from the 1-Wire Triplet command.

Case B: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed



When 1WB has changed from 1 to 0, the 1-Wire Master Status register holds the valid result of the 1-Wire Triplet command.

Case C: 1-Wire Busy (1WB = 1)



The master should stop and restart as soon as the DS2465 does not acknowledge the command code.

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I^2C Communication Examples (continued)

Refer to the full data sheet for this information.

1-Wire Receive Block, e.g., to Read Data from the 1-Wire Slave

Case A: 1-Wire Idle (1WB = 0)

S	AD,0	A	60h	A	1WRB	A	<byte>	A	P	(Idle)

The parameter byte is always acknowledged, regardless of its value (is always valid).

Case B: 1-Wire Busy (1WB = 1)

S	AD,0	A	60h	A	1WRB	A\	P

The master should stop and restart as soon as the DS2465 does not acknowledge the command code.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS2465P+	-40°C to +85°C	6 TSOC
DS2465P+T	-40°C to +85°C	6 TSOC (4k pieces)

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 TSOC	D6+1	21-0382	90-0321

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