IR3094PBF

3 PHASE PWM CONTROLLER FOR POINT OF LOAD

DESCRIPTION

The IR3094 Control IC provides a full featured, cost effective, single chip solution to offers a compact, efficient solution for high current POL converters. Control and 3 Phase Gate Drive functions are integrated into a single space-saving IC.

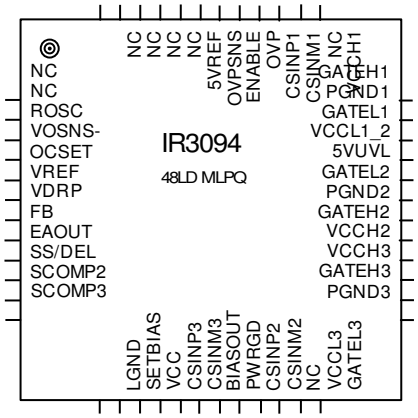
FEATURES

- 0.85V Reference Voltage
- 3A GATELX Pull Down Drive Capability
- Programmable 100KHz to 540KHz oscillator
- Programmable Voltage Positioning (can be disabled)
- Programmable Softstart
- Programmable Hiccup Over-Current Protection with Delay to prevent false triggering
- Simplified Powergood provides indication of proper operation and avoids false triggering
- Operates up to 16V converter input with 7.5V Under-Voltage Lockout
- 4.36V Under-Voltage Lockout threshold for gate driver voltage
- Adjustable Voltage, 150mA Bias Regulator provides MOSFET Drive Voltage
- Enable Input
- OVP Flag Output detects high side fet short at powerup
- Separate OVP sense line to sense the output voltage and latched OVP with protection
- Inductor DCR sensing for current sensing will support up to 5.1V output applications
- Available 48L MLPQ package

ORDERING INFORMATION

Device	Order Quantity
IR3094MTRPBF	3000 per Reel
IR3094MPBF	100 piece strips

PACKAGE INFORMATION



48L MLPQ
(7 x 7 mm Body)
$\theta_{JA} = 27^{o}C/W$

PIN DESCRIPTION

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	NC	Not connected
2	NC	Not connected
3	ROSC	Connect a resistor to VOSNS- to program oscillator frequency, OCSET and STBIAS bias currents.
4	VOSNS-	Remote Sense Input. Connect to ground at the load.
5	OCSET	Programs the hiccup over-current threshold through an external resistor tied to VREF and an internal current source. The bias current is a function of ROSC.
6	VREF	0.85V Reference voltage. Current Sensing and Over Current Protection are referenced to this pin. An external RC network tied to VOSNS- is needed for the compensation.
7	VDRP	Buffered average current information. Connect an external resistor to FB to program converter output.
8	FB	Inverting input to the Error Amplifier.
9	EAOUT	Output of the Error Amplifier.
10	SS/DEL	Controls Converter Softstart, Power Good, and Over-Current Timing. Connect an external capacitor to LGND to program the timing.
11	SCOMP2	Compensation for the Current Share control loop. Connect a capacitor to ground to set the control loop's bandwidth. Phase 2 is forced to match phase 1's current.
12	SCOMP3	Compensation for the Current Share control loop. Connect a capacitor to ground to set the control loop's bandwidth. Phase 3 is forced to match phase 1's current.
13	LGND	Local Ground and IC substrate connection.
14	SETBIAS	External resistor to ground sets voltage at BIASOUT pin. Bias current is a function of ROSC.
15	VCC	Power for internal circuitry and source for BIASOUT regulator.
16	CSINP3	Non-inverting input to the Phase 3 Current Sense Amplifier.
17	CSINM3	Inverting input to the Phase 3 Current Sense Amplifier.
18	BIASOUT	150mA open-looped regulated voltage set by SETBIAS for GATE drive bias.
19	PWRGD	Open Collector output that drives low during Softstart or any fault condition. Connect external pull-up.
20	CSINP2	Non-inverting input to the Phase 2 Current Sense Amplifier.
21	CSINM2	Inverting input to the Phase 2 Current Sense Amplifier.
22	NC	Not connected
23	VCCL3	Power for Phase 3 Low-Side Gate Driver.
24	GATEL3	Phase 3 Low-Side Gate Driver Output and input to GATEH3 non-overlap comparator.
25	PGND3	Return for Phase 3 Gate Drivers.
26	GATEH3	Phase 3 High-Side Gate Driver Output and input to GATEL3 non-overlap comparator.
27	VCCH3	Power for Phase 3 High-Side Gate Driver.
28	VCCH2	Power for Phase 2 High-Side Gate Driver.
29	GATEH2	Phase 2 High-Side Gate Driver Output and input to GATEL2 non-overlap comparator.
30	PGND2	Return for Phase 2 Gate Drivers.
31	GATEL2	Phase 2 Low-Side Gate Driver Output and input to GATEH2 non-overlap comparator.
32	5VUVL	Can be used to monitor the driver supply voltage or 5V supply voltage when converting from 5V. An under voltage condition initiates Soft Start.
33	VCCL1_2	Power for Phase 1 and 2 Low-Side Gate Drivers.
34	GATEL1	Phase 1 Low-Side Gate Driver Output and input to GATEH1 non-overlap comparator.
35	PGND1	Return for Phase 1 Gate Drivers.
36	GATEH1	Phase 1 High-Side Gate Driver Output and input to GATEL1 non-overlap comparator.
37	VCCH1	Power for Phase 1 High-Side Gate Driver.
38	NC	Not connected
39	CSINM1	Inverting input to the Phase 1 Current Sense Amplifier.
40	CSINP1	Non-inverting input to the Current Sense Amplifier.
41	OVP	Output that drives high during an Over-Voltage condition.
42	ENABLE	Enable Input. A logic low applied to this pin puts the IC into Fault mode.
43	OVPSNS	Dedicated output voltage sense pin for Over Voltage Protection.
44	5VREF	Decoupling for internal voltage reference rail.
45	NC	Not connected
46	NC	Not connected
47	NC	Not connected
48	NC	Not connected

ABSOLUTE MAXIMUM RATINGS

Operating Junction Temperature……..0°C to 150°C
Storage Temperature Range…….-65°C to 150°C

PIN	NAME	VMAX	VMIN	ISOURCE	ISINK
3	ROSC	20V	-0.3V	1mA	1mA
4	VOSNS-	0.5V	-0.5V	10mA	1mA
5	OCSET	20V	-0.3V	1mA	1mA
6	VDAC	20V	-0.3V	1mA	1mA
7	VDRP	20V	-0.3V	25mA	5mA
8	FB	20V	-0.3V	1mA	1mA
9	EAOUT	10V	-0.3V	5mA	10mA
10	SS/DEL	20V	-0.3V	1mA	1mA
11	SCOMP2	20V	-0.3V	1mA	1mA
12	SCOMP3	20V	-0.3V	1mA	1mA
13	LGND	n/a	n/a	50mA	1mA
14	SETBIAS	20V	-0.3V	1mA	1mA
15	VCC	20V	-0.3V	1mA	500mA
16	CSINP3	20V	-0.3V	1mA	1mA
17	CSINM3	20V	-0.3V	1mA	1mA
18	BIASOUT	20V	-0.3V	450mA	1mA
19	PWRGD	20V	-0.3V	1mA	20mA
20	CSINP2	20V	-0.3V	1mA	1mA
21	CSINM2	20V	-0.3V	1mA	1mA
22	NC	n/a	n/a	n/a	n/a
23	VCCL3	20V	-0.3V	n/a	3A for 100ns, 200mA DC
24	GATEL3	20V	-0.3V DC, -2V for 100ns	3A for 100ns, 200mA DC	3A for 100ns, 200mA DC
25	PGND3	0.3V	-0.3V	3A for 100ns, 200mA DC	n/a
26	GATEH3	30V	-0.3V DC, -2V for 100ns	3A for 100ns, 200mA DC	3A for 100ns, 200mA DC
27	VCCH3	30V	-0.3V	n/a	3A for 100ns, 200mA DC
28	VCCH2	30V	-0.3V	n/a	3A for 100ns, 200mA DC
29	GATEH2	30V	-0.3V DC, -2V for 100ns	3A for 100ns, 200mA DC	3A for 100ns, 200mA DC
30	PGND2	0.3V	-0.3V	3A for 100ns, 200mA DC	n/a
31	GATEL2	20V	-0.3V DC, -2V for 100ns	3A for 100ns, 200mA DC	3A for 100ns, 200mA DC
32	5VUVL	20V	-0.3V	1mA	1mA
33	VCCL1_2	20V	-0.3V	n/a	3A for 100ns, 200mA DC
34	GATEL1	20V	-0.3V DC, -2V for 100ns	3A for 100ns, 200mA DC	3A for 100ns, 200mA DC
35	PGND1	0.3V	-0.3V	3A for 100ns, 200mA DC	n/a
36	GATEH1	30V	-0.3V DC, -2V for 100ns	3A for 100ns, 200mA DC	3A for 100ns, 200mA DC
37	VCCH1	30V	-0.3V	n/a	3A for 100ns, 200mA DC
38	NC	n/a	n/a	n/a	n/a
39	CSINM1	20V	-0.3V	1mA	1mA
40	CSINP1	20V	-0.3V	1mA	1mA
41	OVP	20V	-0.3V	1mA	1mA
42	ENABLE	20V	-0.3V	1mA	1mA
43	OVPSNS	20V	-0.3V	1mA	1mA
44	5VREF	10V	-0.3V	10mA	20mA

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over: 8.0 ≤ V_{CC} ≤ 16V, 4V ≤ V_{CCLX}≤ 14V, 4V ≤ V_{CCHX} ≤ 28V, C_{GATEHX} =3.3nF, C_{GATELX} =6.8nF, 0°C ≤ T_J ≤ 125 °C

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VREF Reference					
Sink Current	R_{ROSC} = 47kΩ, VREF=OCSET	45	53	61	µA
Source Current	R_{ROSC} = 47kΩ, VREF=OCSET	48	56	64	µA
System Reference Voltage	Connect FB to EAOUT, Measure V(EAOUT)-V(VOSNS-). Applies to -0.3V<VOSNS-<0.3V.	0.8415	0.85	0.8585	V
Error Amplifier					
Input Offset Voltage	Connect FB to EAOUT, Measure V(EAOUT)-V(VREF). Applies to -0.3V<VOSNS-<0.3V. Note 1	-5	-1	3	mV
UVL FB Bias Current		40	90	150	uA
UVL Head Room		1.2	2	2.5	V
DC Gain	Note 1	90	100	105	dB
Gain-Bandwidth Product	Note 1	4	7		MHz
Slew Rate	Note 1, 50mV FB signal		1.25		V/µs
Source Current		300	430	600	µA
Sink Current		.75	1.1	1.5	mA
Max Voltage		4.5	4.9	5.3	V
Min Voltage			50	200	mV
VDRP Buffer Amplifier					
Positioning Offset Voltage	V(VDRP) – V(REF) with CSINMX=CSINPX=0. Note 1.	-125	0	125	mV
Output Voltage Range		0.2		3.75	V
Source Current		4	8	20	mA
Sink Current		200	300	650	µA
Oscillator					
Switching Frequency	R_{ROSC} = 47kΩ	160	200	240	kHz
Phase Shift	Sequence: GATEH1-GATEH2-GATEH3	102	120	138	°

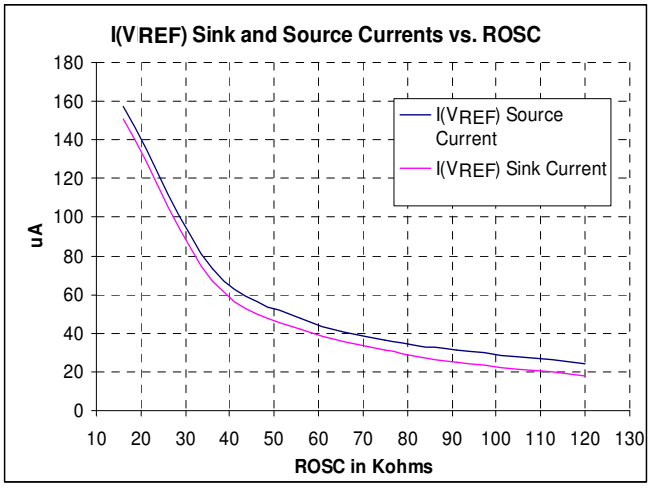
PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
BIASOUT Regulator					
SETBIAS Bias Current	R_{ROSC} = 47kΩ	94	103	117.5	µA
Set Point Accuracy	V(SETBIAS)-V(BIASOUT) @ 100mA	0	0.25	0.55	V
BIASOUT Dropout Voltage	I(BIASOUT)=100mA,Threshold when V(SETBIAS)-V(BIASOUT)=0.45V	1.2	1.8	2.5	V
BIASOUT Current Limit		150	250	500	mA
Soft Start and Delay					
SS/DEL to FB Input Offset Voltage	With FB = 0V, adjust V(SS/DEL) until EAOUT drives high	0.8	1.1	1.8	V
Charge Current		30	60	90	µA
Hiccup Discharge Current		3.5	6	9	µA
OC Discharge Current		25	55	70	µA
Charge/Discharge Current Ratio		9	10	13	µA/µA
Charge Voltage		3.8	4.0	4.2	V
Delay Comparator Threshold	Relative to Charge Voltage	180	245	310	mV
Discharge Comparator Threshold		170	265	350	mV
Over-Current Comparator					
Input Offset Voltage	V(OCSET)-V(VREF), CSINM=CSINP1=CSINP2=CSINP3, Note 1.	-125	0	125	mV
OCSET Bias Current	R_{ROSC} = 47kΩ	23.5	27	29.4	µA
Max OCSET Set Point		3.9			V
Under-Voltage Lockout					
VCC Start Threshold		7.0	7.5	8.0	V
VCC Stop Threshold		6.5	7.0	7.5	V
VCC Hysteresis	Start – Stop	400	500	700	mV
5VUVL Start Threshold		4.05	4.36	4.60	V
5VUVL Stop Threshold		3.92	4.17	4.40	V
5VUVL Hysteresis	Start – Stop	100	200	250	mV
PWRGD Output					
Output Voltage	I(PWRGD) = 4mA		150	400	mV
Leakage Current	V(PWRGD) = 5.5V		0	10	µA

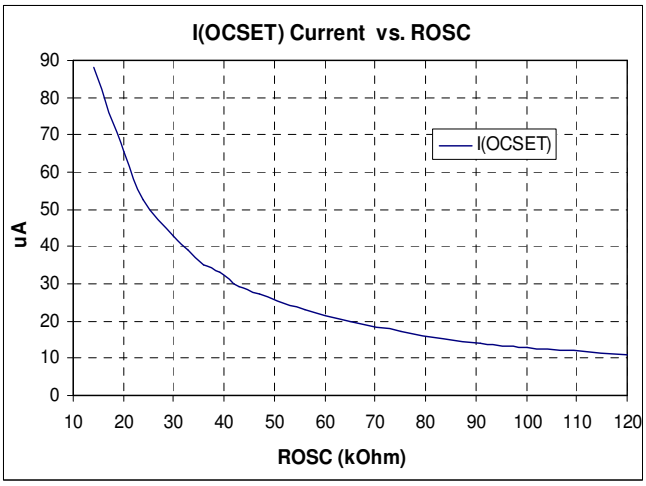
PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Enable Input					
Threshold	Referenced to VOSNS-	1.3	1.5	1.7	V
Input Resistance		5	10	20	kΩ
Pull-up Voltage		2.4	3.0	3.7	V
Gate Drivers					
GATEH Rise Time	VCCHX = 8V, Measure 1V to 7V transition time. Note 1.		25	50	ns
GATEH Fall Time	VCCHX = 8V, Measure 7V to 1V transition time. Note 1.		25	50	ns
GATEL Rise Time	VCCLX= 8V, Measure 1V to 7V transition time. Note 1.		50	90	ns
GATEL Fall Time	VCCLX= 8V, Measure 7V to 1V transition time. Note 1.		30	60	ns
High Voltage (AC)	Measure VCCLX– GATELX or VCCHX – GATEHX, Note 1		0	0.5V	V
Low Voltage (AC)	Measure GATELX or GATEHX, Note 1		0	0.5V	V
GATEL low to GATEH high delay	VCCHX = VCCLX= 8V, Measure the time from GATELX falling to 1V to GATEHX rising to 1V. Note 1.	10	25	50	ns
GATEH low to GATEL high delay	VCCHX = VCCLX= 8V, Measure the time from GATEHX falling to 1V to GATELX rising to 1V. Note 1.	10	25	50	ns
Disable Pull-Down Current	GATHX or GATELX=2V with VCC = 0V. Measure Gate pull-down current	20	35	50	μA
PWM Comparator					
Propagation Delay	Note1		100	150	ns
Common Mode Input Range				4	V
Internal Ramp Start Voltage		0.44	0.6	0.9	V
Internal Ramp Amplitude		35	50	65	mV / %DTC
Current Sense Amplifier					
CSINPX Bias Current		-1	0	1	μA
CSINM2,3 Bias Current		-1	0	1	μA
CSINM1 Bias Current		-2	-0.5	1	μA
Phase 2 and 3 Input Current Offset Ratio			1		μA/μA
Phase 1 Input Current Offset Ratio		0.5	1.7	4	μA/μA
Average Input Offset Voltage	(VDRP-VREF)/GAIN with CSINX=0. Note1	-5	0	5	mV
Offset Voltage Mismatch	Monitor I(SCOMPX), Note1.	-5	0	5	mV
Gain at T_J = 25 °C		22.5	24	25.5	V/V
Gain at T_J = 125 °C		19	20.9	22	V/V
Gain Mismatch	Note 1.	-1	0	1	V/V
Differential Input Range		-25		75	mV
Common Mode Input Range		-0.2		5.5	V

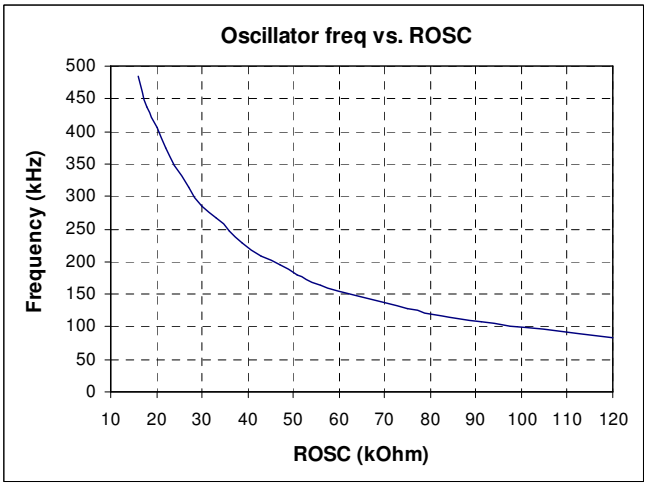
PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Share Adjust Error Amplifier					
Input Offset Voltage	Note 1	-5	0	5	mV
MAX Duty Cycle Adjust Ratio	Compare Duty Cycle to GATEH1	1.5	2.0		
MIN Duty Cycle Adjust Ratio	Compare Duty Cycle to GATEH1	0.6	0.5		
Transconductance	Note 1	100	200	300	μA/V
SCOMPX Source/Sink Current		16	22	28	μA
SCOMPX Precondition and GATELX Release Threshold	V(FB)	0.6	0.67	0.74	V
SCOMP precondition current		160	360	560	μA
Duty Cycle Match at Startup	Compare Duty Cycle to GATEHX	-7	-1	7	%
0% Duty Cycle Comparator					
Threshold Voltage	Below Internal Ramp1 Start Voltage	-25	25	75	mV
Propagation Delay	VCCLX= 8V. Step EAOUT from .8V to .3V and measure time to GATELX transition to < 7V.		200	400	ns
OVP					
Comparator Threshold	Compare to V(VREF)	120	150	200	mV
Power-up Headroom for OVP Flag	VCC=OVPSNS where V(OVP)>0.5V. Same for 5VUVL=OVPSNS.	0.8	1.1	1.8	V
OVPSNS Threshold at Power-up	VCC=2V, V(OVP) >0.5V. Same for V(5VUVL)=2V.	0.3	0.48	0.85	V
SS/DEL Power-up Clear Threshold	VCC=12V, V(OVPSNS)=1V, VREF=1.6V, where OVP<0.5V	0.35	0.60	0.95	V
Propagation Delay	VCCLX= 8V. V(EAOUT)=0V. Step OVPSNS 540mV + V(VREF). Measure time to GATELX transition to >1V. Note 1.	150	350	650	ns
OVP Source Current	V(OVP)=0.5V, VCC=1.8V, 5VUVL=0V	10	75		μA
OVP Pull Down Resistance	OVP to LGND	30	60	100	kΩ
OVP High Voltage	I(OVP)=10uA, V(VCC) or V(5VUVL)-V(OVP), VCC=1.8V	0.4	0.70	1.1	V
OVPSNS Bias Current		-6.0	-3.0	1.5	uA
5VREF					
Short Circuit Current		20	45	60	mA
Supply Voltage	I(5VREF)=0A	4.5	5	5.5	V
General					
VCC Supply Current	V(VCC)=16V	28.5	35	40.5	mA
VOSNS- Current	-0.3V ≤ VOSNS- ≤ 0.3V	0.6	0.8	1.2	mA
VCCHX and VCCL3 Current	V(VCCHX)=28V, V(VCCL3)=14V	3	5	7	mA
VCCL1_2 Supply Current	V(VCCL1_2)=14V	6	10	17	mA
5VUVL Supply Current	V(5VUVL)=5V, no OVP condition	100	200	400	uA
Non_Sync to Sync Threshold		70.6	77.7	87	%VREF

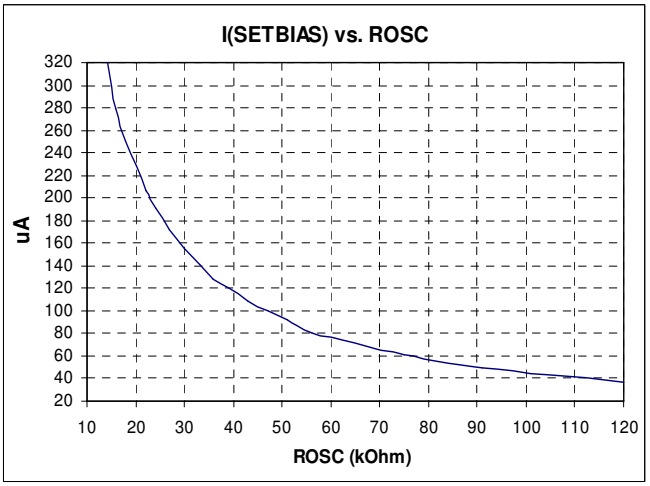
Note 1: Guaranteed by design, but not tested in production
Note 2: VREF Output is trimmed to compensate for Error Amp input offsets errors

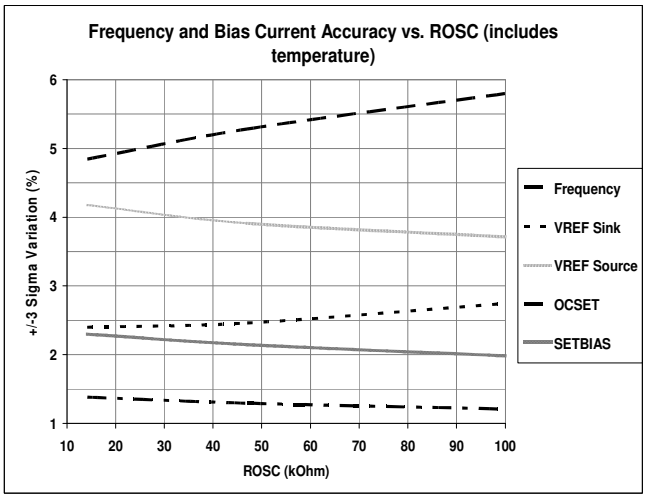
TYPICAL OPERATING CHARACTERISTICS

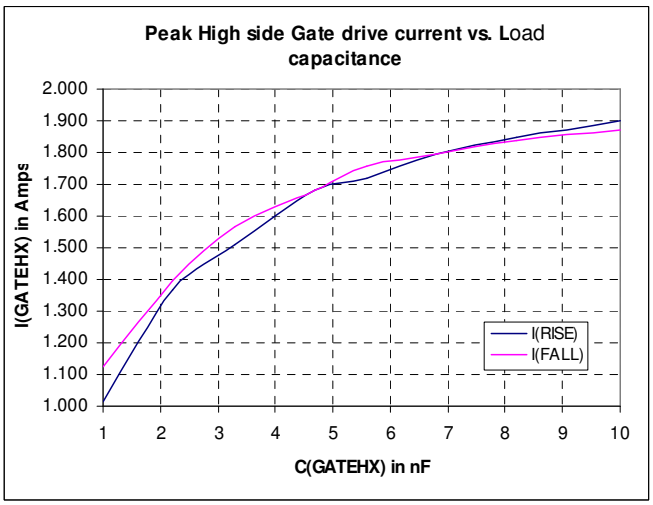


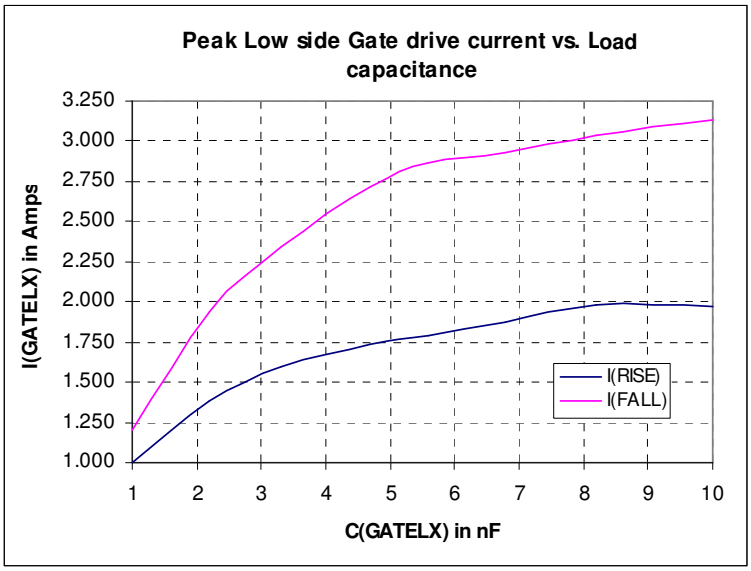




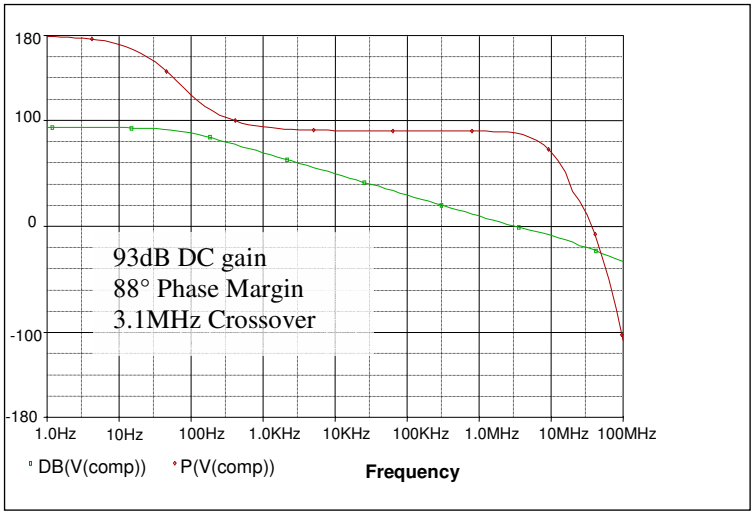








Error Amplifier Frequency Response



IR3094 THEORY OF OPERATION

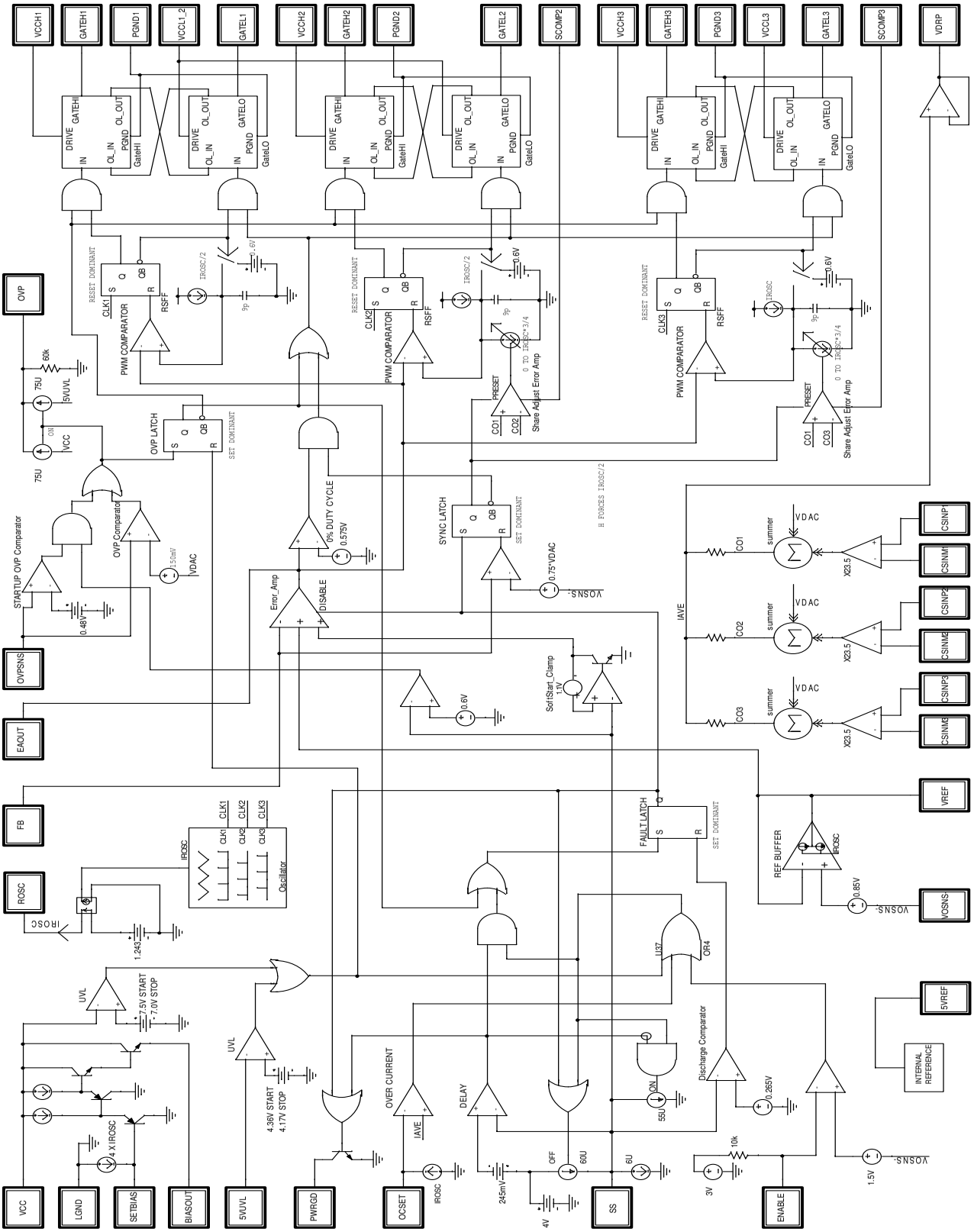


Figure 1 – IR3094 Block Diagram

PWM Operation

The IR3094 is a fully integrated 3 phase interleaved PWM control IC which uses voltage mode control with trailing edge modulation. A high-gain wide-bandwidth voltage type Error Amplifier in the Control IC is used for the voltage control loop. The PWM block diagram of the IR3094 is shown in Figure 2.

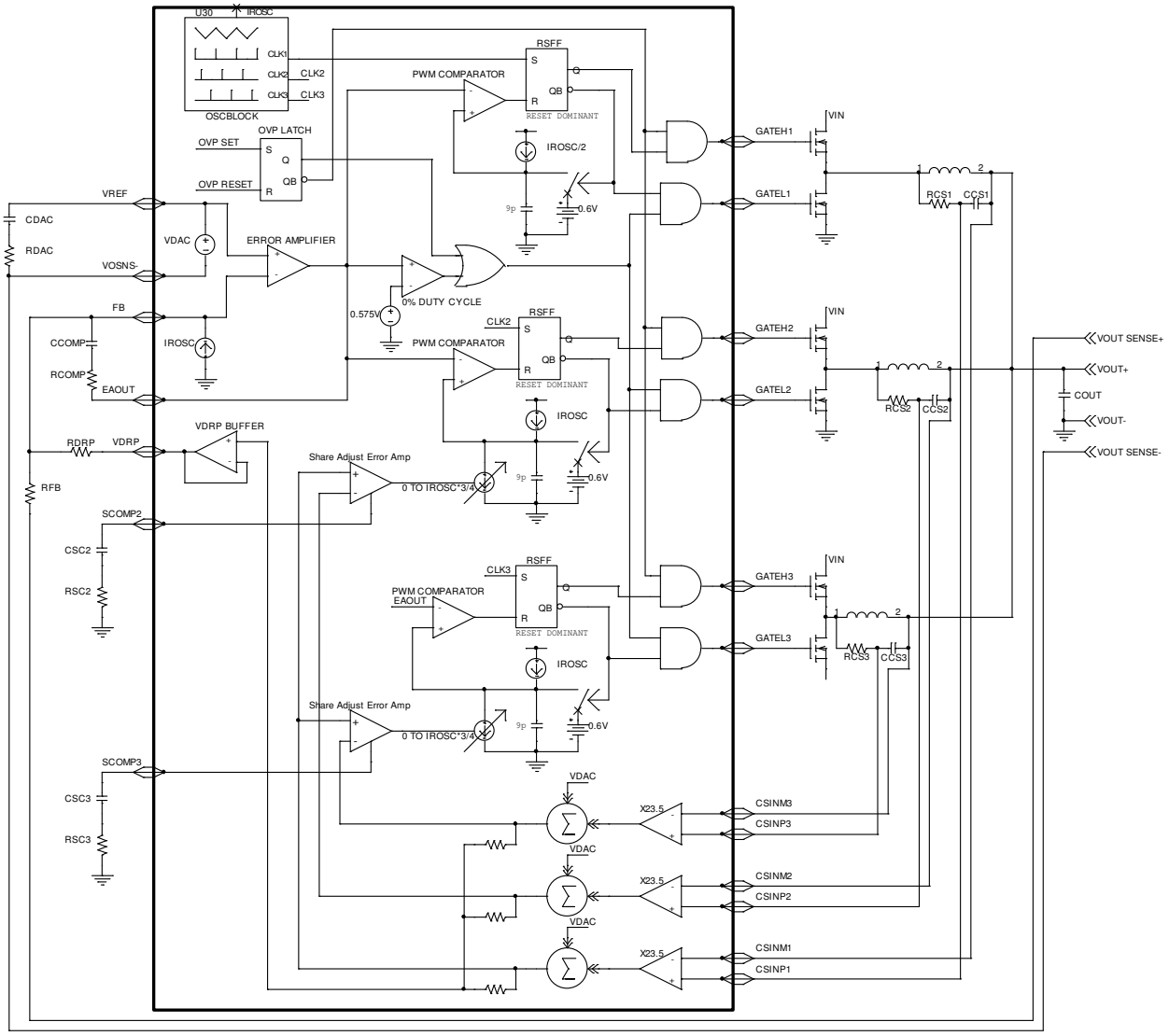


Figure 2 – PWM Block Diagram

Refer to Figure 3. Upon receiving a clock pulse, the RSFF is set, the internal PWM ramp voltage begins to increase, the low side driver is turned off, and the high side driver is then turned on. For phase 1, an internal 9pf capacitor is charged by a current source that proportional to the switching frequency resulting in a ramp rate of 50mV per percent duty cycle. For example, if the steady-state operating switch node duty cycle is 10%, then the internal ramp amplitude is typically 500mV from the starting point (or floor) to the crossing of the EAOUT control voltage. When the PWM ramp voltage exceeds the Error Amplifier's output voltage, the RSFF is reset. This turns off the high side driver, turns on the low side driver, and discharges the PWM ramp to 0.6V until the next clock pulse.

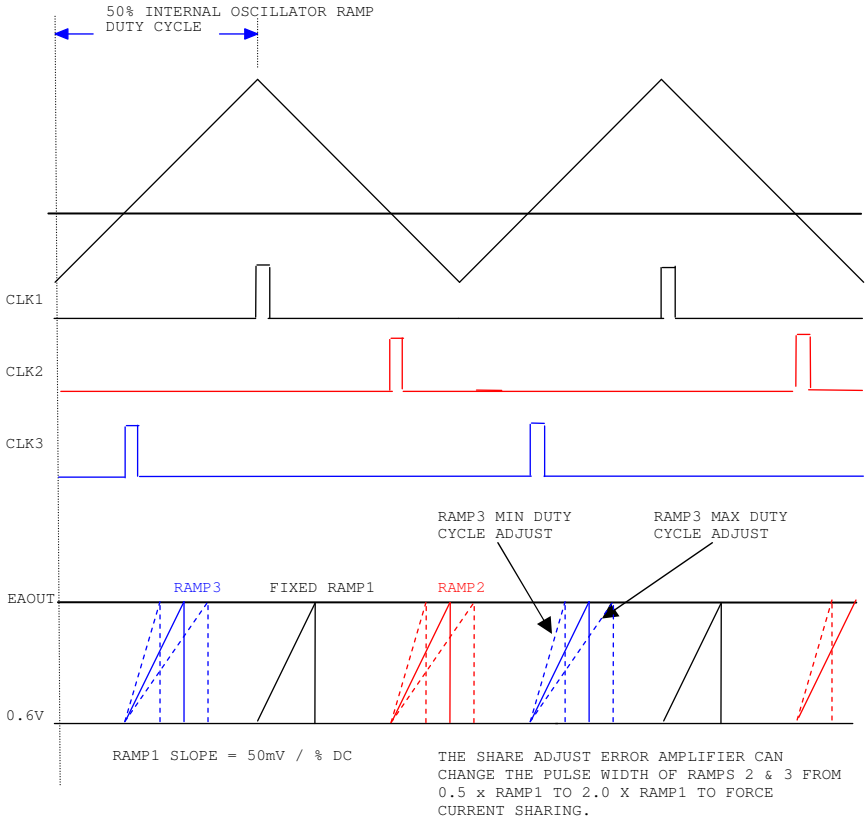


Figure 3 – 3 Phase Oscillator and PWM Waveforms

The RSFF is reset dominant allowing both phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go to 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An Error Amplifier output voltage greater than the common mode input range of the PWM comparator results in 100% duty cycle regardless of the voltage of the PWM ramp. This arrangement guarantees the Error Amplifier is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease which is appropriate given the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients.

This control method is designed to provide “single cycle transient response” where the inductor current changes in response to load transients within a single switching cycle maximizing the effectiveness of the power train and minimizing the output capacitor requirements.

Body Braking™

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load step decrease is;

$$T_{SLEW} = [L \times (I_{MAX} - I_{MIN})] / Vout \qquad (1)$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response to a load step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier’s body diode occurs. This increases the voltage across the inductor from Vout to Vout + $V_{BODY\ DIODE}$. The minimum time required to reduce the current in the inductor in response to a load transient decrease is now;

$$T_{SLEW} = [L \times (I_{MAX} - I_{MIN})] / (Vout + V_{BODY\ DIODE}) \qquad (2)$$

Since the voltage drop in the body diode is often higher than output voltage, the inductor current slew rate can be increased by 2X or more. This patent pending technique is referred to as “body braking” and is accomplished through the “0% Duty Cycle Comparator”. If the Error Amplifier’s output voltage drops below 0.575V, this comparator turns off the low side gate driver.

Figure 4 depicts PWM operating waveforms under various conditions

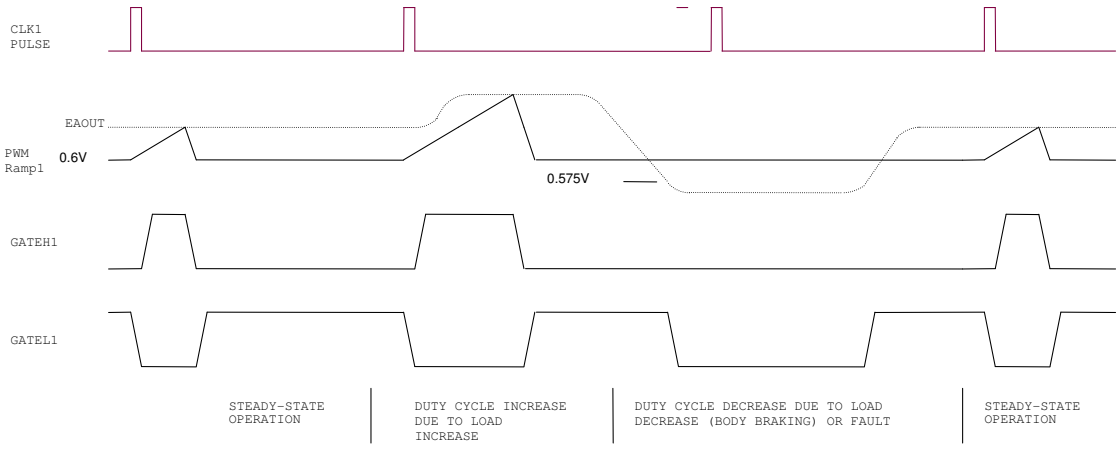


Figure 4 – PWM Operating Waveforms

Current Sense Amplifier

A high speed differential current sense amplifier is shown in Figure 5. Its gain decreases with increasing temperature and is nominally 24 at 25ºC and 20.9 at 125ºC (-1400 ppm/ºC). This reduction of gain tends to compensate the 3850 ppm/ºC increase in inductor DCR. Since in most designs the IR3094 IC junction is hotter than the inductors these two effects tend to cancel such that no additional temperature compensation of the load line is required.

The current sense amplifier can accept positive differential input up to 75mV and negative up to -25mV before clipping. The output of the current sense amplifier is summed with the VREF voltage which is used for over current protection, voltage positioning and current sharing.

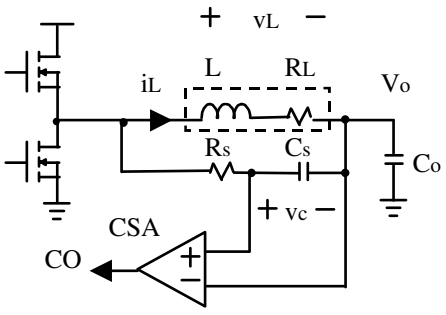


Figure 5 – Inductor Current Sensing and Current Sense Amplifier

Power-up in Non-Synchronous Mode

The SYNC LATCH is set by either a UVLO or a Low Enable fault at the beginning of the power-up cycle, keeping all three low side gate drivers low. The SYNC LATCH is then reset once the FB pin exceeds 78% of VREF to release the low side gate drive control to the Error-Amp. SCOMP preconditioning is also released at this time. Non-Synchronous startup helps preventing negative inductor current until current sharing is stabilized.

VCC Under Voltage Lockout (UVLO)

The VCC UVLO function monitors the IR3094's VCC supply pin and ensures enough voltage is available to power the internal circuitry. During power-up the fault latch is reset when VCC exceeds 7.5V and all other faults are cleared. The fault latch is set when VCC drops below 7.0V and SS/DEL is below 3.75V.

5VUVL Under Voltage Lockout (5VUVL)

The 5VUVL function is provided for converters using a separate voltage supply other than VCC for gate driver bias. The 5VUVL comparator prevents operation by discharging SS/DEL below 3.75V to force EAOUT low. The 5VUVL comparator has an OK threshold of 4.36V ensuring adequate gate drive voltage is present and a fault threshold of 4.17V.

Power Good Output

The PWRGD pin is an open-collector output and should be pulled up to a voltage source through a resistor. During soft start, the PWRGD remains low until the output voltage is in regulation and SS/DEL is above 3.75V. The PWRGD pin becomes low if the fault latch is set. A high level at the PWRGD pin indicates that the converter is in operation and has no fault, but does not ensure the output voltage is within the specification. Output voltage regulation within the design limits can logically be assured however, assuming no component failure in the system.

Tri-State Gate Drivers

The GATELX drivers can pull down up to 3.5A peak current and source up to 1.5A. The GATEHX drivers can source and sink up to 1.5A peak current. An adaptive non-overlap circuit monitors the voltage on the GATEHX and GATELX pins to prevent MOSFET shoot-through current while minimizing body diode conduction.

The Error Amplifier output of the Control IC drives low in response to any fault condition such as VCC input under voltage or output overload. The 0% duty cycle comparator detects this and drives both gate outputs low. This tri-state operation prevents negative inductor current and negative output voltage during power-down.

The Gate Drivers revert to a high impedance "off" state at VCCLX and VCCHX supply voltages below the normal operating range. An 80kΩ resistor is connected across the GATEX and PGNDX pins to prevent the GATEX voltage from rising due to leakage or other cause under these conditions.

Over Voltage Protection (OVP)

The output Over-Voltage Protection comparator monitors the output voltage through the OVPSNS pin, the positive remote sense point. If OVPSNS exceeds VREF plus 150mV, the OVP LATCH will be set. This will set the fault latch immediately pulling the Error Amplifier's output low, reset the PWM latch to fully turn-off the high side MOSFETs and turn-on the low side MOSFETs within approximately 350ns. The low side MOSFETs will remain ON until the OVP LATCH is reset by recycling VCC. OVPSNS exceeding VREF by 150mV also activates 75uA sources on the OVP pin. The lower MOSFETs alone can not clamp the output voltage however an SCR or MOSFET could be triggered with the OVP pin to prevent processor damage.

If powering up with a high side MOSFET short, the OVP flag is activated and the OVP LATCH is set with as little VCC supply voltage as possible. The OVPSNS pin is compared against both VCC and 5VUVL for OVP conditions at power-up. VCC is monitored for conversion off 12V, 5VUVL is monitored for conversion off 5V. The OVP pin flags a voltage greater than 0.48V with supply voltages as low as 1.0V. This headroom voltage varies inversely with temperature. An external comparator can be used to disable the silver box, activate a crowbar, or supply source.

APPLICATIONS INFORMATION

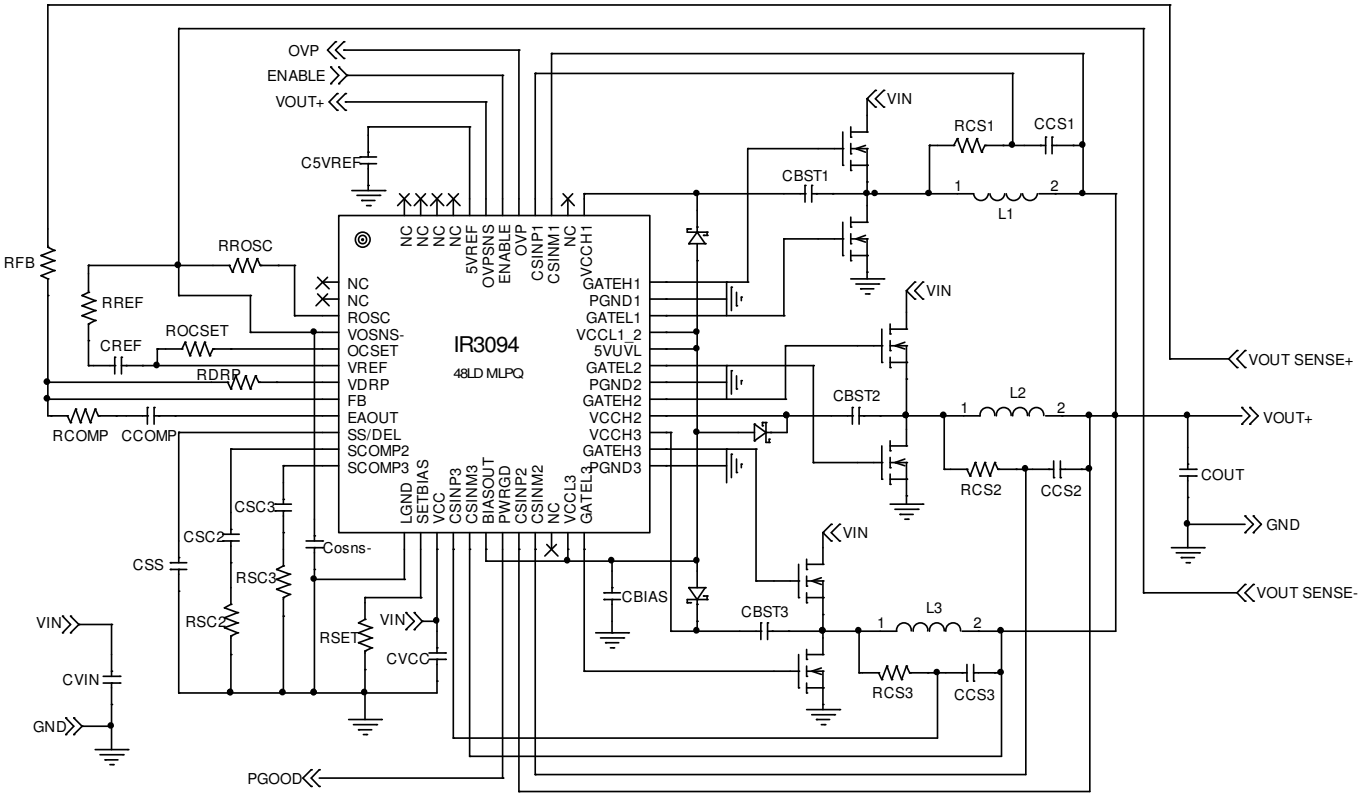


Figure 6 – System Diagram

Oscillator Resistor RROSC

The oscillator frequency is programmable from 100kHz to 540kHz with an external resistor RROSC as shown in Figure 6. The Oscillator generates an internal 50% duty cycle sawtooth signal (Figure 3.) that is used to generate 120° out-of-phase timing pulses to set Phase 1,2 and 3 RS flip-flops. Once the switching frequency is chosen, RROSC can be determined from the curve in the Typical Operating Characteristics Section.

Soft Start, Over-Current Fault Delay, and Hiccup Mode

The IR3094 has a programmable soft-start function to limit the surge current during converter power-up. A capacitor connected between the SS/DEL and LGND pins controls soft start timing as well as over-current protection delay and hiccup mode timing.

Figure 8 depicts the various operating modes of the SS/DEL function. Under a no fault condition, the SS/DEL capacitor will charge. The SS/DEL charge soft-start duration is controlled by a 60uA charge current which charges CSS up to 4.0V. The Error Amplifier output is clamped low until SS/DEL reaches 1.1V. The Error Amplifier will then regulate the converter's output voltage to match the SS/DEL voltage less the 1.1V offset until it reaches the level determined by the VREF voltage. The PWRGD signal is asserted once the SS/DEL voltage exceeds 3.75V.

Four different faults will immediately cause SS/DEL to begin discharging and set the Fault Latch once SS/DEL is below 3.75V;

1. VCC Under Voltage Lock Out
2. 5VUVL Under Voltage Lock Out
3. Low Enable pin
4. Over Current condition.

A delay is included if any of the four fault conditions occurs after a successful soft start sequence. This is required since momentary faults can occur as part of normal operation due to load transients such as exciting an over-current condition. If any fault occurs during normal operation, the SS/DEL capacitor will discharge through a 55uA current sink but will not set the fault latch immediately. If the fault condition persists long enough for the SS/DEL capacitor to discharge below the 3.75V threshold of the delay comparator, the Fault latch will be set pulling the Error Amplifier's output low, inhibiting switching and de-asserting the PWRGD signal. The SS/DEL capacitor is then discharged through a 6uA discharge current resulting in a long hiccup duration.

The SS/DEL capacitor will continue to discharge until it reaches 0.265V where the fault latch is reset allowing a normal soft start to occur. If a fault condition is again encountered during the soft start cycle, the fault latch will be set without any delay and hiccup mode will begin. During hiccup mode the 10 to 1 charge to discharge ratio results in a 9.1% hiccup mode duty cycle regardless of at what point a fault condition occurs.

OVP fault immediately sets the fault latch causing SS/DEL to begin to discharge and this fault can only be cleared by cycling power to the IR3094 on and off.

If SS/DEL pin is pulled below 0.8V, the converter can be disabled.

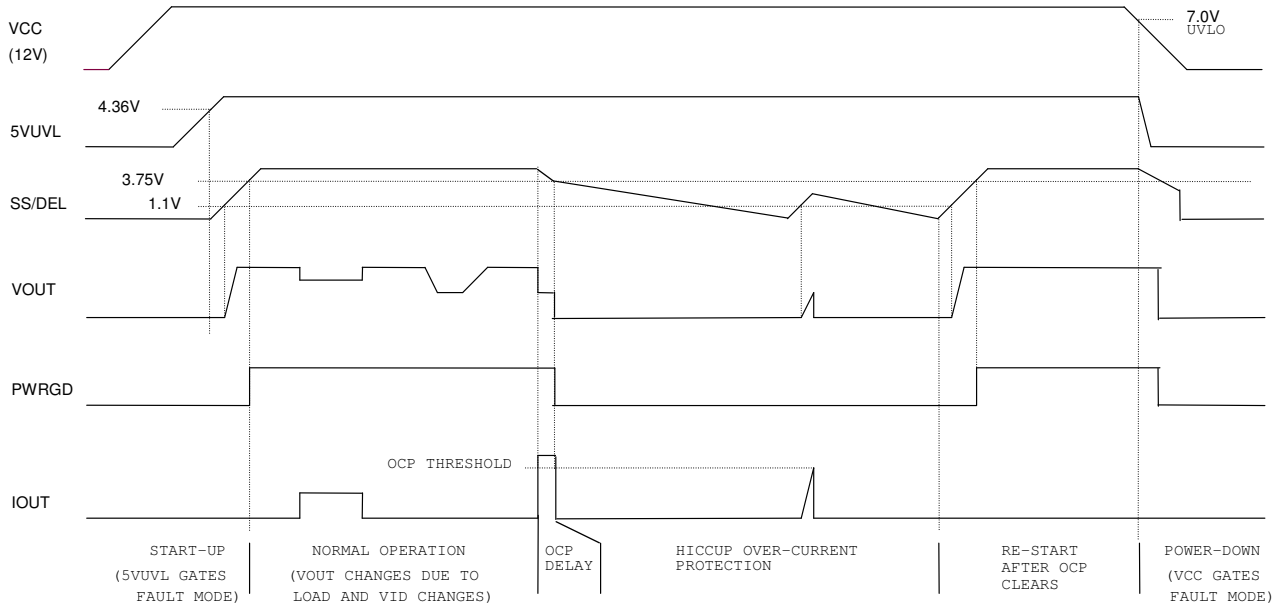


Figure 7 – Operating Waveforms

Soft-start delay time t_{SSDEL} is the time SS/DEL charged up to 1.1V. After that the error amplifier output is released to allow the soft start. The soft start time t_{SS} represents the time during which converter output voltage rises from zero to V_O. t_{SS} can be programmed by C_{SS} using equation (3).

$$C_{SS} = \frac{I_{CHG} * t_{SS}}{V_O} = \frac{60 * 10^{-6} * t_{SS}}{V_O} \qquad (3)$$

Once C_{SS} is chosen, the soft start delay time t_{SSDEL}, the over-current fault latch delay time t_{OCDEL}, and the delay time t_{VccPG} from output voltage (V_O) in regulation to Power Good are fixed and shown in equation (4), (5) and (6) respectively.

$$t_{SSDEL} = \frac{C_{SS} * \Delta V}{I_{CHG}} = \frac{C_{SS} * 1.1}{60 * 10^{-6}} \quad (4)$$

$$t_{OCDEL} = \frac{C_{SS} * \Delta V}{I_{DISCHG}} = \frac{C_{SS} * 0.25}{61 * 10^{-6}} \quad (5)$$

$$t_{VccPG} = \frac{C_{SS} * \Delta V}{I_{CHG}} = \frac{C_{SS} * (3.75 - V_O - 1.1)}{60 * 10^{-6}} \quad (6)$$

VREF Compensation Network R_{REF} and C_{REF}

A RC network tied between VREF pin and VOSENS- is needed to compensate VREF circuit. VREF should come up earlier than SS/DEL pin charged up to 3.75V. For save estimation, use half of the soft start time that is 0.5*t_{SS} as the VREF voltage establishing time. Use equation (7) and (8) to determine R_{REF} and C_{REF} where VREF source current I_{SOURCE} is determained by R_{ROSC} and can be found using the curve in the TYPICAL OPERATING CHARACTERISTICS section.

$$C_{REF} = \frac{I_{SOURCE} * 0.5 * t_{SS}}{V_{REF}} \quad (7)$$

$$R_{REF} = 0.5 + \frac{3.2 * 10^{-15}}{C_{REF}^{\ 2}} \quad (8)$$

Over Current Protection (OCP)

The current limit threshold is set by a resistor connected between the OCSET and VREF pins. If the average Current Sense Amplifier output plus VREF voltage exceeds the OCSET voltage, the over-current protection is triggered.

A delay is included if an over-current condition occurs after a successful soft-start sequence. This is required since over-current conditions can occur as part of normal operation due to load transients. If an over-current fault occurs during normal operation, the Over Current Comparator will initiate the discharge of the capacitor at SS/DEL but will not set the fault latch immediately. If the over-current condition persists long enough for the SS/DEL capacitor to discharge below the 245mV offset of the delay comparator, the Fault latch will be set pulling the Error Amplifier's output low inhibiting switching in the phase ICs and de-asserting the PWRGD signal. The hiccup mode duty cycle of over current protection is determined by the fixed 10:1 ratio of the charge to discharge current.

The inductor DC resistance R_L is utilized to sense the inductor current. The current limit threshold is set by a resistor R_{OCSET} connected between the OCSET and VREF pins, as shown in Fig6. I_{LIMIT} is the required over current limit. I_{OCSET}, the bias current of OCSET pin, is set by R_{ROSC} and is determined by the curve in the Typical Operating Characteristics Section. OCP need to satisfy the high temperature condition. R_{L_MAX} and R_{L_ROOM} are the inductor DCR at maximum temperature T_{L_MAX} and room temperature $T_{_ROOM}$ respectively, the maximum inductor DCR can be calculated from Equation (9)

$$R_{L_MAX} = R_{L_ROOM} * [1 + 3850 * 10^{-6} * (T_{L_MAX} - T_{ROOM})] \quad (9)$$

The current sense amplifier gain of IR3094 decreases with temperature at the rate of 1400 PPM, which compensates part of the inductor DCR increase. The minimum current sense amplifier gain at the maximum IC temperature T_{IC_MAX} is calculated from Equation (10).

$$G_{CS_MIN} = G_{CS_ROOM} * [1 - 1400 * 10^{-6} * (T_{IC_MAX} - T_{ROOM})] \quad (10)$$

R_{OCSET} can be calculated by the following equation (11).

$$R_{OCSET} = (\frac{I_{LIMIT}}{3} * R_{L_MAX}) * G_{CS_MIN} / I_{OCSET} \quad (11)$$

Output Voltage Droop

In some of the applications, output voltage droop is needed to minimize output voltage deviations during load transients and reduce power dissipation of the load when it is drawing maximum current.

The voltage at the VDRP pin is an average of three phase Current Sense Amplifiers and represents the sum of the VREF voltage and the average inductor current of all the phases. The VDRP pin is connected to the FB pin through the R_{DRP} resistor, see figure 6. The Error Amplifier forces the voltage on the FB pin to equal VREF through the power supply loop therefore the current through RDRP is equal to (VDRP-VREF) / R_{DRP}. As the load current increases, the VDRP voltage increases accordingly which results in an increase in R_{FB} current, positioning the output regulated voltage lower thus making the output voltage reduction proportional to an increase in load current. The droop impedance or output impedance of the converter can thus be programmed by the resistor R_{DRP}. The offset and slope of the converter output impedance are independent of the VREF voltage.

The VDRP pin voltage represents the average current of the converter plus the 0.84V reference voltage. The load current can be retrieved by subtracting the VREF voltage from the VDRP voltage.

The converter voltage will be lowered by $R_O * I_O$, where R_O is the required output impedance of the converter. R_{DRP} is determined by Equation (12)

$$R_{DRP} = \frac{R_{FB} * R_{L_MAX} * G_{CS_MIN}}{n * R_O} \quad (12)$$

Lossless Average Inductor Current Sensing

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor. The equation of the sensing network is,

$$v_C(s) = v_L(s)\frac{1}{1 + sR_SC_S} = i_L(s)\frac{R_L + sL}{1 + sR_SC_S} \quad (13)$$

Usually the resistor Rcs and capacitor Ccs are chosen so that the time constant of Rcs and Ccs equals the time constant of the inductor which is the inductance L over the inductor DCR. If the two time constants match, the voltage across Ccs is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of R_L was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak-to-average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak-to-average errors.

Measure the inductance L and the inductor DC resistance R_L. Pre-select the capacitor C_{CS} and calculate R_{CS} as follows.

$$R_{CS} = \frac{L/R_L}{C_{CS}} \qquad (14)$$

Inductor DCR Temperature Correction

If the Current Sense Amplifier temperature dependent gain is not adequate to compensate the inductor DCR TC, a negative temperature coefficient (NTC) thermistor can be added. The thermistor should be placed close to the inductor and connected in parallel with the feedback resistor, as shown in Figure 8. The resistor in series with the thermistor is used to reduce the nonlinearity of the thermistor.

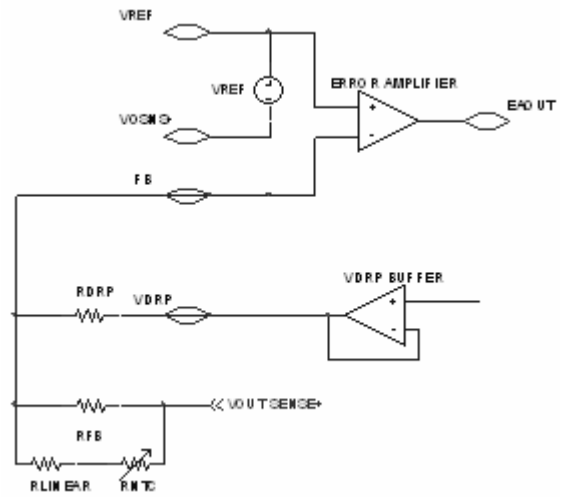


Figure 8 - Temperature compensation of inductor DCR

Remote Voltage Sensing

To compensate for impedance in the ground plane, the VOSNS- pin is used for remote sensing and connects directly to the load. The VREF voltage is referenced to VOSNS- to avoid additional error terms or delay related to a separate differential amplifier. The capacitor connecting the VREF and VOSNS- pins ensure that high speed transients are fed directly into the Error Amplifier without delay.

Master-Slave Current Share Loop

Current sharing between phases of the converter is achieved by a Master-Slave current share loop topology. The output of the Phase 1 Current Sense Amplifier sets the reference for the Share Adjust Error Amplifiers. Each Share Adjust Error Amplifier adjusts the duty cycle of its respective PWM Ramp and to force its input error to zero compared to the master Phase 1, resulting in accurate current sharing.

The maximum and minimum duty cycle adjust range of Ramps 2 & 3 compared to Ramp1 has been limited to a minimum of 0.5x and a maximum of 2.0x typical (see Figure 3.). The crossover frequency of the current share loop can be programmed with a capacitor at the SCOMPX pin so that the share loop does not interact with the output voltage loop.

The SCOMPX capacitor is driven by a trans-conductance stage capable of sourcing and sinking 22uA. The duty cycle of Ramps 2 & 3 inversely tracks the voltage on their SCOMPX pin; if V(SCOMP2) increases, Ramp2's slope will increase and the effective duty cycle will decrease resulting in a reduction in Phase 2's output current. Due to the limited 22uA source current, an SCOMPX pre-conditon circuit has been included to pre-condition V(SCOMPX) so that the duty cycle of Ramps 2 & 3 are equal to Ramp1 prior to any GATEHX high pulses. The pre-condition circuit can source/sink 360uA. The SYNC LATCH (see Figure 1) releases the pre-condition circuit once FB reaches 78% of VREF.

Set BIASOUT voltage

BIASOUT pin provides a 150mA open-loop regulated voltage for GATE drive bias. The voltage is set by SETBIAS through an external resistor Rset connecting between SETBIAS pin and ground. Bias current $I_{SETBIAS}$ is a function of ROSC. Rset is chosen by equation (15). V_{FD} in the equation is the forward voltage drop across the Bootstrap diode.

$$R_{SET} = \frac{V_{BIASOUT} + V_{FD}}{I_{SETBIAS}} \qquad (15)$$

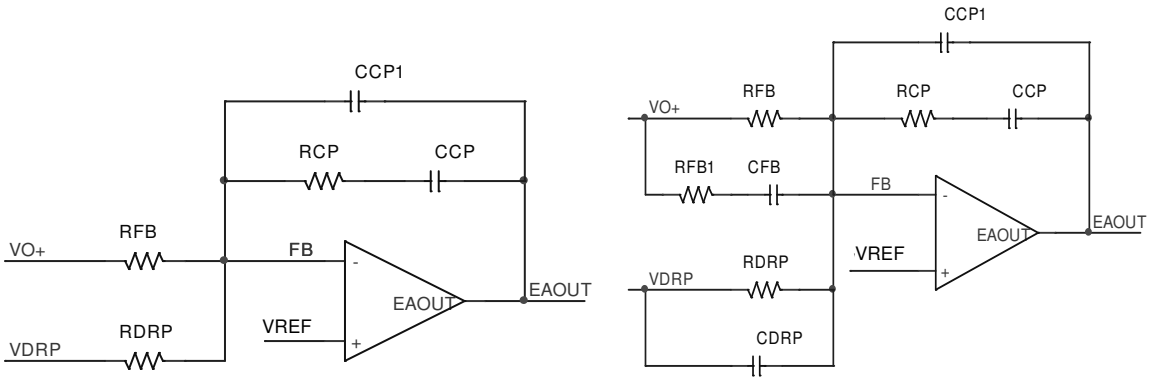
Compensation of the Current Share Loop

The crossover frequency of the current share loop should be at least one decade lower than that of the voltage loop in order to eliminate the interaction between the two loops. A 22nF capacitor from SCOMP to LGND is good for most of the applications. If necessary have a resistor in series with the Csc to make the current loop a little bit faster.

Compensation of Voltage Loop

The selection of compensation types depends on the output capacitors used in the converter. For the applications using Electrolytic, Polymer or AL-Polymer capacitors and running at lower frequency, type II compensation shown in Figure 9(a) is usually enough. While for the applications using only ceramic capacitors and running at higher frequency, type III compensation shown in Figure 9(b) is preferred.

For applications without voltage droop, the compensation is the same as for the regular voltage mode control. For converter using Polymer, AL-Polymer, and ceramic capacitors, which have much higher ESR zero frequency, type III compensation is required as shown in Figure 9(b) with R_{DRP} and C_{DRP} removed.



(a) Type II compensation (b) Type III compensation

Figure 9. Voltage loop compensation networks

Type II Compensation for Voltage Droop Applications

Determine the compensation at no load, the worst case condition. Choose the crossover frequency fc between 1/10 and 1/5 of the switching frequency per phase. Assume the time constant of the resistor and capacitor across the output inductors matches that of the inductor, and determine R_{CP} and C_{CP} from (16) and (17), where L_E and C_E are the equivalent inductance of output inductors and the equivalent capacitance of output capacitors respectively.

$$R_{CP} = \frac{(2\pi * f_C)^2 * L_E * C_E * R_{FB} * 5}{V_I * \sqrt{1 + (2\pi * f_C * C * R_C)^2}} \quad (16)$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} \quad (17)$$

C_{CP1} is optional and may be needed in some applications to reduce the jitter caused by the high frequency noise. A ceramic capacitor between 10pF and 220pF is usually enough.

Type III Compensation for Voltage Droop Applications

Determine the compensation at no load, the worst case condition. Assume the time constant of the resistor and capacitor across the output inductors matches that of the inductor, the crossover frequency and phase margin of the voltage loop can be estimated by (18) and (19), where R_{LE} is the equivalent resistance of inductor DCR.

$$f_{C1} = \frac{R_{DRP}}{2\pi * C_E * G_{CS} * R_{FB} * R_{LE}} \quad (18)$$

$$\theta_{C1} = 90 - A\tan(0.5) * \frac{180}{\pi} \quad (19)$$

Choose the desired crossover frequency fc around fc1 estimated by (18) or choose fc between 1/10 and 1/5 of the switching frequency per phase, and select the components to ensure the slope of close loop gain is -20dB /Dec around the crossover frequency. Choose resistor R_{FB1} according to (20), and determine C_{FB} and C_{DRP} from (21) and (22).

$$R_{FB1} = \frac{1}{2} R_{FB} \quad \text{to} \quad R_{FB1} = \frac{2}{3} R_{FB} \tag{20}$$

$$C_{FB} = \frac{1}{4\pi * f_C * R_{FB1}} \tag{21}$$

$$C_{DRP} = \frac{(R_{FB} + R_{FB1}) * C_{FB}}{R_{DRP}} \tag{22}$$

R_{CP} and C_{CP} have limited effect on the crossover frequency, and are used only to fine tune the crossover frequency and transient load response. Determine R_{CP} and C_{CP} from (23) and (24).

$$R_{CP} = \frac{(2\pi * f_C)^2 * L_E * C_E * R_{FB} * 5}{V_I} \tag{23}$$

$$C_{CP} = \frac{10 * \sqrt{L_E * C_E}}{R_{CP}} \tag{24}$$

C_{CP1} is optional and may be needed in some applications to reduce the jitter caused by the high frequency noise. A ceramic capacitor between 10pF and 220pF is usually enough.

Type III Compensation for No Droop Applications

Resistor R_{DRP} and capacitor C_{DRP} are not needed. Choose the crossover frequency fc between 1/10 and 1/5 of the switching frequency per phase and select the desired phase margin θc. Calculate K factor from (25), and determine the component values based on (26) to (30),

$$K = \tan[\frac{\pi}{4} * (\frac{\theta_C}{180} + 1.5)] \tag{25}$$

$$R_{CP} = R_{FB} * \frac{(2\pi * \sqrt{L_E * C_E} * f_C)^2 * 5}{V_I * K} \tag{26}$$

$$C_{CP} = \frac{K}{2\pi * f_C * R_{CP}} \tag{27}$$

$$C_{CP1} = \frac{1}{2\pi * f_C * K * R_{CP}} \tag{28}$$

$$C_{FB} = \frac{K}{2\pi * f_C * R_{FB}} \tag{29}$$

$$R_{FB1} = \frac{1}{2\pi * f_C * K * C_{FB}} \tag{30}$$

MathCAD file to estimate the power dissipation of the IC

The full featured Control IC IR3094 contain both Control and 3 phase Gate Drive functions. It also has the adjustable voltage bias regulator inside to provide MOSFET Drive Voltage. For the thermal consideration, this Mathcad file step by step shows how to estimate the power dissipation of IR3094 .

Initial Conditions:

No.of Phases: $n := 3$

IC Supply Voltage: $Vcc := 12 \ (V)$, IC Supply Current(quiescent): $Icq := 35 \ (mA)$

Total High side Driver VCCH supply current(quiescent): $Iqh := 5 \cdot n \ (mA)$

Total Low side Driver VCCL supply Current(quiescent): $Iql := 5 \cdot n \ (mA)$

Biasout Voltage: $Vbias := 7.5 \ (V)$

Switching Frequency per phase: $fsw := 450 \ (kHz)$

Thermal Impedance of IC: $\theta_{JA} := 27$ (°C/W)

The data from the selected MOSFETs:

ControI FET IR6637, Number of Control FET per phase: $nc := 1$

Control FET total gate charge: $Qgc := 15 \ (nC)$

Synchronous FET IR6612, Number of sync. FET per phase: $ns := 1$

Sync FET total gate charge: $Qgs := 45 \ (nC)$

Power Dissipation:

The IC will have less power dissipation if using external gate driver supply. For the worst case estimation, assuming using the bias regulator for all the gate drive supply voltage.

1. Quiescent Power dissipation

Total Quiescent Power Dissipation:

$$Pq := (Icq + Iqh + Iql) \cdot Vcc \cdot 10^{-3} \qquad Pq = \quad (W)$$

2. The Power Loss to drive the gate of the MOSFETs

With the assumption of the low MOSFET gate resistances, most gate drive losses are dissipated in the driver circuit.

$$Pdrv := Vbias \cdot fsw \cdot 10^{3} \cdot n \cdot \left[(nc \cdot Qgc + ns \cdot Qgs) \cdot 10^{-9}\right] \qquad Pdrv = \quad (W)$$

Where the $Ig := fsw \cdot 10^{3} \cdot n \cdot (nc \cdot Qgc + ns \cdot Qgs) \cdot 10^{-9}$ term in the equation gives the total average bias current required to drive all the MOSFETs.

3. The bias regulator Power Loss to supply driving the MOSFETs

$$Preg := (Vcc - Vbias) \cdot Ig \qquad Preg = \quad (W)$$

4. Total Power Dissipation of the IC:

$$Pdiss := Pq + Pdrv + Preg \qquad Pdiss = \quad (W)$$

And the total Junction temperature rising is: $Pdiss \cdot \theta_{JA} =$ (°C)

LAYOUT GUIDELINES

The following layout guidelines are recommended to reduce the parasitic inductance and resistance of the PCB layout, therefore minimizing the noise coupled to the IC. Refer to the schematic in Figure 6 – System Diagram.

- Dedicate at least one inner layer of the PCB as power ground plane (PGND).

- The center pad of IC must be connected to ground plane (PGND) using the recommended via pattern shown in "Package Dimensions".

- The IC's PGND1, 2, 3 and LGND should connect to the center pad under IC.

- The following components must be grounded directly to the LGND pin on the IC using a ground plane on the component side of PCB: CSS, RSC2, RSC3, RSET, CVCC and C5VREF. The LGND should only be connected to ground plan on the center pad under IC

- Place the decoupling capacitors CVCC and CBIAS as close as possible to the VCC and VCCL1_2, VCCL3 pins. The ground side of CBIAS should not be connected to LGND and it should directly ground through vias.

- The following components should be placed as close as possible to the respective pins on the IC: RROSC, ROCSET, CREF, RREF, CSS, CSC2, RSC2, CSC3, RSC3, RSET.

- Place current sense capacitors CCS1, 2, 3 and resistors RCS1, 2, 3 as close as possible to CSINP1, 2, 3 pins of IC and route the two current sense signals in pairs connecting to the IC. The current sense signals should be located away from gate drive signals and switch nodes.

- Use Kelvin connections to route the current sense traces to each individual phase inductor, in order to achieve good current share between phases.

- Place the input decoupling capacitors closer to the drain of top MOSFET and the source of the bottom MOSFET. If possible, Use multiple smaller value ceramic caps instead of one big cap, or use low inductance type of ceramic cap, to reduce the parasitic inductance.

- Route the high current paths using wide and short traces or polygons. Use multiple vias for connections between layers.

- The symmetry of the following connections from phase to phase is important for proper operation:
  - The Kelvin connections of the current sense signals to inductors.
  - The gate drive signals from the IC to the MOSFETS.
  - The polygon shape of switching nodes.

PCB AND STENCIL DESIGN METHODOLOGY

- 7x7
- 48 Lead
- 0.5mm pitch MLPQ

See Figures 10-12.

PCB Metal Design (0.5mm Pitch Leads)

1. Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.
2. Lead land length should be equal to maximum part lead length + 0.2 mm outboard extension + 0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
3. Center pad land length and width should be = maximum part pad length and width. However, the minimum metal to metal spacing should be ≥ 0.17mm (2 oz. Copper, ≥ 0.23mm for 3 oz. Copper and ≥ 0.1mm for 1 oz. Copper)
4. Sixteen 0.30mm diameter vias shall be placed in the pad land spaced at 1.2mm, and connected to ground to minimize the noise effect on the IC, and to transfer heat to the PCB.

PCB Solder Resist Design (0.5mm Pitch Leads)

1. Lead lands. The solder resist should be pulled away from the metal lead lands by a minimum of 0.060mm. The solder resist mis-alignment is a maximum of 0.050mm and it is recommended that the lead lands are all NSMD. Therefore pulling the S/R 0.060mm will always ensure NSMD pads.
2. The minimum solder resist width is 0.13mm, therefore it is recommended that the solder resist is completely removed from between the lead lands forming a single opening for each “group” of lead lands.
3. At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
4. Land Pad. The land pad should be SMD, with a minimum overlap of the solder resist onto the copper of 0.060mm to accommodate solder resist mis-alignment. In 0.5mm pitch cases it is allowable to have the solder resist opening for the land pad to be smaller than the part pad.
5. Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.
6. The single via in the land pad should be tented with solder resist 0.4mm diameter, or 0.1mm larger than the diameter of the via.

Stencil Design (0.5mm Pitch Leads)

1. The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
2. The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.
3. The center land pad aperture should be striped with 0.25mm wide openings and spaces to deposit approximately 50% area of solder on the center pad. If too much solder is deposited on the center land pad the part will float and the lead lands will be open.
4. The maximum length and width of the center land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.

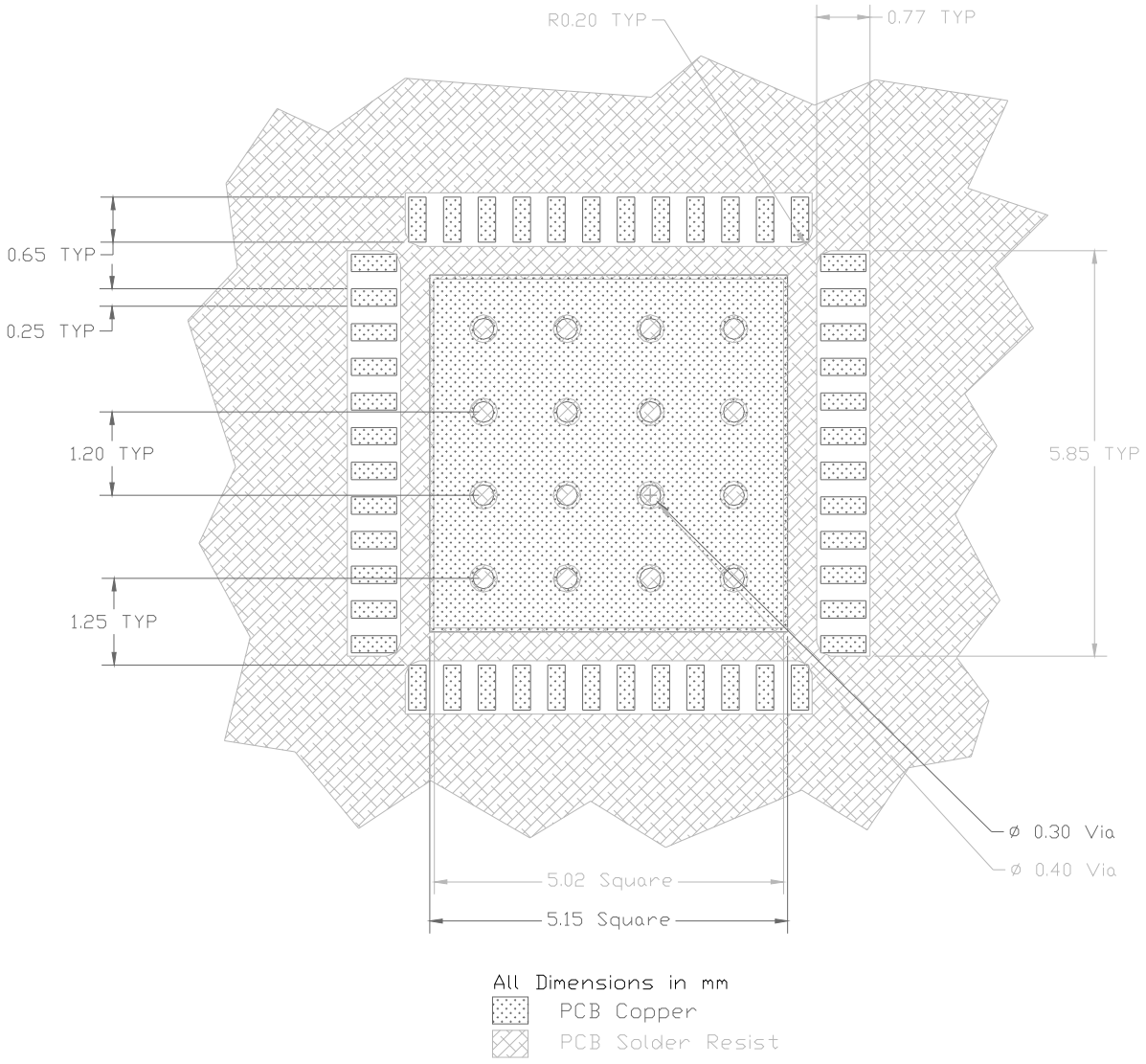


Figure 10. PCB metal and solder resist.

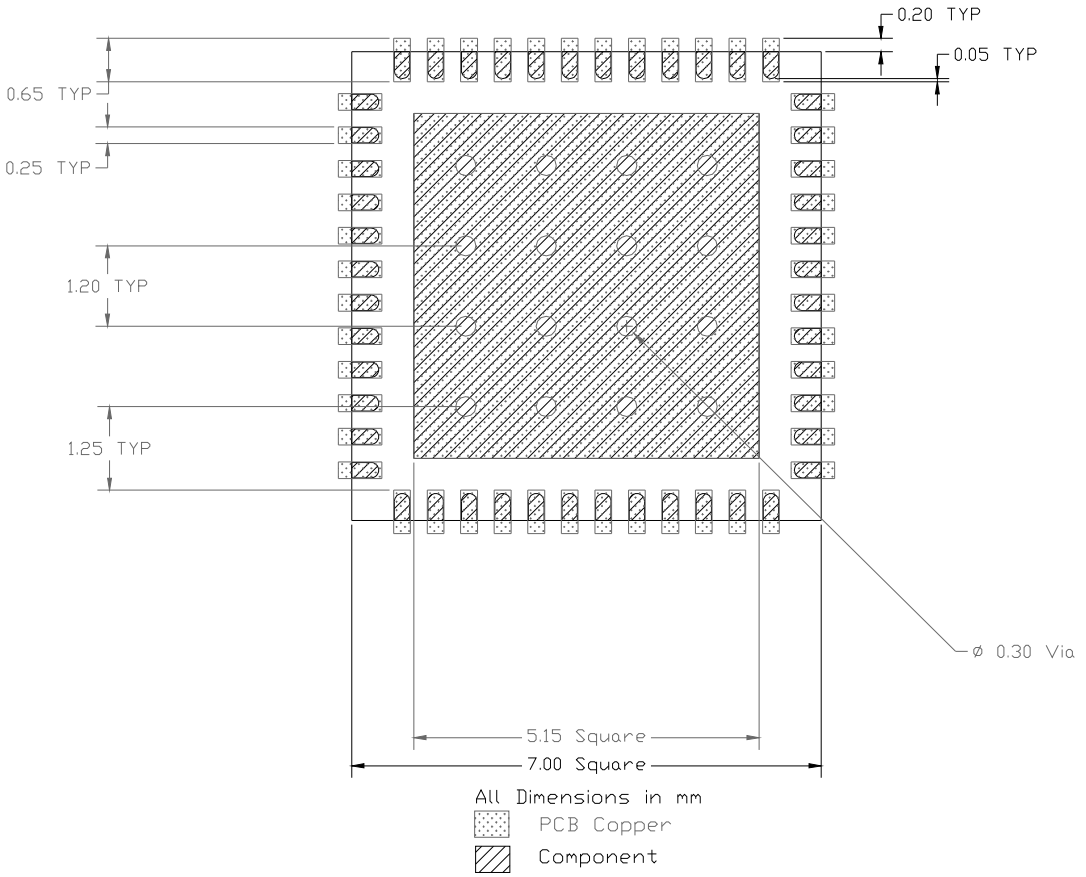


Figure 11. PCB metal and component placement.

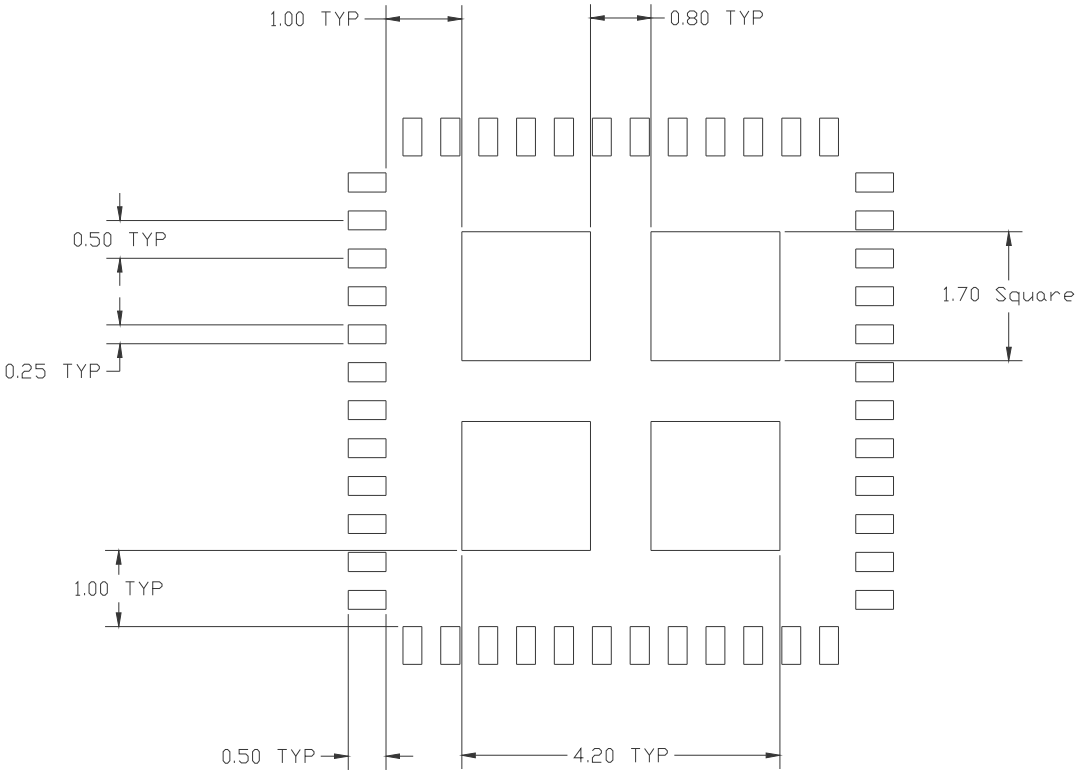
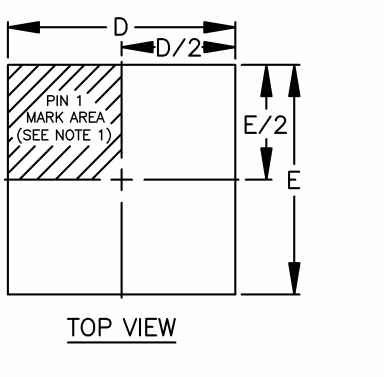
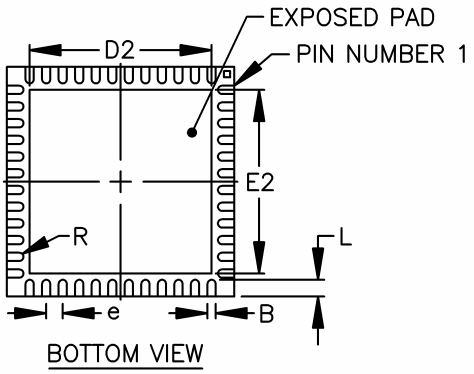
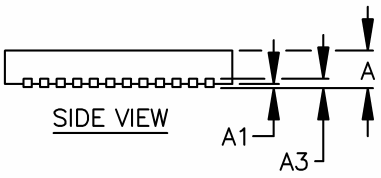


Figure 12. Stencil design.

PACKAGE DIMENSIONS







NOTE 1: DETAILS OF PIN #1 ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE IDENTIFIER MAY BE MOLDED OR MARKED FEATURES.

SYMBOL	48–PIN 7X7		
DESIG	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	0.20 REF		
B	0.18	0.25	0.30
D	7.00 BSC		
D2	5.50	5.65	5.80
E	7.00 BSC		
E2	5.50	5.65	5.80
e	0.50 BSC		
L	0.35	0.40	0.45
R	0.09	—	—

NOTE: ALL DIMENSIONS ARE IN MILLMETERS.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

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