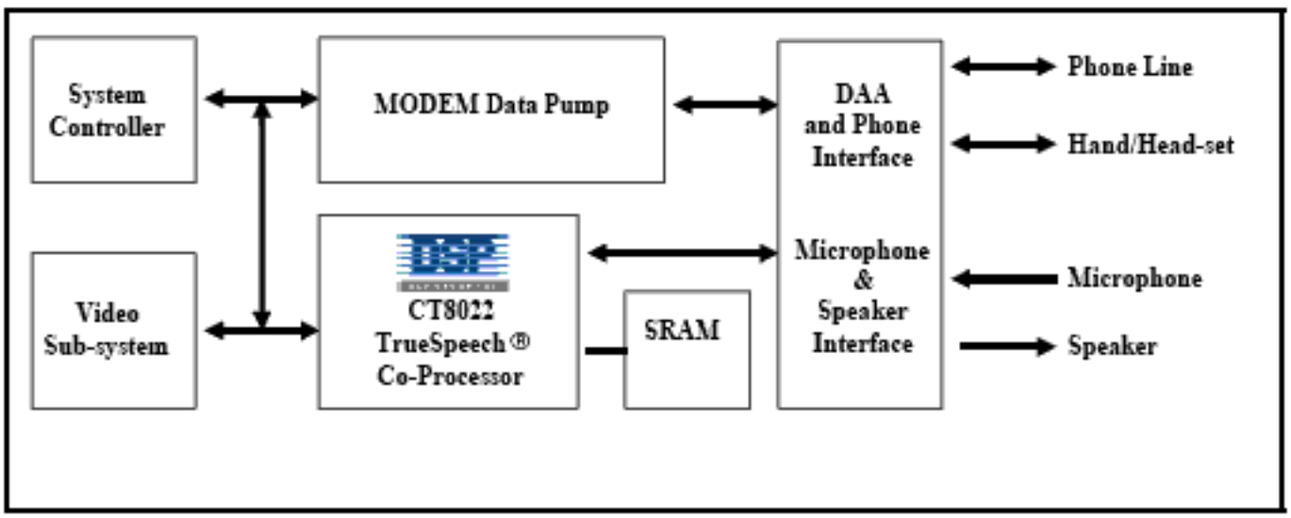
Version: 1.18

DSP GROUP

DATA SHEET

VOIP/VON G.723.1, G729AB TRUESPEECH® CO-PROCESSOR



CT8022 System Block Diagram

DESCRIPTION

The CT8022 is a speech co-processor which performs full-duplex speech compression and de-compression functions. It provides speech compression for H.323 and H.324 Multimedia Visual Telephony/Video Conferencing products and DSVD modems. The CT8022 has built-in TrueSpeech® 8.5 (compatible with Microsoft Sound System 2.0, and a standard part of Microsoft Windows® 95), and TrueSpeech® G.723.1 (for H.323 and H.324). This combination of ITU speech compression standards within a single device enables the creation of a single multimedia terminal, which can operate in all types of H.324 POTS-based and H.323 LAN/Internet-based Video Conferencing systems. TrueSpeech® G.723.1 provides compressed data rates of 8.5, 6.3 and 5.3 KBPS and includes G.723.1 Annex A VAD/CNG *silence* compression, which can supply an even lower average bit rate. The CT8022 provides two additional non-ITU TrueSpeech® data rates at 4.8 and 4.1 KBPS. The CT8022 also supports download of additional speech compression software modules to low-cost external memory (e.g. FlexiSpeech®, G.722 and G.729A/B). The CT8022 operates as a microprocessor peripheral device, and can co-exist with other devices such as modem data pump and video compression chipsets. In addition, the CT8022 includes built-in Acoustical Echo Cancellation, which complements the speech compression functions by providing concurrent hands-free operation.

The TrueSpeech® G.723.1 algorithm delivers highly compressed speech without compromising the speech quality. TrueSpeech® G.723.1 at the 6.3 bit-rate has a MOS score of 3.9 for use with the ITU H.324 and H.323 standards.

The CT8022 is an Application Specific Digital Signal Processor, which is controlled by the system's Host processor through a simple Host Interface command protocol. The Host interface supports full-duplex data transfer using DMA as well as Host-interrupt and Host-polling modes. The CT8022 supports two modes of uncompressed speech input/output. In HOST-CODEC mode, one of the external serial CODECs provides the uncompressed speech input/output. In HOST-HOST (CODEC-less) mode, the Host provides the uncompressed speech input/output via the Host interface.

The only additional external component ICs needed to implement these functions are two low cost 8Kx8 or 32Kx8 SRAMs, a CODEC and oscillator crystal circuit.

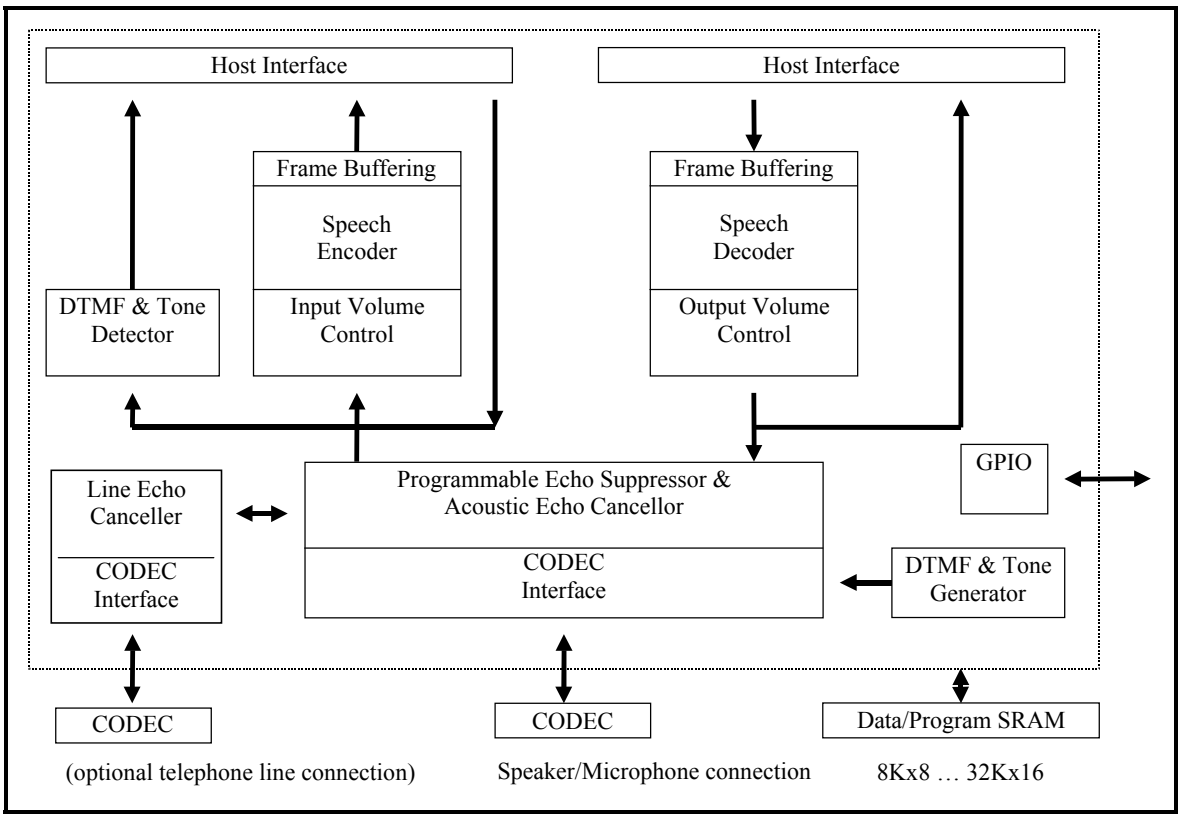
Note: MOS, Mean Opinion Score, is a subjective measure of speech quality where a score of 5 means that the speech quality is Excellent, 4 is Good or Toll Quality (as expected in PSTN), and 3 is fair.

FEATURES

- TrueSpeech® at 8.5, TrueSpeech® G.723.1, 6.3, 5.3, 4.8 and 4.1 KBPS at 8KHz sampling rate (including G.723.1 Annex A VAD/CNG)
- Download of additional speech compression software modules into external SRAM for FlexiSpeech®, G.722 & G.729-A/B
- Real-time Full duplex or Half duplex speech compression and decompression
- Acoustic Echo Cancellation concurrent with full-duplex speech compression
- Full Duplex standalone Speakerphone
- Host-to-Host (CODEC-less) and Host-CODEC modes of operation
- Parallel 8-bit Host interface provides simple memory-mapped I/O Host connection.
- 1 or 2-channel DMA support (Single Cycle and Burst Modes)
- Flexible A-to-D/D-to-A CODEC interface, low cost PCM μ/A-Law and 16-bit Linear
- CODEC interface supports TDM bus connection
- Automatic handling of frame slippage and frame synchronization
- Automatic AGC for message recording
- Speech level detection for silence compression support
- DTMF and Tone Generation
- DTMF and Programmable Tone Detection
- Pass-through modes - 8-bit and 16-bit linear at 8 KHz and 11 KHz (Host programmable CODEC sample rate) and G.711 μ/A-Law
- Power Down and Power Save modes

APPLICATIONS

- Simultaneous Voice and Data Modems
- Teleconferencing and Video Conferencing
- CTI - Computer-Telephony Applications
- Digital Telephony Applications
- Voice Enabled Wireless Terminals
- Real-time compression and de-compression of TrueSpeech 8.5 Windows Sound System and Windows 95 compatible PC speech files
- Store & Forward applications for speech
- Desktop Telephony & Speakerphone
- Internet Telephony Applications



CT8022 Functional Block Diagram

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1 Pinout and Pin Descriptions

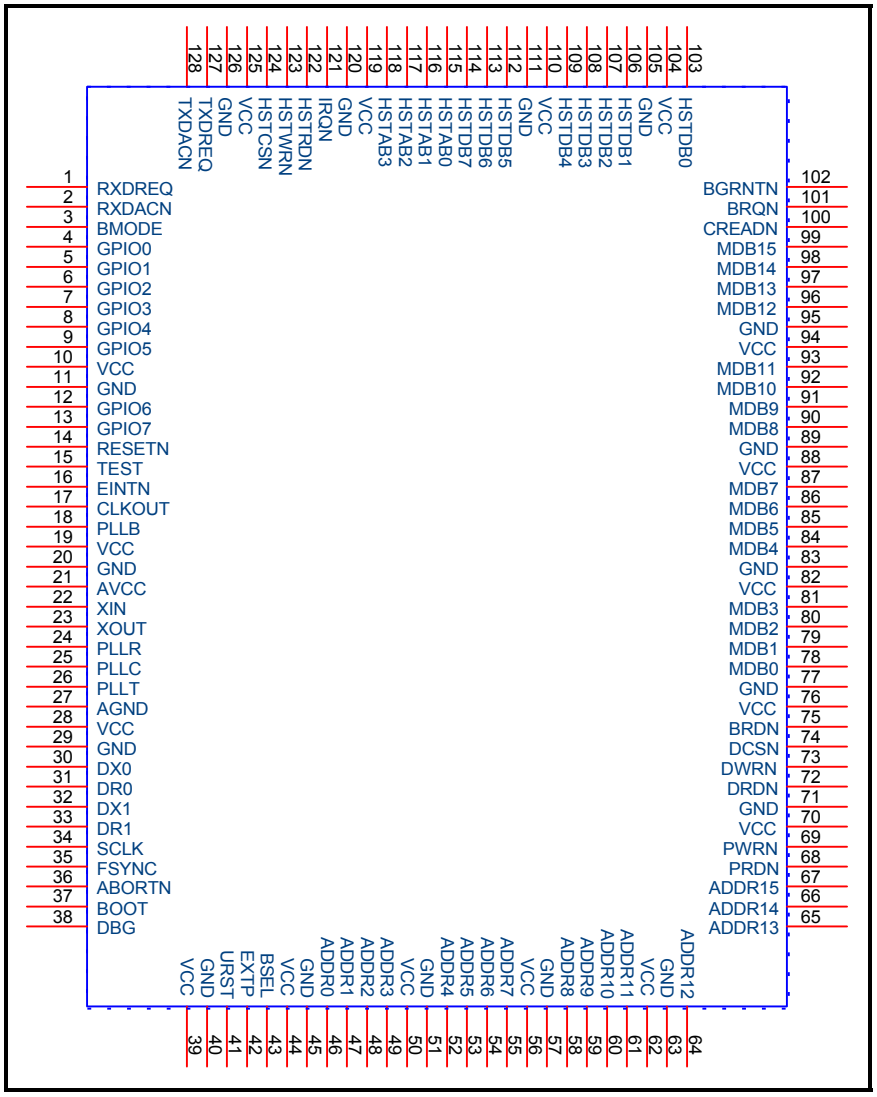


Figure 1-1: 128-Pin PQFP/LQFP

This section contains a list of the CT8022 pins:

Note: The CT8022 is a CMOS device. It is important to make sure that all input pins are connected and have a valid logic level present at all times. Where noted, certain input pins may require external pull-up or pull-down resistors.

Signal naming convention: Active low signals are indicated by a trailing "/" or "N" in the signal name as, for example, SRAMCS/ or SRAMCSN.

Pin Names	Pin Nrs	Type	Function
HSTDB0 HSTDB1 HSTDB2 HSTDB3 HSTDB4 HSTDB5 HSTDB6 HSTDB7	103 106 107 108 109 112 113 114	I/O/Z	Host Data Bus. HSTDB0 is the least significant data bit.
HSTAB0	115	I	HSTAB0 is the least significant Host Address bit. It selects between the high and low byte of the Host interface register selected by HSTAB3-1.
HSTAB1 HSTAB2 HSTAB3	116 117 118	I	Host Address Bus. These address bits are used to select Host interface register addressed by Host (in conjunction with HSTCS/).
HSTRD/ (HSTRDN)	122	I	Host Read signal. Active Low, output enables HSTDB pins, allowing Host to read from the selected Host interface register. The interface register is selected via a decode of HSTAB1-3 if HSTCS/ is active, or the Host Receive Data Buffer access port is selected directly if RXDACK/ is asserted.
HSTWR/ (HSTWRN)	123	I	Host Write signal. Active Low, clocks data from HSTDB pins into selected Host interface register. The interface register is selected via a decode of HSTAB1-3 if HSTCS/ is active, or the Host Transmit Data Buffer access port is selected directly if TXDACK/ is asserted.
HSTCS/ (HSTCSN)	124	I	Host Interface Chip Select. Active Low. This signal gates the HSTWR/ and HSTRD/ and HSTAB3-0 address decode during a Host processor access cycle. The HSTAB3-0 signals should be stable and valid when HSTCS/ is asserted. This signal **must not be asserted** during a DMA cycle on the Host port. **HSTCS/ must be high when either TXDACK/ or RXDACK/ are asserted (low).**
TXDREQ	127	O	Active High signal. DMA transmit request. This signal is asserted to indicate that the device is ready to accept transmit data. Data can be transferred by either DMA or a Host processor access cycle. The Host can enable or disable this signal via the Hardware Control Register. By default, this signal is disabled.
TXDACK/ (TXDACKN)	128	I	Active Low signal. DMA Transmit Acknowledge. This signal is asserted by an external DMA controller on the Host port, together with HSTWR/, to clock a byte from the HSTDB data bus pins into the Host interface Transmit Data Buffer Access port. This signal provides direct access to the Host Transmit Data Buffer Access Port, without involving HSTAB0-3 or HSTCS/. If this signal is not used, it should be connected to VCC via a 10KOhm pull-up resistor. **This signal must not be asserted when either RXDACK/ or HSTCS/ are active**.
RXDREQ	1	O	Active High signal. DMA receive request. This signal is asserted to indicate that the device is ready to provide receive data. Data can be transferred by either DMA or a Host processor access cycle. The Host can enable or disable this signal via the Hardware Control Register. By default, this signal is disabled.
RXDACK/ (RXDACKN)	2	I	Active Low signal. DMA Receive Acknowledge. This signal is asserted by an external DMA controller on the Host port, together with HSTRD/, to accept a receive data byte via the HSTDB data bus pins from the Host interface Receive Data Buffer Access port. This signal provides direct access to the Host Receive Data Buffer Access Port, without involving HSTAB0-3 or HSTCS/. If this signal is not used, it should be connected to VCC via a 10KOhm pull-up resistor. **This signal must not be asserted when either TXDACK/ or HSTCS/ are active**.

Pin Names	Pin Nrs	Type	Function
IRQ/ (IRQN)	121	OC	Interrupt Request. Open collector output (requires external pull-up resistor with min value 1K ohm). This signal is asserted to indicate an interrupt request to the Host controller.
MDB0 MDB1 MDB2 MDB3 MDB4 MDB5 MDB6 MDB7 MDB8 MDB9 MDB10 MDB11 MDB12 MDB13 MDB14 MDB15	78 79 80 81 84 85 86 87 90 91 92 93 96 97 98 99	I/O/Z	External Memory Data Bus used to interface to external memory. The CT8022 requires an external memory configured as 8K or 32K x 16. The 32K x 16 configuration is required for support of downloadable external software modules.
ADDR0 ADDR1 ADDR2 ADDR3 ADDR4 ADDR5 ADDR6 ADDR7 ADDR8 ADDR9 ADDR10 ADDR11 ADDR12 ADDR13 ADDR14 ADDR15	46 47 48 49 52 53 54 55 58 59 60 61 64 65 66 67	O/Z	External Memory Address Bus used to interface to external memory. Note that the CT8022 is a 16-bit device and the address lines indicate access to 16-bit data words.
BSEL	43	O/Z	Byte Select. Used in CT8022 designs to access external byte wide memory.
DRDN	72	O/Z	External Data Memory Read. Active Low, used to indicate a data *read* cycle from external data memory
DWRN	73	O/Z	External Data Memory Write. Active Low, used to indicate a data *write* cycle to external data memory.
PRDN	68	O/Z	External program memory *read*.
PWRN	69	O/Z	External program memory *write*.
CREADN	100	O/Z	Combined external program read and data read. This is equivalent to logical AND combination of PRDN and DRDN. This pin is asserted (active low) whenever an external data or program *read* cycle is executed. Compatibility Note: The CT8020 does not provide this pin. Use this pin instead of DRDN to create a single external combined program/data address space to support external downloadable software modules with the CT8022.
BRDN	75	O/Z	Reserved - NC (do not connect)
DCSN (SRAMCSN)	74	O/Z	External data SRAM chip select. Active low. This signal is asserted during external data access only. This signal is *not* asserted during external program memory *read* or *write* accesses.
RSTN (RESETN)	14	I	Reset signal. Active Low, the pin is driven low to reset the device. **Note - this pin is not a TTL input.** VIH (max) = 4.5 volts. VIL (min) = 1.3 volts. The reset pulse should be a minimum of 10 CLKOUT periods in width (after Vcc has stabilized and a clock is present at XOUT)

Pin Names	Pin Nrs	Type	Function
GPIO0, DATAFLAG\ GPIO1 GPIO2 GPIO3 GPIO4 GPIO5, FR\ GPIO6 GPIO7	4 5 6 7 8 9 12 13	I/O	General-purpose *input/output* pins. For CT8015 compatibility: GPIO 0 may be assigned as DATAFLAG\ (output) GPIO 5 may be assigned as Frame Interrupt, FR\ (output) After and during reset, all the GPIO pins are all configured as inputs. (Compatibility Note: the CT8020 configures GPIO0 and 5 as outputs by default) **Connect 47K ohm pull-down resistors to GND on each GPIO pin to ensure that a valid input signal level is present at all times**.
SCLK	34	I/O	Shift Clock for CODEC interface. During and after reset, this pin is configured as an input. **Connect 47K ohm pull-down resistors to GND to this pin to ensure that a valid input signal level is present at all times.** If an external signal permanently drives this pin, no pull-down is required. The SCLK signal is typically expected to operate at 2.048 MHz. When used as an output (master mode) the SCLK rate is programmable by the Host.
FSYNC	35	I/O	Frame Sync clock for CODEC interface. During and after reset, this pin is configured as an input. **Connect 47K ohm pull-down resistors to GND to this pin to ensure that a valid input signal level is present at all times.** If an external signal permanently drives this pin, no pull-down is required. The FSYNC signal is typically expected to operate at 8 KHz to provide the 8KHz sample clock required by the external serial CODEC. When used as an output (master mode), the FSYNC rate is programmable by the Host.
DX0	30	O/Z	Serial Transmit Data Output for CODEC 0. This output is always high impedance when not transmitting data. This CODEC pin is used for telephone line output in Standalone Speakerphone mode.
DR0	31	I	Serial Receive Data Input for CODEC 0. **Connect 47K ohm pull-down resistors to GND to this pin to ensure that a valid input signal level is present at all times.** Note that CODEC chip output pins typically tri-state when not actually transmitting data. This CODEC pin is used for telephone line input in Standalone Speakerphone mode.
DX1	32	O/Z	Serial Transmit Data Output for CODEC 1. This output is always high impedance when not transmitting data. This is the default CODEC output used for playback.
DR1	33	I	Serial Receive Data Input for CODEC 1 **Connect 47K ohm pull-down resistors to GND to this pin to ensure that a valid input signal level is present at all times.** Note that CODEC chip output pins typically tri-state when not actually transmitting data. This is the default CODEC input used for record.
XIN	22	I	Crystal Input or external oscillator input.
XOUT	23	O	Crystal Output
CLKOUT	17	O	Clock Out = MAINCLOCK/(CLK_RATE+1). This is the internal CT8022 DSP core clock. It is possible to disable the output reduce power consumption. The MAINCLOCK frequency in PLL mode, is the external crystal frequency * 11. In PLL by-pass mode, MAINCLOCK is the external oscillator frequency divided by 2. CLK_RATE is the DSP core clock division factor that the Host controller may program using the ***slow down mode*** command. Note that significant short-term clock jitter may be present on the CLKOUT signal when the PLL is enabled.
TEST	15	I	Reserved - connect to GND.
PLLR PLLC PLLT AVCC(VCC3) AGND(GND3)	24 25 26 21 27	Analog Analog Analog Power Power	PLL support circuitry pins. Connect to external PLL filter circuit. PLL VCC connection PLL GND connection
PLLBYPASS	18	I	Disables internal PLL when high and allows direct use of an external (90.112 MHz) clock applied to the XIN pin. Connect to GND when operating using PLL and external 4.096 MHz crystal.

Pin Names	Pin Nrs	Type	Function
BRQN	101	I	Reserved input, active low. Connect this pin to VCC via a 10KOhm pull-up resistor.
BGRNTN	102	O	Reserved - NC (**do not connect**)
EXTP	42	I	Reserved - connect to GND
BMODE	3	I	Reserved - connect to GND
DBG	38	I	Reserved - connect to GND
ABORTN	36	I	Reserved, active low - connect to VCC via 10 KOhm pull-up resistor.
BOOT	37	I	Reserved - connect to GND
URST	41	I	Reserved - connect to GND
EINTN	16	I	Reserved, active low - connect to VCC via 10 KOhm pull-up resistor.
GND1 GND2 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12 GND13 GND14 GND15 GND16 GND17 GND18	11 20 29 40 45 51 57 63 71 77 83 89 95 105 111 120 126	I	Ground pins
VCC1 VCC2 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18	10 19 28 39 44 50 56 62 70 76 82 88 94 104 110 119 125	I	Power Supply pins

Note **Pins marked *Reserved - NC (no connect)* should be left unconnected. These Reserved pins are outputs; connecting them to either GND or VCC may cause damage to the device. Other pins are marked either *Reserved - connect to GND* or *Reserved - connect to VCC via 10 K ohm pull-up resistor*. These Reserved pins are inputs that require a defined input signal level. They should not be left to *float*. Pins marked as *Reserved* are not intended for active use by the user. However, other devices in the CT8000 series family may use these pins.**

2 External Component Connections

2.1 PLL Circuit

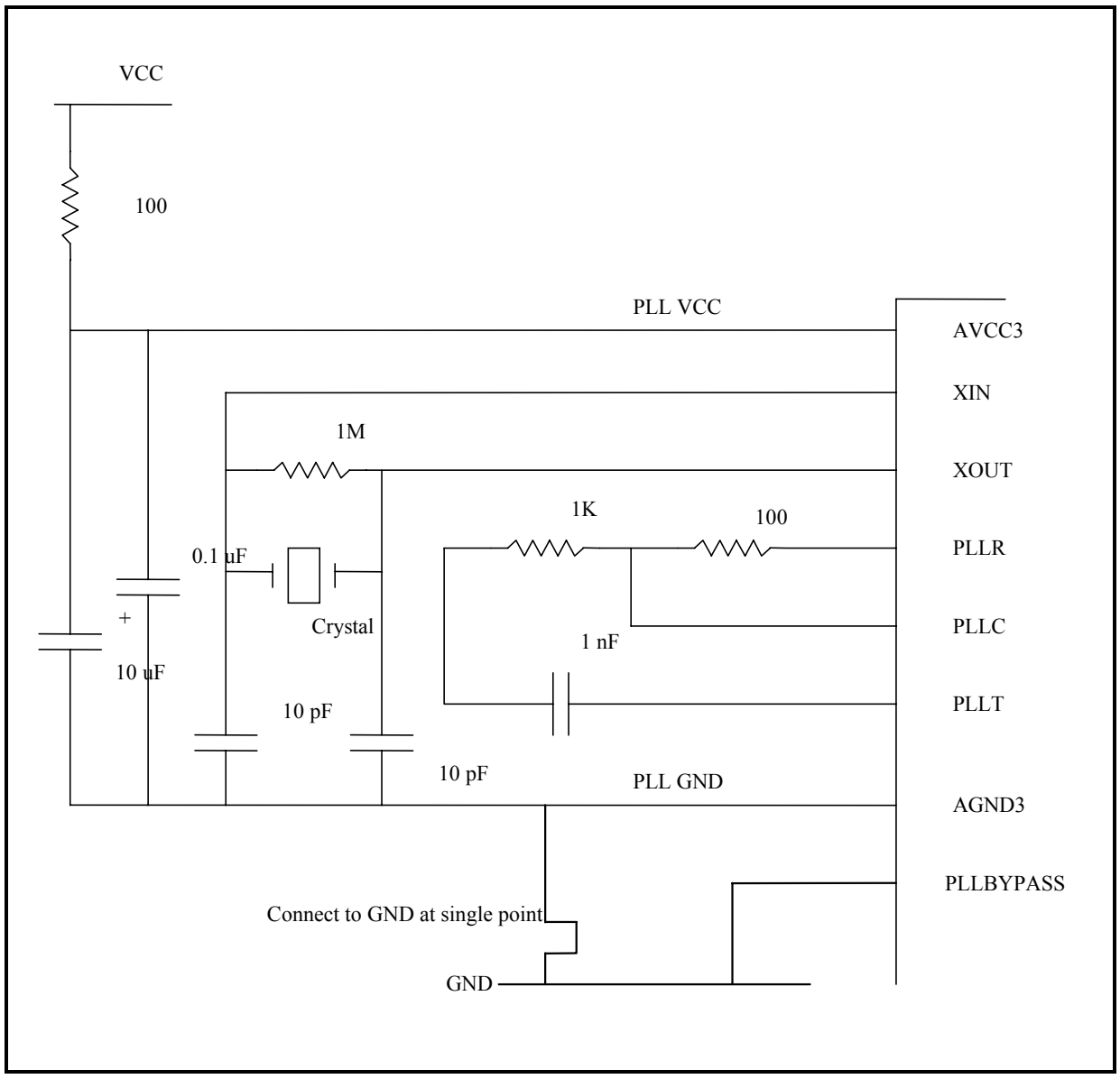


Figure 2-1: PLL Circuit

Crystal frequency is nominal 4.096 MHz. An external 4.096 MHz clock source may replace the Crystal.

2.2 External SRAM CT8022 Connection

All CT8022 configurations require the use of a minimum 8K x 8 external SRAM (32K x 8 is usually less expensive than 8k x 8, and may also be used).

The CT8022 requires an external memory of 8K x 8 for a data only configuration or 32K x 16 for a combined program and data configuration that will support download of external software modules. The first 4K x 16 portion of this memory is used to provide storage for data buffers and other data objects required for normal operation of the device. In the basic data only configuration, the memory is used only for data storage, with execution of code occurring from the CT8022's built-in ROM. This built-in ROM contains all the code required for basic operation of the CT8022, including the G.723.1 and TrueSpeech 8.5 speech compression code.

The CT8022 is capable of expanding the functionality of the device by the addition of external software modules (for example, a software coder module for G.729AB). These software modules require external memory. In the 32K x 16 configuration, only the first 4K words are used as data space with the remainder of the space available for downloaded code.

Refer to the following diagrams.

2.2.1 CT8022 8-Bit External Data Only SRAM Connection

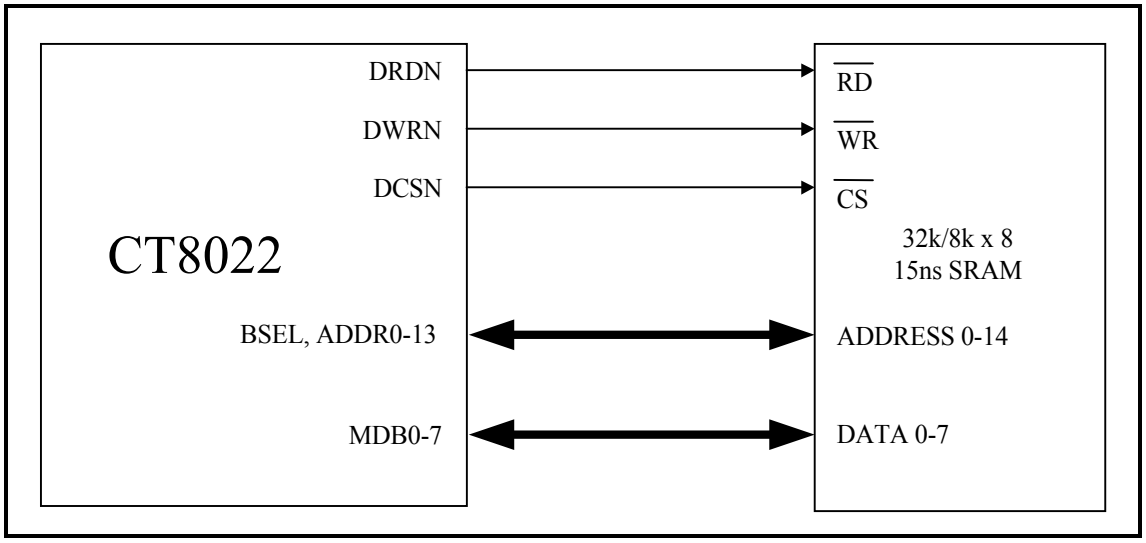


Figure 2-2: External Data Only SRAM Connection

This is the basic external memory configuration showing the CT8022 connected to one external data SRAM chip. This configuration does not support download of external software coder modules.

Note: The BSEL signal is not used in 16-bit wide memory configurations. The connection of the chip select signal DCSN is optional. It is possible to leave the DCSN signal unconnected with the CS input of the SRAM connected to GND.

2.2.2 CT8022 16-Bit Combined Program-Data (Download) SRAM Connection

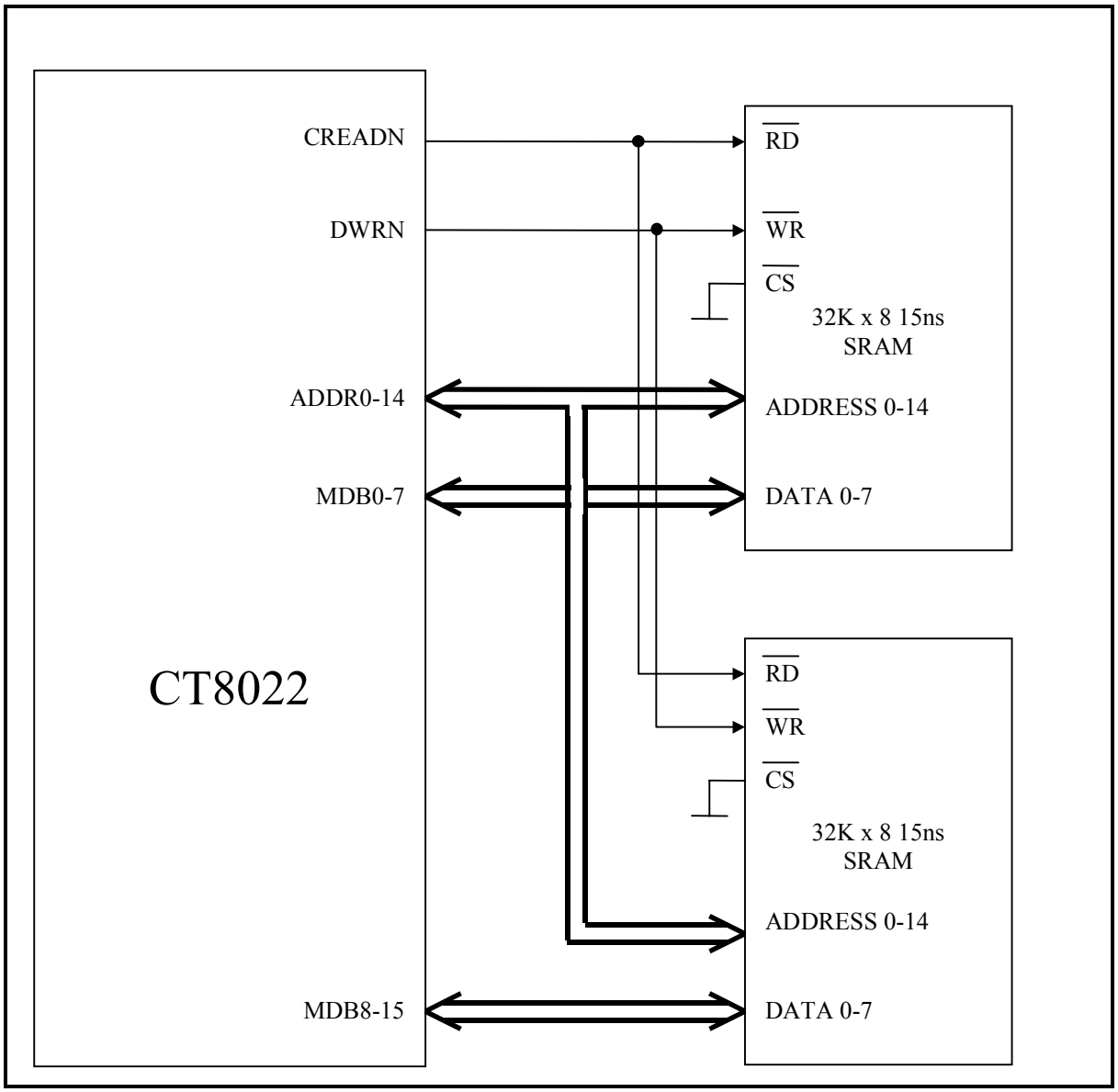


Figure 2-3: External Combined Program-Data SRAM Connection

This is the extended external memory configuration showing the CT8022 connected to two external combined program-data SRAM chips. This configuration supports download of external software coder modules to the combined program-data memory. Use this configuration only if you intend to use the CT8022 with external software coder modules such as TrueSpeech 8.5.

Note: The BSEL signal is not used in 16-bit wide memory configurations.

2.3 CODEC Connection

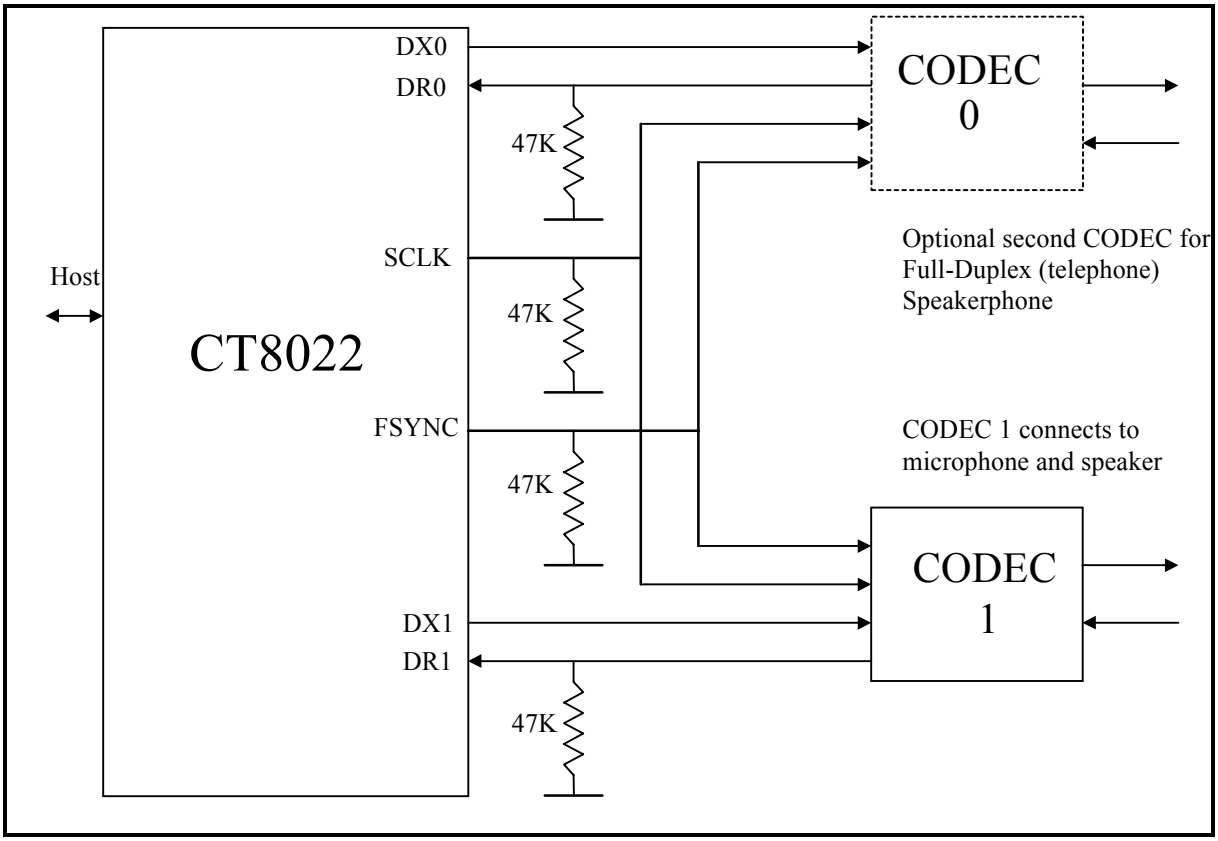


Figure 2-4: CODEC Connection

In Master mode, the CT8022 generates the FSYNC and SCLK signals.

In Slave mode, the FSYNC and SCLK signals are generated externally. In slave mode, the CT8022 FSYNC and SCLK pins are inputs.

Note: During and after reset, the SCLK and FSYNC pins are configured as inputs. As such, they require external pull-down resistors to ensure that a safe and defined logic level is present.

CODEC 0 is required only if *standalone* full-duplex speakerphone operation is desired (e.g. for use as an analog telephone line speakerphone). In this configuration, CODEC 0 connects to the audio input/output of an analog telephone line. CODEC 0 is not required for DSVD/Video Conferencing Speakerphone operation.

For CODEC-less operation, both CODEC0 and CODEC1 may be omitted. In this case, the FSYNC, SCLK, DR0 and DR1 inputs should have pull-down resistors connected to ground to ensure a valid input signal level.

3 Feature Overview

3.1 Introduction

The CT8022 is a full duplex TrueSpeech 8.5 and TrueSpeech G.723.1 real-time speech compression Encoder/Decoder with built-in concurrent echo cancellation. It operates in conjunction with a Host processor and one or two external A-to-D/D-to-A serial CODECs. The Host processor is responsible for managing the bi-directional stream of compressed speech data provided by the CT8022. The CT8022 accepts uncompressed speech in 8-bit A-law/μ-law or 16-bit Linear formats at 64/128 Kbits/sec from the *receive* channel of the external serial CODEC, and compresses the speech to according to the Host-selected format. The compressed speech is passed in frames every 30ms to the Host processor. As the CT8022 is compressing speech, it can concurrently accept compressed speech from the Host for decompression, outputting the uncompressed speech to the *transmit* channel of the external CODEC. The CT8022 supports independent and asynchronous operation of the Host *receive* and *transmit* (compressed) data streams. The *transmit* and *receive* interfaces to the external A-to-D/D-to-A CODEC operate synchronously. The device contains variable depth buffers for each data direction, and provides support of frame deletion and insertion to accommodate sample clock differences between the source and destination devices. The CT8022 can also operate in a CODEC-less mode as a speech compression/decompression accelerator device.

The CT8022 also provides auxiliary telephony functions such as DTMF generation and detection, and Call Progress Tone generation and detection (e.g. dial tone). It is possible to configure the detectors and generators to operate on either the input or the output audio streams (e.g. for detection on DTMF tones in the playback output audio channel).

3.2 Speech Modes

The CT8022 playback (transmit) and record (receive) channels can operate in several different speech modes:

- TrueSpeech G.723.1 6.3/5.3
- TrueSpeech 8.5 (see note 1)
- TrueSpeech 4.8 and 4.1, G.729 Annex A+B (see note 1)
- G.722 (see note 1)
- G.711 A-law/μ-law, 8-bit and 16-bit linear (uncompressed). It is possible to select the mode of operation of the playback and record channel independently of each other.

Speech Coder	Used In
G.723.1 6.3 & 5.3 KBPS	H.324 for video conferencing over dial-up V.34 Modems H.323 multi-media conferencing over LANs and TCP/IP type “packet-data” networks (e.g. Internet)
TrueSpeech 8.5 (1) 8.5 KBPS	DSP Group speech coder built-in to Microsoft Windows 95. Also used in some DSVD Modems and Internet Telephones
TrueSpeech 4.8 & 4.1 4.8/4.1 KBPS	DSP Group proprietary extension of the 6.3/5.3 coder for use in applications requiring lower bit rates (e.g. proprietary non-standard extensions to H.324)
G.729A+B (1) 8 KBPS	optional speech coder used in H.323
G.711 μ-Law/A-Law 64 KBPS	Standard speech compression used in digital telephony systems (e.g. T1/E1)
G.722 64 KBPS (1)	7 KHz Wide bandwidth ADPCM audio coder used in H.320 (ISDN)
16-bit or 8-bit linear uncompressed data 128 or 64 KBPS	Uncompressed audio (e.g. used in Microsoft WAVE files)

Notes:

1. **The CT8022 supports the FlexiSpeech, G.729A+B and G.722 speech coders as external downloadable expansion software modules. These are not built-in to the CT8022 internal program ROM. Use of downloadable expansion software modules requires that the CT8022 be used in conjunction with the appropriate application circuit described in Section 2.2 of this data sheet (with 32K x 16 external SRAMs). All other speech compression functions (G.723.1, TrueSpeech 8.5, 4.8, and 4.1, G.711 and the 8-bit & 16-bit uncompressed modes) are built-in to the CT8022.**

3.3 TrueSpeech

TrueSpeech is a speech compression technology that reduces or compresses the amount of data used to encode a speech waveform. TrueSpeech compression reduces speech sampled (digitized) at 8,000 samples per second, in 16-bit samples (128,000 bits/sec) to 8.5, 6.3, 5.3, 4.8 or 4.1 Kbits/sec with minimal degradation in speech quality. When used with an external G.711 A-law/μ-law CODEC, the CT8022 provides intermediate conversion from G.711 A-law/μ-law to 16-bit linear format prior to the operation of the TrueSpeech function

In the CT8022, uncompressed speech is obtained from an external CODEC operating at 8,000 samples per second. If an external G.711 A-law or μ-law CODEC is used, the speech is sampled by the external CODEC with 14-bits of effective resolution. The G.711 CODEC converts the 14-bits (linear) samples to 8-bit A-law/μ-law for transmission to the CT8022 (at 64,000 bits/sec). The CT8022 receives the speech samples from the CODEC and converts them back to 14-bit linear form. The 14-bit data is converted to 16 bits by appending two zero bits in the least significant bit positions. The 16-bit data is collected into blocks of 240 samples (480 byte) every 30ms and TrueSpeech compressed for transfer to the Host. If an external linear 16-bit CODEC is used, the speech data is sampled with 16-bit resolution and passed directly from the CODEC to the CT8022 at 128,000 bits/sec.

The CT8022 supports simultaneous real-time compression and decompression of TrueSpeech data.

3.4 TrueSpeech 8.5

In TrueSpeech 8.5 mode, speech data is compressed/decompressed into 16-word (32 byte) blocks, which are transferred to or from the Host every 30ms. This corresponds to a data rate of 8,533.33 bits/sec. The CT8022 TrueSpeech 8.5 implementation is compatible with the TrueSpeech 8.5 format used in the CT8005 TrueSpeech Messaging Co-Processor, CT8015 TrueSpeech DSVD Co-Processor and Microsoft Windows Sound System 2.0 and Windows 95 software TrueSpeech CODECs.

3.5 TrueSpeech 6.3 (G.723.1)

The CT8022 implements the final (version 5.1) ITU-T formal release of the G.723.1 speech coder standard, including G.723.1 Annex A VAD/CNG.

In TrueSpeech 6.3 (G.723.1), data is compressed into 12-word blocks. This provides 192 bits per block. However, only 189 bits are used for actual speech data, giving a raw data rate of 6,300 bits/sec. When used in compliance with G.723.1 two of the spare bits are assigned for control information (the 2 least significant bits of the first word of each compressed speech block). The CT8022 G.723.1 implementation includes the optional G.723.1 Annex A VAD/CNG *silence* compression feature (Voice Activity Detection/Comfort Noise Generation). When this feature is enabled, the CT8022 can generate and decode the 4-byte and 1-byte Annex A silence frames. The CT8022 supports dynamic switching between the G.723.1 6.3 and 5.3 rates for both the encoder and decoder. In addition, the G.723.1 6.3 and 5.3 decoders support frame erasure (for corrupt or missing frames) triggered using specially marked data frames.

3.6 TrueSpeech 5.3 (G.723.1)

In TrueSpeech 5.3, data is compressed into 10-word blocks. This provides 160 bits per block. However, only 158 bits per block are used for actual speech data, giving a raw data rate of 5,266.67 bits/sec. When used in compliance with G.723.1, the two *spare* bits are used for control information. The 5.3 rate can be operated in conjunction with the VAD/CNG silence compression feature.

3.7 TrueSpeech 4.8

In TrueSpeech 4.8, data is compressed into 9-word blocks. This provides 144 bits per block. However, only 142 bits per block are used for actual speech data, giving a raw data rate of 4733.33 bits/sec. The 4.8 rate can be operated in conjunction with the VAD/CNG silence compression feature.

3.8 TrueSpeech 4.1

In TrueSpeech 4.1, data is compressed into 8-word blocks. This provides 128 bits per block. However only 124 bits per block are used for actual speech data, giving a raw data rate of 4133.33 bits/sec. The 4.1 rate can be operated in conjunction with the VAD/CNG silence compression feature.

3.9 G.711 μ-law/A-law

The CT8022 is designed to operate with one or two low cost external G.711 μ-law/A-law serial CODECs to provide A-to-D and D-to-A conversion (use of 2 CODECs is required only for standalone analog speakerphone operation). The CT8022 can provide bit-transparent "pass through" access to the serial CODEC data stream. In addition, the CT8022 can also provide volume control (scaling) operating on the G.711 data. G.711 mode is also supported when the CT8022 is used with an external 16-bit linear CODEC, where the CT8022 provides 16-bit linear to G.711 μ-law/A-law conversion.

3.10 G.729 Annex A Downloadable

DSP Group offers an external downloadable expansion software module that can enable the CT8022 to support the G.729 Annex A speech coder that operates at 8 Kbits/sec. The DSP Group implementation of G.729A also includes the G.729 Annex B VAD/CNG *silence* compression feature. G.729A is a reduced complexity version of the earlier G.729 speech coder. The two coders (G.729 and G.729A) are fully inter-operable.

3.11 G.722 Downloadable

DSP Group offers an external downloadable expansion software module that enables the CT8022 to support the G.722 7KHz wideband ADPCM operating at 64 Kbits/sec.

3.12 Automatic Gain Control

In speech record mode (compressed or uncompressed), the CT8022 record process can optionally include an Automatic Gain Control (AGC) function. When this feature is enabled, the CT8022 automatically adjusts the record signal level by internal digital scaling of the input speech signal. The control parameters for the AGC, which include max and min gain (amplification), attack and decay times (response time), are programmable by the Host.

Note: For optimal AEC performance in DSVD mode (videoconferencing), use of the AGC feature concurrently with the Acoustic Echo Canceller is not recommended. However, where the user considers simultaneous use of both AEC and AGC to be necessary, the CT8022 does include a mechanism to reduce the echo amplification effect caused when the AGC gain increases.

3.13 Record and Playback Volume

The CT8022 supports Host programmable record and playback volume controls. This enables internal digital scaling of the input and output speech signal levels. The Host can elect to use fixed level settings during record in situations where AGC operation is not desired (for example, high noise environments). In addition, AGC operation is not appropriate in full duplex speech mode when the Acoustical Echo Canceller (AEC) is active, since the AGC would interfere with the ability of the AEC to operate correctly. In particular, the AGC would operate to amplify the canceled (attenuated) echo signal. Volume control is available in all record and playback modes including G.711μ-law/A-law. In the case of G.711, use of the default 1.0 volume scaling provides bit-transparent pass-though of data from the Host to the external G.711 serial CODEC chip.

3.14 DSVD

Digital Simultaneous Voice and Data is a protocol used to enable collaborative computing where voice conversation and full-duplex data transfers occur simultaneously over a single telephone line via a high speed modem. Since the data transfer rate achievable over a telephone line is limited, speech compression is required to make it possible to send speech simultaneously with data. Applications for DSVD include application sharing, shared whiteboard and interactive games.

3.15 Microsoft Windows® Sound System

In addition to supporting playback and recording of compressed TrueSpeech data, the CT8022 can also playback and record uncompressed data in 16-bit linear, 8-bit linear, 8-bit μ-law and 8-bit A-law formats. The 8-bit linear format supports data in both signed and unsigned form (with or without most significant data bit inversion). This provides true Windows Sound System (WSS) 8 bit ***.wav*** file compatibility. The CT8022 supports 8- and 16-bit 8 KHz, and 11 KHz Microsoft WAVE file mono formats making it an ideal low-cost device for speech enabling personal computers and personal digital assistants (PDAs). The Microsoft WAVE file format also includes support for storing of TrueSpeech 8.5 speech data, making it possible to directly exchange TrueSpeech 8.5 WAVE recordings with WSS compliant PC's. A *software only* TrueSpeech 8.5 encoder/decoder is a standard part of the Sound Recorder application included with Windows® 95.

Note: Sample rates other than 8KHz require that the CT8022 operate with an external A-to-D CODEC capable of supporting the desired sample rate.

3.16 Data Compression/De-Compression Accelerator

The CT8022 can be used as a data compression accelerator. In addition to supporting real-time recording and playback via external CODECs, the CT8022 can operate in a CODEC-less environment where it compresses 16-bit linear speech data from the Host, returning the compressed data to the Host. Simultaneous compression and decompression is supported. This enables the CT8022 to be used in a sound-card type environment where the speech input and output channels are independent of the CT8022.

3.17 DTMF/Tone Generator

The DTMF/Tone generator can generate any single or dual frequency tone in the range of 300Hz to 3KHz. The CT8022 has preset parameters for generating all 16 DTMF digits (0-9, *, #, and the *hidden* digits A, B, C, D) as well as standard USA dial tone, busy signal, and ringing (ringback) tone. The preset parameters can be re-programmed by the Host controller to generate any single or dual frequency tone combination. The relative level (twist) of dual frequency tones can also be selected. The tone generator can be operated concurrently with the record/playback speech operation. Tone generation is performed in the direction of the output speech by default, but can be redirected to the compressed speech path using the loopback configuration.

3.18 Tone Detection

The CT8022 contains a set of four independent programmable call progress tone filters which can be used to detect call progress tones such as dial tone, busy tone, ringing (or ringback) tone and fax calling tone (CNG). The tone detector can be configured to operate on either the incoming (record) data stream or outgoing (playback) data stream. Tone detection can be performed either on the output or on the input speech directions.

3.19 DTMF Detection

The CT8022 includes a DTMF detector that can detect all 16 DTMF digits including the digits ABCD. The tone detector can be configured to operate on either the incoming (*record*) data stream or outgoing (*playback*) data stream. DTMF detection can be performed either in the output or in the input speech directions. This allows detection of DTMF digits in the output audio stream.

3.20 Full Duplex Speakerphone

The CT8022 can operate in either *standalone* speakerphone or in *DSVD* speakerphone mode (for use in a videoconferencing system). In DSVD speakerphone mode, the CT8022 provides Acoustical Echo Cancellation between the speaker and microphone connection, concurrent with speech compression operation. In standalone full-duplex speakerphone mode, Acoustical Echo Cancellation as well as near-end (*electrical*) echo cancellation to the telephone line connection are provided. Standalone speakerphone mode provides support for creating an analog telephone line-based speakerphone.

Unlike many speakerphone implementations, the CT8022 implements a full-duplex speakerphone. In most speakerphones, only one party at a time can speak and, the other party is always muted, sometimes by as much as 50 dB or more. This is *half-duplex speakerphone* operation. In half-duplex operation a speakerphone *listens* to both the microphone and the telephone line inputs and tries to detect which side is speaking. It allows input from the speaking side and mutes input from the other side. If this were not done, acoustical feedback or *howling* would take place. The major problem with a half-duplex speakerphone is that a user experiences *break-up* during the conversation when the speakerphone incorrectly identifies the speaking party (due to noise) or both parties attempt to talk at the same time.

The CT8022 implements a full-duplex speakerphone. This implementation allows both parties to speak and to be heard simultaneously. It does this using DSP technology called *Acoustical Echo Cancellation*.

Acoustical echoing occurs when the speakerphone microphone picks up the audio signal from the speakerphone speaker, *echoing* the output (speaker) signal back along the telephone line. The signal transmitted through the telephone line is also *echoed* by it and output to the speaker again. This creates a *feedback* loop in which the signal from the telephone line is output from the speaker, picked up by the microphone, sent to the telephone line, echoed by the telephone line and re-output by the speaker. This causes *howling* or *howl round*, a loud annoying high-pitched noise. In the CT8022, *howling* is prevented by the use of echo cancellation. This is an adaptive filtering process where the CT8022 compensates for the speaker-to-microphone echo and subtracts the outgoing speaker signal from the incoming microphone signal, reducing or eliminating the acoustic echo. Refer to ***Section 9.21*** for more details on Speakerphone operation.

3.21 Acoustical Echo Cancellation

The CT8022 includes an Acoustical Echo Canceller (AEC) as part of its full-duplex speakerphone feature. In addition to its use in standalone speakerphone mode, the AEC can be operated concurrently with the CT8022 full-duplex speech mode (DSVD mode). This enables the CT8022 to provide acoustic echo cancellation between the speaker and microphone while simultaneously providing full duplex speech compression/decompression. This makes possible hands-free DSVD (DSVD or Video Conferencing Speakerphone) applications avoiding use of a headset or handset for speech input/output. The AEC implementation included in the CT8022 contains features that allow the echo canceller to be used to cancel non-acoustical echoes such as the electrical signal echo from a 2 to 4-wire telephone hybrid. This option supports use of the CT8022 in a digital speech telephony gateway-type application.

3.22 8/16-bit Host Controller Interface

The operation of the CT8022 is controlled via 8 16-bit registers that provide a control/status/data interface. This interface is accessed physically as 16 8-bit wide I/O locations mapped to the Host controller address space. This allows the CT8022 to be used with inexpensive 8-bit micro-controllers or more powerful 16/32 bit microprocessors. The Host controls the CT8022 by writing control words to the CT8022 registers and it obtains status information by reading the CT8022 status registers. Speech data is passed through the receive/transmit buffer registers when recording or playing speech data to or from the Host. *Receive* and *transmit* data buffers are 16 words deep and Host-controllable. In addition, CT8022 provides either single-cycle or continuous (burst) DMA modes for both half-duplex and full-duplex speech transfers.

3.23 CODEC Interface

The CT8022 supports direct connection to one or two external 8-bit G.711 A-law/μ-law or 16-bit Linear CODECs for input and output of audio signals. If two CODECs are used, both CODECs must be of the same type. The CT8022 can act as a CODEC clock master, or it can be driven by an external CODEC clock. In master mode, the CODEC clock SCLK and FSYNC signals are generated by programmable integer division from the internal CT8022 clock.

3.24 CT8022 Crystal

The CT8022 includes a clock frequency multiplying PLL (Phase Locked Loop) to avoid requiring a high frequency external clock source for generation of the internal 45.056 MHz CT8022 clock. The PLL allows generation of the main internal 45.056 MHz DSP core clock from an external 4.096 MHz primary clock or crystal using a x11 multiplication factor. The PLL circuit also includes a by-pass control pin to allow the direct use of an external 2X (90.102 MHz) clock source applied to the XIN pin.

If the PLL is enabled, the CT8022 primary 45.056 MHz clock can be provided either by attaching a 4.096 MHz crystal at XIN/XOUT, or by providing a 4.096 MHz clock input at XIN from an external oscillator. Operation of the PLL is independent of the nature of the primary clock source. If the PLL is disabled, then the clock must be provided by an external 90.102 MHz clock applied at XIN. The XIN-XOUT internal oscillator is not capable of supporting operation with an 90.102 MHz crystal.

Operation of the CT8022 at precisely 45.056 MIPS is needed only if the CT8022 is required to generate CODEC SCLK (master mode) at 2.048 MHz and FSYNC at 8.000 KHz (45.056 MHz = 22 * 2.048 MHz). Selection of the operating frequency of the CT8022 is affected by the desired modes of operation and the desired sample rates. 45.056 MHz is the maximum operating frequency of the CT8022. If concurrent operation of the AEC is not required, the operating frequency may be reduced in order to reduce power consumption.

3.25 Power Save Modes

The CT8022 supports internal clock slow-down modes where the clock rate to the internal DSP core can be reduced. Operation in a slow-down mode affects only the clocks to the CT8022 DSP core. The operation of the CODEC and Host interfaces is not affected by slowing down the DSP core. The CT8022 also has a minimum power mode, where all internal clocks are stopped. The internal clock scaling feature of the CT8022 enables the Host to adjust the available MIPS (and power consumption) to provide just sufficient processing power for the mode of operation used.

The CT8022 supports dynamic clock control, and can be programmed to automatically reduce the clock rate during the idle time between the processing of each speech frame. This enables power to be conserved even when it is not possible to use a lower base clock speed.

4 Host Controller Interface

4.1 8 Or 16-Bit Host Controller Interface

The operation of the CT8022 is controlled via 8 16-bit registers that provide a control/status/data interface. This interface is accessed physically as 16 8-bit wide I/O locations mapped into the Host controller address space. This allows the CT8022 to be used with inexpensive 8 bit micro-controllers or more powerful 16/32-bit microprocessors. The Host controls the CT8022 by writing control words to the CT8022 registers and it obtains status information by reading the CT8022 status registers. Speech data is passed through the *receive*/*transmit* buffer registers when recording or playing speech data to or from the Host. *Receive* and *transmit* data buffers are 16 words deep and Host-controllable. In addition, the CT8022 provides either single-cycle or continuous (burst) DMA modes for both half-duplex and full-duplex speech transfers.

4.2 Host Interface Signals

HSTRDN:	Active low: asserted by the Host to read from the CT8022
HSTWRN:	Active low: asserted by the Host to write to the CT8022
HSTCSN:	Active low: Chip Select, asserted by the Host to enable the HSTRDN, HSTWRN signals
HSTAB3-0:	Host Address lines, select the Host interface register read or written
HSTDB7-0:	8 bit Host data bus to transfer data to/from the CT8022
IRQN:	Active low: Dedicated Host interrupt request (replaces CT8015 ACK signal)
TXDREQ:	TX DMA request (associated with data write buffer)
TXDACKN:	Active low: TX DMA acknowledge
RXDREQ:	RX DMA request (associated with data read buffer)
RXDACKN:	Active low: RX DMA acknowledge

4.3 CT8022 Host Connection With External DMA Controller

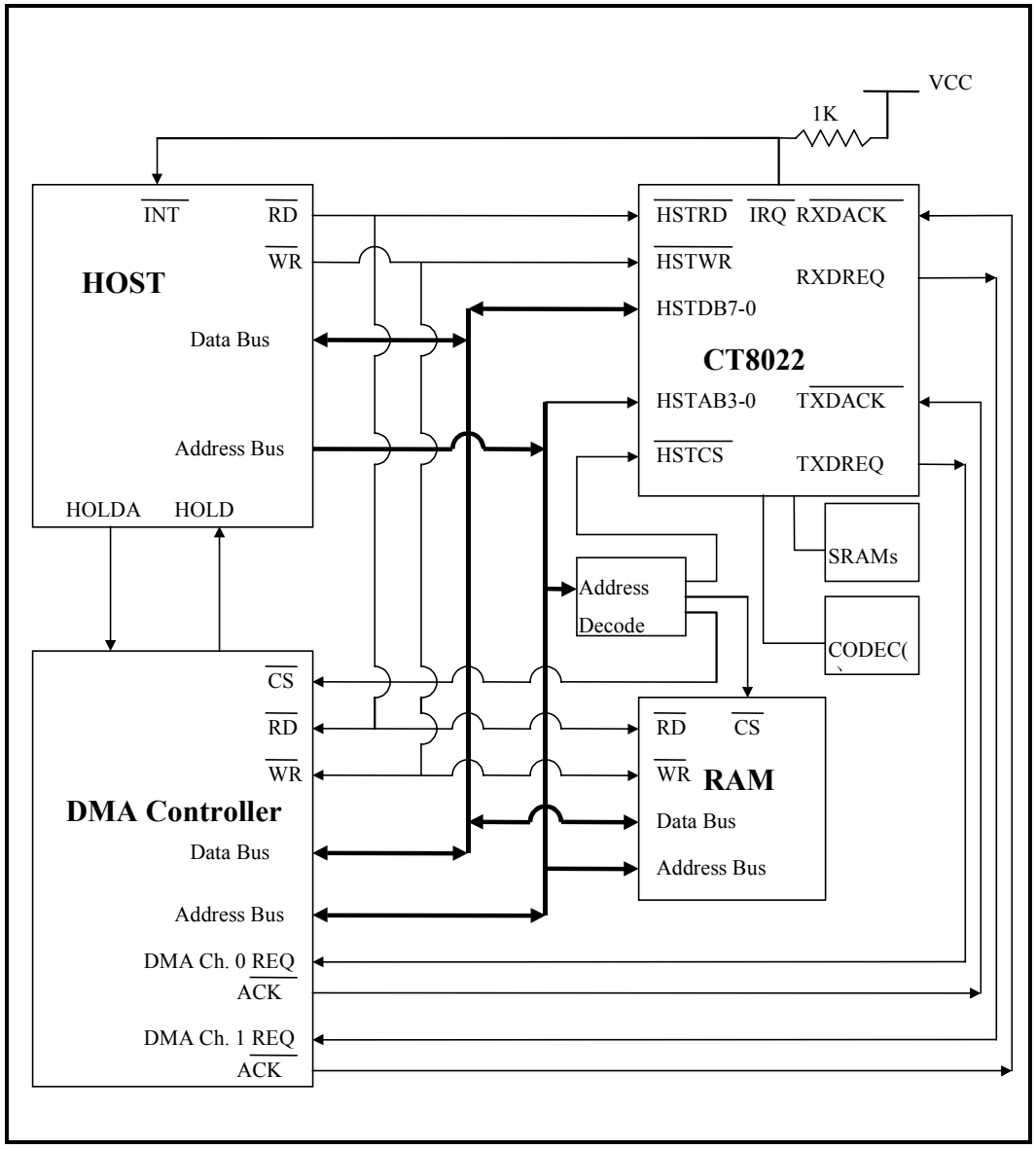


Figure 4-1: CT8022 Connection to Host and External DMA Controller

4.4 Host Programmers Model

Host Byte Address HSTAB3-0	Host Word Address HSTAB3-1	Function	Access
0-1	0	Aux Software Status Register (Reserved)	Read Only
2-3	1	Software Status Register	Read Only
4-5	2	Aux Software Control Register (Reserved)	Read/Write
6-7	3	Software Control Register	Read/Write
8-9	4	Hardware Status Register	Read Only
A-B	5	Hardware Control Register	Read/Write
C-D	6	Host Transmit (Write) Data Buffer Access Port (buffer input)	Write Only
E-F	7	Host Receive (Read) Data Buffer Access Port (buffer output)	Read Only

Note that the CT8022 registers are all internally 16-bits wide. Physical access to these registers is accomplished using two 8-bit access cycles via the Host Interface. The lower byte of each register is accessed when address line HSTAB0 = 0. The upper byte of each register is accessed when address line HSTAB0 = 1. The registers should always be accessed low byte first followed by high byte. Accesses to the upper byte of the Software Status, Software Control, and Data Buffer Access Port Registers trigger certain internal events within the CT8022. For example, reading the upper byte of the Software Status Register clears the Status Ready bit in the Hardware Status Register.

4.5 Register Descriptions

4.5.1 Hardware Control Register

This register has *read/write* access from the Host.

0	0	0	0	0	Host IRQN Master Enable	CONTINUE	DMA Direction
(15)	(14)	(13)	(12)	(11)	(10)	(9)	(8)

TX DMA Burst Mode	RX DMA Burst Mode	TX DMA Enable	RX DMA Enable	Aux Status Update IE	Status Update IE	TX Ready IE	RX Ready IE
(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

TX DMA Burst Mode: When this bit is set, the TX DMA interface operates in Burst Mode. In Burst Mode, the TXDREQ signal is continuously asserted if the TX Ready bit for the Host Transmit buffer is set.
When this bit is clear, the TX DMA interface operates in Single Cycle Mode. In Single Cycle Mode, the TXDREQ signal is de-asserted every time the TXDACKN and HSTWRN signals are asserted, then re-asserted if the TX Ready bit is still set, after a delay (buffer not full). Refer to Section 4.6.

RX DMA Burst Mode: When this bit is set, the RX DMA interface operates in Burst Mode. In Burst Mode, the RXDREQ signal is continuously asserted if the RX Ready bit for the Host Receive buffer is set.
When this bit is clear, the RX DMA interface operates in Single Cycle Mode. In Single Cycle Mode, the RXDREQ signal is de-asserted every time the RXDACKN and HSTRDN signals are asserted, then re-asserted if the RX Ready bit for the Host Receive Buffer is still set, after a delay (buffer not empty). Refer to Section 4.6.

DMA Direction: This field allows the Host to use the DMA features in a full duplex or half duplex configuration. In a half-duplex configuration, the Host needs to interface a single DMA channel to the CT8022, and needs to be able to transfer data in either direction with this single channel. This is accommodated within the CT8022 by permitting the functional exchange of the external (physical) DMA interface pins. Refer to Section 4.6.

0 Normal Direction. The TXDREQ, RXDREQ, TXDACKN and RXDACKN operate in the manner described in the CT8022 pin out. After reset, this bit is set to zero.

1 Reverse Direction. The physical pin functions of TXDREQ and RXDREQ, and also TXDACKN and RXDACKN are exchanged, i.e. the TXDREQ pin assumes the function and behavior of the RXDREQ pin and vice-versa. Refer to Section 4.6.1.2.

TX DMA Enable: Setting this bit to 1 enables the TXDREQ and TXDACKN signals. If this bit is set to zero, the TXDACKN signal is ignored and the TXDREQ signal is not asserted. This control operates on the logical TX DMA signals, not the physical pins whose functions can be exchanged between RX and TX. After reset, this bit is zero.

RX DMA Enable: Setting this bit to 1 enables the RXDREQ and RXDACKN signals. If this bit is set to zero, the RXDACKN signal is ignored and the RXDREQ signal is not asserted. This control operates on the logical RX DMA signals, not the physical pins whose functions can be exchanged between RX and TX. After reset, this bit is zero.

HOST IRQN Master Enable: Setting this bit to 1 enables the IRQN output signal. If this bit is not set the IRQN signal is not asserted. After reset, this bit is zero.

Aux Status Update IE: If this bit is set, the Host IRQN signal is asserted whenever the Aux Status Ready bit in the Hardware Status Register is set. After reset, this bit is zero.

Status Update IE: If this bit is set, the Host IRQN signal is asserted whenever the Status Ready bit in the Hardware Status Register is set. After reset, this bit is zero.

TX Ready IE: If this bit is set, the Host IRQN signal is asserted whenever the TX Ready bit in the Hardware Status Register is set. After reset, this bit is zero.

RX Ready IE: If this bit is set, the Host IRQN signal is asserted whenever the RX Ready bit in the Hardware Status Register is set. After reset, this bit is zero.

CONTINUE: The Host writes a 1 to this bit to clear the COHOST SHUTDOWN bit in the Hardware Status Register. This returns the Host and CODEC logic to normal operation from sleep mode. This bit always reads as a 0.
When COHOST SHUTDOWN is in operation, only the continue bit in the Hardware Control Register is accessible. All other bits are undefined for read and write operations. COHOST SHUTDOWN is a power save state where the CODEC and HOST sections of the CT8022 are disabled in order to reduce power consumption. In this state it is still possible for the CT8022 DSP core to remain active.

4.5.2 Hardware Status Register

This register is *read only* accessible by the Host.

0	0	0	0	0	COHOST SHUTDOWN	TX DMA	RX DMA
(15)	(14)	(13)	(12)	(11)	(10)	(9)	(8)

IRQN Asserted	SYSTEM RESTART	TX Ready	RX Ready	Aux Status Ready	Status Ready	Aux Control Ready	Control Ready
(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

SYSTEM RESTART: Reserved

TX Ready: This bit reflects the state of the TX Ready bit in the DSP's Host Transmit Buffer control register. This bit is set to indicate that the Host Transmit Data Buffer can be accessed by the Host. When the Host writes to the high byte of the Host Transmit Data Buffer access port and the Frame Size limit is reached (buffer full), this bit is cleared. After reset, this bit is clear.
When this bit is set and the TX Ready IE bit in the Hardware Control Register is set, the Host IRQN signal is asserted.

TX DMA: This bit is set if the (logical) TXDREQ signal is asserted. The state of this bit is affected by the TX DMA enable bit in the Host interface hardware control register. If the TX DMA enable is not set, this bit will always be zero.

RX Ready: This bit reflects the state of the RX Ready bit in the DSP's Host Receive Buffer control register. This bit is set to indicate that the Host Receive Data Buffer can be accessed by the Host. When the Host reads from the high byte of the Host Receive Buffer access port, and the Frame Size limit is reached (buffer empty), this bit is cleared. After reset, this bit is clear.
When this bit is set and the RX Ready IE bit in the Hardware Control Register is set, the Host IRQN signal is asserted.

RX DMA: This bit is set if the (logical) RXDREQ signal is asserted. The state of this bit is affected by the RX DMA enable bit in the Host interface hardware control register. If the RX DMA enable is not set, this bit will always be zero.

Status Ready: This bit is set when the Oak core writes to the Software Status Register. When the Host reads the high byte of the Software Status Register, this bit is cleared. After reset, this bit is cleared.
When this bit is set and the Status Ready IE bit in the Hardware Control Register is set, the Host IRQN signal is asserted.

IRQN Asserted: This bit reflects the state of the external IRQN pin. If the IRQN signal is asserted, this bit is set. If the Host IRQN Master Enable is not set, this bit will always be zero.

Control Ready: This bit is set when the Oak core reads from the Software Control Register. When the Host writes to the high order byte of the Software Control Register, this bit is cleared. After reset, this bit is cleared to indicate that the CT8022 is not ready to receive commands. Once the CT8022 is ready to begin communication with the Host, it performs a dummy read of the Software Control Register to set the Control Ready bit.

Aux Status Ready: This bit is set when the Oak core writes to the Aux Software Status Register. When the Host reads the high byte of the Aux Software Status Register, this bit is cleared. After reset, this bit is cleared.
When this bit is set and the Aux Status Ready IE bit in the Hardware Control Register is set, the Host IRQN signal is asserted.

Aux Control Ready: This bit is set when the Oak core reads from the Aux Software Control Register. When the Host writes to the high order byte of the Aux Software Control Register, this bit is cleared. After reset, this bit is cleared to indicate that the CT8022 is not ready to receive commands. Once the CT8022 is ready to begin communication with the Host, it performs a dummy read of the Aux Software Control Register to set the Aux Control Ready bit.

COHOST SHUTDOWN: This bit indicates that the CODEC and Host interface logic is in sleep mode (power save). The Host interface must be re-awakened by writing to the CONTINUE bit in the Hardware Control Register before writing or reading from any other Host register. When COHOST SHUTDOWN is active, all the other bits in the Hardware Status Register are undefined for read operations.

4.5.3 Software Control Register

This is a 16-bit register. It is used to pass commands from the Host to the CT8022. The Host can write commands to this register, and read back the command, after it has been written.

When the Host writes to the upper byte of this register, it clears the Control Ready bit in the Hardware Status Register.

When the CT8022 internally reads from this register, it sets the Control Ready bit in the Hardware Status Register.

The CT8022 hardware includes a second Aux Software Control Register. This register is reserved and is not used by the internal CT8022 firmware.

4.5.4 Software Status Register

This is a 16-bit register. It is used to pass command status/result information from the CT8022 back to the Host. The Host can only read from this register.

When the CT8022 updates this register, it sets the Status Ready bit in the Hardware Status Register and also asserts IRQN to the Host (if enabled).

When the Host reads the upper byte of this register, it clears the Status Ready Hardware Status Register. The IRQN will also clear at this time, if enabled.

The CT8022 hardware includes a second Aux Software Status Register. This register may be used to provide an independent status register for reporting the status of the DTMF and Call Progress Tone detector. This allows the CT8022 to provide an *interrupt on DTMF* feature when used in conjunction with the interrupt enable controls in the Hardware Control Register.

4.5.5 Host Receive and Transmit Data Buffer Blocks

The CT8022 includes two 16-word (32 byte) data buffer blocks for use in transferring blocks of data to or from the Host. Access to these buffers is controlled by the CT8022. The Host accesses these buffers in sequential address order through two 16-bit Host Data Buffer access ports (one for RX and one for TX). The Host address sequence is generated by an internal address counter within the CT8022.

Each buffer is shared between the Host and CT8022. At any one time, either the Host or the CT8022 has access to the buffer. At no time can both Host and CT8022 access the buffer simultaneously. The CT8022 controls whether access belongs to the CT8022 or Host via an internal control register. For example, when the Host transmits data to the CT8022, the CT8022 first grants the Host access to the buffer. The Host fills the *empty* buffer. While the Host is filling the buffer, the CT8022 can not access it. Once the buffer is full, the CT8022 regains access to the *full* buffer. The CT8022 then copies the data from the buffer. At this point, the Host can not access the buffer. Once the buffer has been emptied, the CT8022 can then pass it back to the Host.

The *receive* and *transmit* buffer blocks are conceptually almost identical except for the direction of data transfer associated with Host accesses. The *receive* buffer is used to transfer data from the CT8022 to the Host. The *transmit* buffer is used to transfer data from the Host to the CT8022.

4.5.5.1 Host Receive Data Buffer Block

This block is used to transfer data from the CT8022 to the Host, using an external DMA controller or a Host processor access cycle.

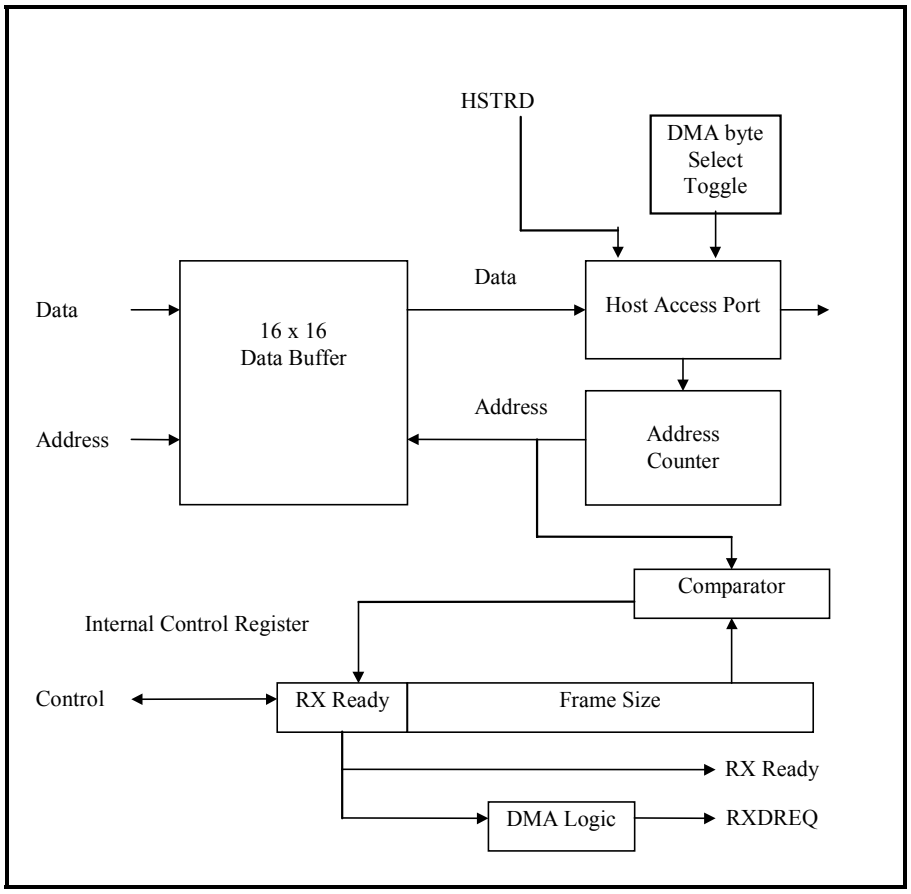


Figure 4-2: Host Receive Data Buffer Block

4.5.5.1.1 Receive Data Buffer Internal Control Register

This is an internal register, and is not accessible by the Host.

0000 0000	RX Ready	00	Frame Size
(15-8)	(7)	(6-5)	(4-0)

RX Ready: When set to zero, the CT8022 has control of the data buffer and has write only access to any location in the buffer.
When set to one, the Host has control of the data buffer and may read its contents via the Host Data Buffer access port.
The state of this bit can be checked by the Host at any time since it is reflected by the RX Ready bit in the Hardware Status register. The RX Ready bit in the Receive Data Buffer Control Register drives the RX Ready bit and also RXDREQ via the DMA logic.
After reset, this bit is zero.

Frame Size: The Frame Size field determines the number of words contained in the data buffer. It acts as the reference input to the Host buffer address comparator.

Address Counter

The 5-bit address counter provides the sequential buffer access address for access by the Host via the Host Data Buffer access port. The address counter is reset to zero when the CT8022 writes a 1 to the RX Ready bit of the internal control register causing control of the buffer to transfer to the Host. Each time the Host accesses the upper byte of the Host Data Buffer access port the address counter increments by 1.

The data buffer access port is only physically 8-bits wide. When an access to this port is made by a Host processor, the byte select address line HSTAB0 is valid and can be used to select the byte accessed. When access is made by a DMA controller, the address decode which selects the data buffer access port is provided by the RXDACKN signal. During a DMA cycle, the HSTAB3-0 address bits are not valid. Generation of an internal HSTAB0 is thus required to select the byte accessed. This is provided by a simple toggle mechanism that changes state on each DMA access. The DMA byte select toggle is set to zero each time the RX Ready bit changes from a zero to a one (this also clears the main address counter). A separate DMA byte select toggle is required for transmit and receive.

Comparator

The 5-bit comparator is active only when the Host has control (the RX Ready bit is set). The comparator compares the value in the address counter with the value in the Frame Size field. If the values are not equal, the Host continues to have access to the data buffer. When the values become equal (after the last Host access), the RX Ready bit is reset, transferring control back to the CT8022.

Transferring Data From CT8022 To Host

The CT8022 determines the size of the data frame to be transferred by some protocol with the Host. At the beginning of data transfer, the RX Ready bit will be zero. The CT8022 then writes the appropriate number of words into the data buffer. It then programs the Frame Size and sets the RX Ready bit. This causes the RX Ready bit, visible to the Host n the Hardware Status Register, to be set. The Host discovers that the RX Ready bit is set (by polling or interrupt). The Host then reads Frame Size words from the Host Receive Buffer Access Port, after each word is read, the address counter increments. When the Host reads the last word, the address counter is incremented and matches the Frame Size value. This is detected by the comparator, which causes the RX Ready bit to be cleared. The CT8022 determines that it has access to the data buffer and loads the next frame into the buffer. This process is repeated to transfer the next frame.

For DMA transfers, the RX Ready bit drives the state of the DMA Request signal. When RX Ready is set, the DMA request is asserted. When the buffer becomes empty, and buffer control automatically returns to the CT8022, the RX Ready bit is cleared and the DMA Request signal is de-asserted.

4.5.5.2 Host Transmit Data Buffer Block

This block is used to transfer data from the Host to the CT8022, using an external DMA controller or a Host processor access cycle.

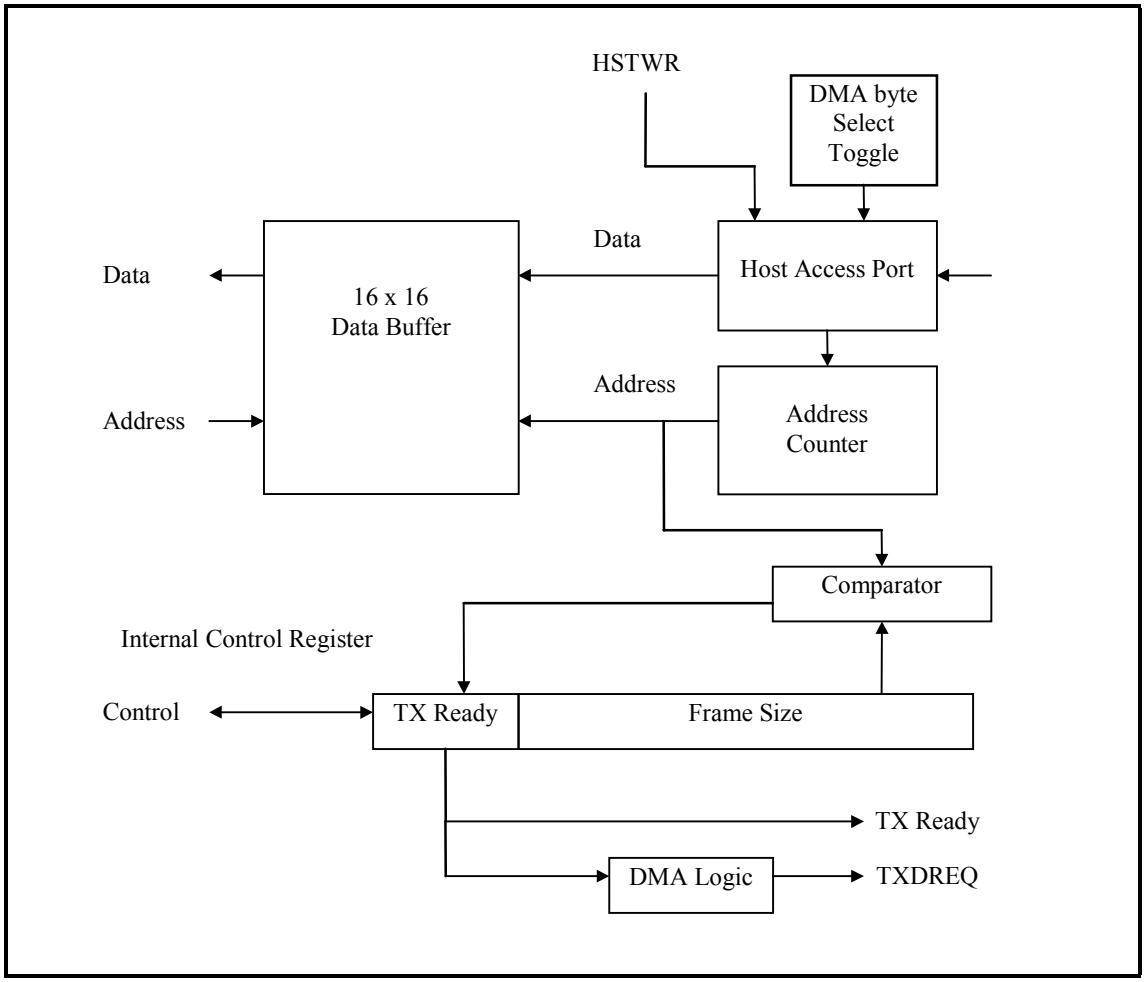


Figure 4-3: Host Transmit Data Buffer Block

4.5.5.2.1 Transmit Data Buffer Internal Control Register

This is an internal register, and is not accessible by the Host.

0000 0000	TX Ready	00	Frame Size
(15-8)	(7)	(6-5)	(4-0)

TX Ready: When set to zero, the CT8022 has control of the data buffer and can read any location in the buffer.
When set to one, the Host has control of the data buffer and may write its contents via the Host Data Buffer access port.
The Host can check the state of this bit at any time since it is reflected by the TX Ready bit in the Hardware Status register. The TX Ready bit in the Transmit Data Buffer drives the TX Ready bit and TXDREQ via the DMA logic.
After reset, this bit is zero.

Frame Size: The Frame Size field determines the number of words contained in the data buffer. It acts as the reference input to the Host buffer address comparator.

Address Counter
The 5-bit address counter provides the sequential buffer access address for access by the Host via the Host Data Buffer access port. The address counter is reset to zero when the CT8022 writes a 1 to the TX Ready bit of the internal control register causing control of the buffer to transfer to the Host. Each time the Host accesses the upper byte of the Host Data Buffer access port the address counter increments by 1.

The data buffer access port is only physically 8-bits wide. When a Host processor accesses to this port, the byte select address line HSTAB0 is valid and can be used to select the byte accessed. When access is by a DMA controller, the *address decode* which selects the data buffer access port is provided by the TXDACKN signal. During a DMA cycle, the HSTAB3-0 address bits are not valid. Generation of an internal HSTAB0 is thus required to select the byte accessed. A simple toggle mechanism, which changes state on each DMA access, performs this function. The DMA byte select toggle is set to zero each time the TX Ready bit changes from a zero to a one (this also clears the main address counter).

A separate DMA byte select toggle is required for transmit and receive.

Comparator
The 5-bit comparator is active only when the Host has control (the TX Ready bit is set). The comparator compares the value in the address counter with the value in the Frame Size field. If the values are not equal, the Host continues to have access to the data buffer. When the values become equal (after the last Host access), the TX Ready bit is reset, transferring control back to the CT8022.

Transferring Data From Host To CT8022
The CT8022 determines the size of the data frame to be transferred by a protocol with the Host. At the beginning of data transfer, the TX Ready bit will be zero. The CT8022 then programs the Frame Size and sets the TX Ready bit (in the same write cycle). This causes the TX Ready bit visible in the Hardware Status Register to be set. The Host discovers that the TX Ready bit is set (by polling or interrupt). The Host then writes Frame Size words into the Host Transmit Buffer Access Port. After each word is written, the address counter is incremented. When the Host writes the last word, the address counter is incremented, and matches the Frame Size value. This is detected by the comparator, which causes the TX Ready bit to be cleared. The CT8022 discovers that it has access to the data buffer and reads the buffer contents, transferring them to the CT8022's local RAM. This process is repeated to transfer the next frame.

For DMA transfers, the TX Ready bit drives the state of the DMA Request signal. When TX Ready is set, the DMA request is asserted. When the buffer becomes full, and buffer control automatically returns to the CT8022, the TX Ready bit is cleared and the DMA Request signal is de-asserted.

4.6 DMA Transfers

The CT8022 interfaces directly to one or two external 8-bit DMA controllers connected to the Host bus. The DMA controllers may be of the *fly-by* type (used in IBM-compatible PCs) or the *flow-through* type (used, for example, in the Intel 80186).

In a fly-by DMA transfer, the DMA controller simultaneously generates the following:

- the address of the source or destination memory location
- the *read/write* signal to the memory
- a *read/write* signal to the peripheral
- a DMA acknowledge signal (which enables the destination or source peripheral)

In a *read from peripheral* cycle, the DMA *acknowledge* signal and the peripheral *read* strobe cause the peripheral to gate it's data onto the data bus. The DMA controller provides the destination memory address and asserts the memory write signal causing the peripheral's data to be written to the memory. In a *write to peripheral* cycle, the DMA controller generates the memory address and asserts the memory *read* signal causing the appropriate data byte to appear on the data bus. The DMA controller also asserts the DMA Acknowledge signal plus the peripheral *write* strobe, which causes the peripheral to read the data currently on the data bus. This type of DMA controller requires both DMA *reques*t and DMA *acknowledge* signals. The peripheral ignores the address signals, since they indicate the memory address, and not the peripheral address. Instead, the peripheral uses the DMA *acknowledge* signal and the *read/write* strobe to indicate that it has been selected.

The alternative type of DMA controller, which uses a *flow-through* transfer, is supported by the normal Host processor data transfer interface. In a *flow-through* transfer, the *read/write* access to the peripheral and the *write/read* memory access are performed as two separate cycles, with the DMA controller providing temporary storage of the data. In this type of transfer, the DMA access cycle to the CT8022 is identical to a Host processor access cycle. In a *read from peripheral* cycle, the DMA controller first drives the address bus with the address of the peripheral, and asserts HSTCS/ and HSTRD/. The DMA controller temporarily saves the peripheral data and then writes the data to memory by performing a normal memory access cycle. This type of controller requires only the DMA request signals, and does not use the DMA acknowledge. When used with this type of controller, the CT8022 DMA acknowledge signals should be connected to VCC via pull-up resistors.

4.6.1 DMA modes

The DMA interface can be operated in two modes:

- full-duplex
- half-duplex

4.6.1.1 Full-Duplex Mode

In full-duplex mode, the RX and TX DMA interfaces operate independently of each other, with physically separate control signals dedicated to the two data transfer directions. Two external DMA channels are required.

4.6.1.2 Half-Duplex Mode

In half-duplex mode, only a single external DMA channel is required. The external DMA controller has only a single DMA *request* line available, and a single DMA *acknowledge* line. Using only these two signals, the DMA controller must be able to transfer data both to and from the CT8022. To accommodate this arrangement without requiring external glue logic, the TXDREQ and RXDREQ and the TXDACKN and RXDACKN pin functions can be swapped by the Host using the control bits in the Hardware Control Register. This allows the DMA controller to be hard-wired to one set of DMA pins, and permits software control of the transfer direction associated with these pins.

4.6.2 Burst Mode and Single Cycle Mode Transfers

DMA transfers can be performed in either Burst Mode (continuous) or Single Cycle Mode. In Burst Mode, the DMA *request* signal TXDREQ or RXDREQ remains asserted whenever the appropriate data buffer can accommodate the transfer. Each time the DMA *acknowledge* signal, TXDACKN + HSTWRN or RXDACKN + HSTRDN, is asserted a byte is transferred. This continues until the Transmit Data Buffer is full or the Receive Data Buffer is empty, at which point the DMA request signal is de-asserted (the appropriate TX or RX Ready bit is cleared). Burst Mode allows for the fastest transfer of data, since the Host is required to perform bus request/bus grant arbitration with it's external DMA controller only once per burst. With a 16-word buffer, up to 32 bytes can be transferred in a single burst.

In Single Cycle Mode, the DMA request signal, TXDREQ or RXDREQ is asserted, and then de-asserted, once for each byte transferred. This mode requires the Host to re-arbitrate bus access with the external DMA controller for each byte transferred. When the CT8022 is ready to perform a DMA transfer, the DMA request signal is asserted. The DMA controller responds with the DMA acknowledge signal (plus HSTRD/ or HSTWR/), which clocks the byte data transfer and also causes the DMA request signal to be withdrawn. After the byte transfer has been completed, the CT8022 delays for a short period and then re-asserts the DMA request signal (assuming it has more data to transfer).

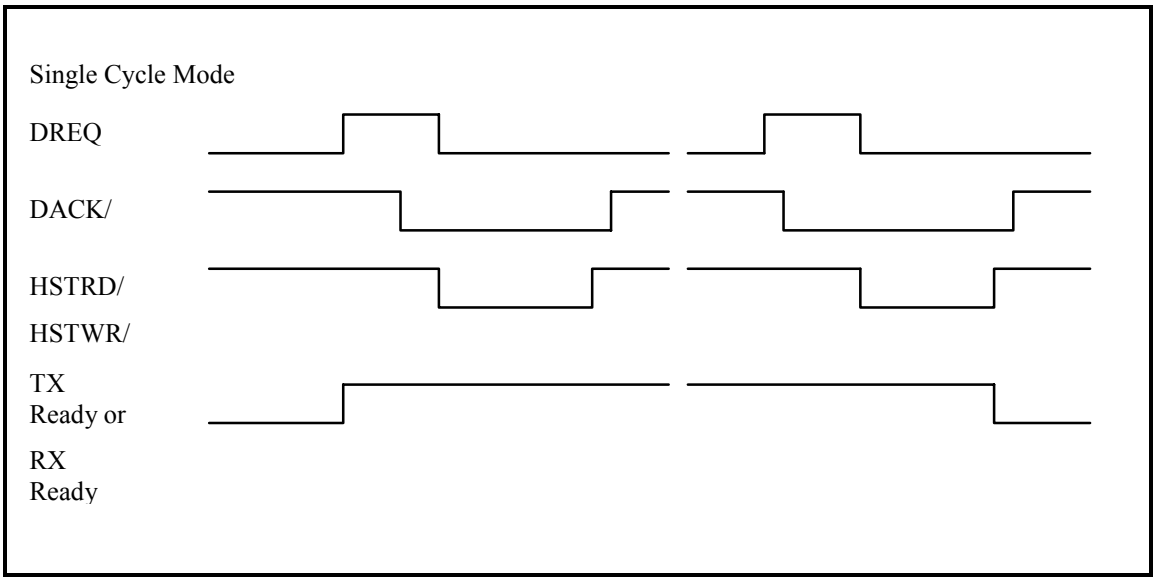


Figure 4-4: Single Cycle DMA Mode

In Single Cycle Mode, the negative going edge of HSTRD/ or HSTWR/ during DACK/ causes the DREQ signal to be de-asserted. If the RX or TX Ready bit is still set after the end of the DMA cycle, then DREQ will be re-asserted 16 MAINCLOCK clock periods after the positive going HSTRD/ or HSTWR/ edge. At 40 MIPS (25ns) this translates to 400 ns. The address counter used to index the data buffer during Host/DMA cycles is incremented by the positive going edge of HSTRD/ or HSTWR/ on alternate DMA cycles (i.e. each time a high byte is accessed). The data buffer block contains a toggle bit used to generate a DMA byte select. This toggle bit is used in place of HSTAB0 during a DMA cycle, and it changes state at the end of each DMA cycle to provide the correct byte access sequence: low-byte, high-byte, low-byte, high-byte etc. The Host address lines HSTAB3-0 are ignored during a DMA cycle. The toggle bit is set to zero each time the data buffer address counter is reset (when the CT8022 writes a 1 to the RX or TX Ready bit). If the counter reaches the Frame Size limit value, then the RX or TX Ready bit is reset following the positive HSTRD/ or HSTWR/ edge.

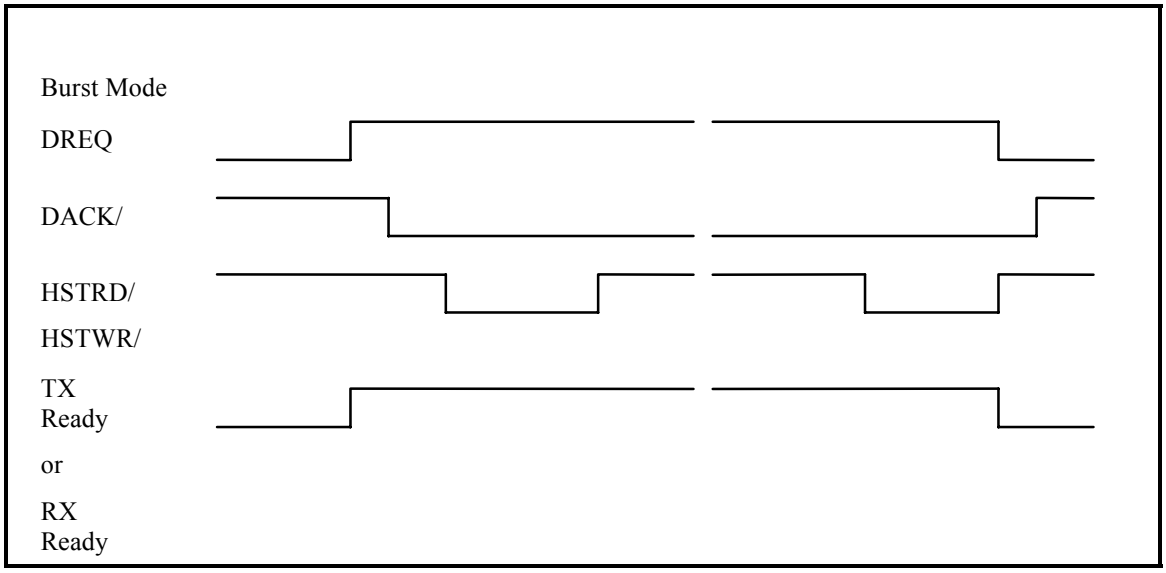


Figure 4-5: Burst Mode DMA

In Burst Mode, DREQ remains asserted until the RX or TX Ready bit is cleared by the final counter increment. Byte transfers are clocked by the HSTRD/ or HSTWR/ signals as appropriate. The positive going edge of these signals toggles the DMA byte select. The data buffer address counter increments on alternate cycles, i.e. each time a high byte is accessed. When the counter reaches the Frame Size limit the RX or TX Ready and DREQ signals are cleared.

4.6.3 Flow-Through DMA Transfers

Programmer's Note:

A *Flow-Through* DMA transfer is one in which the *read* and *write* operations of the DMA transfer take place as separate cycles, with the DMA controller providing intermediate temporary storage of the data. In this type of DMA, the data physically *flows through* the DMA controller:

- **DMA controller outputs source address**
- **DMA controller reads from source**
- **DMA controller stores data in internal temporary register (single byte)**
- **DMA controller outputs destination address**
- **DMA controller writes data to destination**

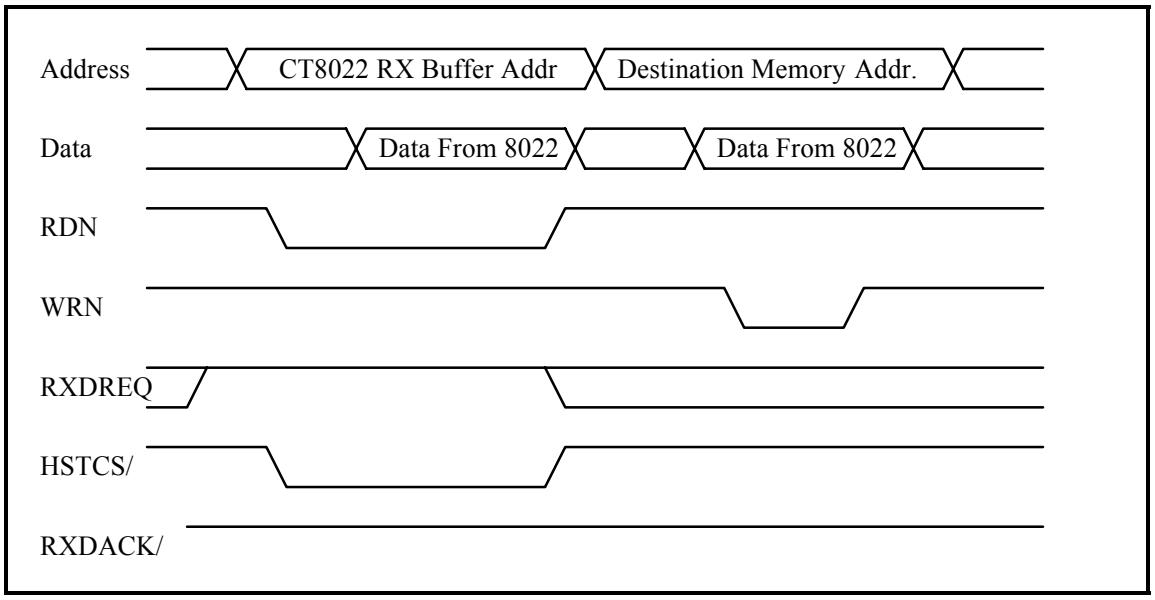


Figure 4-6: Flow-Through DMA

Figure 4-6 is an example of a CT8022 to Memory DMA transfer using *Flow-Through* DMA. The RXDACK/ signal is not used. Note that, from the perspective of the CT8022, an access by a *Flow-Through* type DMA controller looks identical to a normal Host access. The Intel 80186 and 80188 processors contain this type of DMA controller.

5 CT8022 CODEC Interface

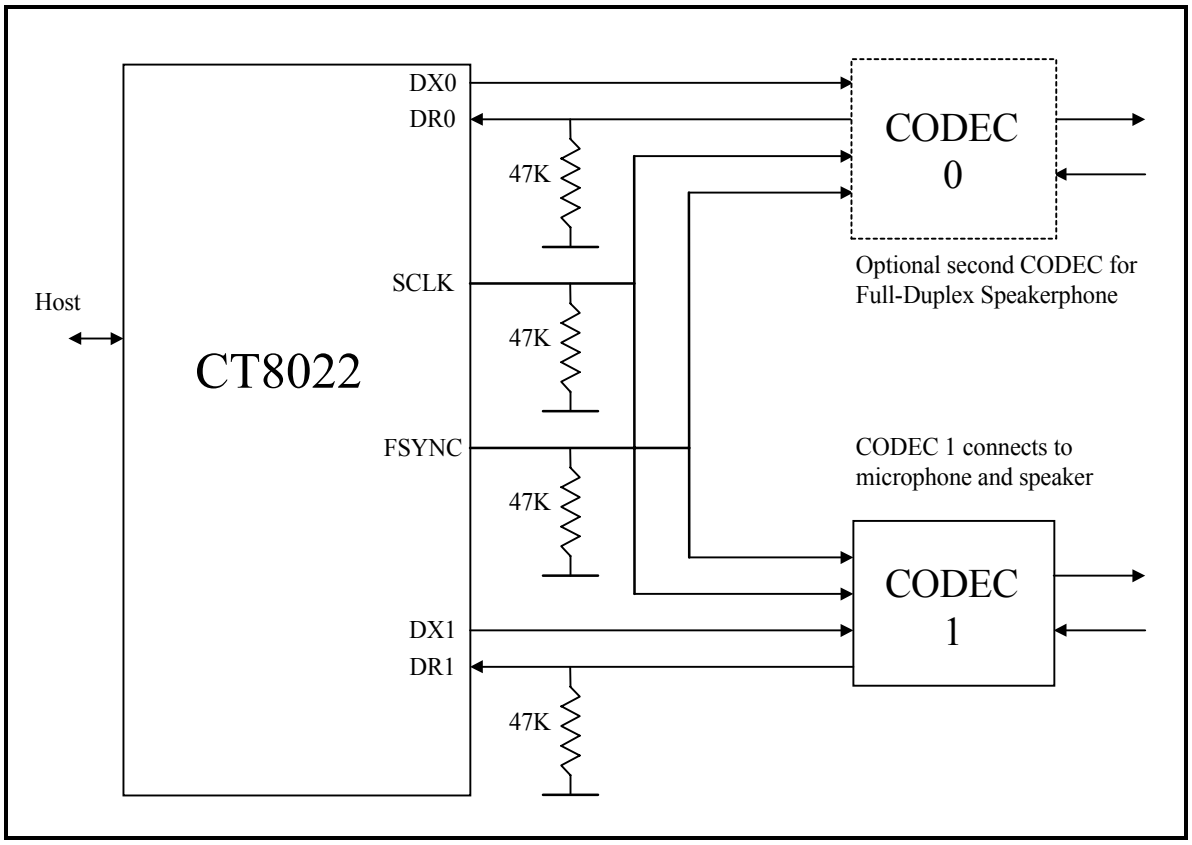


Figure 5-1: CT8022 CODEC Interface Connection

In Master mode, the CT8022 generates the FSYNC and SCLK signals.

In Slave mode, the FSYNC and SCLK signals are generated externally. In slave mode, the CT8022 FSYNC and SCLK pins are inputs.

Note: During and after reset, the SCLK and FSYNC pins are configured as inputs. As such, they require external pull-down resistors to ensure that a safe and defined logic level is present.

5.1 CODEC Options

The CT8022 CODEC interface supports the following features:

- CODEC clock master or slave
- 8-bit A-law/μ-law or 16-bit linear CODEC
- Short or Long FSYNC
- Programmable SCLK and FSYNC clock rates

5.1.1 Master/Slave

The CT8022 can be operated in CODEC master or slave mode.

In master mode, the SCLK and FSYNC signal pins are outputs. The clock frequencies for the two signals are generated by programmable integer division from the internal CT8022 DSP core clock. To achieve an SCLK frequency of 2.048 MHz for operation with an A-law or μ-law CODEC, the CT8022 internal clock should be 45.056 MHz (4.096 MHz crystal). 45.056 MHz = 22 * 2.048 MHz.

In slave mode, the SCLK and FSYNC signals pins are inputs. The SCLK and FSYNC signals must be generated externally. For TrueSpeech® G.723.1 operation, the FSYNC frequency should be exactly 8.0 KHz. In slave mode, it is possible to connect the CT8022 CODEC interface to a TDM (Time Division Multiplexed) bus.

For support of G.722 7 KHz wideband ADPCM (only), the CT8022 must be operated with an external CODEC that supports operation at 16K samples/sec.

Following reset, the CT8022 CODEC interface will be in slave mode, so that SCLK and FSYNC are inputs.

5.1.2 8-bit A-law/μ-law and 16-bit Linear CODEC

The CT8022 CODEC interface can be programmed by the Host to operate in 8-bit or 16-bit mode. In 8-bit mode for each FSYNC, 8 data bits are shifted out of the DX0 and DX1 pins, and 8 data bits are shifted in at the DR0 and DR1 pins. In 16-bit mode for each FSYNC, 16 data bits are shifted out of the DX0 and DX1 pins, and 16 data bits are shifted in at the DR0 and DR1 pins.

In 8-bit mode, the data format may be either μ-law or A-law.

In 16-bit mode, the data format is 16-bit linear, with the most significant bit shift in/out first.

5.1.3 Short or Long FSYNC

In master mode, the CT8022 may be operated in short or long FSYNC mode. In short FSYNC mode, the FSYNC pulse is 1 SCLK period wide. The timing of the FSYNC pulse relative to the data bits conforms to the telecom industry standard for short FSYNC for PCM A-law/μ-law codes when SCLK = 2.048 MHz, and FSYNC = 8.00 KHz. In long FSYNC mode, the FSYNC pulse is 8 or 16 SCLK periods wide, depending on the data width selected. In this mode, the FSYNC pulse is aligned with the *receive* and *transmit* time slot of the data bits.

In slave mode, the width of the FSYNC pulse is not important. Selecting long or short FSYNC mode only affects the assumed timing position of the FSYNC relative to the data bits.

5.1.4 Programmable SCLK and FSYNC Rates

In master mode, the SCLK and FSYNC rates are fully programmable by the Host. This enables Host selection of the CODEC sample rate based on simple integer division from the internal CT8022 clock.

SCLK is generated by a division-by-(N+1) from the internal CT8022 clock. The divisor may be in the range of 4 <= (N+1) <= 32. If the internal CT8022 clock is 45.056, then setting N = 21 will produce a 2.048 MHz SCLK.

FSYNC is generated by a division -by -(M+1) from SCLK. The divisor may be in the range of 18 <= M <= 1023. If SCLK = 2.048 MHz and M = 255, then FSYNC will be 8.0 KHz.

The following table shows possible clock frequencies:

MAINCLOCK = 45.056 MHz (4.096 MHz crystal)			
SCLK	FSYNC	N	M
2.048 MHz	8.000 KHz	21	255
2.048 MHz	11.011 KHz	21	185
2.816 MHz	11.043 KHz	15	254

Note that the AT&T T7525 16-bit linear CODEC requires that the SCLK frequency be exactly 256 times the FSYNC frequency. When using this CODEC, SCLK must be 2.048 MHz in order to achieve a FSYNC frequency of 8.000 KHz.

For supported SCLK-to-FSYNC ratios, please consult the external CODEC manufacturer's data sheet. Note that some G.711 A-law/μ-law CODECs provide strapping options which access different available ranges for the SCLK-to-FSYNC ratio (e.g. for operation at E1 2.048 MHz 32 channel rate or T1 1.544 MHz 24 channel rate). In general, the choice of SCLK frequency often controls the effective audio bandwidth of the CODEC's anti-aliasing filter.

For an 8-bit CODEC, the CT8022 requires that the SCLK frequency is at least 16 times the FSYNC frequency.

For a 16-bit CODEC, the CT8022 requires that the SCLK frequency is at least 32 times the FSYNC frequency.

The CT8022 may be operated at a lower core clock rate to reduce the power consumption of the device, if the clock rate chosen provides sufficient MIP s for the modes of operation used. Operating the CT8022 at a lower clock rate requires that the Host change the SCLK and FSYNC division factors to obtain the desired A-to-D sample rate.

5.1.5 Stop CODEC

In Master mode, the ***Stop CODEC*** command can be used to halt operation of the CODEC interface. In this state, the FSYNC and SCLK signals are held low. ***Stop CODEC*** in Slave mode has no effect.

6 Host Data Transfer Modes

Data transfer between the CT8022 and Host can be performed in two ways:

- via the *transmit* and *receive* Data Buffers (recommended for new designs)
- via the Software Control and Software Status Registers (CT8015-compatible mode)

6.1 Data Transfer using the Data Buffers

This transfer mode is recommended for all new designs.

In this mode, the CT8022 supports DMA transfers as well as low-overhead Host processor-based transfers. Once the CT8022 playback/record options have been selected and activated, speech frames can be transferred with minimal or zero *control overhead* required for device polling or supervision.

6.1.1 DMA Transfers

The CT8022 provides a full-duplex DMA interface with independent Transmit and Receive request and acknowledge signals. The Host issues the commands to the CT8022 to start playback and/or record and then enables DMA transfers by programming the Hardware Control Register. Once playback/record operation has been set up, the CT8022 can continue to transfer speech frames without further involvement of the Host. The Host processor can optionally use the buffer management commands to observe and control the status of the speech data streams.

6.1.2 Host Processor Transfers

In systems where no DMA controller is available, the Host processor can be used to perform the data transfers. The playback and/or record operation is set up as before. Then, the Host processor can configure the Hardware Control Register to generate an interrupt to the Host on the TX/RX ready condition, or the Host may simply periodically poll the TX/RX ready status. Once the Host is ready to perform the data transfer, it can perform *read/write* bursts of up to 16 words of data without needing to recheck the TX/RX ready status. The data buffers can contain a maximum of 16 words of data. This size is sufficient to accommodate a complete TrueSpeech data frame. This allows microprocessors with *repeat* instruction prefixes (e.g. Intel X86: REP INS, REP OUTS) to perform block moves of compressed speech frames. When performing record/playback of non-compressed data, where the speech data frame size is greater than 16 words, the Host may divide the data transfer into 16-word sub-blocks and recheck the TX/RX ready status between the sub-blocks.

6.2 Data Transfer using the Software Control and Status Registers

This transfer mode is provided for software compatibility with the CT8015 and CT8005.

In this mode, the CT8022 supports data transfers using only the Software Control and Status Registers. This mode provides backward compatibility with the data transfer protocol used in the CT8005 TrueSpeech 8.5 Messaging Co-Processor and the CT8015 TrueSpeech 8.5 DSVD Co-Processor.

To perform data transfers, the Host must interrogate the CT8022 using the playback/record ***C2-S2-C3-S3*** command/status sequence. When the CT8022 is ready to transfer data, it returns the available transfer count in the ***S3*** status response. The Host then performs the required number of command-write-status-read cycles using the Software Control and Status registers to transfer the data.

6.2.1 Host Control/Status Register Data Transfer Synchronization Modes

The synchronization modes described here are for use *only* with speech data transfers performed via the Software Control and Status Registers. The synchronization options control the manner in which data transfers are coordinated with control operations performed via these registers. When data is transferred via the *transmit* and *receive* data buffers, the CT8022 provides dedicated TX/RX ready/DMA signals.

Generally, the rate of transfer of data between the Host and the CT8022 must be synchronized with the rate at which speech data is transferred between the CT8022 and its external CODEC(s). Data is exchanged between the CT8022 and the CODEC, one sample every 125 microseconds (at 8.0 KHz). This data is accumulated into blocks of 240 samples, which correspond to a period of 30 milliseconds. If the channel is operating in A-law/μ-law or linear mode etc., this data block (or frame) is transferred to the Host without compression. If the channel is operating in TrueSpeech mode (compressed), the frame is compressed before transfer. The 30ms period is derived from the external CODEC clock by counting 240 samples.

The CT8022 devices are intended to be used in pairs, at opposite ends of a communications link. The CT8022 at each end of the link will have its own external CODEC and its own independent clock source or crystal. Data is moved between the two devices in real-time via the Host processors attached to each CT8022 at each end of the link. Although the CT8022 clocks will probably be derived from a crystal source to generate the 8.0 KHz CODEC sample rate, the precise frequencies of these clocks will most likely be fractionally different. The frequencies may well also vary with temperature and time. As a result, one CT8022 at one end of the link will source/consume speech data at a rate fractionally different from the CT8022 at the other end of the link. Over time, this difference will accumulate, if left alone. If the playback channel at one end consumes data more slowly than it arrives, the *transmit* buffer queue will gradually fill, increasing the apparent transmission delay until the transmit buffer queue becomes full. At this point, frames of data will begin to be discarded. If the playback channel consumes data more quickly than it arrives, the *transmit* buffer will become empty over time until the playback channel becomes starved of data. At this point gaps will be introduced into the outgoing speech, or extra frames of data will have to be synthesized to make up for the short fall in frames.

To assist with dealing with this end-to-end synchronization problem, the CT8022 playback and receive channels can be operated in one of four different sync modes. The sync mode of operation of the playback (*transmit*) and record (*receive*) channel can be selected independently. The CODEC Sync mode provides for backward software compatibility with the CT8005 TrueSpeech Messaging Co-Processor.

The four sync modes are:

1. CODEC Sync Mode
2. Data Sync Mode
3. Poll Sync Mode
4. Host Sync Mode

6.2.1.1 CODEC Sync Mode

In CODEC Sync Mode, Host-CODEC synchronization is maintained on a 30ms frame-by-frame basis. The CT8022 does not perform any additional internal buffering. This mode provides minimum delay with the tightest coupling between CODEC-CT8022 transfers and CT8022-Host transfers (there is a 1-frame delay). In this mode, the Host must ensure that it is able to perform a data transfer every 30ms. Data transfers are performed by the Host processor and take place through the Software Control and Status Registers. This mode is compatible with the data transfer protocol used by the CT8005 TrueSpeech Messaging Co-Processor. In this protocol, the ***playback***/***record*** command sequence is directly synchronized with the 30ms frame rate by delaying the Status responses until the frame is ready. This causes the CT8022 Host interface to *block* or *wait* on a command to transfer data. This blocking means that this mode can only support half-duplex data transfers, i.e. concurrent playback/record is *not* supported in this mode. While the command/status interface is blocked waiting for the next frame, the CT8022 is unable to process other commands. The blocking effect also means that only 1 frame can be transferred to the CT8022 each frame period. Consequently, the effective buffer depth of the CT8022 is 1, regardless of the buffer limit setting. Software designed to support the CT8005 may depend on the blocking feature in order to use the rate at which the CT8005 responds in order to measure the progress of time. An additional property of this mode is that a data frame can always be transferred once the CT8022 has returned a status response (the transfer count returned in the ***S3*** status response is always non-zero). CODEC Sync Mode is the default mode of the CT8022 following reset.

6.2.1.2 Data Sync Mode

This mode operates in a manner similar to the CODEC Sync Mode, but with additional buffering being provided within the CT8022. This relaxes the requirement that the Host be able to respond to a transfer request from the CT8022 every 30ms (depending on the buffer limit set). This mode provides a degree of compatibility with the CT8005 TrueSpeech Messaging Co-Processor, while also providing additional buffering.

Blocking of the command/status interface can be avoided in this mode by using the buffer depth polling commands prior to issuing the data transfer (play/record) commands. By checking the buffer depth, the Host can avoid reading from an empty record buffer, or writing to a full playback buffer.

This mode is selected automatically when the CT8022 enters Host-to-Host (CODEC-less) compression or decompression mode. This default can be over-ridden by changing the sync mode after the start of Host-to-Host mode.

6.2.1.3 Poll Sync Mode

In Poll Sync Mode, the CT8022 maintains internal frame buffers that are linked directly to the Host interface *transmit/receive* data buffers. Available *receive* data is transferred automatically to the Host interface *receive* buffer unless the buffer is full. Any data placed in the Host interface *transmit* buffer is automatically transferred to the internal *transmit* buffer unless that buffer is full. This mode is recommended for DMA transfers where there is no frame-by-frame Host supervision (no ***C2-S2-C3-S3*** play/record command sequence is required).

Poll Sync Mode is a non-blocking variant of Data Sync Mode. Regardless of the data transfer option selected, the command/status responses occur without waiting to synchronize with the 30ms frame period. When the record buffer is empty or the playback buffer is full, the CT8022 returns zero as the transfer count in the playback/record ***S3*** status response. Data may be transferred via the Software Control and Status Registers, via the *transmit* and *receive* data buffers using the Host processor, or via the *transmit* and *receive* data buffers using a DMA controller.

6.2.1.4 Host Sync Mode

Host Sync mode is similar to Poll Sync Mode, except that the Host is always given permission to perform the transfer it requests, irrespective of the internal *transmit* and *receive* state. The CT8022 accommodates this by creating or discarding data as necessary.

6.3 Data Transfer Options Summary

The following table summarizes the data transfer options:

Data Transfer Options			
Sync Mode	Host via Software Control & Status Registers	Host via Data Buffer	DMA via Data Buffer
CODEC	X		
Data	X		
Poll	X	X	X
Host	X		

Poll Sync Mode should be selected when performing data transfers via the *transmit* and *receive* data buffers. In this mode, data transfer can be performed by the Host processor itself, or with an external DMA controller.

7 Play & Record Delay Management

7.1 Delay and Latency Management

The CT8022 has features that allow the Host to manage and control the amount of delay and latency provided by the CT8022. The CT8022 includes data buffering in both the playback and record channels that allows the Host to operate with relaxed timing requirements when transferring data to or from the device. Internally, the CT8022 operates within a strict single-frame 30ms time limit when compressing and decompressing speech frames in real-time. The CT8022's buffering capabilities allow the Host to operate with programmable additional latency so as to avoid requiring the Host to perform data transfers that are synchronized exactly to the 30ms frame period. By programming the buffer depth for the record and playback channels, the Host can select the trade-off made between the time allowed for the Host to respond to a request for data transfer and the amount of delay introduced. Further, the Host is able to manage any accumulation of data, which causes additional delay that results from differences in precise clock rate between the two ends of a speech link.

7.2 Data Over-run And Under-run

Data over-run occurs when data arrives at a point faster than data departs from that point. Data under-run occurs when data attempts to leave a point faster than it arrives. In addition to providing buffer depth management support functions such as buffer depth monitoring and variable buffer depth control for Host-based buffer management, the CT8022 has a built-in or default buffer management scheme. When the Host allows the record (*receive*) buffer to over-run, the CT8022 responds by simply discarding frames until the Host causes the record buffer to be less than full. When the Host allows the playback (*transmit*) queue to become empty, the CT8022 responds by repeating the last frame until new data becomes available.

7.3 Buffer Monitoring

The CT8022 provides buffer monitoring functions that allow the Host to determine at any time the amount of speech data in the device's *transmit* and *receive* queues.

7.4 Frame Creation and Deletion

The CT8022 provides frame creation and deletion commands to allow the Host to dynamically control the *transmit* and *receive* speech channel delays. The frame creation function causes the CT8022 to create an extra frame (provided the relevant queue is not full) by duplicating the most recent frame. The frame deletion function causes the CT8022 to discard the most recent frame from its *receive* or *transmit* buffers (assuming the buffers are not empty). These functions are an essential part of managing a full-duplex communications link for two reasons.

The first reason is that, since the clock rates at the two ends of the link will always be fractionally different, one end of the link will tend to accumulate data, progressively increasing the end-to-end delay. The other end will consume data more quickly than it arrives. This causes any intentional delay or speech buffer created by the Host, for the purpose of *smoothing* or averaging out of the data transmission rate, to be gradually consumed, until the link operates with zero delay.

The creation and deletion functions allow the Host to monitor the buffer depths continually, and introduce periodic corrections to the overall effective data rate to keep the buffers filled to the desired depth. For example, if the Host detects that the *transmit* buffer depth has become too low, it can correct this by instructing the CT8022 to create an additional frame.

The second reason is that, since the communications link connecting the two ends of the speech channel may be prone to occasional errors or data corruption, speech frames will be lost or damaged from time-to-time, and thus discarded. This has the same effect as the data under-run process. Again, the Host can use the frame create function to make up for the lost frames. If the Host-to-Host link includes error correction, this second issue will not be a problem.

However, use of error correction schemes either entails a higher bit rate (in the case of forward-error correction) or increased latency (delay) in the case of error correction by error-detection-and-re-transmission. Both techniques are usually undesirable on real-time speech links. The Host-to-Host link should include some error detection mechanism (e.g. checksum or CRC) so that the Host can detect corruption of speech data frames. Since the speech is highly compressed, every bit in the speech frame is significant. If a single bit is in error, a major disturbance (noise) may be generated in the speech signal if the damaged frame is decoded. In this situation, the Host should detect and discard damaged speech frames and instruct the CT8022 to create a (undamaged) frame to replace it. This process of detecting, discarding and replacing damaged frames is known as *frame erasure*.

The G.723.1 (and G.729 Annex A) includes a built-in frame erasure mechanism for replacing missing or corrupt speech frames. The frame erasure system (for use with the G.723.1 6.3, 5.3, TrueSpeech 4.8 and 4.1 rates, and G.729A) is independent of the mechanism described above. The G.723.1/G.729A frame erasure system performs an intelligent extrapolation of data from previous speech frames in order to replace missing frames. This feature is activated by use of specially coded speech frames.

7.5 Buffer Freezing (Pausing)

The CT8022 supports freezing or pausing of the *transmit* and *receive* buffers. Freezing of the *transmit* (playback) queue enables the Host to pre-load frames into the playback channel before the start of playback. In a system where the Host deliberately introduces delay into the channel to smooth an uneven data transmission rate, this feature allows the Host to utilize the CT8022 internal buffer space to store the *speech reservoir* used for smoothing.

7.6 Variable Buffer Depth

The CT8022 includes 480 bytes each of buffer space for the playback (*transmit*) and record (*receive*) queues. In A-law/μ-law or 8-bit mode, this is sufficient for two 240-byte μ-law frames (60ms delay) or 15 32-byte TrueSpeech 8.5 frames (450ms delay). In 16-bit mode, this space can hold only a single 480-byte frame (30ms). By default, the CT8022 will use all of this space. However, the Host may wish to limit the amount of buffering the CT8022 uses in order to limit the maximum amount of delay in the speech channel. The CT8022 includes functions to set a limit on the effective buffer depth, which is lower than the physical size for just this purpose.

7.7 Silence Generation During Transmit (Playback) Data Under-run

If data under-run occurs during playback, the **transmit** buffer becomes empty and the CT8022 will default to repeatedly outputting the most recent speech frame up to a (default) limit of 8 times. This behavior is appropriate to mask a short 1 or 2-frame period in which playback data is not available. Repeating the most recent frame once or twice causes the least perceptible break in the playback continuity. However, if the data under-run condition persists for a longer period, the repeated playback of a single frame can be annoying to the user. The Host can program the auto-repeat limit in the range of 1-15. Programming the auto-repeat limit to zero will cause auto-repeat to operate continuously. When the auto-repeat limit is exceeded, the CT8022 will output silence until more playback data becomes available.

With the G.723.1 and G.729A coders, the Host may elect to trigger the frame erasure mechanism instead of using the auto-repeat feature.

7.8 Inserting Silence Frames during TrueSpeech Playback

The CT8022 will interpret TrueSpeech 8.5-4.1 data frames that have all words set to zero as silence frames. Each time the CT8022 receives an all-zero TrueSpeech frame, it will output 30ms of silence. This applies to all five TrueSpeech Rates - 8.5, 6.3, 5.3, 4.8 and 4.1. Note that this is a CT8022-specific feature. It is not a part of the standard TrueSpeech or G.723.1 implementation. The G.729A speech coder reserves the all-zero speech frame for use in triggering frame erasure.

8 Test Modes

The CT8022 supports special modes of operation to facilitate both in-system testing of the device itself, and as an aid to external system testing.

8.1 Test Mode 1: Count Mode

In this test mode, data received from the external A-law/μ-law CODEC by the *record* channel is discarded and replaced by an incrementing count. This test mode is intended for use in A-law/μ-law speech mode where the CODEC *receive* data is passed directly to the Host (without compression, and with *record* volume set to nominal).

8.2 Test Mode 2: Digital Milliwatt

In this test mode, data received from the external μ-law CODEC by the *record* channel is discarded and replaced by the CCITT G.711 A-law/μ-law digital milliwatt (0 dBm0) code sequence. This is a sequence of 8 repeating bytes (A-law μu-law samples) representing a 1 KHz sinewave at 0 dBm0. Selection between A-law and μ-law is made using the CODEC configuration command. Digital milliwatt operation is not supported for use with a 16-bit linear CODEC.

8.3 Test Mode 3: Internal Loopback

In this test mode, data received from the external A-law/μ-law CODEC by the *record* channel is discarded and replaced by the output data from the *transmit* (playback) channel. This mode of operation does not affect the playback channel. The playback speech data is transmitted to the output CODEC.

The Host can perform *receive* CODEC-to-*transmit* CODEC loopback with the CT8022 operating in normal mode. To do this, the Host simply copies frames from the record (*receive*) channel back to the playback (*transmit*) channel using A-law, μ-law, or 16-bit linear modes as appropriate.

8.4 CODEC Loopback and Monitoring

The CT8022 also supports CODEC loop-back and monitoring configurations.

9 CT8022 Host Control Protocol

9.1 Operational Modes

It is possible to operate the CT8022 in eight main modes:

- **Idle Mode**
  In this mode, the CT8022 *transmit* and *receive* buffers are empty. Data from the *receive* CODEC is ignored, silence is output to the *transmit* CODEC.
- **Playback Mode**
  In this mode, the playback buffer is active and the TrueSpeech frame decompression function operates (if in TrueSpeech mode). The Host should provide data for output in this mode. If no data is available, the most recent frame present in the playback buffer is replicated, and output until new data is available. By default, speech is output via CODEC 1.
- **Record Mode**
  In this mode, the *record* buffer is active and the TrueSpeech compression function inserts speech frames into the *record* buffer (if in TrueSpeech mode). The Host should extract frames from the CT8022 in this mode. If the Host does not take data from the CT8022, the record buffer will fill, and then frames will be discarded. By default, speech is input via CODEC 1.
- **Full Duplex Speech Mode**
  This mode is equivalent to the *playback* and *record* modes operating concurrently.
- **CODEC Loopback Mode**
  This mode provides a test mode which enables CODEC-input to CODEC-output loopback.
- **Line Monitor Mode**
  In this mode, the CT8022 provides DTMF and Call Progress Tone detection. These services are also available during record and playback operations.
- **Full Duplex Speech Mode plus Acoustic Echo Canceller (AEC) (DSVD Speakerphone Mode)**
  In this mode, the AEC is active and attempts to remove the acoustic echo of the speaker output that is picked up at the microphone input.
- **Full Duplex (Standalone) Speakerphone Mode**
  In this mode, the CT8022 operates as a Full Duplex Speakerphone using an analog telephone line connection. This requires operation with two external CODECs. The CODEC0 connection must be used for the telephone line audio (*analog*) input/output. The CODEC1 connection must be used for the speaker-microphone audio input/output. In Full-Duplex Speakerphone mode, the CT8022 attempts to cancel the speaker-to-microphone acoustic echo and also the telephone line transmit to telephone line receive electrical echo.

Note: The terms *Standalone Speakerphone* and *DSVD Speakerphone* are used throughout this document to distinguish between conventional analog telephone Speakerphone operation and Speakerphone operation in a *hands-free* DSVD or Video Conferencing system (compressed digital speech via a modem or LAN).

9.2 Basic Protocol

The Host controls the CT8022 via a command-response protocol. For each command the Host writes to the CT8022, the CT8022 will generate a status response. The Host should read the response before issuing the next command.

Commands are written to the CT8022 via the Software Control Register (SCR). The CONTROL READY bit in the Hardware Status Register (HSR) is set to indicate that the CT8022 is ready to accept a command. The Host should only write to the Software Control Register when the CONTROL READY bit is set. The CT8022 will respond to the command by writing a status response to the Software Status Register (SSR). The Host should wait for the STATUS READY bit in the Hardware Status Register to be set before reading from the Software Status Register. Reading from the Software Status Register will clear the STATUS READY bit.

Commands to the CT8022 always result in an acknowledgment via the Software Status Register. The CT8022 registers are 16-bit. The Host accesses these registers using two 8-bit cycles: *low* byte and then *high* byte.

The response time for most commands is usually in the 5-10 **microsecond** range. However there are a small number of commands with significantly longer response times of up to 50-60 **milliseconds**. Notable examples of this are the commands for starting playback and record, where the command delays its response in order to synchronize with the internal speech frame period. Detailed information is provided with the individual command descriptions.

Note: Actual command value constants are presented in expanded 16-bit binary form, and also where appropriate in hexadecimal form with the *X* value used to indicate user-selected values. For example, the command 10XXH indicates that the *base* command is hexadecimal 1000H, but that the least significant eight bits of the 16-bit command are user-selected, depending on the command options desired.

9.3 Reset & Start-up Sequence

After Reset, the CT8022 performs internal initialization operations and then sets the CONTROL READY bit in the Hardware Status Register. The Host should wait for this bit to be set before issuing the first command. After initialization, the CT8022 enters IDLE mode and awaits a command from the Host. The Host should program the CODEC configuration before attempting further operations.

Operating Start-up Sequence:

1. Power-on or Reset
2. Host polls Hardware Status Register and waits for CONTROL READY indication.
3. Host writes first command (IDLE = 0000H) to Software Control Register.
4. CT8022 generates command response (0000H) and sets STATUS READY.
5. Host waits for STATUS READY then reads response from Software Status Register.
6. Host writes CODEC configuration command(s) to Software Control Register
7. CT8022 configures the CODEC (master/slave, A-law/μ-law/16-bit and sample rate) and generates a status response.
8. Host waits for STATUS READY then reads response from Software Status Register.

Optional:

9. Host writes Get Device Identification Code = 3400H to the Software Control Register.
10. CT8022 responds with device code = 8021H and sets STATUS READY.
11. Host waits for STATUS READY then reads response from Software Status Register.

9.4 Idle

Command: 0000H

Status: 0000H

The ***Idle*** command instructs the CT8022 to enter IDLE mode. If the CT8022 is in Record, Playback, Full Duplex, or Speakerphone modes, speech processing is stopped. In IDLE mode, the CT8022 performs no processing except to wait for a command from the Host.

Idle should be the first command written to the CT8022 following reset.

9.5 Codec Configuration

9.5.1 CODEC Configuration Command

The CT8022 supports connection to two external G.711 A-law, μ-law or 16-bit linear CODECs, labeled CODEC0 and CODEC1. When two CODECs are used, both CODECs must be of the same type. CODEC 1 is normally required for DSVD operation (*record/playback*). CODEC 0 is optional, and is required only for standalone Speakerphone mode. The data source for the *record* channel can be selected to be either CODEC. The data output for the *playback* channel can be selected to go to either CODEC, or both CODECs simultaneously.

Note: After Reset, the Host *must* program the CODEC configuration before attempting any other operations (with the exception of Host-to-Host compression/decompression). Certain CODECs may impose additional restrictions on the choice of the CT8022's external crystal or clock source frequency.

Command C1 (= C4XXH or C5XXH):

1100	010	Width	Law	Master	Long	OUTPUT CODEC	INPUT CODEC	Set Rate	0
(15-12)	(11-9)	(8)	(7)	(6)	(5)	(4-3)	(2)	(1)	0

Status S1:

1100	010	Width	Law	Master	Long	OUTPUT CODEC	INPUT CODEC	Set Rate	0
(15-12)	(11-9)	(8)	(7)	(6)	(5)	(4-3)	(2)	(1)	0

Command C2 (only if Set Rate = 1, not required for slave mode operation):

WIDE	FSYNC_RATE	CO_RATE
(15)	(14-5)	(4-0)

Status S2 (only if Set Rate = 1):

WIDE	FSYNC_RATE	CO_RATE
(15)	(14-5)	(4-0)

Width:	0:	selects 8-bit A-law or μ-law CODEC
	1:	selects 16-bit linear CODEC
Law:	0:	selects external μ-law CODEC
	1:	selects external A-law CODEC (also affects μ-law/A-law selection of RECMODE and PLAYMODE)
Master:	0:	selects slave mode (FSYNC and SCLK are inputs - default after reset)
	1:	selects master mode (FSYNC and SCLK are outputs)
Long:	0:	selects short frame sync mode when WIDE=0
	1:	selects long frame sync mode when WIDE=1
OUTPUT CODEC:	00:	default output CODEC routing (playback to CODEC 1)
	01:	output signal goes to CODEC 1 only
	10:	output signal goes to CODEC 0 only
	11:	output signal goes to both CODEC 0 and CODEC 1
INPUT CODEC:	0:	normal input CODEC routing (record from CODEC 1)
	1:	input from CODEC 0 and CODEC 1 are exchanged (record from CODEC 0)
Set Rate:	0:	no action
	1:	next command word programs CODEC sample rate dividers
CO_RATE:	This field sets the division factor used to divide the main 45.056 MHz CT8022 clock to generate SCLK. Division factor is (CO_RATE+1). For example, 45.056 MHz/(21+1) = 2.048 MHz SCLK. The 45.056 MHz main clock is normally generated by the x11 PLL from an external 4.096 MHz crystal or clock input. CO_RATE must be greater than 4 (master mode only).	
FSYNC_RATE:	This field sets the division factor used to divide the SCLK clock to generate FSYNC. Division factor is (FSYNC_RATE+1). For example, 2.048 MHz/(255+1) = 8.0 KHz. F_SYNC_RATE must be greater than 17 (master mode only).	
WIDE:	0:	FSYNC is 1 SCLK period wide
	1:	FSYNC is 8 SCLK periods wide if Width=0 or 16 SCLK periods wide if Width=1. Note that setting the WIDE bit to 1 only has an effect if the LONG bit is also set.

Before entering Standalone Speakerphone mode, Output CODEC must be set to 00 and Input CODEC set to 0.

9.5.2 Sample CODEC Configurations

C1	C2	SCLK	FSYNC	Description
C442H	1FF5H	2.048 MHz	8.000 KHz	Texas Instruments μ-law TP3054 CODEC Short Frame Sync pulse Master Mode CO_RATE = 21 FSYNC_RATE = 255 external crystal = 4.096 MHz
C542H	1FF5H	2.048 MHz	8.000 KHz	AT&T 16-bit linear CODEC T7525 Short Frame Sync pulse Master Mode CO_RATE = 21 FSYNC_RATE = 255 external crystal = 4.096 MHz
C462H	9FF5H	2.048 MHz	8.000 KHz	OKI Semiconductor μ-lawmsM7543 CODEC Long (+ wide) Frame Sync pulse Master Mode CO_RATE = 21 FSYNC_RATE = 255 external crystal = 4.096 MHz

Notes:

The AT&T T7525 16-bit linear CODEC *requires* that the FSYNC frequency be exactly 1/256 of the SCLK frequency. When using this CODEC, the FSYNC_RATE value *must* be set to 255. In order to accommodate this requirement, when operating in Master Mode, the CT8022 *must* be driven from a crystal or clock source that is an exact multiple of 2.048 MHz (so that FSYNC operates at 8KHz).

For 8-bit CODECs the SCLK frequency must be at least equal to FSYNC x 16.

For 16-bit CODECs the SCLK frequency must be at least equal to FSYNC x 32.

Other CODECs may permit a range of values for the FSYNC to SCLK ratio. However, for some CODECs (e.g. TP3054 or TP3057) the actual usable range of ratios may depend on selection of the default or nominal ratio, based on certain control pins. Depending on the operational mode selected, the TP3054 and TP3057 can support nominal ratios of 1:256, 1:193 and 1:192, using nominal 2.048 MHz, 1.544 MHz and 1.536 MHz values for SCLK (for 32-channel, E1 mode or 24-channel, T1 mode). Informal tests have shown that the CODECs can support ratio ranges of at least +/- 5% centered on these nominals.

The PLL multiplication factor used to scale the XIN frequency is 11 for the CT8022. With a 4.096 MHz crystal or clock at XIN and the PLL enabled, the CT8022 will operate at 45.056 MIPS.

9.6 Setting the Base Frame Size

The CT8022 supports programmable base frame sizes to allow operation with different speech compression algorithms that may operate on different fundamental frame sizes and frame periods (e.g. 30ms or 10ms). The following table shows the base frame sizes recommended for different speech compression algorithms in combinations with various other CT8022 features. Note that the higher processing overhead incurred when operating on smaller speech frames leaves less processing resources available for the operation of additional features like AEC. The *fundamental* frame and period sizes shown are the basic sizes of the corresponding speech compression algorithm.

Speech Compression Type	Fundamental Algorithm Frame Size (Samples)	Fundamental Frame Period (Milliseconds)	Minimum Base Frame Size Recommend For Operation With The CT8022 (Samples) See Note 1	Minimum Frame Period Recommended For Operation With The CT8022	Compressed Speech Block Size (16-Bit Words)
G.723.1 6.3/5.3 (all feature combinations)	240	30ms	240	30ms	12/10
TrueSpeech 8.5 (all feature combinations)	240	30ms	240	30ms	16
TrueSpeech 4.8/4.1 (all feature combinations)	240	30ms	240	30ms	9/8
G.729A+B 8 KBPS	80	10ms	80	10ms	6 (includes 1 word frame type indicator)
G.722 KHz wideband 64KBPS ADPCM			80	10ms	40

Note 1: For correct operation of the CT8022, the base frame size selected must be an integer multiple of the fundamental frame size for the speech compression algorithm(s) used.

Note 2: Transfers of compressed speech data between the Host controller and the CT8022 should be made via the CT8022's Transmit/Receive Data Buffer. Use of the CT8015-style transfer protocol consumes additional CT8022 processing resources during data transfer, leaving less processing power available for compression + AEC etc.

G.729 Annex A operates at exactly 8.0 Kbits/sec. With a 10ms frame size, this rate should produce 80 bits every 10ms. 80 bits of data requires exactly five 16-bit words. However, with the inclusion of the G.729 Annex B VAD/CNG *silence* compression, the combined G.729AB coder can produce three different types of speech frame. These are the normal speech 80 bit speech frame, a 16-bit *noisy silence* frame, and a *no transmit* indication frame. For the CT8022 to indicate the G729AB frame type, an extra frame type indicator word is added at the beginning of each speech block so that the total size of each compressed speech block is 6 words instead of 5.

The base frame size selected affects the operation of the entire CT8022 device. The same base frame size is used for both the record and playback channels.

The DTMF and Call Progress Tone detectors themselves are designed to operate with frame sizes of 30, 20 or 10ms. The status from these detectors is updated and reported after every frame processed, regardless of the actual frame size.

To set the base frame size use the following command:

Command 07XXH

Status 07XXH or 0000H

Where XX selects the desired frame size (for example 07F0H selects a base frame size of 240 (decimal) for 30ms operation, 0750H selects a base frame size of 80 (decimal) for 10ms operation)

Note that the base frame size can only be changed when the CT8022 is in the Idle state and the AEC is in the *Off* state. The Host must ensure that the base frame size selected matches the requirements of the speech compression algorithms that the Host activates. If the command to set the base frame size is completed successfully, the status response is 07XXH, echoing the command sent. If an attempt is made to change the base frame size when the CT8022 is not in the Idle state, the status response will be 0000H and the actual base frame size in the device is not changed.

For the uncompressed modes (G.711 μ-law/A-law, and 8-bit and 16-bit linear) any frame size may be used. Changing the frames size also causes corresponding changes in the size of the data block transferred to the Host:

Uncompressed Data Type	Frame Size Selected	Size Of Data Transfer Block (16-Bit Words)
16-bit linear	240 (30ms XX=F0)	240
16-bit linear	160 (20ms XX=A0)	160
16-bit linear	80 (10ms XX=50)	80
8-bit linear/μ-law/A-law	240 (30ms XX=F0)	120
8-bit linear/μ-law/A-law	160 (20ms XX=A0)	80
8-bit linear/μ-law/A-law	80 (10ms XX=50)	40

9.7 Record

Command (C1 = 1XXXH):

0001	11	RECMODE	0	0	000	TFR Mode
(15-12)	(11-10)	(9-7)	(6)	(5)	(4-2)	(1-0)

Status (S1):

0001	11	RECMODE	0	0	000	TFR Mode
(15-12)	(11-10)	(9-7)	(6)	(5)	(4-2)	(1-0)

9.7.1 Transfer Mode

The TFR Mode field selects the mode of data transfer used:

TFR Mode	Data Transfer Mode
00	Data Transfer via Software Command and Status Registers (CT8015/CT8005 protocol mode). See sections 6 (***Host Data Transfer Modes***) and 9.7.4 (***Record Protocol***). Not recommended for new designs.
01	Reserved
10	Reserved
11	Data Transfer via Host Transmit Data Buffer Access Port. Poll Sync Mode should be selected when using this data transfer option. This data transfer mode must be selected if performing DMA transfers using the TXDREQ and TXDACKN signals. See section on Host Data Transfer Modes and Record Protocol.

The following C2, C3 and Data Transfer commands are required *only* if TFR Mode = 00 (CT8015/CT8005 protocol mode). See section 9.7.4. These commands are used only if transferring speech data via the Software Control and Status Registers.

For new designs using TFR Mode = [binary] 11 is recommended.

Command (C2 = 1000H):

0001	0000	0000	0000
(15-12)	(11-8)	(7-4)	(3-0)

Status (S2):

0001	F3	F2	F1	F0	0	PEAK	DTMF VALID	CPF VALID	DTMF DIGIT
(15-12)	(11)	(10)	(9)	(8)	(7)	(6)	(5)	(4)	(3-0)

Command (C3 =10XXH):

0001	0000	REQUEST NUMBER OF WORDS TO TRANSFER
(15-12)	(11-8)	(7-0)

Status (S3):

0001	0000	**ACTUAL** NUMBER OF WORDS TO TRANSFER
(15-12)	(11-8)	(7-0)

The NUMBER OF WORDS TO TRANSFER should be set either to the (compressed) frame size of the selected speech mode, or to zero to indicate no transfer is to take place. The ACTUAL NUMBER OF WORDS TO TRANSFER will be the compressed frame size if data is available for transfer, or it will be zero to indicate that no data is available.

Data Transfer Command:

0001	0000 0000 0000
(15-12)	(11-0)

Data Transfer Status:

16-bit speech data word
(15-0)

9.7.2 Recording Modes

RECMODE	Frame Size (Words)	Recording Modes
000	48-4	Compressed Speech: TrueSpeech (8.5, G.723.1 6.3/5.3, 4.8 and 4.1) etc. See: Select TrueSpeech/G.723.1 Record Rate
001		Reserved
010		Reserved
011		Reserved
100	120	64 Kbits/sec A-law/μ-law PCM (120 words per 30ms data frame)
101	240	128 Bit/sec 16-bit linear (240 words per 30ms data frame)
110	120	64 Kbits/sec 8-bit signed linear (120 words per 30ms data frame)
111	120	64 Kbits/sec WSS 8-bit unsigned linear (120 words per 30ms data frame)

Notes:

All data rates assume that the CODEC connected to the CT8022 operates at 8000 samples/sec

The 30ms frame interval is based on counting 240 samples from the CODEC. Refer to the section on setting the base frame size

Mode 100, PCM A-law/μ-law is a *pass- through* mode, where the data from the CODEC is passed to the Host entirely unmodified, (if the record volume is set to 0100H).

16 bit linear data is signed integer (2's complement form), positive full scale is 7FFFH, negative full scale is 8000H, zero is 0000H

8 bit linear data is signed byte (2's complement form), positive full scale is 7FH, negative full scale is 80H, zero is 00H

8-bit linear WSS data is unsigned byte, positive full scale is FFH, negative full scale is 00H, and 0 is 80H. This is the format used for 8-bit WAVE format data (Microsoft Windows Sound System). Data can be converted between the two 8-bit signed/unsigned formats by simply inverting them.

The compressed speech rate for TrueSpeech 8.5,6.3/5.3 (G.723.1), 4.8 or 4.1 KBPS etc. is selected using the Select TrueSpeech Rate command

Selection between A-law/μ-law is made using the CODEC configuration command. With an external μ-law CODEC configured, RECMODE = 100 selects μ-law data. With an external A-law CODEC configured, RECMODE = 100 selects A-law data.

The RECMODE and PLAYMODE bit assignments are different. See Playback command (Section 9.8)

9.7.3 Peak Level Indication

The PEAK bit in the S2 status response is set if the average input level for the current speech frame exceeds the threshold configured using the ***Set Peak Threshold*** command. The Host can use this bit to perform silence detection during recording. Note that the ***record*** signal level can also be accessed using the ***Read Record Level*** command. This is the recommended method of determining the ***record*** input signal level, when TFR Mode = [binary] 11 and the C2-S2, C3-S3 sequence is not used.

9.7.4 Record Protocol

Example 1: TrueSpeech 6.3 Record via Host Receive Data Buffer Access Port - Host Polling
This example shows how to start recording using TrueSpeech 6.3 with data transfers performed via the Host Receive Data Buffer Access Port. The Host controller performs all data transfers in this example. The Host polls the Hardware Status Register to synchronize data.

Starting Record

1. CT8022 is in IDLE or PLAYBACK state.
2. Host checks for CONTROL READY state in Hardware Status Register.
3. Host selects TrueSpeech 6.3 recording by writing the Select TrueSpeech Record Rate command = 5131H to the Software Control Register.
4. CT8022 responds via the Software Status Register
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.
6. Host selects Poll Sync Mode for record using the command 5102H.
7. CT8022 responds via the Software Status Register.
8. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.
9. Host selects Record by issuing the RECORD C1 command = 1C03H via the Software Control Register. This also informs the CT8022 that data transfers will occur via the Host Receive Data Buffer Access Port (TFR Mode = [binary] 11).
10. CT8022 performs internal synchronization then responds with the RECORD S1 status response after a delay of up to 2 speech frame periods.
11. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.
12. The CT8022 is now in record mode. The CT8022 will produce a compressed speech frame every 30ms (assuming the base frame size is set to 240). The following sequence is used to transfer each compressed speech data frame from the CT8022 to the Host:
    a. Host waits for the RX Ready bit to be set in the Hardware Status Register
    b. Host reads 12 words (for TrueSpeech 6.3) from the Host Receive Data Buffer Access Port.

Note: For transfer of speech blocks larger than 16 words via the Host Receive Data Buffer Access Port, the transfer will be split into sub-blocks of 16 words each or less. The CT8022 will create a small pause between each sub-block during which it will re-fill the data access port (approximately 5 microseconds).

Terminating Record

1. Host writes IDLE = 0000H command or STOP RECORD = 5120H command to the Software Control Register.
2. CT8022 terminates record and clears RX Ready if set (in Hardware Status Register).
3. CT8022 writes status response to Software Status Register.
4. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.

Note: After writing the *Idle* or *Stop Record* command to terminate recording, the Host should not attempt to access the Host Receive Data Buffer Access Port even if the RX Ready bit is set.

Example 2: TrueSpeech 5.3 Record via Host Receive Data Buffer Access Port - Host Interrupt

This example shows how to start recording using TrueSpeech 5.3 with data transfers performed via the Host Receive Data Buffer Access Port. The Host controller performs all data transfers in this example. The Host uses an interrupt service routine (ISR) to transfer data.

Starting Record

1. CT8022 is in IDLE state or PLAYBACK.
2. Host checks for CONTROL READY state in Hardware Status Register.
3. Host selects TrueSpeech 5.3 recording by writing the Select TrueSpeech Record Rate command = 5132H to the Software Control Register.
4. CT8022 responds via the Software Status Register
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.
6. Host selects Poll Sync Mode for record using the command 5102H.
7. CT8022 responds via the Software Status Register.
8. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.
9. Host selects Record by issuing the RECORD C1 command = 1C03H via the Software Control Register. This also informs the CT8022 that data transfers will occur via the Host Receive Data Buffer Access Port (TFR Mode = [binary] 11).
10. CT8022 performs internal synchronization then responds with the RECORD S1 status response after a delay of up to 2 speech frame periods.
11. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.
12. Host sets up an ISR to service interrupts from the CT8022.
13. Host programs the Hardware Control Register to generate an interrupt from the CT8022 on the RX Ready condition by writing 0401H (Master Enable set, RX Ready IE set).
13. The CT8022 is now in record mode. The CT8022 will produce a compressed speech frame every 30ms (assuming the base frame size is set to 240). The following sequence is used by the Host ISR to transfer each compressed speech data frame from the CT8022 to the Host:
    a. Host gets interrupt from CT8022 (optionally checks that RX Ready is set).
    b. Host reads 10 words (for TrueSpeech 5.3) from the Host Receive Data Buffer Access Port.

Terminating Record

1. Host disables interrupts from the CT8022 by writing 0000H to the Hardware Control Register.
2. Host writes IDLE = 0000H command or STOP RECORD = 5120H command to the Software Control Register.
3. CT8022 terminates record and clears RX Ready if set (in Hardware Status Register).
4. CT8022 writes status response to Software Status Register.
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.

Note: After writing the IDLE or STOP RECORD command to terminate recording, the Host should not attempt to access the Host Receive Data Buffer Access Port even if the RX Ready bit is set.

Example 3: Linear 16-bit Record via Host Receive Data Buffer Access Port - Using DMA

This example shows how to start recording in uncompressed 16-bit Linear Format Speech with data transfers performed via the Host Receive Data Buffer Access Port. An external DMA controller performs all data transfers in this example.

Starting Record

1. CT8022 is in IDLE state or PLAYBACK state.
2. Host checks for CONTROL READY state in Hardware Status Register.
3. Host selects Poll Sync Mode for record using the command 5102H.
4. CT8022 responds via the Software Status Register.
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.
6. Host selects Record by issuing the RECORD C1 command = 1E83H (RECMODE = [binary] 101) via the Software Control Register. This also informs the CT8022 that data transfers will occur via the Host Receive Data Buffer Access Port (TFR Mode = [binary] 11).
7. CT8022 performs internal synchronization then responds with the RECORD S1 status response after a delay of up to 2 speech frame periods.
8. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.
9. Host programs external DMA controller to accept DMA requests from the CT8022 (See DMA Direction bit in Hardware Control Register). Host configures a data buffer in the Host memory to receive the DMA-ed speech data. The DMA memory buffer should be an integral multiple of the speech frame size. In the case of uncompressed 16-bit Linear, this should be N*480 (bytes).
10. Host sets up an ISR to handle an end-of-transfer (EOT) interrupt from the DMA controller when it reaches the end of the DMA buffer. Alternatively, if the DMA supports circular-buffering (auto-initialize), the Host can poll the DMA to determine when the end of the buffer is reached.
11. Host programs the Hardware Control Register to generate a DMA request from the CT8022 on the RX Ready condition by writing 0050H (RX DMA Burst Mode, RX DMA enable) - or 0150H (RX DMA Burst Mode, RX DMA enable, DMA Direction bit set).
12. The CT8022 is now in record mode. The CT8022 will produce a uncompressed speech frame every 30ms (assuming that the base frame size is set to 240). The following sequence occurs between the CT8022 and the DMA controller to transfer data:
    a. CT8022 has 240 word (480 byte) uncompressed 16-bit speech data frame ready for transfer.
    b. CT8022 transfers first 16 words into the Host Receive Data Buffer.
    c. CT8022 asserts RX Ready.
    d. RX Ready drives RXDREQ.
    e. DMA controller responds to RXDREQ by asserting RXDACKN.
    f. DMA controller performs a burst transfer of 16 words (32 bytes) from the CT8022 to the Host DMA memory buffer.
    g. CT8022 de-asserts RX Ready.
    h. CT8022 transfers next 16 words into the Host Receive Data Buffer.
    i. CT8022 asserts RX Ready.
    j. RX Ready drives RXDREQ.
    k. DMA controller responds to RXDREQ by asserting RXDACKN.
    l. DMA controller performs a burst transfer of 16 words (32 bytes) from the CT8022 to the Host DMA memory buffer.
    m. CT8022 de-asserts RX Ready.
    n. Repeat a-f until all 240 words of the speech data frame have been transferred.

The Host processor also needs to supervise the operation of the DMA controller and arrange for the transfer of the *DMA-ed* data to its final destination (e.g. transfer to disk). When the DMA controller reaches the end of the DMA buffer, the Host must process the data (transfer data to disk). The Host can arrange to receive an EOT interrupt from the DMA controller, or it can periodically poll the DMA's internal transfer count register to determine the status of the DMA.

Terminating Record

1. Host disables DMA requests from the CT8022 by writing 0000H to the Hardware Control Register.
2. Host writes IDLE = 0000H command or STOP RECORD = 5120H command to the Software Control Register.
3. CT8022 terminates record and clears RX Ready if set (in Hardware Status Register).
4. CT8022 writes status response to Software Status Register.
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.

Note: After writing the *Idle* or *Stop Record* command to terminate recording, the Host/DMA should not attempt to access the Host Receive Data Buffer Access Port even if the RX Ready bit is set. When *cleaning up* at the end of recording, the Host should ensure that any partial frame at the end of the recording is discarded. When the recorded data is sent back to the CT8022 for playback, the CT8022 can playback only complete frames. It is recommended that the Host synchronize the termination of recording with the end of transfer of a complete speech frame. This synchronization can be achieved by examining the DMA's transfer count register, or by performing the final speech data frame transfer using the Host processor.

Example 4: TrueSpeech 8.5 Recording using CT8005/CT8015 protocol via Software Control and Status Registers.

This example shows how to perform TrueSpeech 8.5 recording with TFR Mode = 00 using the CT8015-compatible protocol. Data is transferred via the Software Control and Status Registers. The Host processor performs all data transfers. The example shown uses the CT8015 Poll Sync Mode.

1. CT8022 is in IDLE or PLAYBACK state.
2. Host checks for CONTROL READY state in Hardware Status Register.
3. Host selects TrueSpeech 8.5 recording by writing the Select TrueSpeech Record Rate command = 5130H to the Software Control Register.
4. CT8022 responds via the Software Status Register
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.
6. Host selects Poll Sync Mode for record using the command 5102H.
7. CT8022 responds via the Software Status Register.
8. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.
9. Host writes Record C1 command = 1C00H (TrueSpeech 8.5) to the Software Control Register.
10. CT8022 activates record mode and performs internal synchronization (1-2 frame delay).
11. CT8022 responds with Record status S1 = 1C00H.
12. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.
13. **Host sends Record C2 command = 1000H.**
14. **CT8022 responds with Record S2 status = 10X0H, where X is defined by the PEAK bit state.**
15. **Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.**
16. **Host sends Record C3 with the number of (16 bit) words it wishes to transfer = 1010H.**
17. **CT8022 checks number of words ready to transfer.**
18. **CT8022 responds with Record S3 = 1000H or 1010H. If number of words is not zero DATAFLAG/ signal is asserted to indicate the beginning of data transfer.**
19. **Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.**
20. **If number of words to transfer is zero (S3 = 1000H), Host goes back to step 13.**
21. **Optional: Host waits for DATAFLAG/ signal to be asserted**
22. **Host writes data transfer command = 1000H to Software Control Register**
23. **CT8022 responds with 16-bit data word in Software Status Register**
24. **Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.**

25. Repeat steps 22-24 until all (16) data words are transferred
26. CT8022 de-asserts DATAFLAG/ signal to indicate the end of data transfer
27. Optional: Host waits for DATAFLAG/ to be de-asserted
28. Repeat steps 13-27 until recording finished

To end recording, Host writes ***Idle*** command or ***Record Stop*** command and waits for status response.

Note: Bold text indicates the record software data transfer loop. By default, The DATAFLAG signal on external pin GPIO0 is disabled. Refer to Section 9.25 for more information regarding GPIO pins.

9.7.5 Select TrueSpeech/G.723.1 Record Rate

This command allows the Host to select the TrueSpeech data rate used in Compressed Record mode. The standard (built-in) available CT8022 rates are TrueSpeech 6.3, 5.3, 4.8 and 4.1. This command should be issued prior to starting record using the ***Record*** command. The TrueSpeech Record Rate remains in effect until the next TrueSpeech ***Record Rate*** command.

Command (513XH):

0101	0001	0011	RATE
(15-12)	(11-8)	(7-4)	(3-0)

Status (513XH):

0101	0001	0011	RATE
(15-12)	(11-8)	(7-4)	(3-0)

RATE	TrueSpeech Compression Rate	Compressed Frame Size (16-bit words)
0	8.5 (**see Note**)	16
1	6.3 (G.723.1) (default)	12
2	5.3 (G.723.1)	10
3	4.8	9
4	4.1	8
5	Reserved	
6	G.729AB (**see Note**)	6 (10ms)
7	G.722 (**see Note**)	40 (10ms)
8-15	Reserved	

The Frame Size value indicates the number of 16-bit words in a compressed speech frame for each coding rate. When any of the TrueSpeech compression rates is selected, the frame size is always 16 words or less. Since the size of the CT8022 hardware buffer within the Host port is 16 words, the Host can *burst read* the complete speech frame of 16-8 words without checking the RX Ready bit before each individual word is read. Where the frame size is larger than 16 words, the CT8022 splits the data transfer into sub-blocks of 16 words or less.

Note: The CT8022 supports the G.729-A/B and G.722 coders only as external downloadable software expansion modules. The Host must ensure that the appropriate module is loaded to the CT8022 external program/data memory before attempting to activate any of these coders. Contact DSP Group for details on availability for these coders.

9.7.6 Enable VAD

The G.723.1/TrueSpeech 6.3, 5.3, 4.8 and 4.1 rates support Voice Activity Detection (VAD) and Comfort Noise Generation (CNG) as defined in the ITU-T G.723.1 Annex A specification. This provides a form of built-in *silence compression*. On the *speech encode* (record) side, the VAD feature can be selectively enabled or disabled. On the *decode* (playback) side, CNG is automatic and is triggered by specially formatted speech frames that are generated by the encoder when VAD is enabled. By default, the encoder VAD is disabled.

Note: The size of the physical data transfer performed for each speech frame when reading or writing to the CT8022 is determined by the initial speech mode selection. For example, if the *record* session is started in 6.3 mode, then all data transfers will consist of 12 word frames. The VAD/CNG frames containing a smaller amount of significant data (2 words or 2 bits) have the unused portions of the frame padded with zeros.

To enable VAD:

Command	513FH
Status	513FH

To disable VAD:

Command	513EH
Status	513EH

9.7.7 Dynamic Switching between TrueSpeech/G.723.1 6.3 and 5.3

The CT8022 supports on-the-fly switching between TrueSpeech 6.3 and 5.3 data rates as required by the ITU G.723.1 specification. To enable switching between these two rates, the RECORD operation *must* be started with the 6.3 rate selected. This sets the frame size used for CT8022-to-Host transfer to 12 words. When dynamically switching between the 6.3 and 5.3 rates the frame size remains fixed throughout the record process. The 12-word frame size is used for both the 6.3 and 5.3 speech data frames, although the 5.3 speech frame only contains 10 words. This prevents synchronization problems between the time at which the compression rate is changed and the time at which the compressed data is read out from the CT8022. When a 5.3 frame is read from the CT8022 Hardware Receive Buffers after on-the-fly switching from the 6.3 rate, the Host must read 12 words instead of 10. In this case, the last two words of data may be discarded.

Switching between the 6.3 and 5.3 rates is performed using the ***Select TrueSpeech Record Rate*** command (above). To support on-the-fly switching, the CT8022 will accept this command after the start of the *record* process. If the CT8022 is instructed to make an unsupported rate switch (for example, between TrueSpeech 6.3 and TrueSpeech 8.5), the status response from the ***Select TrueSpeech Record Rate*** command will be zero. The CT8022 *record* operation will continue to operate with the old TrueSpeech rate.

The two least significant bits of the first data word of a G.723.1 6.3 or 5.3 speech frame are encoded to indicate the speech frame type.

During playback (de-compression) the CT8022 will test the two least significant control bits only when the current Host-selected TrueSpeech rate is 6.3 or 5.3. In this case, the CT8022 will automatically perform the correct decoding of the speech frames independently of which rate the Host selected. To support on-the-fly switching for playback, playback must be started with the 6.3 rate selected.

This fixes the frame size used for Host-to-CT8022 transfer at 12 words. When transferring a 5.3 speech frame into the CT8022 when the 6.3 rate was initially selected, the Host should append two dummy words (zeros) at the end of the 10-word TrueSpeech 5.3 frame.

To switch between other speech rates, the Host must stop and re-start playback/record. The Host is responsible for synchronizing the rate switch between playback and record sources.

9.7.8 G.723.1 Frame Type Encoding

The two least significant bits of the first word of the TrueSpeech 6.3 and 5.3 frames are defined by the ITU-T G.723.1 v5.1 (final formal release) specification to indicate the speech data rate as shown:

Bit 1-0	Frame Type	Data Rate	Number of Significant Data Words
00	0	TrueSpeech 6.3 data frame (12 words)	12
01	1	TrueSpeech 5.3 data frame (10 words)	10
10	2	Silence/Comfort Noise Generation frame (only first two words contain useful data). All other data words are set to zero	2
11	3	Repeat last CNG frame (only two least significant bits of first data word are used). All other data words are set to zero	2 Bits

Compatibility Note:

The Bit 1-0 encoding of the CT8022 is different from that used in older firmware versions of the CT8020 which implemented pre-release versions of G.723.1, (firmware revisions 0109 and 0112 part numbers CT8020A11AQC and CT8020A11BQC). The full production release, CT8020D11AQC (firmware revision 0114) implements the final v5.1 G.723.1 release, as do all versions of the CT8022.

The Host can examine these two bits to distinguish between 6.3 and 5.3 frames (only) to determine the data rate and the number of valid data words in the frame. This bit encoding applies *only* to the 6.3 and 5.3 TrueSpeech frames. There is no bit encoding provided for the 8.5, 4.8 and 4.1 rates.

When implementing a real-time digital compressed speech link, the Host and data transport service should be able to transfer all four sub-types of speech frame end-to-end. The Host may take advantage of the smaller effective frame size of the silence frames by using the unused portion of the frame for transporting non-speech data. However, before writing the silence frames back to the decoder, the Host should restore the unused portions of the silence frames to zero.

The CT8022 implements additional non-standard frame encoding as follows:

A speech frame that consists of all zeros will be interpreted as an instruction to the playback channel to output pure silence for one frame period. This applies to all TrueSpeech rates, including 8.5, 6.3, 5.3, 4.8 and 4.1.

A speech frame that has the first two data words set to FFFFH, with the remaining words set to all zeros, will be interpreted as an instruction to activate the G.723.1 frame erasure mechanism. This should be used where the Host needs to instruct the CT8022 playback channel to replace a dropped or corrupt speech frame by extrapolating speech data from previous speech frames. This feature is available only with the TrueSpeech 6.3, 5.3, 4.8 and 4.1 data rates.

When reading or writing speech frames to or from the CT8022, the number of physical words transferred for each individual frame is fixed during each record/playback session. For example, if the record/playback session starts in 6.3 mode, then all frames will contain 12 words.

Frames that use less than this number of words for actual data will have the unused portion of the frame set to zero. This approach simplifies the coding of low-level driver software such that it does not need to deal with variable-sized data frames. This is particularly significant when dealing with DMA-type transfer.

9.7.9 Programming the Record Peak Threshold

The PEAK bit in the Record mode status S2 response can be used by the Host to implement silence detection during *record*. The PEAK bit is set whenever the average signal level for the most recent record frame is greater than the Input Peak Threshold. Although the CT8022 includes a record data frame buffer which can hold a number of record data frames, the PEAK indication provided always refers to the most recent frame recorded. In most cases, where the Host services the CT8022 record data frame buffer every frame period (30ms), there should never be more than one data frame in the buffer. The signal level measured is the input signal level before any scaling occurs due to the Record Volume Control or AGC.

Command C1 (CF99H):

1100 1111 1001 1	001
(15-3)	(2-0)

Status S1:

1100 1111 1001 1	001
(15-3)	(2-0)

Command C2:

Threshold Value
(15-0)

Status S2:

Threshold Value
(15-0)

The default Threshold Value is 0100H.

9.7.10 Reading the Record Level Value and Threshold Value

It is possible to read the programmed Threshold Value, together with the actual current frame average Level Value, using the following command:

Command (CF88H or CF89H):

1100 1111 1000 1	00X
(15-3)	(2-0)

Status:

Threshold or Level Value
(15-0)

Where X = 0 selects reading the Level Value.
X = 1 selects reading the Threshold Value.

The level value is calculated using the following algorithm:

LEVEL = 0

FOR each of 240 INPUT samples per frame

IF INPUT < 0 THEN INPUT = -1 * INPUT

LEVEL = LEVEL + INPUT

LEVEL = LEVEL/256

Note that this is an average signal level (not r.m.s.). Dividing by 256 instead of 240 leads to a slight understatement of the true average level. The fractional error is 240/256 = 0.9375, or 6.25%. Dividing by 256 instead of 240 requires less processing by the CT8022.

When the CT8022 is operated with a base frame size that is not set to 240, the level calculation is adjusted to report the same level as if the base frame size were set to 240. However, since the CT8022 will update and report the level for each frame processed, with a smaller base frame size, the CT8022 will report the level measured over a shorter period. This may result in more frame-by-frame variation in the signal level measured. When measuring the level of a signal with lower frequency components, or with a low frequency modulation, more *ripple* may be observed in the reported signal level. One example of this would be reporting the signal level of a 350+440 Hz dial tone.

9.7.10.1 Threshold Level Scale

The threshold level scale is relative to the maximum positive full-scale value of 7FFFH (decimal 32767). This corresponds to an input signal level of approximately + 3dBm0 from the external μ-law CODEC.

The precise input signal level scale can be calculated thus:

Input Level in dBm0 = +3.17 - 20 log(base 10) ((input level/32767) * 256/240)

so the default threshold level of 0100H = 256 decimal, corresponds to 44.753 dBm0.

To calculate the actual average input signal level, read the LEVEL from the device and then perform the following calculation:

CORRECTED LEVEL = (LEVEL * 256)/240

Input level in dBm0 = 3.17 - 20 * log10(CORRECTED LEVEL/32767)

9.8 Playback

Command (C1 = 2CXXH):

0010	11	000	PLAYMODE	00	TFR Mode
(15-12)	(11-10)	(9-7)	(6-4)	(3-2)	(1-0)

Status (S1):

0010	11	000	PLAYMODE	00	TFR Mode
(15-12)	(11-10)	(9-7)	(6-4)	(3-2)	(1-0)

9.8.1 Transfer Mode

The TFR Mode field is used to select the mode of data transfer:

TFR Mode	Data Transfer Mode
00	Data Transfer via Software Command and Status Registers (CT8015/CT8005 protocol mode). Refer to Section 6 (***Host Data Transfer Modes***) and Section 9.7.4 (***Record Protocol***).
01	Equivalent to TFR Mode 11, with the addition of strict maintenance of data frame alignment. Refer to Section 9.8.4 (***Playback Frame Alignment Using Transmit Data Buffer***) for more details. Not available in some older versions of the CT8020.
10	Reserved
11	Data Transfer via Host Transmit Data Buffer Access Port. Poll Sync Mode should be selected when using this data transfer option. This data transfer mode must be selected if performing DMA transfers using the TXDREQ and TXDACKN signals. Refer to Section 6 (***Host Data Transfer Modes***) and Section 9.7.4 (***Record Protocol***).

For new designs using TFR Mode = [binary] 11 or 01 is recommended.

The C2-S2, C3-S3 commands detailed below are used once at the beginning of playback (or Host-to-Host decompression) if TFR Mode = [binary] 11 or 01. If TFR Mode = 00, the C2-S2, C3-S3 commands are used to transfer playback speech data via the Software Control and Status Register.

The ***Data Transfer*** command is required only if TFR Mode = 00 (CT8015/CT8005 protocol mode). This command is used only if transferring speech data via the Software Control and Status Registers.

Refer to Section 9.8.3 (***Playback Protocol***).

Command (C2 = 2000H):

0010	0000	0000	0000
(15-12)	(11-8)	(7-4)	(3-0)

Status (S2):

0001	F3	F2	F1	F0	0	0	DTMF VALID	CPF VALID	DTMF DIGIT
(15-12)	(11)	(10)	(9)	(8)	(7)	(6)	(5)	(4)	(3-0)

Refer to Section 9.20 for information on CPF F3-0 and DTMF detection.

Command (C3= 20XXH):

0010	0000	REQUEST NUMBER OF WORDS TO TRANSFER
(15-12)	(11-8)	(7-0)

Status (S3):

0010	0	0	00	**ACTUAL** NUMBER OF WORDS TO TRANSFER
(15-12)	(11)	(10)	(9-8)	(7-0)

The NUMBER OF WORDS TO TRANSFER should be set either to the (compressed) frame size of the selected speech mode, or to zero to indicate no transfer is to take place. The ACTUAL NUMBER OF WORDS TO TRANSFER will be the compressed frame size if the device is ready to accept data for transfer, or it will be zero to indicate that the device is not ready for data transfer.

Data Transfer Command:

16-bit speech data word
(15-0)

Data Transfer Status:

16-bit speech data word
(15-0)

9.8.2 Playback Modes

PLAYMODE	Frame Size (words)	Playback Modes
000	16-8	Compressed Speech: TrueSpeech (8.5, G.723.1 6.3/5.3, 4.8 and 4.1) etc. Refer to Section 9.8.5 (***Select TrueSpeech Playback Rate***).
001		Reserved
010	120	64 Kbits/sec A-law/μ-law PCM (120 words per 30ms data frame)
011		Reserved
100	120	64 Kbits/sec 8-bit signed linear (120 words per 30ms data frame)
101	120	64 Kbits/sec 8-bit unsigned linear (120 words per 30ms data frame)
110	240	128 Kbits/sec 16-bit signed linear (240 words per 30ms data frame)
111		Reserved

Notes: All data rates assume that the CODEC connected to the CT8022 operates at 8000 samples/sec

The 30ms frame interval is based on counting 240 samples from the CODEC (refer to the command for setting base frame size.

Mode 010, PCM μ-law is a *pass-through* mode, where the data from the Host is passed to the CODEC entirely unmodified, (if the playback volume is set to 0100H).

16-bit linear data is signed integer (2's complement form), positive full scale is 7FFFH, negative full scale is 8000H, zero is 0000H

8-bit linear data is signed byte (2's complement form), positive full scale is 7FH, negative full scale is 80H, zero is 00H

8-bit linear WSS data is unsigned byte, positive full scale is FFH, negative full scale is 00H, and zero is 80H. This is the format used for 8-bit WAVE format data (Windows Sound System). Data can be converted between the two 8-bit formats by simply inverting the most significant bit.

The TrueSpeech rate 8.5,6.3,5.3,4.8 or 4.1 etc. is selected using the *Select TrueSpeech Playback Rate* command.

Selection between A-law/μ-law is made using the *CODEC configuration* command. With an external μ-law CODEC configured, RECMODE = 100 selects μ-law data. With an external A-law CODEC configured, RECMODE = 100 selects A-law data.

9.8.3 Playback Protocol

Example 1: TrueSpeech 6.3 Playback via Host Transmit Data Buffer Access Port - Host Polling
This example shows how to start playback with TrueSpeech 6.3, using data transfers performed via the Host Transmit Data Buffer Access Port. The Host controller performs all data transfers in this example. The Host polls the Hardware Status Register to synchronize data.

Starting Playback
1. CT8022 is in IDLE or RECORD state.
2. Host checks for CONTROL READY state in Hardware Status Register.
3. Host selects TrueSpeech 6.3 playback by writing the Select TrueSpeech Playback Rate command = 5231H to the Software Control Register.
4. CT8022 responds via the Software Status Register.
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.
6. Host selects Poll Sync Mode for playback using the command 5202H.
7. CT8022 responds via the Software Status Register.
8. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.
9. Host selects Playback by issuing the PLAYBACK C1 command = 2C03H or 2C01H via the Software Control Register. This also informs the CT8022 that data transfers will occur via the Host Transmit Data Buffer Access Port (TFR Mode = [binary] 11 or 01).
10. CT8022 responds via the Software Status Register after a delay of up to 2 speech frame periods.
11. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register S1 = 2C03H or 2C01H. This clears the STATUS READY bit.
12. Host writes PLAYBACK C2 command = 2000H to the Software Control Register.
13. CT8022 responds via the Software Status Register.
14. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register S2 = 2000H. This clears the STATUS READY bit.
15. Host writes PLAYBACK C3 command = 200CH to the Software Control Register. This command includes the requested number of words per frame to transfer. In this case (TrueSpeech 6.3) this is 12 = 0CH.
16. CT8022 responds via the Software Status Register.
17. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register S3 = 200CH. This clears the STATUS READY bit.
18. The CT8022 is now in playback mode. The CT8022 will be ready to consume a compressed speech frame every 30ms (assuming the base frame size is set to 240). The following sequence is used to transfer each compressed speech frame from the Host to the CT8022:
    a. Host waits for TX Ready bit to be set in the Hardware Status Register
    b. Host writes 12 words (for TrueSpeech 6.3) to the Host Transmit Data Buffer Access Port.

Note: For transfer of speech blocks larger than 16 words via the Host Transmit Data Buffer Access Port, the transfer will be split into sub-blocks of 16 words each or less. The CT8022 will create a small pause between each sub-block during which it will move the sub-block from the data access port (approximately 5 microseconds).

The CT8022 can buffer up to 20 TrueSpeech 6.3 speech data frames (600ms). At the start of playback, the CT8022 will keep re-asserting the TX Ready condition until the internal 480 byte buffer is full, and the CT8022 has *pre-fetched* 20 frames. If the Host must reduce the number of speech data frames pre-fetched by the CT8022, it can do so using the playback ***Set Buffer Depth*** command (528XH). This can be set to reduce the effective size of the internal buffer.

Terminating Playback:

1. Host writes IDLE = 0000H command or STOP PLAYBACK = 5220H command to the Software Control Register.
2. CT8022 terminates playback, discards data in its internal playback buffer, and clears TX Ready if set (in the Hardware Status Register).
3. CT8022 writes status response to the Software Status Register.
4. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.

When either the ***Idle*** or ***Stop Playback*** command is used to terminate playback, the CT8022 will discard data in its internal playback buffer. In some cases, this may not be desired. For example, when playing back TrueSpeech 6.3 data stored in a disk file, if either the ***Idle*** or ***Stop Playback*** command is issued immediately at end-of-file (EOF), the last 20 frames (600ms) of the message will not be played. The Host may wish to use the playback ***Buffer Monitoring*** command (5212H). With command, the Host can poll the CT8022 and wait until all the internally stored speech data has been played out before issuing the ***Idle*** or ***Stop Playback*** command.

Note: After writing the *Idle* or *Stop Playback* command to terminate playback, the Host should not attempt to access the Host Transmit Data Buffer Access Port even if the TX Ready bit is set.

Example 2: TrueSpeech 5.3 Playback via Host Receive Data Buffer Access Port - Host Interrupt

This example shows how to start playback with TrueSpeech 5.3 using data transfers performed via the Host Transmit Data Buffer Access Port. The Host controller performs all data transfers in this example. The Host uses an interrupt service routine (ISR) to transfer data.

Starting Playback

1. CT8022 is in IDLE or RECORD state.
2. Host checks for CONTROL READY state in Hardware Status Register.
3. Host selects TrueSpeech 5.3 playback by writing the Select TrueSpeech Playback Rate command = 5232H to the Software Control Register.
4. CT8022 responds via the Software Status Register.
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.
6. Host selects Poll Sync Mode for playback using the command 5202H.
7. CT8022 responds via the Software Status Register.
8. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.
9. Host selects Playback by issuing the PLAYBACK C1 command = 2C03H or 2C01H via the Software Control Register. This also informs the CT8022 that data transfers will occur via the Host Transmit Data Buffer Access Port (TFR Mode = [binary] 11 or 01).
10. CT8022 responds via the Software Status Register after a delay of up to 2 speech frame periods.
11. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register S1 = 2C03H or 2C01H. This clears the STATUS READY bit.
12. Host writes PLAYBACK C2 command = 2000H to the Software Control Register.
13. CT8022 responds via the Software Status Register.
14. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register S2 = 2000H. This clears the STATUS READY bit.
15. Host writes PLAYBACK C3 command = 200AH to the Software Control Register. This command includes the requested number of words per frame to transfer. In this case (TrueSpeech 5.3) this is 10 = 0AH.
16. CT8022 responds via the Software Status Register.
17. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register S3 = 200AH. This clears the STATUS READY bit.
18. Host sets up an ISR to service interrupts from the CT8022.
19. Host programs the Hardware Control Register to generate an interrupt from the CT8022 on the TX Ready condition by writing 0402H (Master Enable set, TX Ready IE set).

20. The CT8022 is now in playback mode. The CT8022 will consume a compressed speech frame every 30ms. The following sequence is used by the Host ISR to transfer each compressed speech data frame from the Host to the CT8022:
    a. Host gets interrupt from CT8022 (optionally checks that TX Ready is set).
    b. Host writes 10 words (for TrueSpeech 5.3) into the Host Transmit Data Buffer Access Port.

The CT8022 can buffer up to 20 TrueSpeech 5.3 speech data frames (600ms). At the start of playback, the CT8022 will keep re-asserting the TX Ready condition until the internal playback buffer is full, and the CT8022 has *pre-fetched* 20 frames. If the Host needs to reduce the number of speech data frames pre-fetched by the CT8022, it can do so using the playback Set Buffer Depth command (528XH). This can be set to reduce the effective size of the internal buffer.

Terminating playback:

1. Host disables interrupts from the CT8022 by writing 0000H to the Hardware Control Register.
2. Host writes IDLE = 0000H command or STOP PLAYBACK = 5220H command to the Software Control Register.
3. CT8022 terminates playback, discards data in its internal playback buffer and clears TX Ready if set (in Hardware Status Register).
4. CT8022 writes status response to Software Status Register.
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.

When either the ***Idle*** or ***Stop Playback*** command is used to terminate playback, the CT8022 will discard data in its internal playback buffer. In some cases, this may not be desired. For example, when playing back TrueSpeech 6.3 data stored in a disk file, if either the ***Idle*** or ***Stop Playback*** command is issued immediately at end-of-file (EOF), the last 20 frames (600ms) of the message will not be played. The Host may wish to use the playback ***Buffer Monitoring*** command (5212H). With command, the Host can poll the CT8022 and wait until all the internally stored speech data has been played out before issuing the ***Idle*** or ***Stop Playback*** command.

Note: After writing the *Idle* or *Stop Playback* command to terminate playback, the Host should not attempt to access the Host Transmit Data Buffer Access Port even if the TX Ready bit is set.

Example 3: Linear 16-bit Playback via Host Transmit Data Buffer Access Port - Using DMA

This example shows how to start playback in uncompressed 16-bit Linear Format Speech with data transfers performed via the Host Transmit Data Buffer Access Port. An external DMA controller performs all data transfers in this example.

Starting Playback

1. CT8022 is in IDLE state or RECORD state.
2. Host checks for CONTROL READY state in Hardware Status Register.
3. Host selects Poll Sync Mode for playback using the command 5202H.
4. CT8022 responds via the Software Status Register.
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.
6. Host selects Playback by issuing the PLAYBACK C1 command = 2C63H or 2C61H (PLAYMODE = [binary] 110) via the Software Control Register. This also informs the CT8022 that data transfers will occur via the Host Transmit Data Buffer Access Port (TFR Mode = [binary] 11 or 01).
7. CT8022 responds via the Software Status Register after a delay of up to 2 speech frame periods.
8. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register S1 = 2C63H or 2C61H. This clears the STATUS READY bit.
9. Host writes PLAYBACK C2 command = 2000H to the Software Control Register.
10. CT8022 responds via the Software Status Register.
11. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register S2 = 2000H. This clears the STATUS READY bit.
12. Host writes PLAYBACK C3 command = 20F0H to the Software Control Register. This command includes the requested number of words per frame to transfer. In this case (uncompressed 16-bit linear) this is 240 = F0H.
13. CT8022 responds via the Software Status Register.
14. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register S3 = 2000H. This clears the STATUS READY bit. The S3 response sets the actual number of words to transfer to 00H. This transfer count indicates the number of words to be transferred via the Software Control and Status Registers. Since this example uses TFR Mode = [binary] 11, no data is transferred via the Software Control and Status Registers, instead the data transfer takes place via the Host Transmit Data Buffer Access Port.
15. Host programs external DMA controller to accept DMA requests from the CT8022 (See DMA Direction bit in Hardware Control Register). Host configures a data buffer in the Host memory to store the speech data ready for DMA. The DMA memory buffer should be an integral multiple of the speech frame size. In the case of uncompressed 16-bit Linear, this should be N*480 (bytes).
16. Host sets up an ISR to handle an end-of-transfer (EOT) interrupt from the DMA controller when it reaches the end of the DMA buffer. Alternatively, if the DMA supports circular-buffering (auto-initialize), the Host can poll the DMA to determine when the end of the buffer is reached.
17. Host programs the Hardware Control Register to generate a DMA request from the CT8022 on the TX Ready condition by writing 00A0H (TX DMA Burst Mode, TX DMA enable) - or 01A0H (TX DMA Burst Mode, TX DMA enable, DMA Direction bit set).
18. The CT8022 is now in playback mode. The CT8022 will consume an uncompressed speech frame every 30ms. The following sequence occurs between the CT8022 and the DMA controller to transfer data:
    a. CT8022 is ready to receive 240 words (480 bytes) of uncompressed 16-bit speech data.
    b. CT8022 asserts TX Ready.
    c. TX Ready drives TXDREQ.
    d. DMA controller responds to TXDREQ by asserting TXDACKN.
    e. DMA controller performs a burst transfer of 16 words (32 bytes) from the Host DMA memory buffer to the CT8022.
    f. CT8022 de-asserts TX Ready.
    g. CT8022 transfers 16 words from the Host Transmit Data Buffer into its internal playback buffer.
    h. Repeat b-g until all 240 words of the speech data frame have been transferred.

The Host processor also needs to supervise the operation of the DMA controller and arrange for the re-filling of the DMA buffer during playback (e.g. read from disk). When the DMA controller reaches the end of the DMA buffer, the Host must re-fill the data (read from disk). The Host can arrange to receive an EOT interrupt from the DMA controller or can periodically poll the DMA's internal transfer count register to determine the status of the DMA.

Terminating Playback

1. Host disables DMA requests from the CT8022 by writing 0000H to the Hardware Control Register.
2. Host writes ***IDLE = 0000H*** command or ***STOP PLAYBACK = 5220H*** command to the Software Control Register.
3. CT8022 terminates playback and clears TX Ready if set (in Hardware Status Register).
4. CT8022 writes status response to Software Status Register.
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.

Note: After writing the *Idle* or *Stop Playback* command to terminate playback, the Host/DMA should not attempt to access the Host Transmit Data Buffer Access Port even if the TX Ready bit is set.

Example 4: TrueSpeech 8.5 Playback using CT8005/CT8015 protocol via Software Control and Status Registers.
This example shows how to perform TrueSpeech 8.5 playback with TFR Mode = 00 using the CT8015 compatible protocol. Data is transferred via the Software Control and Status Registers. The Host processor performs all data transfers. The example shown uses the CT8015 Poll Sync Mode.

1. CT8022 is in IDLE or PLAYBACK state.
2. Host checks for CONTROL READY state in Hardware Status Register.
3. Host selects TrueSpeech 8.5 playback by writing the Select TrueSpeech Playback Rate command = 5230H to the Software Control Register.
4. CT8022 responds via the Software Status Register
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.
6. Host selects Poll Sync Mode for playback using the command 5202H.
7. CT8022 responds via the Software Status Register.
8. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.
9. Host writes Playback C1 command = 2C00H (TrueSpeech 8.5) to the Software Control Register.
10. CT8022 activates playback mode and performs internal synchronizations (1-2 frame delay) .
11. CT8022 responds with Playback status S1 = 2C00H after a delay of up to 2 speech frame periods.
12. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.
13. **Host sends Playback C2 command = 2000H.**
14. **CT8022 responds with Playback S2 status = 2000H.**
15. **Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.**
16. **Host sends Playback C3 with the number of (16 bit) words it wishes to transfer = 2010H. For TrueSpeech 8.5 the requested transfer count should be 16 = 10H.**
17. **CT8022 checks number of words it is able ready to transfer.**
18. **CT8022 responds with Playback S3 = 2000H or 2010H. If number of words is not zero DATAFLAG/ signal is asserted to indicate the beginning of data transfer.**
19. **Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.**
20. **If number of words to transfer is zero (S3 = 2000H), Host goes back to step 13.**
21. **Optional: Host waits for DATAFLAG/ signal to be asserted**
22. **Host writes 16-bit data word to Software Control Register**
23. **CT8022 responds by echoing the 16-bit data word in Software Status Register**

24. **Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8022 response from the Software Status Register. This clears the STATUS READY bit.**
25. **Repeat steps 22-24 until all (16) data words are transferred**
26. **CT8022 de-asserts DATAFLAG/ signal to indicate the end of data transfer**
27. **Optional: Host waits for DATAFLAG/ to be de-asserted**
28. **Repeat steps 13-27 until playback finished**

To end playback Host writes ***Idle*** command or ***Playback Stop*** command and waits for status response.

Note: Bold text indicates the playback software data transfer loop. By default, The DATAFLAG signal on external pin GPIO0 is disabled. Refer to Section 9.25 for more information regarding GPIO pins.

9.8.4 Playback Frame Alignment Using Transmit Data Buffer

CT8022 provides an additional TFR_MODE = 01 [binary] which maintains strict 30ms data frame alignment for all playback rates. This mode was not available in older versions of the CT8020. The following section describes non-frame-aligned playback using TFR_MODE = 11 [binary].

If performing Playback via the Transmit Data Buffer with TFR_MODE = 11 [binary], the following should be noted:

1. When the CT8022 completes transfer of a speech data frame from the Transmit Data Buffer to its playback queue (in the external data SRAM), the CT8022 immediately returns the (empty) Transmit Data Buffer to the Host and grants the Host access to this buffer. This causes the TX READY signal (and interrupt) to be re-asserted. This happens even when the CT8022's internal memory playback buffer is full.
2. In the case of *compressed* speech playback (TrueSpeech 8.5 - 4.1), the effect is simply to allow the Host to transfer one extra compressed speech frame to the CT8022. When the Host writes the next compressed speech frame to the CT8022, the CT8022 is unable to empty the Transmit Data Buffer to its internal memory, since it is full. In this case, the speech data remains in the Transmit Data Buffer until the next 30ms frame period when space becomes available in the internal memory. In this *memory full + transmit data buffer full* state, the TX READY will not be set. This provides an indication to the Host that the CT8022 is not ready to accept more data. The effect of all this is to allow the CT8022 to effectively buffer one extra frame. This extra frame is not included in the frame count returned by the ***Buffer Monitoring*** Command.
3. In the case of *non-compressed* speech, the effect of this behavior is not as simple. With non-compressed playback (16-bit linear, 8-bit linear and 8-bit μ-law/A-law), the empty Transmit Data Buffer is also returned to the Host upon conclusion of transfer of each complete speech frame (120 or 240 words). However in this case, the Transmit Data Buffer is not large enough to take the entire next frame. Instead it is able to hold only the first 16 words of the next frame. The result is that the frame-by-frame transfer of data to the CT8022 will occur with a 16-word offset relative to the 120 or 240-word frame boundaries. For example:

   In 16-bit linear playback, the 240-word speech frame is broken into 15 sub-frames of 16 words each for transfer via the Transmit Data Buffer. Therefore, the data transfer pattern, broken down into 30ms frame periods, will appear as follows:

Playback Frame Number	Data Transferred	Number Of Sub-Frames Transferred
1	240 words of frame 1 + 16 words of frame 2	16 (256 words)
2	224 words of frame 2 + 16 words of frame 3	15 (240 words)
3	224 words of frame 3 + 16 words of frame 4	15 (240 words)
Final Frame	224 words of final frame	14 (224 words)

In 8-bit playback (all types), the 120 word speech frame is broken up into seven sub-frames of 16 words plus one sub-frame of 8 words.

Playback Frame Number	Data Transferred	Number Of Sub-Frames Transferred
1	120 words of frame 1 (16,16,16,16,16,16,16,8) + 16 words of frame 2 (16)	9 (136 words)
2	104 words of frame 2 (16,16,16,16,16,16,8) + 16 words of frame 3 (16)	8 (120 words)
3	104 words of frame 3 (16,16,16,16,16,16,8) + 16 words of frame 4 (16)	8 (120 words)
Final Frame	104 words of final frame (16,16,16,16,16,16,8)	7 (104 words)

Of particular significance is the sequence of sub-frame sizes transferred by the Host to the CT8022 each 30ms period. For 8-bit playback, as a result of the playback frame alignment offset, the sequence per frame is: 16,16,16,16,16,16,8,16.

Note: In view of this, it is recommended that Host software performing 8-bit playback should re-check the status of the TX READY bit at least every 8 words transferred to the CT8022.

9.8.5 Select TrueSpeech Playback Rate

This command allows the Host to select the TrueSpeech data rate used in compressed playback mode. The standard built-in available rates are: TrueSpeech 6.3, 5.3, 4.8 and 4.1 KBPS. This command should be issued prior to starting playback using the ***Playback*** command. The TrueSpeech Playback Rate remains in effect until the next TrueSpeech ***Playback Rate*** command.

Command (523XH):

0101	0010	0011	RATE
(15-12)	(11-8)	(7-4)	(3-0)

Status (523XH):

0101	0010	0011	RATE
(15-12)	(11-8)	(7-4)	(3-0)

RATE	TrueSpeech Compression Rate	Compressed Frame Size (16-bit words)
0	8.5 (**see Note**)	16
1	6.3 (G.723.1) (default)	12
2	5.3 (G.723.1)	10
3	4.8	9
4	4.1	8
5	Reserved	
6	G.729AB (**see Note**)	6 (10ms)
7	G.722 (**see Note**)	40 (10ms)
8-15	Reserved	

The Frame Size value indicates the number of 16-bit words in a compressed speech frame for each coding rate. When any of the TrueSpeech compression rates are selected, the frame size is always 16 words or less. Since the size of the CT8022 hardware buffer within the Host port is 16 words, the Host can *burst write* the complete speech frame of 16-8 words without checking the RX Ready bit before each individual word is read. Where the frame size is larger than 16 words, the CT8022 splits the data transfer into sub-blocks of 16 words or less.

Note: The CT8022 supports the G.729AB and G.722 coders only as external downloadable software expansion modules. The Host must ensure that the appropriate module is loaded to the CT8022 external program/data memory before attempting to activate any of these coders. Contact DSP Group for information.

The two least significant bits of the first data word of a G.723.1 6.3 or 5.3 speech frame are encoded to indicate the speech frame type.

During Playback (*de-compression*) the CT8022 will test the two least significant control bits only when the current Host-selected TrueSpeech rate is 6.3 or 5.3. In this case, the CT8022 will automatically perform the correct decoding of the speech frames independently of which rate is selected by the Host. This includes automatic decoding of the G.723.1 CNG (Comfort Noise Generation or *silence*) frames.

To support on-the-fly switching for Playback, Playback must be started with the 6.3 rate selected. This fixes the frame size used for Host-to-CT8022 transfer at 12 words. When transferring a 5.3 speech frame to the CT8022 when the 6.3 rate was initially selected, the Host should append two dummy words (zeros) at the end of the 10 word TrueSpeech 5.3 frame.

Refer to Section 9.7.7 regarding on-the-fly switching between TrueSpeech 6.3 and 5.3 data rates.

9.8.6 Inserting Silence During Compressed Speech Playback

When the CT8022 performs *playback* in any of the TrueSpeech modes (8.5, 6.3, 5.3, 4.8 or 4.1) it interprets a speech frame that contains all zeros as an instruction to output 30ms (one frame period) of pure silence.

9.8.7 Activating The G.723.1 Frame Erasure Mechanism

When the CT8022 performs *playback* of G.723.1/TrueSpeech 6.3, 5.3, 4.8 or 4.1 speech frames, it interprets a speech frame that has the first two words set to FFFFH. The remainder of the speech frame is set to all zeros as an instruction to perform *Frame Erasure*. When Frame Erasure is activated, the CT8022 attempts to construct a replacement for a missing speech frame by extrapolation from previous valid speech frames. The Host software and system communication protocol are responsible for sending of a Frame Erasure frame to the CT8022 based upon detection of dropped or corrupted speech frames. The G.723.1 speech frames themselves do not include any built-in error detection mechanism.

9.8.8 G.723.1 Comfort Noise Generation (CNG)

In accordance with Annex A of the ITU G.723.1 specification, the CT8022 will automatically decode CNG frames generated by the Voice Activity Detector (VAD) of a G.723.1 encoder. Decoding of CNG frames is based on examination of the two least significant bits of the first data word of each G.723.1 speech frame. The purpose of the VAD/CNG frame in the G.723.1 Annex A specification is to provide approximate reconstruction of the background noise level and energy spectrum during periods of *silence* that occur between periods of active speech.

The two least significant bits of the first word of the TrueSpeech 6.3 and 5.3 frames are defined by the ITU-T G.723.1 v5.1 (final formal release) specification to indicate the speech data rate as shown:

Bit 1-0	Frame Type	Data Rate	Number of Significant Data Words
00	0	TrueSpeech 6.3 data frame (12 words)	12
01	1	TrueSpeech 5.3 data frame (10 words)	10
10	2	Silence/Comfort Noise Generation frame (only first 2 words contain useful data) All other data words are set to zero	2
11	3	Repeat last CNG frame (only least significant 2 bits of first data word are used) All other data words are set to zero	2 bits

Compatibility Note:

The Bit 1-0 encoding of the CT8022 is different from that used in older firmware versions of the CT8020 that implemented pre-release versions of G.723.1, (firmware revisions 0109 and 0112 part numbers CT8020A11AQC and CT8020A11BQC). The full production release, CT8020D11AQC (firmware revision 0114) implements the final v5.1 G.723.1 release, as do all versions of the CT8022.

When sending a type 3 frame to the CT8022 playback channel (two least significant bits = 11), it is necessary to distinguish this type of frame from the Frame Erasure frame (FFFF FFFFH). All the unused bits in the type 3 frame should be set to zero. Although the CNG frames require fewer bits for actual transmission, the Host must pad the CNG frames with zeros when writing the frame to the CT8022 so that the CNG frame size matches the size of the normal speech frame. The CNG frame should be in the form 0000 0003H to avoid confusion with the special FFFF FFFFH Frame Erasure frame.

When reading or writing speech frames to or from the CT8022, the number of physical words transferred for each individual frame is fixed during each record/playback session. For example, if the record/playback session starts in 6.3 mode, then all frames will contain 12 words. Frames that use less than this number of words for actual data will have the unused portion of the frame set to zero. This approach simplifies the coding of low-level driver software such that it does not need to deal with variable-sized data frames. This is particularly significant when dealing with DMA-type transfer.

9.8.9 Reading the Playback Signal Level Value

It is possible to read the current average Playback signal level value using the command:

Command CF8FH:

1100 1111 1000 1	111
(15-3)	(2-0)

Status:

Average Playback Level Value
(15-0)

The level value is calculated using the following algorithm:

LEVEL = 0

FOR each of 240 OUTPUT samples per frame

IF OUTPUT < 0 THEN OUTPUT = -1 * OUTPUT

LEVEL = LEVEL + OUTPUT

LEVEL = LEVEL/256

Note: This is an average signal level (not r.m.s.). Division by 256 instead of 240 leads to a slight understatement of the true average level. The fractional error is 240/256 = 0.9375, or 6.25%. Dividing by 256 instead of 240 requires less processing by the CT8022 device.

When the CT8022 is operated with a base frame size that is not set to 240, the level calculation is adjusted to report the same level as if the base frame size had been set to 240. However, since the CT8022 will update and report the level for each frame processed, with a smaller base frame size the CT8022 will report the level measured over a shorter period. This may result in more frame-by-frame variation in the signal level measured. When measuring the level of a signal with lower frequency components, or with a low frequency modulation, more *ripple* may be observed in the reported signal level. One example of this would be reporting the signal level of a 350+440 Hz dial tone.

9.8.9.1 Level Scale

The level scale is relative to the maximum positive full scale value of 7FFFH (decimal 32767). This corresponds to an input signal level of approximately + 3dBm0 from the external μ-law CODEC.

The precise input signal level scale can be calculated thus:

Output Level in dBm0 = +3.17 - 20 log(base 10) ((output level/32767) * 256/240)

so the default threshold level of 0100H = 256 decimal, corresponds to 44.753 dBm0.

To calculate the actual average output signal level, read the LEVEL from the device and then perform the following calculation:

CORRECTED LEVEL = (LEVEL * 256)/240

output level in dBm0 = 3.17 - 20 * log10(CORRECTED LEVEL/32767)

9.9 Stop Record/Playback

Playback and Record can be stopped using the ***Idle*** command. However, this stops both Playback and Record. To stop Playback without stopping Record or to stop Record without stopping Playback, the ***Stop*** command may be used. There are three ***Stop*** commands, two for Playback and one for Record:

Stop Record:

Command: 5120H
Status: 5120H

Stop Playback:

Command: 5220H
Status: 5220H

Stop Playback and flush CODEC output buffer (immediate stop) *recommended*.

Command: 5221H
Status: 5221H

In PLAYBACK mode, ***Stop Playback*** causes the CT8022 to enter IDLE mode. In full-duplex speech mode, this command changes the CT8022 state to RECORD.

In RECORD mode, ***Stop Record*** causes the CT8022 to enter IDLE mode. In full-duplex speech mode, this command changes the CT8022 state to PLAYBACK.

Use ***Stop Playback*** with flush option to terminate playback if the *record* channel remains active after playback was completed.

When operating playback only or record only, it is recommended that the ***Idle*** command be used to stop playback/record.

9.10 Playback & Record Volume Control

9.10.1 Read Record/Playback Volume Control Command

Command: CF00H/CF01H

1100 1111	0000 00	0	INPUT
(15-8)	(7-2)	(1)	(0)

Status:

RECORD/PLAYBACK VOLUME
(15-0)

INPUT: Set to 0, reads current playback (output) volume
Set to 1, reads current record (input) volume

9.10.2 Set Record/Playback Volume Control

Command (C1): CF02H/CF03H

1100 1111	0000 00	1	INPUT
(15-8)	(7-2)	(1)	(0)

Status (S1):

1100 1111	0000 00	1	INPUT
(15-8)	(7-2)	(1)	(0)

INPUT: Set to 0, writes playback (output) volume
Set to 1, writes record (input) volume

Command (C2):

RECORD/PLAYBACK VOLUME
(15-0)

Status (S2):

RECORD/PLAYBACK VOLUME
(15-0)

The Record/Playback volume is a "Q8" number that is used to scale the input (record) signal or output (playback) signal.

The scaling performed is input or output signal multiplied by (RECORD or PLAYBACK VOLUME)/100H.

So that a record/playback volume setting of:

100H scales the signal by 1.0

200H scales the signal by 2.0

80H scales the signal by 0.5

There is no protection against over-scaling. If the multiplication factor x the input signal exceeds 16 bits, overflow (distortion) will occur.

With an external G.711 A-law or μ-law CODEC, the CT8022 provides bit-transparent data transfer between the CODEC and the Host when operated in A-law/μ-law record/playback mode with a volume setting of 1.0 (0100H).

For best audio performance, external hardware should perform optimal scaling of the record signal before A-to-D conversion by the CODEC, such that the full dynamic range of the CODEC is utilized. Failure to use appropriate external gain will introduce increased quantization noise b into the recording. Note however, that excessive external gain may cause problems with correct operation of the Acoustic Echo Canceller. Further, if the AEC feature is used, the external gains must be fixed.

Note: Do not attempt to use the CT8022 AEC feature with an external hardware AGC or ALC circuit.

The 8-bit PCM μ-law codes produced by the CODEC when converted to a linear representation occupy 14 bits (including the sign bit). The CT8022 handles these 14-bit codes using a 16-bit word representation such that the 14 μ-law bits are *left-justified* within the 16 bits. The lower (least significant) two bits are padded with zeros. This ensures compatibility with digital recordings originating from external systems where a full 16 bits of significant input are encoded or compressed. When the CT8022 is used to decode or de-compress such recordings for output to a μ-law CODEC, the two least significant bits of the de-compressed 16-bit signal are discarded before conversion to μ-law encoding and output to the CODEC occurs. For 8-bit PCM A-law, the linear representation occupies 13 bits. This is also *left-justified* within 16 bits and the lower bits are filled with zeros.

Q8 format is a notation used to represent fractional numbers. In normal integer arithmetic, it is not possible to represent numbers less than zero or any fractional number. To overcome this limitation, multiplication by fractional numbers is performed by *up-scaling* the multiplier by a fixed base number and then *downscaling* the result by the same base number. The base number provides an effective decimal point placed at the base number. That is, when the multiplier equals the base number, the effective multiplication is by 1.0 (multiply by base number, then divide by base number). To keep the downscaling process simple, the base number selected is always a multiple of 2. This makes downscaling (dividing) by the base a simple binary bit-shift. In Q8 arithmetic, the *decimal point* is placed between bits 8 and 7 of the 16-bit binary multiplier word (least significant bit is bit 0, ms bit is bit 15). The base number used is 2 to the power of 8 or 256 = 100H. Therefore, to multiply by 0.5, the Q8 number 80H (= 0.5 * 100H) is used thus: 400H * 0.5 is performed as 400H * 80H/100H. The divide by 100H is performed not as a division but as a binary 8-bit right shift.

The record and playback volume controls described here do not affect the operation of the CT8022 when in standalone speakerphone mode (analog telephone line speakerphone). Refer to Section 9.21 for a description of volume control in Speakerphone Mode.

9.10.3 Automatic Gain/Level Control (AGC or ALC)

The CT8022 includes an AGC feature that can be used in record mode for automatic level adjustment when recording messages.

Note: For optimal Acoustic Echo Canceller (AEC) performance, the Host should ensure that the AGC is switched *Off* before activating the AEC.

The purpose of the Acoustic Echo Canceller (AEC) is to attenuate, as far as possible, acoustic echoes from the speaker that are picked up by the microphone. The purpose of the Automatic Gain Control (AGC) is to amplify low-level signals that the microphone picks up. Consequently, the AGC and AEC tend to conflict with each other.

The CT8022 incorporates an additional feature that reduces the amount of conflict between the AEC and AGC. The AGC includes a feature that reduces that rate of gain increase allowed when the AEC status indicates that the active speech direction is from the remote talker. If the user requires that the AGC and AEC operate concurrently, then the following recommendations should be followed:

1. Limit the maximum AGC gain to the lowest value that produces acceptable results.
2. Make use of the hold time feature of the AGC to minimize gain increases during short pauses in conversation.
3. Increase the amount of Echo Suppression (loop attenuation) used by the echo canceller to compensate for the additional gain introduced by the AGC.
4. Activate the advanced AEC features.

Activating the AGC disables the Record Volume Control. The Record Volume Control has no effect when the AGC is active. However, Record Volume Control setting changes are retained by the CT8022 and will become effective when the AGC is de-activated.

The AGC provides the following parameters, which are Host-programmable:

Max Gain: The maximum gain (*max amplification*) provided by the AGC

Min Gain: The minimum gain (*max attenuation*) provided by the AGC

Attack Threshold: The AGC output signal level above which attack occurs in the attack phase (*gain reduction*) and below which decay occurs when in the decay phase (*gain increase*).

Attack time-constant: This controls the rate at which the gain decreases during the attack phase

Decay time-constant: This controls the rate at which the gain increases during the decay phase.

Hold Time: The length of time that the AGC gain is held constant following the end of the attack phase and before the beginning of the decay phase.

Start Gain: The initial gain setting to use when the AGC is activated. This may be set anywhere between the min and max gain values.

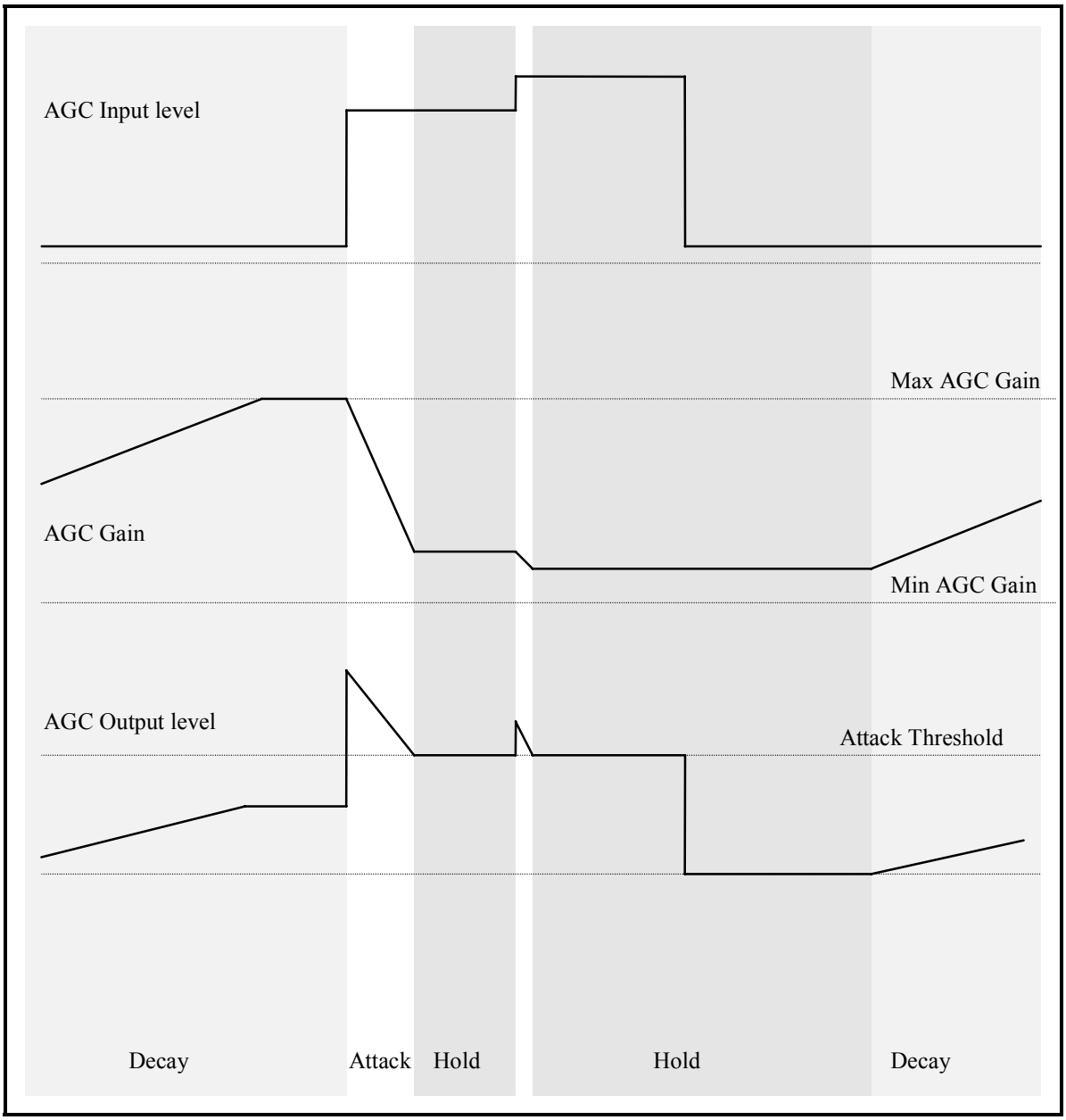


Figure 9-1: AGC Attack Hold & Decay

The above figure illustrates the AGC Input signal level (*signal envelope*), the AGC Gain, and the AGC Output signal level.

During the initial Decay phase shown, the input signal is constant at a low level. Since the AGC output level is below the Attack Threshold, the AGC gain increases, which in turn increases the output signal level. In this example, the gain increases until the AGC Max Gain value is reached, at which point no further increase in gain is possible.

In the next phase, the input signal level suddenly increases, causing the output signal level to exceed the Attack Threshold. At this point, the AGC enters the Attack Phase, and the AGC gain is decreased until the output signal level is below the Attack Threshold.

Once the output level is once more below the Attack Threshold, the AGC enters the Hold Phase. In this phase, the output level remains at, or below, the Attack Threshold. On entering the Hold phase, the AGC sets an internal Hold timer, which then starts to decrement.

Before, the Hold timer can expire, the input signal level increases again, resulting in a second attack phase. After the output level goes below the Attack Threshold again, the AGC re-starts the Hold phase.

Next, the input signal level is suddenly reduced. Since the AGC is still in the Hold phase, no change in the AGC gain occurs, and the AGC output follows the reduction in input signal level.

When the Hold timer expires, the AGC enters the Decay phase again, and the AGC gain starts to increase.

The rate at which the gain increases during the Decay phase (decay time constant) and the rate in which the gain reduces during the Attack phase (attack time constant) are programmable. Best results for speech recording are normally achieved by selecting a fast Attack time constant (allows rapid gain reduction) and a slow Decay time constant (allows only slow gain increase). This configuration causes the AGC to primarily respond to the peak speech level, thus providing relative attenuation of any background noise audible during gaps in the speech. If the Hold time is set to 2-3 seconds, the background noise will remain attenuated even during short pauses in the input speech.

The AGC is automatically reset to the Start Gain value every time a new record session is started (that is, every time a Record C1 command is issued).

9.10.3.1 Programming the AGC

Setting AGC parameters (CF9xH):

Command C1:

1100 1111 1001 0	SELECTOR
(15-3)	(2-0)

Status S1:

1100 1111 1001 0	SELECTOR
(15-3)	(2-0)

Command C2:

Parameter Value
(15-0)

Status S2:

Parameter Value
(15-0)

Where SELECTOR is defined:

SELECTOR	Parameter Description
000	AGC Min Gain. The 16-bit parameter value used to set the AGC Min Gain is treated as a Q8 value. That is, the decimal point used to construct the value is considered to be to the right of bit-8. So in Q8 notation, the value 1.00 is represented by the hex number 0100H (decimal 256). The default value for this parameter is 0020H, this represents the fraction 0.125 in Q8 format. The default min gain is a multiplier factor of 0.125, or one-eighth, or approximately -18 dB. The min gain value can also be regarded as the maximum attenuation of the AGC. In this case, the maximum attenuation is by a factor of 8 or approximately +18 dB.
001	AGC Max Gain. The 16-bit parameter value used to set the AGC Min Gain is treated as a Q8 value (see Min Gain). The default value for this parameter is 1000H. This represents the fraction 16.0 in Q8 format. The default max gain is a multiplier factor of 16, or approximately 24 dB. The default max and min gains give the AGC gain a range from -18 dB to +24 dB, which is a range of 42 dB.
010	AGC Start Gain. The 16-bit parameter value used to set the AGC Start Gain is treated as a Q8 value (see Min Gain). The default value for this parameter is 0800H. This represents the fraction 8.0 in Q8 format. The default max gain is a multiplier factor of 8 or approximately +18 dB. Since the default decay time constant is much larger than the default attack time constant, the default start gain is set high. This is because the time taken to reduce the gain (attack) is much less than the time taken to increase the gain (decay). For example, if the initial speech level is very high, the gain will be reduced quickly (attack) to adjust to the high input level. If the initial speech level is low, since the decay time constant is large (slow), increasing the gain to amplify the low speech level may take several seconds. Therefore, starting with a high gain that can be quickly reduced provides the best initial performance.
011	AGC Hold Time. The 16-bit parameter value used to set the AGC Hold time has units of 250 microseconds. The default value of this parameter is 1F40H (8000 decimal) which corresponds to a Hold Time of 2.00 seconds.
100	AGC Attack Time Constant. See Time Constant table. The default value of this parameter is 0005H.
101	AGC Decay Time Constant. See Time Constant table. The default value of this parameter is 000DH (14 decimal).
110	AGC Attack Threshold. The AGC Attack Threshold is the AGC output value above which the AGC enters the Attack phase (gain reduction). The default value of this parameter is 2000H. The value can be set anywhere in the range of 0000H to 7FFFH. Note that 7FFFH is the maximum internal (digital) signal level. Therefore, a value of 2000H selects AGC attack when the peak signal amplitude is above 0.25 full scale.
111	AGC On/Off. Setting this parameter to 0001H enables AGC operation, setting the parameter to 0000H disables AGC operation. By default, the parameter is 0000H with the AGC in the *Off* state.

Reading AGC parameters (CF8xH):

The AGC parameters programmed can be read back using the command below:

Command:

1100 1111 1000 0	SELECTOR
(15-3)	(2-0)

Status:

Parameter Value
(15-0)

Table 9-1: Time Constant Table

Time Constant Parameter	attack/decay fraction per 125 microseconds = 1/2^(n+1) U(n+1) = U(n) - U(n) * fraction	Time Constant inms (assuming 8 KHz sample rate)
0	0.5	250 us
1	0.25	512 us
2	0.125	1ms
3	0.0625	2ms
4	0.03125	4ms
5	0.015625	8ms
6	0.0078125	16ms
7	0.00390625	32ms
8	0.001953125	64ms
9	0.0009765625	128ms
10	0.00048828125	256ms
11	0.000244140625	512ms
12	0.0001220703125	1024ms
13	0.00006103515625	2048ms
14	0.00003051757813	4096ms
15	0.00001525878906	8192ms

In the Attack phase (gain decreases) , the AGC gain is recalculated every CODEC sample (125 us) such that:

AGC gain = AGC gain - ((AGC gain - min AGC gain) * 1/2^(n+1))

This behaves as an approximately exponential decay from the current instantaneous gain value towards the min AGC value.

In the Decay phase (gain increases), the AGC gain is recalculated every CODEC sample (125 us) such that:

AGC gain = AGC gain + ((max AGC gain - AGC gain) * 1/2^(n+1))

This behaves as an approximately exponential decay from the current instantaneous gain value towards the max AGC value.

Note that the time constant, is the time that it takes for an initial value to decay to 1/e of its initial value where:

e = 2.71828.

9.11 Pre-Scaling of DTMF and Call Progress Filter Input

The CT8022 provides a pre-scaler multiplier, which allows independent adjustment to be made to the input signal level that goes to the tone detection sub-system (DTMF and Call Progress Tone Filters). This pre-scaler (input volume) control is separate from the record and playback volume controls.

The pre-scaler setting can be read using the following command:

Command = CF05H
Status = pre-scaler value (default is 0040H)

The pre-scaler setting can be written using the following command:

C1 Command = CF07H
S1 Status = CF07H

C2 Command = new pre-scaler setting
S2 Status = new pre-scaler setting

The default value for the pre-scaler is 0040H, and it acts as a linear scaler. Changing the pre-scaler setting to 0020H will multiply the signal by 0.5 relative to the normal setting.

9.12 Host Sync Modes

The playback and record sync modes can be set independently:

RECORD SYNC:

Set CODEC sync mode: 5100H
Status: 5100H

Set DATA sync mode: 5101H
Status: 5101H

Set POLL sync mode: 5102H
Status: 5102H

Set HOST sync mode: 5103H
Status: 5103H

PLAYBACK SYNC:
Set CODEC sync mode: 5200H
Status: 5200H

Set DATA sync mode: 5201H
Status: 5201H

Set POLL sync mode: 5202H
Status: 5202H

Set HOST sync mode: 5203H
Status: 5203H

Notes:

1. **The sync modes should normally be changed only when the device is in IDLE mode.**

2. **CODEC sync mode is the default following reset.**

3. **DATA sync mode is selected automatically during Host-to-Host compression or decompression. This sync mode will remain in effect until a new *sync mode* command is issued. Once Host-to-Host compression has been started (after the C1 command), another *sync mode* command can be issued to change to a different sync mode.**

4. **Select POLL sync mode if TFR_MODE = [binary] 11. Use this mode for DMA and if transferring data via the Host Transmit/Receive Data Buffer Access Ports.**

9.13 Playback & Record Buffer Control

9.13.1 Monitoring Buffer Depth

The buffer monitoring commands for the record and playback channels return the number of frames currently present in the respective *receive* and *transmit* queues. Each frame corresponds to 30ms of speech (assuming the base frame size is set to 240). The Host uses these commands for buffer management purposes. The frame count does not include data held in the Host interface transmit or receive data buffer registers.

RECORD:

Read Buffer Depth
Command: 5112H
Status: the number of record frames currently in the receive buffer.

PLAYBACK:

Read Buffer Depth
Command: 5212H
Status: the number of playback frames currently in the transmit buffer.

9.13.2 Speech Frame Create

The ***frame create*** command creates an additional speech frame in the transmit or receive buffer, if the buffer is not full. Copying the most recent frame in the buffer creates the frame.

RECORD:

Create Record Frame:	5117H	
Status:	0 or 1	The number of frames created. If the buffer is full thestatus reply will be 0. If the buffer is not full, and the frame can be created, the status reply will be 1.

PLAYBACK:

Create Playback Frame:	5217H	
Status:	0 or 1	The number of frames created. If the buffer is full the status reply will be 0. If the buffer is not full, and the frame can be created, the status reply will be 1.

Note: For playback, the G.723.1/TrueSpeech 6.3, 5.3, 4.8 and 4.1 rates include a built-in frame creation mechanism that is activated using a specially encoded speech playback frame. This mechanism allows replacement of a dropped or corrupted speech frame by extrapolation of speech data from previous frames. Refer to Section 9.8.7 for information regarding frame erasure.

9.13.3 Speech Frame Delete

The frame delete command deletes a speech frame from the *transmit* or *receive* buffers, if the buffer is not empty. The status reply indicates the number of frames deleted.

RECORD:

Delete Record Frame:	5116H	
Status:	0 or 1	The number of frames deleted. If the buffer is empty at the time this command is called, there will be no frames to delete and the status reply will be 0. If the buffer is not empty, and a frame is deleted, the status reply will be 1.

PLAYBACK:

Delete Playback Frame:	5216H	
Status:	0 or 1	The number of frames deleted. If the buffer is empty at the time this command is called, there will be no frames to delete and the status reply will be 0. If the buffer is not empty, and a frame is deleted, the status reply will be 1.

9.13.4 Playback & Record Buffer Freeze (Pause)

The ***Buffer Freeze*** command stops output from the playback buffer in the playback channel and input to the record buffer in the record channel. The ***Buffer Freeze*** command can be used to implement a pause feature. When the playback channel is paused, it outputs silence to the external CODEC. Freezing the playback channel can also be used at the start of playback to pre-load the channel with buffers before the actual start of playback. This creates a reservoir of speech frames within the CT8022 that can be used for smoothing out fluctuations in the rate at which speech frames arrive for playback. The state of the CT8022 internal freeze flag bits can be modified in any mode of operation: IDLE, PLAYBACK, RECORD or FULL DUPLEX.

RECORD:

Freeze Record Channel:	5113H	
Status:	5113H	
Unfreeze Record Channel:	5114H	
Status:	5114H	
Read Record Freeze State:	5115H	
Status:	0 or 1	The status returns 1 if the channel is currently in the freeze state, 0 otherwise.

PLAYBACK:

Freeze Playback Channel:	5213H	
Status:	5213H	
Un-Freeze Playback Channel:	5214H	
Status:	5214H	

Read Playback Freeze
State: 5215H
Status: 0 or 1 The status returns 1 if the channel is currently in the freeze state, 0 otherwise.

Compatibility Note:

Revision 0112 onwards of the CT8020 firmware (CT8020A11BQC) fixed a minor bug which caused incorrect operation of the *Buffer Freeze* command for Playback when the CT8020's internal playback buffer was completely empty. In earlier versions of the CT8020 firmware, the CT8020 would not output silence when *Buffer Freeze* was activated, if the Playback buffer was empty. In this situation, the CT8020 would continuously re-output the most recent two speech frames. Refer to the Playback Auto-Repeat feature described in Section 9.13.6 of this document.

9.13.5 Buffer Depth Limit

The ***Buffer Depth Limit*** command can be used to limit the number of speech frames held in the playback or record channel buffers. This allows the Host to strictly limit the amount of delay and latency that the buffering of speech frames in the CT8022 can add to an end-to-end speech link. At the same time, the CT8022's buffering capability helps to reduce the load on the Host processor by permitting more relaxed real-time deadlines in moving data into or out of the CT8022. The CT8022 has 480 bytes available for storage space for each channel (physically located within the external data SRAM). This is sufficient for up to:

- 1 uncompressed (480 byte) 16-bit linear frame
- 2 uncompressed (240 byte) 8-bit/A-law/μ-law frames
- 15 TrueSpeech 8.5 frames
- 20 TrueSpeech 6.3, 5.3, 4.8 or 4.1 frames

The CT8022 does not check the buffer limit set by the Host, but simply takes as the actual limit the minimum value of the physical buffer capacity and the Host-programmed limit. For example, in μ-law mode, if the Host programs a limit of 10 frames, the limit used will actually be only 2, which is the physical capacity of the device. In TrueSpeech 6.3 mode, if the Host programs a limit of 10 frames, the limit used will be 10, since this is within the physical capacity of the device.

RECORD:

Set Record Channel
Limit: 5180H + X where X is in the range 0 to 60 (decimal)
Status: 5180H + X

Read Record Channel
Limit: 5118H
Status: 00XXH where XX is the limit programmed

PLAYBACK:

Set Playback Channel
Limit: 5280H + X where X is in the range 0 to 60 (decimal)
Status: 5280H + X

Read Playback Channel
Limit: 5218H
Status: 00XXH where XX is the limit programmed

9.13.6 Playback Auto-Repeat

If data under-run occurs during playback, the transmit buffer empties and the CT8022 will default to repeatedly outputting the most recent speech frame up to a (default) limit of 8 times. This behavior is appropriate for *masking* a short 1 or 2-frame period in which playback data is not available. Repeating the most recent frame once or twice causes the least perceptible break in playback continuity. However, if the data under-run condition persists for a longer period, the repeated playback of a single frame can cause annoyance to the user. The Host can program the auto-repeat limit in the range of 1-15. Programming the auto-repeat limit to zero will cause auto-repeat to operate continuously. When the auto-repeat limit is exceeded, the CT8022 will output silence until more playback data becomes available.

Command:	525XH
Status:	525XH

Where X selects the number of repeats in the range 1-15. If X is set to zero, the CT8022 will continuously auto-repeat the most recent frame.

9.14 Full-Duplex Speech Mode

Full-duplex (DSVD) speech mode is the simple combination of *playback* and *record* operating concurrently (and independently). Starting both Playback and Record (which starts first doesn't matter) will enter full-duplex mode.

If the Host wishes to take advantage of the fact that the CT8022 *record* and *playback* data streams are synchronous, so as to use a single interrupt source to generate an interrupt for both *record* and *playback*, the RX READY interrupt should be used. Internally, the CT8022 process the *playback* data stream before processing the *record* data stream. Therefore, under normal circumstances, the RX READY (*record*) indication will be asserted after TX READY (*playback*). Because of the playback-then-record order, at the time the RX READY condition is asserted, the TX READY will normally also be set. At this time, the Host can perform data transfers for both TX and RX directions.

The only disadvantage to this approach is the restriction imposed on the Host response time when the CT8022's internal playback buffer is *empty* and the internal DSP is operating at close to 100% load. In a minimum delay environment, the Host may wish to attempt to keep the CT8022's internal buffers empty for as long as possible. Reducing the amount of speech buffered within the CT8022 will keep the end-to-end delay to a minimum. Under these circumstances, the response time of the Host using the RX READY assertion until completion of *playback* data transfer to the CT8022 must be shorter, otherwise *playback* data under-run will occur.

The diagram below shows typical CT8022 internal processing activity during one 30ms frame period.

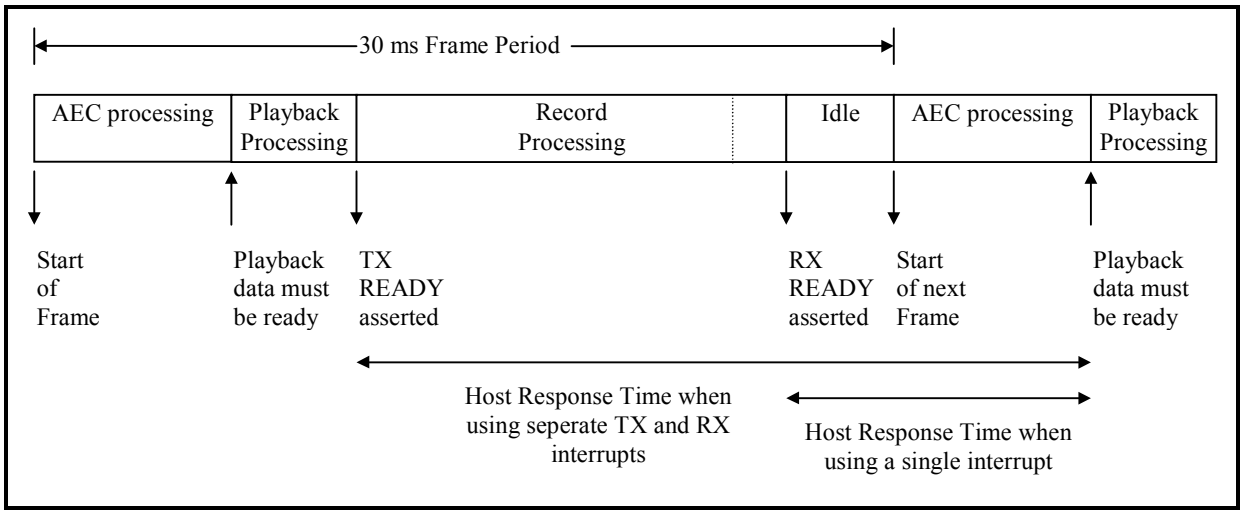


Figure 9-2: CT8022 Internal Processing Activity

The Host Response Time is only an issue if the Host is attempting to implement a *minimum* delay system, where the CT8022's internal buffers are not used to provided additional latency (buffering or de-jitter). If minimum delay is not required, the CT8022's *playback* buffer can be used to provide extra buffering such that there is always at least 1 speech frame ready and waiting in the *playback* buffer. In this situation, the Host always has at least a 1-frame period latency in which to respond to the TX READY condition.

9.15 Acoustic Echo Canceller In DSVD Mode

It is possible to use the Acoustic Echo Canceller (AEC) to cancel echoes in the input signal during full-duplex (DSVD) speech mode. It is possible to use it when only *playback* is in operation to remove playback echoes from the signal input to the DTMF and Call Progress Tone Detectors. When used to cancel playback-only echoes, it is recommended that the Echo Suppressor (loop attenuation) feature and Advanced AEC feature be disabled. For the AEC to function, both an outgoing (*playback*) and incoming (for *record* or tone detection) audio data stream are necessary. When the AEC is operating, the Automatic Gain Control (AGC) feature (available in conjunction with record mode) should be de-activated. However, the *playback* and *record* level controls are still available when the AEC is active. Care must be taken when setting the *record* and *playback* levels so as not to compromise operation of the AEC. The purpose of the AEC is to reduce, as much as possible, the acoustic echo of the outgoing speech (*playback*) reflected from the speaker into the microphone (*record* speech stream). Increasing the *playback* or *record* volumes will increase the level of audible echo. Note that the *record* level setting does not affect the signal level input to the tone detectors.

The AEC is switched ***On*** or ***Off*** using the following commands.

Command:	B001H	AEC on
Status:	B001H	
Command:	B002H	AEC off
Status:	B002H	

These commands can be issued at any time, but the AEC will only be active when *playback* is active (otherwise there is no echo to cancel).

The commands **Get Speakerphone Status**, ***Set Speakerphone Parameters*** (speaker and line volume and loop attenuation), and ***Speakerphone Configuration*** (loop adjustment mode) can be used to control the AEC. Refer to Section 9.21 for detailed descriptions of these commands.

The Speakerphone commands listed above only work when *record* and/or *playback* are already active. Sending these commands when the CT8022 is in IDLE mode will cause improper entry to standalone Speakerphone mode.

Attempting to train the Electrical Echo Canceller (EEC) in DSVD speakerphone mode is not permitted. The EEC is used *only* in standalone Speakerphone mode to cancel the stationary (fixed, non-varying) electrical signal echo from the telephone line (via the second, optional, CODEC0).

Use the following sequence of commands (from IDLE mode):

Start Playback and/or Start Record

1. AEC on
2. Set Speakerphone Parameters
3. optional - Speakerphone Configuration
4. optional - Get Speakerphone Status

9.15.1 Concurrent AEC and Speech Operation

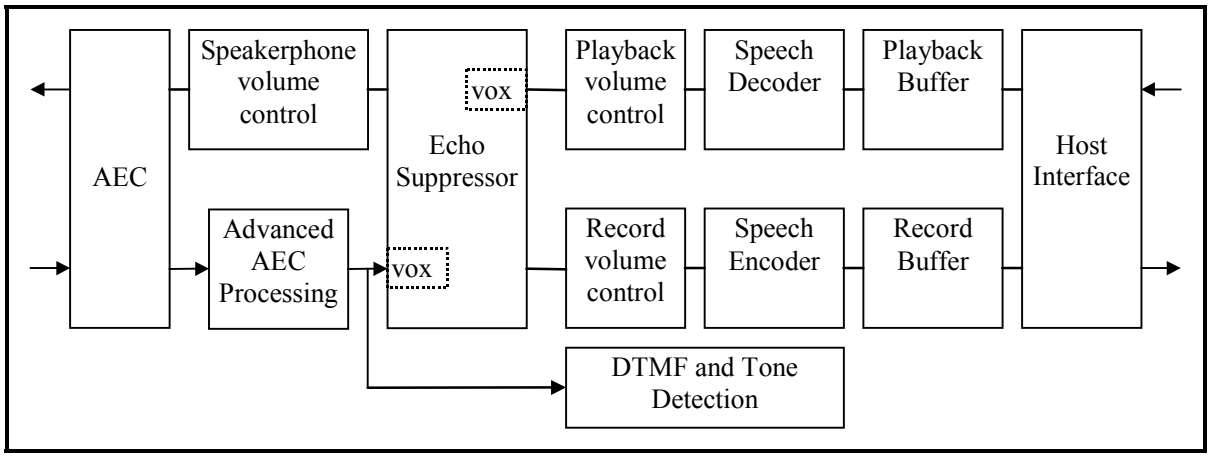


Figure 9-3: AEC and Speech Compression

Figure 9-3 shows the relationship of the Speakerphone Acoustic Echo Canceller (AEC) and Echo Suppressor components to the *record/playback* channels when DSVD Speakerphone mode is used.

Note that the VOX detectors at the Echo Suppressor inputs make the decision regarding Echo Suppressor speech direction. Changes to the playback level made through the playback volume control (recommended) will be detected by the VOX and affect the direction decision. Changes to the playback level made through the Speakerphone volume control (***Set Speakerphone Parameters*** command) will not be detected by the *VOX* and will not affect the direction decision.

When removing playback echoes at the Tone Detector inputs only (and *speech compression/record* is not used) through the AEC, set the Echo Suppressor (loop attenuation) 0dB, disable the automatic loop adjust mode, and set the Advanced AEC feature to ***Off***:

1. Enable AEC
2. Disable Advanced AEC
3. Enable DTMF and/or Tone Detectors
4. Start playback
5. Set loop attenuation to 0dB
6. Switch automatic loop adjustment off
7. Set loop attenuation to 0dB (to force removal of any attenuation added by the auto loop adjustmet mode)

Once this combination of features has been set up, you may stop and restart playback without reprogramming the AEC.

9.15.2 AEC Tail Length

The CT8022 supports programmable AEC Tail Length up to 30ms. The maximum available Tail-Length depends on which other features of the CT8022 are active as shown in the following table:

CT8022 Operating Mode	Maximum AEC Tail-Length	
	Milliseconds	AEC Filter Taps
Full Duplex TrueSpeech 6.3, 5.3, 4.8, 4.1 (G.723.1) with DTMF Detection and Call Progress Tone Detection	30	240
TrueSpeech 8.5 (external) with DTMF Detection and Call Progress Tone Detection	30	240
Standalone Speakerphone Mode	30	240

Each AEC Filter Tap is equivalent to 125 microseconds of Tail Length (at 8.0 KHz).

The AEC Tail Length is programmable in units of 2ms or 16 Taps.

It is possible to change the AEC Tail Length only when the CT8022 is in IDLE mode and the AEC is switched ***Off***.

To program the AEC Tail Length use the command:

Command: B0X0H
Status: B0X0H

Where X0H is the AEC Tail Length in Taps:

B050H Selects 10ms, 80 Taps
B0A0H Selects 20ms, 160 Taps
B0F0H Selects 30ms, 240 Taps

The default AEC Tail Length is 10ms, 80 Taps

9.15.3 Controlling the AEC Adaptation (Training) Rate

The Host may limit the AEC adaptation (training) rate to limit the CT8022 processing resources consumed by the AEC. This also reduces the adaptation rate of the AEC (increases the time taken to train or converge the AEC). Reducing the adaptation rate increases the time taken for the AEC to train, but it also increases the time taken for the AEC to diverge (un-train). Reducing the *adaptation* rate increases the *stability* of the AEC.

The Host may control the AEC adaptation rate in real-time. Therefore, the Host may enable rapid adaptation in the initial stages of a call to quickly train the AEC, and then select slower adaptation in the later stages of a call. This increases the stability of the AEC and makes the AEC more immune to *double-talk* conditions, which can destabilize the AEC.

The processing load (MIPS) consumed by the AEC feature is the sum of three main components:

- control overhead
- actual cancellation
- adaptation (training)

The control overhead is approximately constant.

The cancellation load is proportional to the AEC Tail Length and does not vary frame-by-frame.

The peak adaptation load is proportional to the AEC Tail Length, but switches ***On*** or ***Off*** on a sample-by-sample basis, as determined by the internal control function (speech direction).

For a given frame size and Tail Length, the processing load due to the first two factors is fixed.

The adaptation load varies on a frame-by-frame basis and depends on the speech direction which is evaluated on a sample-by-sample basis within the speech frame.

To prevent the Host from over-committing the CT8022 processing resources (by configuring an inappropriate combination of Tail Length, Speech Coder and Frame Size) , the AEC function monitors the CT8022 processing load in real-time. If the AEC senses that the CT8022 DSP processor is over-committed, it can automatically throttle (limit) the AEC adaptation process to reduce the amount of processing resources consumed by the AEC adaptation.

The AEC adaptation throttle limits the number of adaptation cycles that may run during the processing of each speech frame. By default, the maximum number of adaptation cycles is set to the number of samples in the speech frame. For example: a 30ms speech frame contains 240 samples, so the AEC may run the AEC adaptation operation up to a maximum of 240 times during the speech frame. The number of adaptation cycles actually run depends on the measured speech direction for each speech sample within the frame. Adaptation of the AEC is enabled only when the speech direction is in the *playback* (decompression) direction. If the speech direction is sensed to be in the *record* (compression) direction, no adaptation (training) takes place. The speech direction is sensed on a sample-by-sample basis, so the number of adaptation cycles that run in a particular speech frame can vary from a minimum of zero, to a maximum equal to the speech frame length. For a 30ms speech frame, the number of adaptation cycles can vary from 0 to 240.

The AEC adaptation cycle limit is set equal to the speech frame size at the beginning of each full-duplex speech session. For each speech frame that the AEC senses the CT8022 running out of processing resources, the AEC adaptation cycle limit is reduced (in decrements of 16).

The Host may override the maximum and minimum AEC adaptation cycle limits by programming a maximum and minimum value for the AEC adaptation cycle limit. If the maximum and minimum values are programmed such that they are equal, then the AEC adaptation cycles operate with a fixed limit.

Whenever the AEC cycle adaptation limit is set to a value lower than the current frame size, the peak processing load due to the AEC adaptation (training) process is reduced. The side effect of this is that the AEC adaptation (training) time is correspondingly increased.

If the speech frame is 240 and the AEC adaptation limit is set to 120, the peak adaptation processing load is reduced by 50% and the AEC adaptation (training) time is doubled. If the limit is set to 60, then the load is reduced by 25%, and the adaptation (training) time is quadrupled.

The following command sequences can be used to program the AEC adaptation limits:

To set the maximum AEC adaptation limit:

C1	E02CH
S1	E02CH
C2	00XXH
S2	00XXH

Where XX is the adaptation limit

To set the minimum AEC adaptation limit:

C1	E02DH
S1	E02DH
C2	00XXH
S2	00XXH

Where XX is the adaptation limit

9.15.3.1 Reading the CT8022 DSP Processor Load

The Host can check if the CT8022 DSP Processor is being over-committed by polling the DSP processor load for the current speech frame.

Command:	511BH
Status	load-value

When the load value returned is 0, the DSP processor is 100% loaded.

The load value is measured by counting the number of internal CODEC interrupts that the DSP receives when it is an internal idle loop waiting for availability of the next speech frame to process. When this value reaches zero, it indicates that as soon as the DSP code reaches the idle loop, it finds that the next speech frame is immediately available for processing.

The maximum value read (lowest amount of load) depends upon the speech frame size and the 8/16-bit CODEC configuration. In 8-bit mode, the CODEC generates a single interrupt for every two 8-bit CODEC samples. With an 8.0 KHz CODEC fsync rate, a CODEC interrupt is generated every 250 µs. In 16-bit mode, the CODEC interrupt is generated for each sample, once every 125 µs.

In 8-bit CODEC mode, with a 30ms speech frame, there will be 120 CODEC interrupts per speech frame, so that the DSP processor load can be calculated as:

(1 - load-value/120) * 100%

In 16-bit mode with a 10ms speech frame, there will be 80 CODEC interrupts per speech frame, so that the DSP load is:

(1 - load-value/80) * 100%

In both cases, a load value of zero indicates the DSP processor is 100% loaded. At this load level, the DSP may start to drop speech frames.

The load level is only meaningful in Host-to-CODEC mode. It is not valid in Host-to-Host mode.

9.15.4 Adding Additional Echo Suppression

Additional echo attenuation can be achieved by increasing the level of echo *suppression* used by the CT8022. Echo suppression is different from echo cancellation. In echo cancellation, only the echo component of the input signal is affected, and any input signal that originates at the microphone input is not affected. With echo suppression the entire input signal is affected, both the component due to echo and the component due to the *real* microphone input.

Echo suppression was the technique used in traditional half-duplex speakerphones. In this type of telephone, only one audio signal direction is enabled at any given time. This takes advantage of the fact that in a normal conversation only one user is talking at a given moment. This allows a decision to be made to attenuate one speech direction, based on which speech direction is the inactive direction. The audio signal for the inactive speech direction is always completely muted. To completely mute one direction of speech, half-duplex speakerphones introduce greater than 60dB of attenuation into the inactive speech path.. In a half-duplex speakerphone, since only one speech direction is enabled at any time, there is no possibility of hearing an echo. The problem with this solution comes when both users attempt to talk at the same time. When this happens, the direction decision-making logic in the half-duplex speakerphone is unable to function correctly and the result is often that both speech directions are attenuated.

The CT8022 implements a scaleable form of Echo Suppression where the amount of attenuation added to the inactive direction can be programmed in the range of 0 to -28dB. Using 0dB of echo suppression effectively de-activates the echo suppressor. Providing scaleable echo suppressor attenuation allows a gradual compromise between full-duplex operation (0dB suppression) and half-duplex operation (with -28 dB suppression). With a scaleable echo suppressor, even when a speech direction is attenuated, it is not completely muted, so it is possible to tell that speech is present.

By adding a small amount of echo suppression to the CT8022 (around 16 dB), it is possible to ensure that any residual echo not fully cancelled by the AEC will be removed.

The echo suppression attenuation (loop attenuation) can be programmed only after the AEC is activated, and after *playback* and *record* have been started. Use the ***Set Speakerphone*** command described in Section 9.21.3.

9.15.4.1 Set Echo Suppressor Attenuation

This is the ***Set Speakerphone Parameters*** command used in Standalone Speakerphone mode. It may be used in DSVD Speakerphone mode to set the echo suppressor attenuation. This command should be sent only *after* starting *playback* and *record*.

Command:

1110	001	Line Volume	Speaker Volume	Loop Attenuation
(15-12)	(11-9)	(8-7)	(6-3)	(2-0)

Status:

1110	001	Line Volume	Speaker Volume	Loop Attenuation
(15-12)	(11-9)	(8-7)	(6-3)	(2-0)

Line Volume: This controls the volume transmitted to the telephone line

00	+8 dB
01	+4 dB
10	+0 dB (normal setting)
11	Mute Microphone (also resets AEC)

Speaker Volume: This controls the volume to the speakerphone loudspeaker.

0000	+14 dB
0001	+12 dB
0010	+10 dB
0011	+8 dB
0100	+6 dB
0101	+4 dB
0110	+2 dB
0111	0 dB (normal setting)
1000	-2 dB
1001	-4 dB
1010	-6 dB
1011	-8 dB
1100	-10 dB
1101	-12 dB
1110	-14 dB
1111	Speaker Mute

Loop Attenuation: (Echo Suppression) Total attenuation used by receive and transmit attenuators

Full Duplex Operation

000	0 dB
001	-4 dB
010	-8 dB (default for DSVD mode)

Half Duplex Operation

011	-12 dB
100	-16 dB
101	-20 dB
110	-24 dB
111	-28 dB

9.15.5 Activating the Advanced Echo Canceller Features in the CT8022

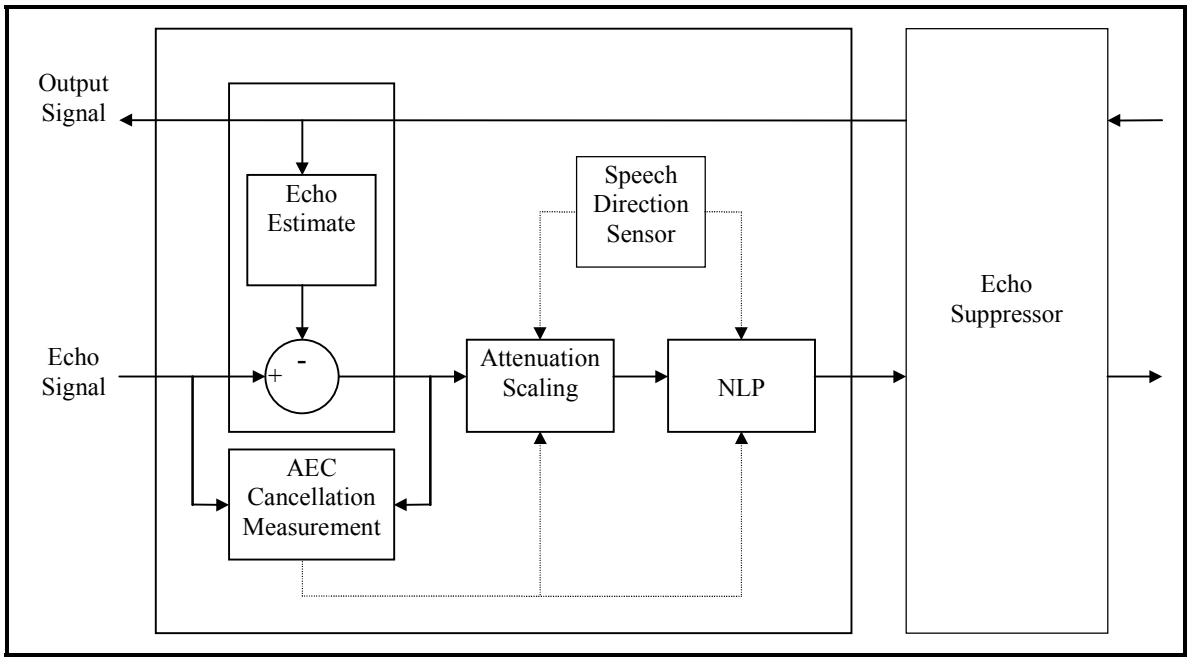


Figure 9-4: Advanced AEC

To increase the amount of echo attenuation provided by the AEC, the Host may enable the Advanced AEC features of the CT8022. The Advanced AEC is actually comprised of two independent mechanisms that can be used to reduce the residual echo left after actual cancellation.

- Non-Linear Processing (NLP)
- Attenuation Scaling or Boosting (AS/AB)

The NLP and AS/AB features are available both in DSVD and Standalone Speakerphone Mode.

9.15.5.1 Non-Linear Processing (NLP)

NLP introduces deliberate distortion into the signal so that low-level signals are distorted to a greater extent than high-level signals. The CT8022 offers two NLP modes:

- center-clipping
- center-subtraction

Center-clipping uses the following algorithm:

if input is < +Threshold and input > -Threshold, then input is forced to zero.

Center-subtraction uses the following algorithm:

if input is > +Threshold then input = input - Threshold

else if input < -Threshold the input = input + Threshold

else input is forced to zero

Center-clipping produces a quantization distortion effect for small amplitude signals. Center-subtraction produces an effect similar to *cross-over* distortion in a push-pull amplifier.

The NLP threshold is set dynamically relative to the output signal amplitude (in CT8020 devices, the NLP threshold was set relative to the input (echo) signal). The minimum NLP threshold is controlled by setting the NLP threshold floor:

NLP threshold = output signal * scale factor (1/16)

if NLP threshold < NLP threshold floor, then NLP threshold = NLP threshold floor.

The NLP threshold floor is set using the following command:

C1	E011H
S1	E011H
C2	XXXXH
S2	XXXXH

where XXXX is the NLP threshold floor. Recommended values are 0080H or 0100H.

The output signal scale factor can be adjusted using the additional control bits in the AEC ***train and lock*** command.

This command may be sent at any time.

To disable NLP use the following command

C1	E011H
S1	E011H
C2	FFFFH
S2	FFFFH

9.15.5.2 Attenuation Scaling (AS) & Attenuation Boost (AB)

Attenuation Scaling (AS) is a technique that allows the CT8022 to increase the amount of echo attenuation achieved when dealing with acoustic echoes in environments which prevent the AEC canceller from fully training. One example of this is environments with high background noise levels or significant non-linear distortion in the echo path.

The dynamic Attenuation Scaling mechanism measures the amount of cancellation attenuation (in dB) produced by the AEC canceller, scales this attenuation, and then adds attenuation (suppression) equal to the scaled attenuation to the cancelled echo signal.

For example, if the AEC measures 6dB of attenuation due to the canceller, and the scale factor is set to 2, then the Attenuation scaling adds 6*2 = 12dB of attenuation (suppression).

The Attenuation Scaling mechanism can also be operated in fixed Attenuation Boost (AB) mode where a fixed amount of extra attenuation (suppression) is added.

To set the Attenuation Scaling mode, use the following command:

C1	E013H
S1	E013H
C2	XXYYH
S2	XXYYH

For fixed scaling, set XX=fixed attenuation, and set YY=00. For example, 0600H selects 6dB of fixed Attenuation Boost. Valid values for XX are 0,6,12,18, etc., in steps of 6dB

For dynamic Attenuation Scaling set YY= attenuation scaling factor and XX=00. For example 0002H sets attenuation scaling with a scale factor of 2. Valid range for YY is 0-10.

This command may be sent at any time.

To disable AS/AB:

C1	E013H
S1	E013H
C2	0000H
S2	0000H

The NLP/AS/AB commands may be sent at any time, before or after the Acoustic Echo Canceller is activated. It is necessary to send these commands only once. It is not necessary to send them every time the AEC is started, but, sending them more than once will not cause any problems.

9.15.5.3 Dynamic Activation of NLP and Attenuation Scaling (AS)

The NLP and AS/AB features are designed to be activated only in the presence of far-end speech or echo. The CT8022 offers two mechanisms for activating the NLP/AS/AB features:

- NLP/AS/AB activation controlled by speech direction
- NLP/AS/AB activation when the measured AEC cancellation exceeds the attenuation lock threshold

Refer to Section 9.15.6.3 for details concerning the cancellation threshold used for activating NLP/AS/AB.

Refer to Section 9.15.6 for details concerning the NLP/AS/AB activation mode

9.15.5.4 Sample Advanced AEC Configurations

The CT8022 offers flexibility in controlling the advanced AEC features (NLP/AS/AB) to allow customization of AEC performance to meet the requirements of different echo environments.

9.15.5.4.1 Acoustic Echo Environments

Acoustic Echo environments tend to show the following typical properties:

- High levels of background noise
- Very short direct (microphone-speaker) echoes with short durations (< 5ms) with high amplitude echoes
- Significantly extended multi-path echo durations (> 50-100ms) producing very low amplitude echoes
- Increased non-linearity in the echo path
- Low input user signal levels relative to speaker output levels (user is far from microphone, but speaker and microphone are close together)
- Echo path varies in real-time requiring rapid AEC training

9.15.5.4.2 Telephone Hybrid Echoes

Telephone Hybrid (2-to-4 wire interface) echo environments tend to show the following typical properties:

- Low noise levels
- Short echo durations (< 10ms)
- Very little non-linear distortion in the echo path
- Input (microphone) and Output (speaker) signal levels are approximately equal
- Echo path is constant for a single call

Large duration (> 100ms) multi-path echoes can be handled using echo cancellers with very long filter lengths (512-1024 tap filters) or using multiple sub-band (frequency division) techniques. This approach tends to require significant computation and processing resources resulting in a relatively high-cost solution.

In cost sensitive applications, acoustic type echoes are more appropriately handled using techniques like NLP and AS/AB together with some degree of Echo Suppression.

High background noise levels and non-linear echo paths tend to reduce the amount of echo cancellation achieved, thus requiring increased reliance on the NLP/AS/AB features to compensate.

C1	E011H	Set NLP threshold floor
S1	E011H	
C2	0100H	Use higher threshold floor value
S2	0100H	
C1	E013H	Set Attenuation Scaling
S1	E013H	
C2	0002H	Set attenuation scale factor to x2
S2	0002H	
C1	E012H	Train & Lock Command
S1	E012H	
C2	0023H	NLP threshold = Speaker Output >> 3 (divided by 8) NLP Mode = 1, activate NLP/AS based on measured AEC attenuation
S2	0023H	
C1	E014H	Set lock threshold (used to activate NLP/AS)
S1	E014H	
C2	0003H	Set threshold to 3dB measured attenuation
S2	0003H	

Example: Telephone Echo environment (local 2-to-4 wire hybrid provides 6-12 dB or cancellation - large amplitude echoes).

C1	E011H	Set NLP threshold floor
S1	E011H	
C2	0080H	Use lower threshold floor value
S2	0080H	
C1	E013H	Set Attenuation Scaling
S1	E013H	
C2	0002H	Set attenuation scale factor to x2
S2	0002H	
C1	E012H	Train & Lock Command
S1	E012H	
C2	0024H	NLP threshold = Speaker Output >> 4 (divided by 16) NLP Mode = 1, activate NLP/AS based on measured AEC attenuation
S2	0024H	
C1	E014H	Set lock threshold (used to activate NLP/AS)
S1	E014H	
C2	0006H	Set threshold to 6dB measured attenuation
S2	0006H	

Example: Telephone Echo environment (local 2-to-4 wire hybrid provides 20+ dB or cancellation - small amplitude echoes).

C1	E011H	Set NLP threshold floor
S1	E011H	
C2	0100H	Use higher threshold floor value
S2	0100H	
C1	E013H	Set Attenuation Scaling/Boost
S1	E013H	
C2	0600H	Set attenuation boost to 6dB
S2	0600H	
C1	E012H	Train & Lock Command
S1	E012H	
C2	0004H	NLP threshold = Speaker Output >> 4 (divided by 16) NLP Mode = 0, activate NLP/AS based on measured speech direction
S2	0004H	
C1	E014H	Set lock threshold (used to activate NLP/AS)
S1	E014H	
C2	0003H	Set threshold to 3dB measured attenuation
S2	0003H	

For low-level echoes, it is recommend that the NLP activation mode be set to 0, since for low-level input echoes the AEC may not be able to accurately measure the achieved AEC cancellation. Activating the NLP/AS/AB using the sensed speech direction will often produce better results.

Increasing the NLP threshold floor and reducing the NLP Threshold Scaling can often produce increased echo attenuation. It can also increase the AS or AB values.

Use of NLP activation mode 1 (use measured AEC attenuation to enable NLP/AS/AB) will tend to produce better full-duplex operation at the expense of reduced echo attenuation.

9.15.6 AEC Train-and-Lock

The CT8022 AEC includes features that allow it to cancel fixed non-acoustic echoes. For example, the AEC can be used to cancel electrical echoes created by a 2-to-4-wire telephone hybrid.

When the AEC is used to cancel acoustic echoes, it must cope with real-time changes in the echo path of the acoustic signal. These changes may be caused by movement of the user in front of the speaker and microphone, or by actual physical movement of the speaker or microphone. As a result, the AEC must continuously attempt to adapt and search for the optimum echo cancellation setting. The constant search process inevitably means that the AEC may not always be operating at its optimum.

If the AEC is required to cancel a fixed path electrical echo, it is possible to train the AEC against the fixed path and then lock the AEC training control.

The AEC can be instructed to perform an automatic train-and-lock sequence using the following command:

	Command	Status Response
C1	E012	E012
C2	4004	4004

If the AEC is already locked when this command is set, the AEC is unlocked, allowing re-training.

To de-activate the train-and-lock feature, use the following command sequence:

	Command	Status Response
C1	E012	E012
C2	0004	0004

To force the AEC into a locked state, use the following sequence:

	Command	Status Response
C1	E012	E012
C2	C004	C004

Refer to Section 9.15.6.1 for a detailed description of the **Train & Lock** command.

9.15.6.1 Detailed Train & Lock Command Description

C1 E012
S1 E012

C2/S2: (The default C2 parameter command value for this command is 0004H)

Force Lock State	Enable Lock Mechanism	Microphone Input Pre-Scale	0	Mic Vox Sensitivity	Far-End Vox Sensitivity
(15)	(14)	(13-12)	(11)	(10)	(9)

0	NLP/AS/AB Control	AEC Train Speed	AEC NLP Mode	Force NLP	NLP Threshold Scaling
(8)	(7)	(6)	(5)	(4)	(3-0)

Force Lock State: Set this bit to 1 to force the AEC into the locked state

Enable Lock Mechanism: Set this bit to 1 to enable the AEC train and lock mechanism

Microphone Input Pre-Scale:
- 00: Sets normal microphone input scaling
- 01: Sets x2 (+6dB) microphone input scaling
- 10: Sets x4 (+12dB) microphone input scaling
- 11: Sets x8 (+18dB) microphone input scaling

Sets the microphone signal input scaling; this modifies the microphone input signal prior to all other signal processing.

Mic Vox Sensitivity:
- 0: Set normal microphone VOX sensitivity
- 1: Reduce microphone VOX sensitivity by 12 dB

This affects the speech direction decision algorithm.

Far-End Vox Sensitivity:
- 0: Set normal far-end (line-side) VOX sensitivity
- 1: Reduce far-end VOX sensitivity by 12 dB

This affects the speech direction decision algorithm.

NLP/AS/AB Control:
- 0: Activate NLP/AS/AB if speech direction detected is from far-end *or* if measured AEC cancellation exceeds threshold programmed for LOCK
- 1: Activate NLP/AS/AB ONLY if measured AEC cancellation exceeds threshold programmed for LOCK

AEC Train Speed:
- 0: Adapt AEC at normal rate
- 1: Adapt AEC at half-rate

This reduces the AEC processing load at the expense of increasing the training time. This control acts independently of the mechanism for limiting the number of AEC training cycles per speech frame. The AEC Train Speed control affects both DSVD speakerphone mode and Standalone Speakerphone mode.

AEC NLP Mode:
- 0: center clipping mode
- 1: center subtraction mode

Force NLP: Force NLP processing to be always activated. This over-rides the NLP/AS/AB control.

NLP Threshold Scaling: This field sets the scaling factor (SF) used to calculate the NLP center clipping threshold:
Threshold = Speaker Output signal >> SF
The default SF is 4, so the threshold is calculated by right-shift-by-4 (division by 16)

9.15.6.2 AEC Locked State

In the *locked* state, the AEC will not undergo further updates of its internal coefficients unless the amount of instantaneous attenuation measured is greater than the Lock Threshold. This places a significant restriction on the AEC adaptation control algorithm. It is designed to prevent a hunting effect where the AEC attempts to adapt to low-level noise instead of to a real echo signal.

Use of this feature is not recommended for echo paths that can vary in real-time. If the echo path changes while the AEC is in the locked state, the amount of attenuation achieved may never exceed the Lock Threshold. In this situation, the AEC will never update its internal coefficients.

9.15.6.3 Setting the Lock Threshold

The attenuation threshold at which the AEC enters the *locked* state is programmable. Use the following command sequence:

	Command	Status Response
C1	E014	E014
C2	XXXX	XXXX

where XXXX is the attenuation threshold in dB.

For example, the default threshold is -12 dB and so XXXX = FFF4 (-12 in hexadecimal form).

9.15.6.4 Setting the Un-lock Threshold

The AEC can be programmed to automatically un-lock if the instantaneous measured attenuation indicates that the AEC is not canceling the echo. This may happen if the echo path was changed.

If the echo path was changed significantly, it is possible that the echo estimate calculated by the AEC is so badly in error that the AEC creates an effect where it *increases* the echo signal level instead of reducing it. In this situation, the AEC can be programmed to automatically un-lock when amplification of the echo signal is detected:

	Command	Status Response
C1	E01B	E01B
C2	XXXX	XXXX

where XXXX is the attenuation threshold in dB.

For example, the default threshold is +3dB and so XXXX=0003.

Note: When measuring the AEC attenuation, a negative dB value represents a reduction in the output signal level (attenuation), whereas a positive dB value represents an increase in the output signal level (amplification).

9.15.6.5 Freezing the AEC

In the *locked* state, the AEC coefficients are updated if the measured attenuation exceeds the Lock Threshold. To cause a complete freeze of the AEC, where no updating of the AEC coefficients takes place, simply program the Lock and Un-Lock Thresholds to large values and force the AEC into the locked state.

For example:

	Command	Status Response	
C1	E01B	E01B	program the un-lock threshold to a large positive value
C2	7FFF	7FFF	
C1	E014	E014	program the lock threshold to a large negative value
C2	FF00	FF00	
C1	E012	E012	Force the AEC into the locked state
C2	C004	C004	

9.15.7 Controlling the Automatic Loop Adjustment Attenuation

When the AEC is operating under normal conditions, it constantly monitors the effect of the echo cancellation process. The intent of the AEC is to reduce the amplitude of any echo signals passing through it. When a signal originating at the near end (a signal caused by the local user talking, and not an echo of the speaker output) passes through the AEC, the signal should pass through without any change in amplitude. Under either of these conditions, the output signal level from the AEC block should never be larger than the input signal level.

If the AEC detects that its output level is greater than its input level, this indicates a fault condition. This state may arise if the acoustic echo path is rapidly changed, for example by suddenly moving the microphone to a position immediately in front of the speaker. Under these circumstances, the AEC by default will increase the amount of echo suppression in use to try to prevent positive feedback in the audio loop (*howling*).

9.15.7.1 Programming the Loop Adjustment Threshold

The Host can program the Loop Adjustment Threshold at which the additional loop attenuation is activated:

	Command	Status Response
C1	E01A	E01A
C2	XXXX	XXXX

where XXXX is the Loop Adjustment Threshold in dB.

For example, the default threshold is +1 dB, so XXXX=1dB.

The automatic loop adjustment feature can be disabled by programming the Loop Adjustment Threshold to a large positive value, e.g. XXXX=7FFFH, or by programming the amount of attenuation added to zero (see below).

It is also possible to disable the automatic loop adjustment feature with the ***Speakerphone Configuration*** Command described in Section 9.21.

Note: When using the AEC concurrently with speech compression modes, this particular command can only be sent *after* enabling the AEC and entering the playback and record states.

9.15.7.2 Programming the Loop Adjustment Attenuation

When the AEC detects error-state amplification in excess of the Loop Adjustment Threshold, by default it adds 12dB of echo suppression in addition to the echo suppression (loop attenuation) selected by the ***Set Echo Suppressor Attenuation*** command. The maximum amount of total echo suppression in operation is limited to 28dB.

The Host can program the amount of additional echo suppression introduced using the following command:

	Command	Status Response
C1	E015	E015
C2	000X	000X

where X is between 0 and 7 and represents units of 4dB steps.

For example, the default attenuation added is 12 dB, so X=3.

When the AEC detects that the error conditions that caused the need for the additional echo suppression (loop attenuation) no longer exist, it is removed automatically.

9.15.8 Setting AEC Microphone Noise Cut-Off Level When Canceling Telephone Line Echoes

When operating the AEC, the CT8022 checks the microphone *input level*, and if it is below the microphone *noise cut-off level*, adaptation of the AEC is disabled. This helps the AEC prevent mis-training in the presence of low level acoustic noise. This also helps deal with prevention of mis-training if the microphone is fitted with a mute switch.

When the AEC is used to cancel electrical telephone line echoes from a telephone line 2-to-4 wire hybrid, it may be desirable to reduce the cut-off level since telephone line environments typically have less noise. This is particularly true if operating with a hybrid that provides a high degree of echo cancellation. This may result in the echo signal created by the hybrid falling below the Microphone Noise Cut-Off Level. In this case, the AEC *may not* train since the signal level of the echo is considered too low.

To set the AEC Microphone Noise Cut-Off Level use the command:

C1:	E007H
S1:	E007H
C2:	cut-off level
S2:	cut-off level

The default cut-off level is 0. In the CT8020 and CT8021 devices, the default value is 50 (decimal) which represents a signal level of around -35 dBm0.

For telephone line echoes, this threshold can be safely set to zero.

9.15.9 Reading the Instantaneous AEC Attenuation

The Host can read the approximate instantaneous attenuation as measured internally by the AEC using the following command:

Command	E00A
Status response	XXXX

where XXXX is the approximate attenuation in dB. This can be a negative value that indicates the current instantaneous echo signal is being attenuated, or a small positive value indicating that either the AEC is not trained, or that no input or echo signal is present. If the attenuation value read is a positive value larger than +6dB, this indicates that the AEC is operating under adverse or error conditions.

The value read can only show a significant negative value (indicating a significant amount of attenuation) when a speaker output signal is present which causes a large input echo. When no input signal is present, the amount of attenuation achieved is indeterminate.

Note that the reported attenuation is the difference in signal level between the microphone input signal and the echo-cancelled microphone input signal. It is *not* the difference between the speaker output and the echo-cancelled microphone input signal. Any attenuation provided by the external echo path is *not* included in the reported attenuation. Example: if the echo path returns an echo -20 dB relative to the output signal, and the AEC succeeds in canceling a further 6dB of echo, then the reported cancellation is -6dB (not -26dB which is the overall cancellation attenuation). Further, the reported AEC cancellation does *not* include the effect of the NLP/AS/AB feature). The reported cancellation is the cancellation effect due to the CT8022 AEC only.

9.15.10 Saving and Restoring the AEC and EEC Coefficients

The current AEC and EEC echo estimation filter coefficients can be saved and restored to the external data SRAM attached to the CT8022 device. Coefficients saved in the external SRAMs are never lost except in the case of a power on-off cycle. The coefficients saved are not affected by a device reset. The coefficients will be lost if the external SRAM self test command is used.

The working filter coefficients of the AEC and EEC are reset each time the echo canceller is restarted. In the case of the AEC, the filter coefficients are reset by an AEC-off, AEC-on sequence.

9.15.10.1 Save AEC Coefficients

Command	E016
Status	E016

9.15.10.2 Restore AEC Coefficients

Command	E017
Status	E017

9.15.10.3 Save EEC Coefficients

Command	E018
Status	E018

9.15.10.4 Restore EEC Coefficients

Command	E019
Status	E019

9.15.11 Evaluating Echo Canceller Performance

The CT8022 AEC uses a pair of VOX detectors to detect the presence of speech and to control the operation of the echo canceller and echo suppressor. These detectors respond to short-term rates of change in signal energy. This enables the detectors to distinguish between real voice activity and background noise. Therefore, it is not appropriate to test CT8022 AEC performance using continuous sine waves. The CT8022 should only be tested using real speech or alternatively using pulsed (dual) sine waves or pulsed white noise. The pulse duration should typically be less than 500ms.

9.16 Speech Frame Interrupt

The CT8022 can provide a speech frame-by-frame interrupt from the TX READY and RX READY signals of the Hardware Status Register. For added flexibility two additional mechanisms are provided for generating interrupts derived from the frame rate.

9.16.1 Frame Interrupt via the FR Pin

For compatibility with the CT8015, the CT8022 can provide a Frame Interrupt signal via the FR/ pin GPIO5. For the CT8022, by default, this pin is not enabled, and GPIO5 is configured as an input. Refer to Section 9.25 for instructions on enabling FR pin functionality.

If the FR/ pin functionality is enabled, then when record, playback or full-duplex speech mode is active, the FR/ pin is asserted (driven low) every frame period. This makes the FR/ signal useful as a frame interrupt to the Host. Since FR/ is asserted every frame period, a new record frame will be available to the Host in the *receive* frame buffer, or a space will be available for a new playback frame in the *transmit* frame buffer, each time the FR/ is asserted. The Host can clear the FR/ signal using the ***CLEAR FR*** command:

The FR/ pin is implemented using the GPIO 5 pin. This is an optional signal provided for CT8015 TrueSpeech DSVD Co-Processor compatibility. If this pin is not required, the GPIO 5 pin is available for general-purpose use. Instead of using the FR/ pin, the Host can use the IRQN interrupt pin and enable it to be driven from the *transmit/receive* data buffer TX or RX READY signal by programming the Hardware Control Register. This will then provide an interrupt each time a compressed data frame is ready (30ms). The interrupt is cleared by filling or emptying the data buffer as appropriate.

The following commands are available for controlling the FR/ pin: Enable, Disable, Clear and Read.

Enable FR:

Command: 5141H
Status: 5141H

by default, the FR pin is enabled.

Disable FR:

Command: 5142H
Status: 5142H

Clear FR:

Command (5140H):

0101 0001 0100 0000
(15-0)

Status:

XXXX XXXX XX	FR	X XXXX
(15-6)	(5)	(4-0)

The state of the FR/ pin (before it is cleared) is returned in bit 5. If the FR pin was asserted prior to being cleared, FR = 0, otherwise FR = 1. The FR/ is active low (when asserted, the pin is low).

Read FR:

Command (5143H):

0101 0001 0100 0011
(15-0)

Status = YYXXH:

YYYY YYYY	GPIO-7	GPIO-6	FRN	X	GPIO-3	GPIO-2	GPIO-1	DATAFLAG
(15-8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

The state of the FR/ pin is returned in bit 5. If the FR pin is asserted, FR = 0, otherwise FR = 1. The FR/ is active low (when asserted, the pin is low). The state of the FR/ pin is not affected by the ***Read FR*** command. Refer to Sections 9.25.3 and 9.25.4 for information on writing and reading the GPIO pins.

9.16.2 Frame Interrupt via Aux Software Status Register

It is possible to program the CT8022 to generate a frame interrupt every N frames via the Aux Software Status Register (ASSR).

Set ASSR update rate:

Command C1 = 5145H
Status S1 = 5145H

Command C2 = N (update ASSR every N frames)
Status S2 = N

If RECORD or PLAYBACK is active, the CT8022 will write its internal frame count to the ASSR every N frames. The Host can then program the CT8022 Hardware Control Register to generate an interrupt on the Aux Status Ready condition. The Host clears the interrupt by reading the ASSR. Setting N to zero disables update of the ASSR. This is the default setting.

The Host can also read the current value of the internal frame count at any time using the command:

Read Frame Count:

Command = 5144H
Status = current frame count.

This frame count is incremented every frame period (30ms) if either RECORD or PLAYBACK is active.

The frame counter is cleared on entry to either RECORD or PLAYBACK from IDLE mode.

9.17 Device Self-Test

9.17.1 Check Internal Program ROM Integrity

Command = 3000H:

0011	00	00 0000 000	0
(15-12)	(11-10)	(9-1)	(0)

Status:

0011	X	DATA ROM STATUS	PROGRAM ROM STATUS	X XXXX XXXX
(15-12)	(11)	(10)	(9)	(8-0)

PROGRAM ROM STATUS: Set to 0 to indicate internal program ROM checksum is valid.
Set to 1 to indicate internal program ROM failure.

DATA ROM STATUS: Set to 0 to indicate internal data ROM checksum is valid.
Set to 1 to indicate internal data ROM failure.

X: Reserved bits

9.17.2 Test External Data SRAM

Command = 3001-3004H:

0011	00	00 0000 0	size
(15-12)	(11-10)	(9-3)	(2-0)

Status:

0011	SRAM TEST	XXX XXXX XXXX
(15-12)	(11)	(10-0)

SRAM TEST: Set to 0 to indicate external data SRAM test passed OK
Set to 1 to indicate external data SRAM failure.

X: Reserved bits

size
1 tests 8K bytes/4K words
2 tests 32K bytes/16K words
3 tests 64K bytes/32K words
4 tests 16K bytes/8K words

After running the external SRAM test, the CT8022 device should be reset. This will re-initialize the external SRAM contents to their normal operational values. Running the SRAM test destroys all the data values held in the external SRAM. SRAM tests start at external memory address 4000H.

9.17.3 External Data SRAM Configuration

After reset, the CT8022 automatically probes the external memory to detect if the memory configuration is 8 or 16 bits wide. For normal operation of the CT8022, the external memory must be 16 bits wide. The memory width setting detected can be over-ridden with the following commands.

Command: = 0821H to select a 8-bit wide memory (15 ns)

Command: = 0801H to select a 16-bit wide memory (15 ns)

This command does not generate a status response. When this command is received, it halts all current operations and performs an internal reset. After issuing this command, the Host should wait for a period of 10ms and then write the ***Idle*** command (0000H) to the CT8022. Once this is done, the Host should then re-configure the CODEC configuration before proceeding with further operations.

9.18 Device Identification

9.18.1 Get Device Identification Code

Command = 3400H:

0011	01	00 0000 0000
(15-12)	(11-10)	(9-0)

Status:

1000	0000	0010	0010
(15-12)	(11-8)	(8-4)	(3-0)

The status reply is the device code as a hexadecimal number i.e. CT8022 = 8022H.

9.18.2 Get Device Version (Revision) Code

Command = 3800H:

0011	10	00 0000 0000
(15-12)	(11-10)	(9-0)

Status:

XXXX	XXXX	XXXX	XXXX
(15-12)	(11-8)	(8-4)	(3-0)

XXXX = 4 bit hexadecimal code.

The status reply is the device version code as a hexadecimal number i.e. version 1.18 = 0117H.

9.19 Tone Generation In Idle Playback & Record Modes

This command is used to generate tones in IDLE, PLAYBACK and RECORD modes only. To generate DTMF tones during Standalone Speakerphone mode, refer to the ***Speakerphone*** commands in Section 9.21. When tone generation is completed in IDLE mode, the Host should use the ***Idle*** command to return the CT8022 to the IDLE state.

Generate Tone Command:

0110	000	MASTER GAIN	TONE INDEX
(15-12)	(11-9)	(8-5)	(4-0)

MASTER GAIN: Modifies (reduces) the level of the tone to be generated with respect to the level programmed into the tone table. The level value in this field is added to the level value programmed into the tone table. The resulting value is used to select the output level (refer to table in Section 9.19.5). For example, if the Tone Table contains level 5, and the master gain is set to level 8, the tone is actually output with a level value of 5 + 8 = 13. The result of the addition is limited <= 15, so if the tone level is 8, and the master gain is 9, the result, 8+ 9 = 17, is limited to 15 and the tone is output using level value 15. An alternate view of this control is to note that the output level is reduced by MASTER GAIN x 2dB, with a minimum output level of -24 dB.

TONE INDEX: Selects the tone to be generated.

Status:

0110	0000 000	MASTER GAIN	TONE INDEX
(15-12)	(11-5)	(4)	(3-0)

In IDLE mode, with default output CODEC routing (= 00) tone is output via CODEC0 only (telephone line side). To output tone to CODEC1, change the output CODEC routing in the ***CODEC configuration*** command.

In PLAYBACK or RECORD mode, tone is output to the default CODEC (normally CODEC1) unless over-ridden by the ***CODEC configuration*** command

Tone generation is possible in two modes: synchronous or asynchronous. Tone generation can be directed to the compressed audio stream using the loopback configuration.

9.19.1 Stop Tone Generation

To terminate tone generation in IDLE mode, use the IDLE command 0000H.

To terminate tone generation during playback/record mode use the following command:

Stop Tone:

Command: 6E0AH
Status: 6E0AH

Note that when generating tones during playback/record, it is recommended that tone generation be configured for asynchronous mode. If tones are generated during playback, the tone output replaces the normal output audio data generated by the playback data. Playback data is consumed at the normal rate even when tone generation is active.

9.19.2 Synchronous Mode

In this mode (default), the duration of the tone is determined by the number of frame periods for which the command is repeated. Synchronous mode is the default mode and is compatible with the tone generation of the CT8005 TrueSpeech Messaging Co-Processor.

The CT8022 creates the output waveform in frames of 30ms each (240 samples at 8.0 KHz). The CT8022 will check for a Host command at the end of each frame after updating the status response and asserting Status Ready in the Hardware Status Register. If the Host repeats the original command, the status reply is repeated, and tone generation is continuous. If the Host changes the tone parameters, the waveform output is changed accordingly. If the command is the ***Idle*** command, tone generation is terminated. Note that the CT8022 requires that the ***Idle*** command be used to correctly terminate tone generation. If the Host does not issue any command, the CT8022 continues to check for a command every 30ms and continues to generate the tone specified by the last command.

To generate a tone of 90ms duration in this mode, the Host performs the following sequence:

1. Write tone command 60XXH.
2. Wait for Status Ready (30ms delay).
3. Repeat tone command.
4. Wait for Status Ready.(30ms delay).
5. Repeat tone command.
6. Wait for Status Ready.(30ms delay).
7. Write idle command (0000H).

To generate a silence gap of 90ms, use the above sequence with the tone command 6000H. This generates a special *silence* tone.

9.19.3 Asynchronous Mode

In this mode, the ***On*** and ***Off*** period for the tone is pre-programmed by the Host, and then complete generation of the tone (***On*** and ***Off*** periods) is executed with a single command. The Host may poll the CT8022 during execution of the command to determine when generation of the complete tone has finished.

Additional Tone Mode Commands

SET SYNCHRONOUS (default, CT8005 compatible) TONE MODE
Command: 6E00H
Status: 6E00H

SET ASYNCHRONOUS TONE MODE
Command: 6E01H
Status: 6E01H

GET TONE MODE
Command: 6E02H

If in synchronous mode:
Status: 0000H

If in asynchronous mode:
Status: 00001H

This command can be used to determine the current tone mode.

The following group of commands are only effective in ASYNCHRONOUS tone mode:

SET TONE ON PERIOD
Command C1: 6E04H
Status S1: 6E04H
Command C2: XXXXH = data value
Status S2: XXXXH = data value echoed

SET TONE OFF PERIOD
Command C1: 6E05H
Status S1: 6E05H
Command C2: XXXXH = data value
Status S2: XXXXH = data value echoed

GET TONE ON PERIOD
Command: 6E06H
Status: XXXXH = data value

GET TONE OFF PERIOD
Command: 6E07H
Status: XXXXH = data value

The units used for setting and reading the tone ***On*** and ***Off*** period are 250 microseconds. By default the tone ***On*** and tone ***Off*** periods are both set to 0192H (400 decimal) which is equivalent to a period of 100ms, (i.e. 400 * 250 microseconds = 100 milliseconds).

GET TONE STATE

Command: 6E03H

If tone generation is still in progress then:
Status: 0001H

Otherwise:
Status: 0000H

9.19.4 Tone Generation in Asynchronous Mode

To generate a tone ***On*** = 90ms followed by a tone ***Off*** = 90ms use the following sequence:

1. Write ***Set Asynchronous Tone*** mode command.
2. Wait for Status Ready in Hardware Status Register and read status response (this needs to be done only once).
3. Write ***Set Tone On Period*** command
4. Wait for Status Ready and read status response.
5. Write tone ***On*** period value command = 0168H (0168H = 360 decimal, 360 * 250 us = 90ms)
6. Wait for Status Ready and read status response.
7. Write ***Set Tone Off Period*** command
8. Wait for Status Ready and read status response.
9. Write tone ***Off*** period value command = 0168H
10. Wait for Status Ready and read status response (this needs to be done only once, unless the ***On***/***Off*** period requires further change).
11. Write tone command 60XXH
12. Wait for Status Ready and read response
13. Poll device using ***Get Tone State*** command
14. Wait for Status Ready and check status reply to determine if tone has completed yet (repeat this last step as often as required).

Once tone generation has been completed, the Host should issue the ***Idle*** command.

9.19.5 Tone Level Table

Level Value (Index)	CODEC Output Level (dB Relative to 0.707 VRMs)	Digital Output Level dBm0
0	+6	+1.5
1	+4	-0.5
2	+2	-2.5
3	0	-4.5
4	-2	-6.5
5	-4	-8.5
6	-6	-10.5
7	-8	-12.5
8	-10	-14.5
9	-12	-16.5
10	-14	-18.5
11	-16	-20.5
12	-18	-22.5
13	-20	-24.5
14	-22	-26.5
15	-24	-28.5

This table shows the actual tone output level as a function of the level value. It is calculated by adding the level value contained in the tone table to the level value specified in the MASTER GAIN field of the ***Generate Tone*** command.

The CODEC output levels given are those produced by the VFR0 output pin of a *Texas Instruments* TP3054 μ-law CODEC when connected to the CT8022 (600 Ohm load).

Note: A power amplifier with approximately 4 dB of gain drives the TP3054 output. A digital signal at 0 dBm0 (0.775 VRMs) will produce an output signal of 1.3 VRMs (+4.5 dBm-600 ohms) at the CODEC output.

9.19.6 New Tone Initialization

Command (C1):

0110	10	00000	TONE INDEX
(15-12)	(11-10)	(9-5)	(4-0)

Status (S1):

0110	10	00000	TONE INDEX
(15-12)	(11-10)	(9-5)	(4-0)

Command (C2):

0110	0000	Gain 1	Gain 0
(15-12)	(11-8)	(7-4)	(3-0)

Status (S2):

0110	0000	Gain 1	Gain 0
(15-12)	(11-8)	(7-4)	(3-0)

Command (C3):

Frequency Factor for Tone 0
(15-0)

Status (S3):

Frequency Factor for Tone 0
(15-0)

Command (C4):

Frequency Factor for Tone 1
(15-0)

Status (S4):

Frequency Factor for Tone 1

(15-0)

TONE INDEX:	index in range 1 to 31, index 0 is reserved for a “silent” tone.
Gain1,Gain0:	level value from tone level table
Frequency Factor:	32767 x cosine(2 x pi x F/8000) Where pi = 3.14159 F is the desired frequency 8000 is the sample rate at which the CODEC is operating

Note: Single frequencies can be generated by setting either frequency factor to 7FFFH

9.19.7 Default (Power-On) Tone Table Contents

Tone Index	Freq. 0	Gain 0	Freq. 1	Gain 1	DTMF Digit
0	No Tone				
1	697	1	1209	0	1
2	697	1	1336	0	2
3	697	1	1477	0	3
4	770	1	1209	0	4
5	770	1	1336	0	5
6	770	1	1477	0	6
7	852	1	1209	0	7
8	852	1	1336	0	8
9	852	1	1477	0	9
10	941	1	1209	0	* (Star)
11	941	1	1336	0	0
12	941	1	1477	0	# (Pound)
13	800	1			
14	1000	1			
15	1250	1			
16	950	1			
17	1100	1			
18	1400	1			
19	1500	1			
20	1600	1			
21	1800	1			
22	2100	1			
23	1300	1			
24	2450	1			
25	350	1	440	0	
26	440	1	480	0	
27	480	1	620	0	
28	697	1	1633	0	A
29	770	1	1633	0	B
30	852	1	1633	0	C
31	941	1	1633	0	D

Note: Index zero is reserved for a silent tone. This can be used to generate gaps or pauses between tones; for example when generating a series of DTMF digits.

Refer to the ***Tone Level Table*** for gain value equivalent levels.

9.20 CT8022 Line Monitor Commands

The CT8022 ***Line Monitor*** command can be used to access 5 detectors (1 DTMF and 4 Call Progress). It is possible to individually enable or disable these detectors. When enabled, the detectors run whenever the CT8022 is in any of the following modes: Line Monitor, Record, Playback or Full-Duplex Speech (record + playback) mode. By default, all the detectors are disabled.

9.20.1 Line Monitor Command

Command (7000H):

0111	0000	0000	0000
(15-12)	(11-8)	(7-4)	(3-0)

Synchronous Mode Status:

0111	F3	F2	F2	F0	0	PEAK	DTMF VALID	CPF VALID	DTMF DIGIT
(15-12)	(11)	(10)	(9)	(8)	(7)	(6)	(5)	(4)	(3-0)

Asynchronous Mode Status:

ls 4-bits Frame Count	F3	F2	F2	F0	0	PEAK	DTMF VALID	CPF VALID	DTMF DIGIT
(15-12)	(11)	(10)	(9)	(8)	(7)	(6)	(5)	(4)	(3-0)

This command activates Line Monitor Mode. To terminate Line Monitor Mode, use the ***Idle*** command (0000H). If asynchronous mode is selected (see below) it can also be used during *record*/*playback* to poll the state of the detectors.

DTMF DIGIT: The DTMF digit value (only valid if DTMF VALID is set):

1-9	1-9
0	0BH
*	0AH
#	0CH
A	0DH
B	0EH
C	0FH
D	0

CPF VALID: Indicates that at least 1 of the 4 detector outputs F0-F3 is set (logical OR of F0-F3)

DTMF VALID: Set when a valid DTMF digit is detected

PEAK: Only valid when RECORD is active. This bit has the same meaning as the PEAK bit in the Record S2 status response

F0-F3: Individual filter output valid bits for filters 0 -3

ls 4-bits Frame Count: Only present when asynchronous mode is selected. This field can be used by the Host to track the number of frames processed by the CT8022 since the last Line Monitor Status.

9.20.2 Synchronous and Asynchronous Monitor Mode

By default, the ***Line Monitor*** command operates in synchronous mode (CT8005-compatible). In this mode, the Line Monitor Status response is delayed until the next 30ms frame has been completely processed. In this mode, it is possible to use the Line Monitor Status response as a *frame clock* since the status response is synchronized to the frame period. For continuous monitoring, the Host should issue a new ***Line Monitor*** command each frame period (each time the previous Line Monitor Status response is received).

Note: In synchronous mode, after issuing the *Line Monitor* command, the Host must wait for the (delayed) status response before it can issue another command.

In asynchronous mode, the status response to the ***Line Monitor*** command is immediate. The status reported represents the most recent 30ms frame processed. To assist the Host in correlating the time of the response with other system events, these 4-bits of the response contain the least significant 4 bits of the CT8022's internal frame counter. This frame counter increments once every 30ms frame period. The Host can use this count value to measure the duration of a valid filter output.

Select asynchronous mode if the Host needs to poll the detectors during *record*/*playback*.

To select synchronous mode, use the command:

Set Synchronous Mode	7E00H
Status Response	7E00H

To select asynchronous mode, use the command:

Set Asynchronous Mode	7E01H
Status Response	7E01H

To read the current mode, use the command:

Read Sync Mode	7E02H
Status Response	0000H = Synchronous Mode
	0001H = Asynchronous Mode

9.20.3 Enabling and Disabling the DTMF Detector

To Enable the DTMF Detector, use the command:

Enable DTMF Detector	5151H
Status Response	5151H

To Disable the DTMF Detector, use the command:

Disable DTMF Detector	5150H
Status Response	5150H

9.20.4 Controlling the Call Progress Tone Filters F0-F3

The CT8022 includes 4 Call Progress Filters. Each filter can be addressed using the ***select filter*** command to set the current value of the CT8022's filter ID parameter (CPFID):

Select Filter Command (5154H - 5157H):

0101	0001	0101	01	SELECT
(15-12)	(11-8)	(7-4)	(3-2)	(1-0)

Status Response (5154H - 5157H):

0101	0001	0101	01	SELECT
(15-12)	(11-8)	(7-4)	(3-2)	(1-0)

SELECT= CPFID:	00	Filter F0
	01	Filter F1
	10	Filter F2
	11	Filter F3

Once selected, the following commands can be used to control the filter:

Filter Enable (5153H)
Filter Disable (5152H)

Status response:

0000	000	DTMF Detector Enabled	0000	F3	F2	F1	F0
(15-12)	(11-9)	(8)	(7-4)	(3)	(2)	(1)	(0)

The F3-F0 and DTMF Detector Enabled bits are set to show which filters are enabled.

To enable all 4 filters the following command sequence can be used:

Command	Status Response	Action
5154H	5154H	Select Filter F0
5153H	0001H	Filter F0 is enabled
5155H	5155H	Select Filter F1
5153H	0003H	Filters F1+F0 are enabled
5156H	5156H	Select Filter F2
5153H	0007H	Filters F2+F1+F0 are enabled
5157H	5157H	Select Filter F3
5153H	000FH	Filters F3+F2+F1+F0 are enabled

9.20.5 Reading the Filter Energy Output

It is possible to read the actual Filter Energy output values using the following command (516XH):

0101	0001	0110	FILTER	INDEX
(15-12)	(11-8)	(7-4)	(3-2)	(1-0)

FILTER:
- 00 F0
- 01 F1
- 10 F2
- 11 F3

INDEX:
- 00 Broadband Energy ls word (bits 15-0)
- 01 Broadband Energyms word (bits 31-16)
- 10 In Band Energy ls word (bits 15-0)
- 11 In Band Energyms word (bits 31-16)

The status response contains the 16-bit value selected by INDEX.

Each filter provides two 32-bit energy parameters:

- The broadband energy of the un-filtered input signal.
- The in-band energy at the filter output.

The energy value is calculated over a 240 sample (30ms) input frame:

$$\text{Energy} = 1/32 * \sum (x/4) * (x/4)$$

If more than one filter is enabled, the broadband energy from each enabled filter will be the same.

9.20.6 Selecting the Filter Characteristics

The CT8022 includes Filter Parameter Sets for eight different call progress tone (CPT) fixed filters plus an additional set of four Filter Parameters that may be programmed by the Host. Each of the four filters F0-F1 can be mapped onto any of the twelve available filter parameter sets. The first four filter parameter sets are stored in the CT8022s internal RAM and may be re-programmed by the Host.

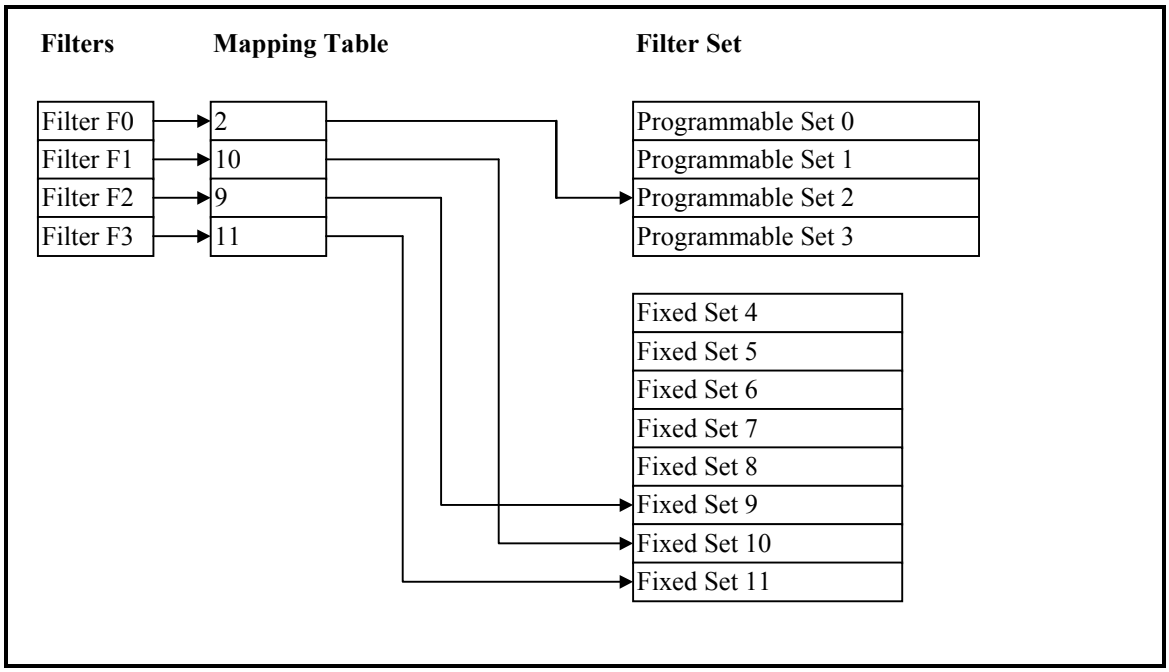


Figure 9-5: Filter Mapping

The following table shows the default contents of the Filter Parameter Sets:

Filter Parameter Set	
0	Programmable Filter Set 0 (by default this is loaded with Fixed Set 4)
1	Programmable Filter Set 1 (by default this is loaded with Fixed Set 5)
2	Programmable Filter Set 2 (by default this is loaded with Fixed Set 6)
3	Programmable Filter Set 3 (by default this is loaded with Fixed Set 7)
4	Fixed Filter Set 4 (wide CPT filter 300Hz - 640 Hz)
5	Fixed Filter Set 5 (narrow CPT filter 300Hz - 500 Hz)
6	Fixed Filter Set 6 (fax calling tone CNG 1100Hz +/- 5%)
7	Fixed Filter Set 7 (350 Hz +/- 5%)
8	Fixed Filter Set 8 (400 Hz +/- 5%)
9	Fixed Filter Set 9 (480 Hz +/- 5%)
10	Fixed Filter Set 10 (440 Hz +/- 5%)
11	Fixed Filter Set 11 (620 Hz +/- 5%)

The Host may program the Filter Parameter Set used by each of the Filters F0-F3. The filter set used by each filter is controlled by the CT8022's Filter Parameter Set Mapping Table. The default Filter Set selection is shown below:

Table 9-2: Default Filter Parameter Set Mapping Table

Filter	Table Value	Filter Parameter Set used by Filter
F0	0	Programmable Filter Set 0 (equivalent to Fixed Set 4 after reset)
F1	1	Programmable Filter Set 1 (equivalent to Fixed Set 5 after reset)
F2	2	Programmable Filter Set 2 (equivalent to Fixed Set 6 after reset)
F3	3	Programmable Filter Set 3 (equivalent to Fixed Set 7 after reset)

Therefore, after reset the following filter parameters are selected

Filter	Filter Parameter Set used by Filter
F0	Wide CPT filter 300Hz - 640 Hz
F1	Narrow CPT filter 300 Hz - 500 Hz
F2	Fax calling tone CNG filter 1100 Hz +/- 5%
F3	350 Hz +/- 5%

At reset, the filter parameters in Programmable Filter Sets 0-3 are loaded from the parameters in Fixed Filter Sets 4-7.

After reset, the Programmable Filter Sets may be re-loaded from Fixed Filter Sets using the following command:

Restore Initial Filter Parameters Command 515DH

Status Response 515DH

9.20.7 Changing the Filter Parameter Set Mapping Table

The contents of the Filter Parameter Set Mapping Table can be changed using the following:

Command (517XH):

0101	0001	0111	MAPPING VALUE
(15-12)	(11-8)	(7-4)	(3-0)

Status Response:

0101	0001	0111	MAPPING VALUE
(15-12)	(11-8)	(7-4)	(3-0)

Where MAPPING VALUE is in the range 0-11 (decimal) corresponding to Filter Parameter Sets 0-11.

To change a Filter Parameter Set Mapping Table entry:

1. First select the entry to be changed (F0-F3) using the Select Filter Command 5144H-5147H.
2. Change the table entry using the command 517XH.

This Mapping Table can be created using the command sequence provided after it:

Filter	Table Value	Filter Parameter Set used by Filter
F0	7	Set 7 = 350 Hz
F1	10	Set 9 = 440 Hz
F2	9	Set 10 = 480 Hz
F3	11	Set 11 = 620 Hz

Command Sequence:

5154H	Select Filter F0
5177H	Select Filter Set 7
5155H	Select Filter F1
517AH	Select Filter Set 10
5156H	Select Filter F2
5179H	Select Filter Set 9
5157H	Select Filter F3
517BH	Select Filter Set 11

9.20.8 Filter Detection Algorithm

The Filter Detection Algorithm has three stages:

1. The In-Band filter energy for each 15ms half-frame (120 samples) is compared against a minimum threshold. By default, this is set to approximately -37 dBm0. If the energy is less than the threshold a *no detect* decision is made for the half-frame.
2. The In-Band filter energy for each 15ms half-frame (120 samples) is compared against the Broad-Band energy. If the In-Band energy is greater than 21/32 * Broad-Band energy then a *detect* decision is made for the half-frame.
3. A filter detect history is constructed every frame period which covers the last 4 frames, or 8 half-frames. If a *detect* decision was made in at least 5 of the last 8 half-frames, then the corresponding Filter Output Valid bit is set in the Line Monitor Status response.

Note: dBm0 scale - For a μ-law or a-law CODEC, the full-scale input signal range of the CODEC corresponds to approximately 3.14 dBm (0 dBm is 1 mW in 600 ohms). For signal level compatibility across digital systems, this signal level is referred to as 3.14 dBm0. When using a 16-bit linear CODEC, the full-scale range of this CODEC is also assumed to be 3.14 dBm0.

9.20.9 Reading the Filter History Register

The Filter History Register for each Filter F0-F3 can be read using the command:

Command (515CH):

0101	0001	0101	1100
(15-12)	(11-8)	(7-4)	(3-0)

Status:

....	n-12	n-11	n-10	n-9	n-8	n-7	n-6	n-5	n-4	n-3	n-2	n-1	n
(15-13)	(12)	(11)	(10)	(9)	(8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

The status response shows the detection decision for the most recent 15ms half-frame ***n*** and up to the last 15 half-frames ***n-1*** to ***n-15***. By default, the CT8022 only checks from ***n*** to ***n-7***, and ignores ***n-8*** to ***n-15***. The default detection algorithm looks for five "1" bits in the range "n" to "n-7".

To read the History Register for Filter F1, use the following command sequence:

Command	Status Response	Action
5155H	5155H	Select Filter F1
515CH	XXXXH	Filter F1 History Register is read

9.20.10 Reading the Frame Counter

The CT8022's internal 16-bit frame counter can be read using the following command:

Command (5144H):

0101	0001	0100	0100
(15-12)	(11-8)	(7-4)	(3-0)

Status:

16-bit Frame Counter
(15-0)

9.20.11 Programming the CT8022 Filters

The Host can program Filter Parameter Sets 0-3 t. The Filter Parameter Set to be programmed is selected by the CPFID parameter set using the ***Filter Select command*** 5154H-5157H.

Each Filter Parameter Set contains 19 words of parameter data.

To start programming of the Filter Parameter Set, use the following command:

Command (515BH):

0101	0001	0101	**1011**
(15-12)	(11-8)	(7-4)	(3-0)

Status (515BH):

0101	0001	0101	**1011**
(15-12)	(11-8)	(7-4)	(3-0)

After writing this command, the next **19** words written to the Software Control Register (command register) will be written to the Filter Set selected.

Command (XXXXH):

Filter Parameter Set Data Word
(15-0)

Status (XXXXH):

Filter Parameter Set Data Word
(15-0)

CT8022 Compatibility Note:

> **Note that the earlier CT8020A11BQC (firmware revision 0112) only allowed downloading of the first 15 words of the filter parameter set. This was implemented using the 515EH command. The new 515BH command implemented in the CT8022 (firmware revision 0117) and the CT8020D11AQC (firmware revision 0114) allows downloading of all 19 parameters in the filter parameter set. The CT8022 continues to support the 515EH command for purposes of backward compatibility with the older CT8020A11BQC version.**

The filter data consists of 15 words of filter coefficients for the sixth order filter (3 x 5 words), plus 4 additional control parameters.

Each filter is a sixth-order filter constructed from 3 cascaded second-order stages.

The following table shows the parameter order and sample values for Fixed Filter Set 4 (300-640 Hz):

Word	Sample Value	Description
0	28967	A1 (Q14) = 1.768028
1	-28798	A2 (Q15) = -0.878854
2	-1988	B2 (Q15) = -0.060682
3	0	B1 (Q14) = 0
4	1988	B0 (Q15) = 0.060682
5	28017	A1 (Q14) = 1.710051
6	-30963	A2 (Q15) = -0.944905
7	12605	B2 (Q15) = 0.384666
8	0	B1 (Q14) = -0.620271
9	12607	B0 (Q15) = 0.384720
10	31398	A1 (Q14) = 1.916387
11	-31859	A2 (Q15) = -0.972276
12	30541	B2 (Q15) = 0.932033
13	-30020	B1 (Q14) = -1.832294
14	30542	B0 (Q15) = 0.932074
15	7	Internal Filter numeric scaling
16	159	Minimum in-band energy threshold
17	21	21/32 in-band to broad-band ratio parameter
18	0FF5H	shift-mask = 0FFH, bit count=5 for History test

Q15 format uses 32768 to represent 1.000
Q14 format uses 16384 to represent 1.000

The internal filter numeric scaling is set to compensate for the internal gain within the filter to prevent numeric overflow. The higher the internal gain (Q factor), the lower the numeric scaling value required. For a narrow bandpass filter (high Q) this should be set to around 5; for a wide bandpass filter this should be set to around 7. The value used is best determined by experimentation, by looking for non-linearity in the filter output value as a function of input signal frequency and level.

The minimum in-band energy is squared by the CT8022, and used for comparison with the in-band filter energy.

The in-band to broadband ratio parameter is used to create a scaling ratio by dividing by 32 and using the resulting fractional multiplier to scale the broadband energy for comparison with the in-band energy.

The final parameter is split into two parts. These 12-bits create an AND mask to control how many History Register bits are counted. The least significant 4 bits provide the bit count threshold 0-15 for counting the "1" bits in the History Register.

The filter coefficients themselves have to be created using special Digital Filter Design Software. This software is available from a number of sources specializing in DSP design software. Filter design packages vary in the nomenclature used to label the A and B parameters as well the sign value +/- of the constants. The best approach to take when designing a new filter is to first create a design for the 300-640Hz filter defined above. The filter coefficients generated can usually be approximately compared against the sample given above to determine if any of the parameters need to be re-ordered or have their sign +/- inverted.

The sample filter above (300-640 Hz) was designed with the following parameters:

type	6th order elliptic
lower stop-band cut-off	250 Hz
lower pass-band cut-off	300 Hz
upper pass-band cut-off	640 Hz
upper stop-band cut-off	800 Hz
sample rate	8000 Hz
pass band ripple	0.1 (1 dB)
stop band ripple	0.05 (-26 dB stop band attenuation)

9.20.12 Generating Interrupts from Line Monitor Events

The CT8022 can generate line monitor event interrupts to the Host controller via the Auxiliary Software Status Register (ASSR). The Host can set an interrupt mask corresponding to the status response bits for the normal line monitor status response.

Set line monitor status interrupt mask:

C1: 5148H
S1: 5148H

C2/S2 Interrupt Mask:

000X	F3	F2	F2	F0	0	0	DTMF VALID	CPF VALID	DTMF DIGIT
(15-12)	(11)	(10)	(9)	(8)	(7)	(6)	(5)	(4)	(3-0)

Setting a mask bit to "1" will update the ASSR with the current line monitor status, if the corresponding bit in the line monitor status changes state. If the X bit is set to "1", the ASSR will be automatically updated every speech frame period even if there is no change to the line monitor status value.

By default, the line monitor status interrupt mask is set to zero.

To generate a Host interrupt from the line monitor status, the Host should set the Aux Status Update IE bit in the Hardware Control Register. Reading the ASSR will clear the interrupt.

For interrupt-driven line monitor status updates, the line monitor feature should be operated in asynchronous mode.

For example: to generate an ASSR update on detection of any DTMF digit, use the following command sequence:

C1 5148H
S1 5148H
C2 0020H
S2 0020H

9.20.13 Operating the Line Monitor Detectors On the Outgoing Playback Audio Stream

By default, the Line Monitor detectors operate on the incoming (*record*) audio stream. However, the CT8022 can be configured so that the detectors operate on the outgoing (*playback*) audio stream. This enables the detector to detect tones and DTMF digits in the decompressed (*playback*) audio.

To set the Line Monitor detector direction, use the following command.

C1: 5149H
S1: 5149H
C2: direction
S2: direction
Set direction=0 for normal operation
Set direction=1 for tone detection on the outgoing (playback) audio stream

9.21 Standalone Speakerphone

9.21.1 Enter Standalone Speakerphone Mode Command

This command is not available in DSVD Speakerphone mode.

1110	01	01	Line Sensitivity	Microphone Sensitivity	Priority	0
(15-12)	(11-10)	(9-8)	(7-5)	(4-2)	(1)	(0)

Status:

1110	01	01	Line Sensitivity	Microphone Sensitivity	Priority	0
(15-12)	(11-10)	(9-8)	(7-5)	(4-2)	(1)	(0)

Line Sensitivity:

000	2 dB
001	4 dB
010	6 dB
011	8 dB (normal setting)
100	10 dB
101	12 dB
110	14 dB
111	16 dB

Microphone Sensitivity:

000	2 dB
001	4 dB
010	6 dB (normal setting)
011	8 dB
100	10 dB
101	12 dB
110	14 dB
111	16 dB

The line and microphone sensitivity determine the signal-to-noise ratio (SNR) at which the voice detectors for the *transmit* and *receive* directions will be activated. The voice detectors are used in half-duplex mode to determine which direction is talking, and which direction should be attenuated.

Priority:

0	both directions have equal priority
1	microphone side (near end) has priority

The priority control determines the behavior of the system when both directions are silent. In the *equal priority* (or *no priority*) mode, the loop attenuation is distributed equally between the *receive* and *transmit* directions. If the priority bit is set, the line side gets all the attenuation and the microphone (near end) has priority.

Note: Before entering Standalone Speakerphone mode, the CODEC Configuration must be programmed with Output CODEC set to 00 and Input CODEC set to 0.

9.21.2 Get Speakerphone Status Command

This command may be used in DSVD Speakerphone mode.

1110	000	0 0000 0000
(15-12)	(11-9)	(8-0)

Status:

1110	000	0	Direction	0	Current Loop Attenuation
(15-12)	(11-9)	(8)	(7-4)	(3)	(2-0)

Current Loop Attenuation: This indicates the amount of loop attenuation currently in use.

Refer to Section 9.21.3, following, for the format of this field.

Direction: This indicates which direction (microphone/speaker) is considered active by the CT8022 Speakerphone control logic. This is a 4-bit field used to represent the number range from +7 to -8. The most positive values indicate that the signal from the microphone side is dominant (*microphone speaking*). The most negative values indicate that the signal from the line side is dominant (*telephone line speaking*). Mid-range values can either indicate a transition from one side to the other, or, if the value stays at approximately the zero position, that neither side is talking.

+7	0111	
+6	0110	Microphone side is speaking.
+5	0101	
+4	0100	
+3	0011	Transition to/from microphone active
+2	0010	
+1	0001	
0	0000	Both sides silent (constant energy) or transition
-1	1111	
-2	1110	
-3	1101	
-4	1100	Transition to/from line side active
-5	1011	
-6	1010	
-7	1001	Line side is speaking
-8	1000	

9.21.3 Set Speakerphone Parameters Command

This command may be used in DSVD Speakerphone Mode.

1110	001	Line Volume	Speaker Volume	Loop Attenuation
(15-12)	(11-9)	(8-7)	(6-3)	(2-0)

Status:

1110	001	Line Volume	Speaker Volume	Loop Attenuation
(15-12)	(11-9)	(8-7)	(6-3)	(2-0)

Line Volume: This controls the volume transmitted to the telephone line.

00	+8 dB
01	+4 dB
10	+0 dB (normal setting)
11	Mute Microphone

Speaker Volume: This controls the volume to the speakerphone loudspeaker.

0000	+14 dB
0001	+12 dB
0010	+10 dB
0011	+8 dB
0100	+6 dB
0101	+4 dB
0110	+2 dB
0111	0 dB (normal setting)
1000	-2 dB
1001	-4 dB
1010	-6 dB
1011	-8 dB
1100	-10 dB
1101	-12 dB
1110	-14 dB
1111	Speaker Mute

Loop Attenuation: Total attenuation used by *receive* and *transmit* attenuators.

Full Duplex Operation

000	0 dB
001	-4 dB
010	-8 dB

Half Duplex Operation

011	-12 dB
100	-16 dB (startup condition)
101	-20 dB

Abnormal Conditions

110	-24 dB
111	-28 dB

9.21.4 Speakerphone Configuration Command

This command may be used in DSVD Speakerphone mode provided that Line Training = 00.

1110	010	0 0000	Line Training	Automatic Loop Adjustment
(15-12)	(11-9)	(8-4)	(3-2)	(1-0)

Status:

1110	010	0 0000	Line Training	Automatic Loop Adjustment
(15-12)	(11-9)	(8-4)	(3-2)	(1-0)

Automatic Loop Adjustment:

00: Loop Attenuation is not automatically adjusted
01: Increase loop attenuation by 12 dB on detection of abnormal conditions. Maintain modified attenuation until a new command is received from Host.
10: Increase loop attenuation by 12 dB on detection of abnormal conditions. Attempt to restore normal loop attenuation when possible. This is the preferred (normal) setting.
11: Reserved

Line Training:

00: Do not modify line-side (electrical) echo canceller settings.
01: Send training pulse to line to set (electrical) echo canceller coefficients.
10: Reserved
11: Reserved

When the Acoustic Echo Canceller (AEC) is active in DSVD speakerphone mode, the Line Training field should always be set to 00.

9.21.5 Generate Tone (In Speakerphone Mode)

This command is not available in DSVD Speakerphone mode.

1110	100	Master Gain	Tone Index
(15-12)	(11-9)	(8-5)	(4-0)

Status:

1110	100	Master Gain	Tone Index
(15-12)	(11-9)	(8-5)	(4-0)

See ***Generate Tone*** command (mode 6) for usage.

Each command/status interaction generates tone for 30ms.

Use Tone Index #0 to generate silence between dialed digits. During tone generation, the speech path between CODEC0 and CODEC1 is disabled. To re-enable this path at the end of DTMF dialing, the Host should issue command E000H (***Get Speakerphone Status***) to inform the CT8022 that dialing is complete.

9.21.6 Get Electrical Echo Canceller Quality Factor Command

This command is not available in DSVD Speakerphone mode.

1110	101	0 0000 000	HIWORD
(15-12)	(11-9)	(8-1)	(0)

Status:

Electrical Echo Canceller Quality Factor
(15-0)

This command returns either the low-order (HIWORD = 0) or high-order (HIWORD = 1) 16 bits of the electrical (line-side) echo-cancelled 32-bit quality factor. The quality factor is a measure of how well the training pulse succeeded in configuring the electrical echo canceller coefficients.

During training, the echo canceller sends the training pulse and receives an echo of the training pulse back from the line. The echo canceller coefficients are adjusted to achieve maximum cancellation of the training pulse echo.

If no echo occurs (for example, if a 4-wire telephone connection is used), all the echo canceller coefficients are set to zero, no cancellation is required (*perfect* cancellation is achieved; there is no reflected signal), and the quality factor is zero in all 32 bits.

If the training pulse is sent while there is a high-level incoming signal (such as dial tone), the echo canceller is unable to cancel the incoming signal (training pulse echo + dial tone) and the quality factor becomes very large (> 100000H). This indicates that training failed and that full duplex operation of the speakerphone can not be activated (loop attenuation must be greater than or equal to 12 dB).

If the training pulse echo is successfully cancelled, the quality factor should be less than 10000H (all high-order bits zero). Under these circumstances, full duplex speakerphone operation may be selected (loop attenuation less than 12 dB).

If the training pulse has not been sent, the quality factor will be set to FFFFFFFFH.

The numbers given here are approximate, and depend largely on the design of the external hardware. The user is expected to experiment and discover suitable threshold values appropriate to his hardware environment.

Note: This command reports the current value of the Electrical Echo Canceller (EEC) Quality Factor. Since training of the EEC takes several milliseconds, it is possible to read this value before training has completed. In this case the Quality Factor from the state prior to training will be read. The Host should allow about 50ms to elapse between sending the command to train the EEC and attempting to read the new Quality Factor. During the training period, the Host should not issue any additional commands to the CT8022, as this will delay or disrupt the training process.

The additional AEC control features described in the DSVD AEC section may also be used in standalone speakerphone mode unless otherwise noted.

9.22 Host-to-Host Data Compression and Decompression

The CT8022 can be operated as a full or half-duplex TrueSpeech compression engine in a CODEC-less configuration. In this situation, the CT8022 routes the uncompressed data stream to the Host instead of to the CODEC.

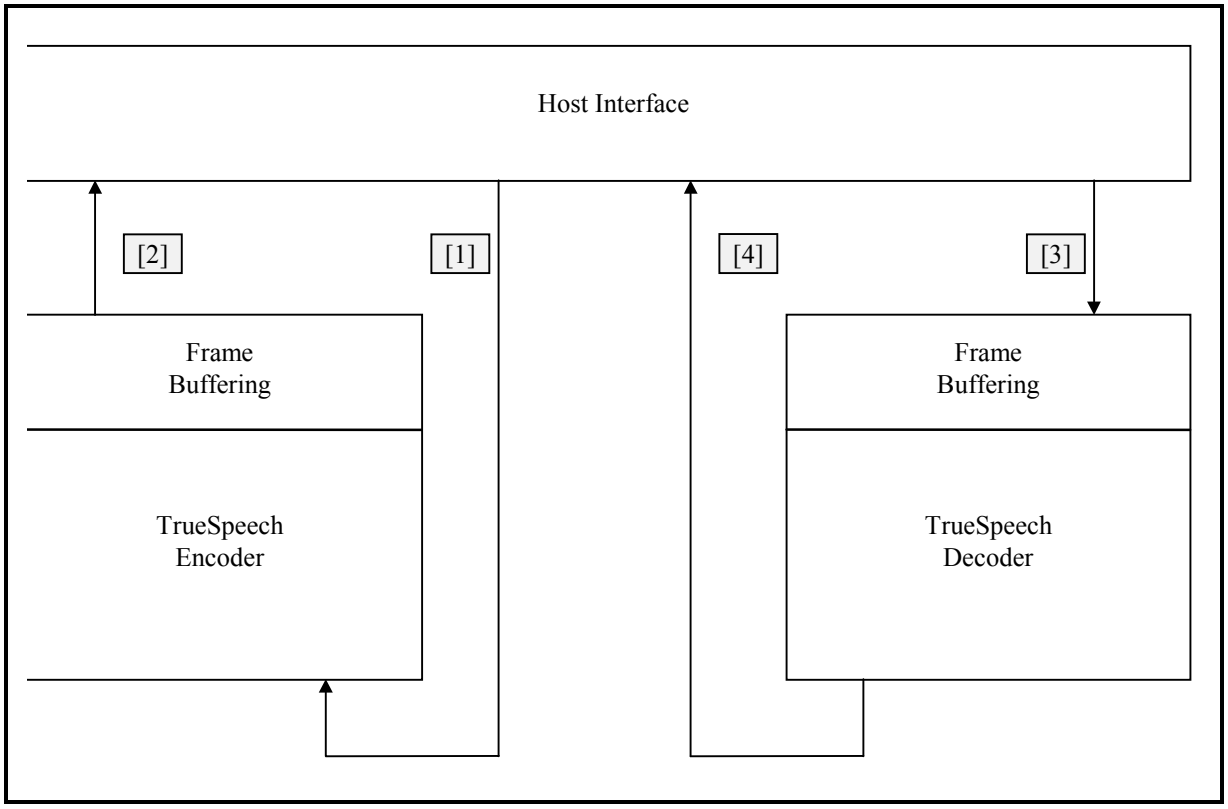


Figure 9-6: Host-to-Host Operation

The Host-to-Host compression/decompression protocol is structured so that the four data exchange operations are independent. The four data exchange operations that take place are:

1. Uncompressed 16-bit linear data transfer from Host to CT8022, denoted using [1] in the following explanations.
2. Compressed TrueSpeech data transfer from CT8022 to Host, denoted using [2] in the following explanations.
3. Compressed TrueSpeech data transfer from Host to CT8022, denoted using [3] in the following explanations.
4. UnCompressed 16-bit linear data transfer from CT8022 to Host, denoted using [4] in the following explanations.

The compressed data exchanges, [2] and [3] to and from the CT8022 internal Frame Buffers take place using the same transfer protocol as used for *record* and *playback* (TFR Mode = 00). The Host should ensure that the AEC (Acoustic Echo Canceller) state is set to ***Off*** for Host-to-Host operation.

9.22.1 Host-to-Host Compression

Host-to-Host compression from the viewpoint of the Host is similar to the *record* process. The protocol used to transfer compressed data frames from the CT8022 to the Host [2] is the same as that used for recording in DATA sync mode with TFR Mode = 00. However, instead of using the ***record C1*** command to start the process, the ***Host-to-Host compression C1*** command is used. The **compression C1** command is also used to transfer the actual uncompressed data frames to the CT8022 [1].

The following command initiates Host-to-Host compression:

Compress Command C1 (= FXXXH):

1111 01	RECMODE	000 0	TFR_MODE	DATA
(15-10)	(9-7)	(6-3)	(2-1)	(0)

Status Response S1:

1111 01	RECMODE	000 0	TFR_MODE	READY
(15-10)	(9-7)	(6-3)	(2-1)	(0)

9.22.1.1 Recording (Compression) Modes

RECMODE	Recording Modes
000	TrueSpeech at 8.5, 6.3, 5.3, 4.8 or 4.1 Kbits/sec
001	Reserved
010	Reserved
011	Reserved
100	64 Kbits/sec A-law/μ-law PCM (120 words per 30ms data frame)
101	128 Bit/sec 16-bit linear (240 words per 30ms data frame)
110	64 Kbits/sec 8-bit signed linear (120 words per 30ms data frame)
111	64 Kbits/sec WSS 8-bit unsigned linear (120 words per 30ms data frame)

Refer to Section 9.7 for more details on RECMODE and TFR_MODE.

DATA
In the first C1 command (used to start compression) the DATA flag is set by the Host to indicate whether the Host wishes to immediately transfer the first uncompressed speech frame [1] to the CT8022 for compression.

In subsequent ***compression C1*** commands, the DATA flag is ignored by the CT8022. In this case, the CT8022 always assumes that the Host will be ready to transfer uncompressed data [1].

READY
If the READY flag is set in the status response, the CT8022 expects that immediately following the S1 response, the Host will transfer 240 words (480 bytes) of uncompressed data. The READY flag will always be set in the first S1 response if the Host set the DATA flag in the first C1 command. When the Host receives a status response with the READY flag set, it *must* immediately commence the transfer of uncompressed speech data.

Host-To-Host Compression Data Transfer [1] and [2]

Host starts compression process [1] by issuing ***compression C1*** command, and waits for Status Ready in the Hardware Status Register to be asserted.

CT8022 acknowledges start of compression with ***compression S1*** response.

If the READY flag is set in status response S1:

Host transfers uncompressed data by writing the (240) uncompressed data words to the Software Control register and waiting for STATUS READY to be set after each word written. Each time STATUS READY is set, the Host must read the Software Status Register in order to clear STATUS READY. The actual value read from the Software Status Register is the same as (*echo of*) the last data word written.

The compression C1 and S1 status response - READY flag are used to control subsequent uncompressed speech data transfers[1] to the CT8022.

Once compression has been started, the Host transfers compressed data from the CT8022 [2] using the normal *record* data transfer protocol (TFR Mode = 00 or 11).

The record protocol used to transfer compressed speech data frames from the CT8022 also supports the ***Buffer Monitoring***, ***Frame Create***, **Frame Delete**, and ***Record Stop*** commands.

Host-to-Host compression can be terminated either using the ***Record Stop*** command or the ***Idle*** command. One of these commands should be issued during the command-status sequence in place of the ***compression C1*** command.

Compression READY Polling

Instead of using the ***compression S1*** status READY response to determine if the CT8022 is ready to accept more uncompressed speech data, the Host can poll the READY state using the following command:

command:	5119H	
status:	0000H	if CT8022 is ready to accept more uncompressed data.
	0001H	if CT8022 is *not* ready to accept more uncompressed data.

This command is only valid if compression mode is active.

The advantage this command offers over simple use of the ***compression C1-S1*** command-status is that it allows the Host to query the READY state without immediately committing to performing the data transfer. With the ***compression C1-S1*** command-status, if the READY bit in the S1 status response is set, the Host *must* immediately transfer data.

9.22.2 Host-to-Host Decompression

Host-to-Host decompression from the viewpoint of the Host is similar to the playback process. The protocol used to transfer compressed data frames from the Host to the CT8022 [3] is the same as that used for playback in DATA sync mode. However, instead of using the ***playback C1*** command to start the process, the Host-to-Host ***decompression C1*** command is used. Note that in the case of decompression, the Host must still send the ***playback C2 and C3*** commands after sending the ***decompression C1*** command to start the decompression process. The ***decompression C1*** command replaces the ***playback C1*** command, but the ***playback C2 and C3*** commands are still required when starting decompression. The decompression C1 command is also used to transfer the actual uncompressed data frames from the CT8022 [1].

The following command is used to start Host-to-Host decompression:

Decompress Command C1:

1111 11	PLAYMODE	000 0	TFR_MODE	0
(15-10)	(9-7)	(6-3)	(2-1)	(0)

Status Response S1:

1111 11	PLAYMODE	000 0	TFR_MODE	READY
(15-10)	(9-7)	(6-3)	(2-1)	(0)

When starting decompression, this command must then be followed immediately by the ***playback C2 and C3*** commands. Note that when the first ***decompression C1 command*** is sent to start decompression, the READY flag in the status response will not be set, since at this point the CT8022 will have no decompressed data available.

To Start Playback:	To Start Decompression:
Playback C1	Decompress C1
Playback C2	Playback C2
Playback C3	Playback C3

9.22.2.1 Playback (Decompression) Modes

PLAYMODE	Playback Modes
000	TrueSpeech at 8.5, 6.3, 5.3, 4.8, 4.1 Kbits/sec
001	Reserved
010	64 Bit/sec A-law/μ-law PCM (120 words per 30ms data frame)
011	Reserved
100	64 Kbits/sec 8-bit signed linear (120 words per 30ms data frame)
101	64 Kbits/sec 8-bit unsigned linear (120 words per 30ms data frame)
110	128 Kbits/sec 16-bit signed linear (240 words per 30ms data frame)
111	Reserved

Refer to Section 9.8 for more details on PLAYMODE and TFR_MODE.

READY
If the READY flag is set in the status response, the CT8022 expects that immediately following the S1 response, the Host will transfer 240 words (480 bytes) of uncompressed data. When the Host receives a status response with the READY flag set, it *must* immediately commence the transfer of uncompressed speech data.

Host-to-Host Decompression Data Transfer [3] and [4]
Host starts decompression process [3] by issuing ***decompression C1*** command, and waits for Status Ready bit in the Hardware Status Register to be asserted.

CT8022 acknowledges start of decompression with ***decompression S1*** response.

Host reads S1 status, Status Ready is cleared (Since no data has been decompressed at this time, the READY flag will not be set).

Host sends ***playback C2 and C3*** commands

Once decompression has been started, the Host transfers compressed data to the CT8022 [3] using the normal playback data transfer protocol.

Subsequent decompressed speech is transferred using the ***decompression C1*** command. The S1 status - READY flag is used to control the transfers:

Host sends ***decompression C1*** command

CT8022 returns S1 status response including READY flag.

IF the READY flag is set:

Host transfers decompressed data by writing the dummy ***decompression*** command F000H to the Software Control register and then waiting for STATUS READY to be set. Each time STATUS READY is set, the Host must read the Software Status Register in order to clear STATUS READY. The data read from the Software Status Register is the decompressed data. The Host writes the F000H command 240 times in order to read 240 data words from the Software Status Register.

The playback protocol used to transfer compressed speech data frames to the CT8022 also supports the ***Buffer Monitoring***, ***Frame Create***, ***Frame Delete***, and ***Playback Stop*** commands.

Host-to-Host decompression can be terminated either using the ***Playback Stop*** command or the ***Idle*** command. One of these commands should be issued during the command-status sequence in place of the ***playback C2*** command.

Decompression READY polling
Instead of using the ***decompression S1*** status READY response to determine if the CT8022 is ready with more uncompressed speech data, the Host can poll the READY state using the following command:

command:	5219H	
status:	0000H	if CT8022 is ready to provide more uncompressed data.
	0001H	if CT8022 is NOT ready to provide more uncompressed data.

This command is only valid if decompression mode is active.

The advantage this command offers over simple use of the ***decompression C1-S1*** command-status, is that it allows the Host to query the READY state without immediately committing to performing the data transfer. With the ***decompression C1-S1*** command-status, if the READY bit in the S1 status response is set, the Host *must* immediately transfer data.

9.22.3 Full Duplex Host-to-Host Compression-Decompression

The following command sequence is recommended for performing full duplex Host-to-Host Compression-Decompression. The sequence is described in summary form. For details on the individual steps listed, see the detailed descriptions above.

1. Start decompression using the ***decompression C1*** command and ***playback C2 and C3*** commands.
2. Start compression using the C1 command with DATA set to zero.
3. Perform data transfers using the following command loop:
   Check if CT8022 is ready for more playback data using the playback ***Buffer Monitoring*** command.
   If the playback buffer is empty:
   Transfer compressed speech data to CT8022.
4. Check if the CT8022 has decompressed data ready using the ***decompression ready*** polling command.
   If the CT8022 has decompressed data ready (status = 0000H):
   Transfer uncompressed speech data from CT8022.
5. Check if the CT8022 is ready to accept data for compression using the ***compression ready*** polling command.
   If the CT8022 is ready to accept more data for compression (status = 0000H):
   Transfer uncompressed speech data to CT8022.
6. Check if the CT8022 has record data available using the ***record buffer monitoring*** command.
   If the record buffer is not empty:
   Transfer compressed speech data from CT8022.

Repeat the above loop until all data has been processed.

Terminate the process after reading the last uncompressed playback data and reading the last compressed record data from the CT8022 by issuing the ***Idle*** command

9.23 Test Modes

The CT8022 includes test modes that are useful in verifying device and system operation.

9.23.1 Test Mode 1: Count Mode

Command: 511FH
Status: 511FH

In this test mode, data received from the external CODEC by the *record* channel is discarded and replaced by an 8-bit incrementing count. This is intended for use in a-law/μ-law speech mode, where the 8-bit CODEC *receive* data is passed directly to the Host.

9.23.2 Test Mode 2: Digital Milliwatt

Command: 511DH
Status: 511DH

In this test mode, data received from the external μ-law CODEC by the *record* channel is discarded and replaced by the CCITT G.711 a-law/μ-law digital milliwatt (0 dBm0) code sequence. This is a sequence of eight repeating bytes (a-law/μ-law samples) representing a 1 KHz sinewave at 0 dBm0.

9.23.3 Test Mode 3: Loopback

Command: 511CH
Status: 511CH

In this test mode, data received from the external CODEC by the record channel is discarded and replaced by the CODEC output data from the *transmit* (playback) channel. The playback channel is not affected by this mode of operation. The playback speech data is also transmitted to the output CODEC.

Note: *Receive* CODEC to *transmit* CODEC loopback can be performed by the Host with the CT8022 operating in normal mode. To do this, the Host simply copies μ-law frames from the *record* (receive) channel back to the *playback* (transmit) channel.

Use this command to support tone generation to the compressed speech direction (e.g. for generating far-end ringback tone).

9.23.4 Exit Test Mode

Command: 511EH
Status: 511EH

This command is used to exit test mode and return the *record* and *playback* channels to their normal operating mode.

9.23.5 CODEC Loopback

The CT8022 supports CODEC-input to CODEC-output loopback, independently of the test modes described previously. In this mode, every frame period (30ms), the CT8022 will loop-back 240 samples from the input CODEC back to the output CODEC. To enter this mode, the CT8022 must be in the IDLE state. To activate this mode use the command:

Command = 4000H
Status = 4000H

This loop-back mode can be used in conjunction with Test Mode 2 (Section 9.23.2) to generate a digital milliwatt output signal to the CODEC.

The ***CODEC Configuration*** command can be used to select the input and output CODECs used for the loop-back operation. For example, the following CODEC routings are possible:

Input Signal From	Output Signal To	CODEC Configuration Command	
		Output CODEC	Input CODEC
CODEC1	CODEC1	00	0
CODEC1	CODEC0	10	0
CODEC1	CODEC0 & 1	11	0
CODEC0	CODEC0	10	1
CODEC0	CODEC1	00	1
CODEC0	CODEC0 & 1	11	1

The Input CODEC field operates to exchange (swap) the input signals from CODEC0 and CODEC1.

Use of this form of loopback operation requires that the CT8022 be in the IDLE state when the command to activate loopback is issued. This loopback configuration cannot be used in conjunction with other CT8022 operational modes (e.g. *playback* and *record*). To perform loopback type operations in *record* or *playback*, refer to Section 9.23.6.

To exit loopback mode, the Host should issue the ***Idle*** command (0000H).

9.23.6 CODEC (Audio) Monitoring

CODEC Monitoring provides a mechanism that allows the input signal at one CODEC to be monitored (echoed) to the output of either or both CODECs. This mechanism operates independently of the primary CT8022 operational modes (e.g. *record*). This allows the Host to implement *call-screening* type functions where the user can monitor a recording being made via the input from CODEC 0 via the output of CODEC 1.

Command: CE1XH
Status: CE1XH
where X selects the action from the following table:

X	CODEC Routing Configuration
0	Normal operation This setting must be selected for standalone speakerphone operation
1	CODEC 0 input echoed to CODEC 0 output and CODEC 1 input echoed to CODEC 1 output
2	CODEC 0 input echoed to CODEC 1 output and CODEC 1 input echoed to CODEC 0 output
3	CODEC 0 input echoed to CODEC 0 and CODEC 1 output
4	CODEC 1 input echoed to CODEC 0 and CODEC 1 output

The values selected for Input CODEC and Output CODEC in the CODEC Configuration command override the CODEC routing described here. For example, setting CODEC Input to '1' will reverse the CODEC input entries in the above table.

For any operations involving playback or tone generation, X should be set to zero.

9.23.7 Speech Algorithm Testing

The CT8022 supports the following commands to support compliance verification of certain speech algorithms based on ITU standards. Note that these are special test mode commands only. Refer to the appropriate ITU Speech Coder Standard documentation for further information:

Set Post Filter Control

C1: 5416H
S1: 5416H
C2: 00XXH
C3: 00XXH

XX=00 Post Filter On (normal, default operating state)
XX=01 Reserved
XX=10H Post Filter Off for G.723.1

Set High Pass Filter

C1: 5417H
S1: 5417H
C2: 00XXH
C3: 00XXH

XX=00 High Pass Filter On (normal, default operating state)
XX=01 High Pass Filter Off (G.723.1)

9.24 Power Save Modes

9.24.1 CT8022 Stop Mode

The CT8022 can be placed into Stop Mode using the following command:

Command: 0FF0H

Since the CT8022 halts all internal operations in response to this command, there is no status response.

The CT8022 can only be released from Stop mode using the external RESET pin. After reset, the CT8022 performs internal initializations and then asserts the Control Ready bit in the Hardware Status Register. The Host must wait for the Control Ready bit to be set before issuing the first command. Following reset, the Host must re-program the CODEC configuration before attempting any other operations.

In stop mode, the CODEC signals FSYNC and SCLK are also stopped.

9.24.2 Stop CODEC Mode

Command: 0FF2H
Status: 0FF2H

In Stop CODEC mode, the CT8022 FSYNC and SCLK output pins are forced *low*. Holding FSYNC *low* and stopping SCLK will cause some CODECs to enter power down mode. See your CODEC data sheet to see if this feature is supported.

To achieve maximum system power saving, the CODEC interface should be placed in stop mode before placing the CT8022 itself in stop mode. Following this sequence will guarantee that FSYNC halts in *low* state.

Note: If pull-up/down resistors are connected to the FSYNC and SCLK pins to provide proper input voltages during reset, use of pull-down resistors will result in lower power consumption when the CODEC is in stop mode. However, pull-up resistors may be used if desired.

9.24.3 Re-Start CODEC

The CODEC can be re-started using the following command:

Command: 0FF3H
Status: 0FF3H

9.24.4 CT8022 Slowdown (Power Save) Modes

The Host can program the CT8022 to enter slowdown mode. In slow down mode, the clock rate of the internal DSP core is reduced to allow sufficient processing power for the operation selected. For example, when the CT8022 is performing full-duplex TrueSpeech 6.3 operation in conjunction with AEC operation, the DSP core must be run at full speed. However, when the CT8022 is being used in pass-through mode to playback uncompressed 16-bit linear data, the DSP core can be operated at greatly reduced speed.

To enter slow-down mode use the following command:

Command = 0FEXH where X is the internal DSP clock division factor
Status = 0FEXH

The internal DSP core clock is divided by (X+1), such that:

X=0 selects full speed
X=1 selects 1/2 speed
X=2 selects 1/3 speed
X=3 selects 1/4 speed
X=F selects 1/16 speed

The internal DSP clock frequency can be observed on the CLKOUT pin.

The following table gives an approximate guide to the processing speed required for some sample operations:

Operation	X Value	DSP Internal Speed Factor	Typical Power Consumption
Full-duplex TrueSpeech 6.3-4.1 + AEC	0	1.0	230 mA
Full-duplex TrueSpeech 8.5 + AEC	1	1/2	120 mA
Playback only (all modes)	3	1/5	60 mA
Full Duplex uncompressed speech	3	1/5	60 mA
Line Monitoring (tone detection)	3	1/5	60 mA
IDLE	F	1/16	35 mA

AEC = Acoustic Echo Canceller

9.24.5 Disable CLKOUT

To further conserve power and reduce EMI emissions, the CLKOUT signal of the CT8022 may be disabled with the following command:

Disable CLKOUT

Command: 0FF6H
Status: 0FF6H

Enable CLKOUT

Command: 0FF7H
Status: 0FF7H

9.24.6 Inter-Frame Idle Power Save

When the CT8022 is operating in Host-CODEC mode and providing real-time speech input/output during playback/record operation, the CT8022 executes an internal idle loop while waiting to begin processing of the next speech frame.

During this Inter-Frame Idle period, the CT8022 can be programmed to dynamically reduce the internal DSP core clock rate in order to further conserve power.

The command to set the Inter-Frame Idle Clock Division Factor is:

C1:	514AH
S1:	514AH
C2:	000XH
S2:	000XH

where X+1 is the division factor.

Note: The Inter-Frame Idle Clock Division Factor is reset each time the primary clock division factor is set using the 0FEXH command. Each time the Primary Clock Division Factor is programmed, the Inter-Frame Idle Clock Division Factor is set to the same value as the Primary Clock Division Factor.

Care should be taken not to reduce the clock to too low a value during the Inter-Frame Idle period as this may cause the CT8022 to respond as if there are insufficient MIPS available for overall processing. This may result in the AEC convergence/training being limited. Refer to Section 9.15.3.1.

9.25 General Purpose Input Output pins (GPIO)

The CT8022 provides 8 GPIO pins, GPIO-0 to GPIO-7. Two of these pins may be configured for system use to provide CT8015compatibility as DATAFLAGN and Frame Interrupt FR.

GPIO-0 may be used to provide the DATAFLAGN output signal
GPIO-5 may be used to provide the frame interrupt output signal

After reset, all pins are configured as inputs and are available for general purpose use by the Host controller.

9.25.1 Configure GPIO System Use

GPIO pins are configured for system use by setting the system/user control mask:

Command = 0AXXH:

0000 1010	0	0	GPIO5	0	0	0	0	GPIO0
(15-8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

Status = 00XXH:

0000 0000	0	0	GPIO5	0	0	0	0	GPIO0
(15-8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

Setting GPIO0 to 1enables GPIO0 as an output to provide the DATAFLAGN signal

Setting GPIO5 to 1 enables GPIO5 as an output to provide the Frame Interrupt pin FR

By default, both of these control bits are set to zero.

9.25.2 Configure GPIO Input/Output Direction:

Command = 09XXH:

0000 1001	GPIO-7	GPIO-6	X	X	GPIO-3	GPIO-2	GPIO-1	X
(15-8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

Status = 00XXH:

0000 0000	GPIO-7	GPIO-6	1	1	GPIO-3	GPIO-2	GPIO-1	1
(15-8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

Setting the GPIO bit to ‘1’ configures the pin as an output; setting the bit to ‘0’ configures the pin as an input.

9.25.3 Write GPIO Pins

Command = 0BXXH:

0000 1011	GPIO-7	GPIO-6	X	X	GPIO-3	GPIO-2	GPIO-1	X
(15-8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

Status = 00XXH:

0000 0000	GPIO-7	GPIO-6	FRN	X	GPIO-3	GPIO-2	GPIO-1	DATA FLAG
(15-8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

The status response echoes the GPIO bit values in the 0BXXH commands. Regardless of the GPIO direction configured, the status echoes the value written in the 0BXXH command. If the pin is an input, it is not affected by this operation. Bits 0, 4 and 5 of the status response show the current state of the CT8022 reserved output bits.

9.25.4 Read GPIO Pins

Command = 5143H (this is the Read FR - frame interrupt command):

0101	0001	0100	0011
(15-12)	(11-8)	(7-4)	(3-0)

Status = YYXXH:

GPIO-7 (read)	GPIO-6 (read)	GPIO-5 (read)	GPIO-4 FRN (read)	GPIO-3 (read)	GPIO-2 (read)	GPIO-1 (read)	GPIO-0 DATA-FLAG (read)
(15)	(14)	(13)	(12)	(11)	(10)	(9)	(8)

GPIO-7 (readback)	GPIO-6 (readback)	GPIO-5 (readback)	GPIO-4 FRN (readback)	GPIO-3 (readback)	GPIO-2 (readback)	GPIO-1 (readback)	GPIO-0 DATA-FLAG (readback)
(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

The most significant 8 bits "YY" of the status response show the state of the GPIO input pins.

The least significant 8 bits "XX" of the status response show the last data written to the GPIO pins (readback).

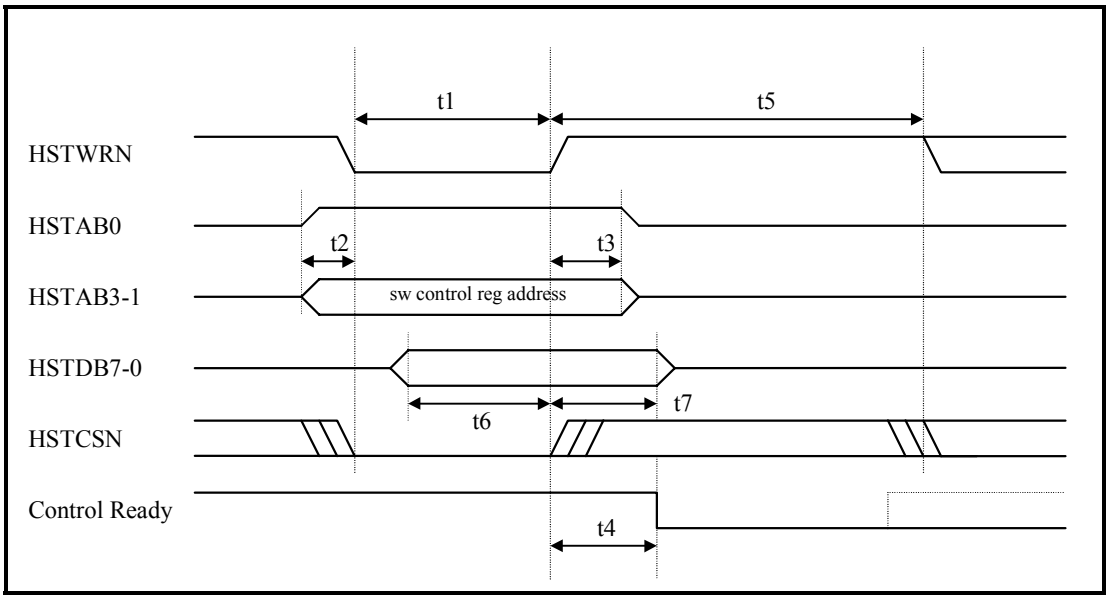
If the GPIO pin is configured as an input, the state of the input pin is reflected in the matching bit in the YY upper byte of the status reply. The matching bit in the XX lower byte shows the last value written to the pin. This *readback* value will control the state of the pin if the direction bit is changed to program the pin as an output. This represents the *potential* state of the pin, if it is changed to an output.

If the GPIO pin is configured as an output, the state of the pin as sensed by the GPIO hardware will be reflected in the YY upper byte (reading the state of the actual output pin). The last value actually written to the pin will be shown in the XX lower byte. Under normal circumstances, the bit value in XX and YY will match. Only under abnormal circumstances, for example a short circuit to ground, will the XX and YY bit states be different.

This is also the command shown in Section 9.16 of this data sheet, used for reading the state of the Frame Interrupt pin (FRN).

10 CT8022 Host Interface Timing

10.1 Host Write to Software Control Register Most Significant Byte

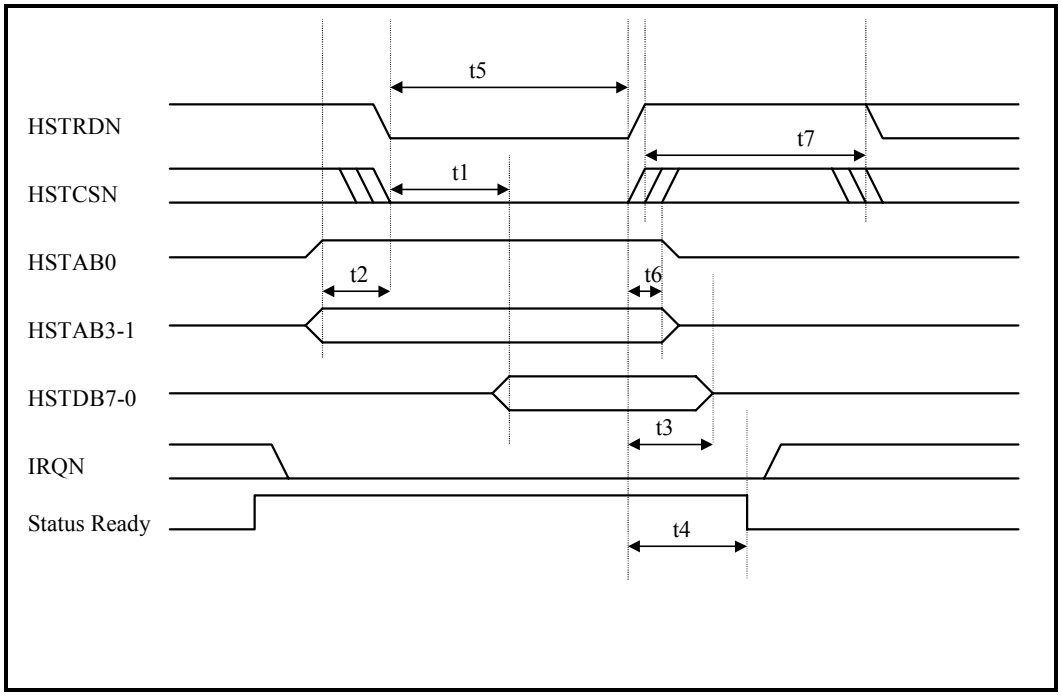


Parameter	Description	Min	Max
t1	HSTWRN pulse width	2 * MAINCLOCKP	
t2	HSTAB3-0 setup time before falling edge of HSTWRN or HSTCSN	5 ns	
t3	HSTAB3-0 hold time after rising edge of HSTWRN or HSTCSN	2 ns	
t4	Delay from rising edge of HSTWRN or HSTCSN to Control Ready cleared		MAINCLOCKP
t5	Recovery time between Host accesses	2 * MAINCLOCKP	
t6	HSTDB7-0 setup time before rising edge of HSTWRN or HSTCSN	20 ns	
t7	HSTDB7-0 hold time after rising edge of HSTWRN or HSTCSN	5 ns	

Notes:

1. **Host writes to most significant byte of Software Control Register.**
2. **Same timings apply to *writes* to Aux Control Register.**
3. **Control Ready (or Aux Control Ready) cleared by Host Write to Software Control Register (or Aux Software Control Register). Control Ready bit visible to Host in Hardware Status Register. Must be valid in time for *rea*d by next Host access.**
4. **MAINCLOCKP period = 2/XIN (effective) = 22.2 ns at 45.056 Mips with 4.096 MHz external crystal or 90.112 MHz external clock.**
5. **t4 may be negative.**
6. **t4 must be less than t5 so that Control Ready is valid for the next Host access. The Control Ready signal illustrated is the bit visible to the Host in the Hardware Status Register.**

10.2 Host Read from Software Status Register Most Significant Byte

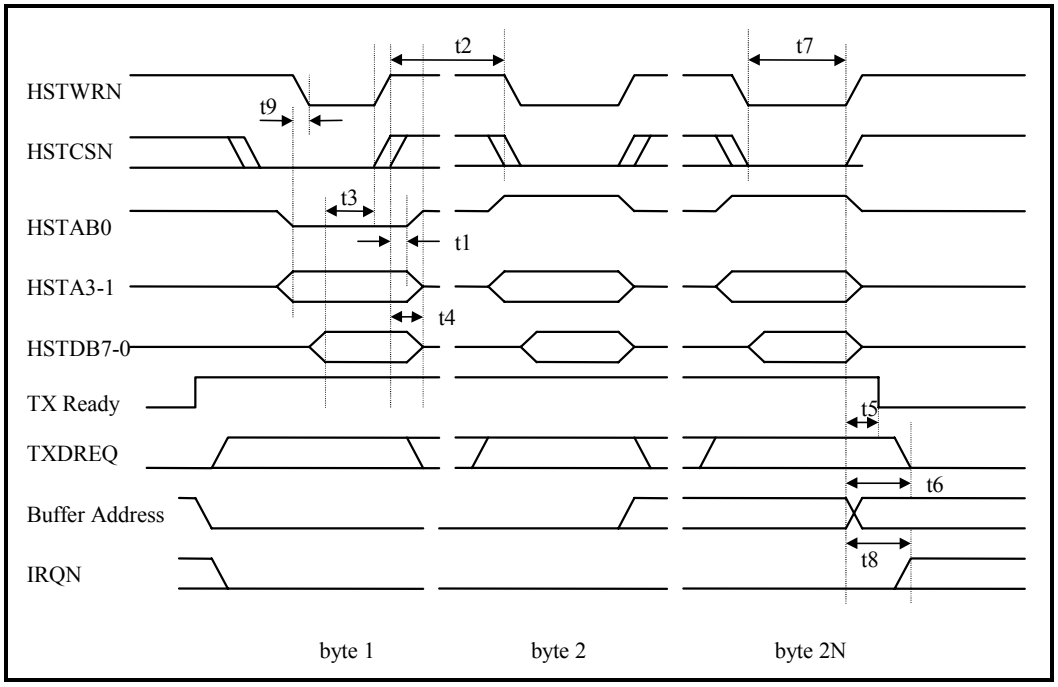


Parameter	Description	Min	Max
t1	HSTRDN or HSTCSN to data out valid		30 ns
t2	HSTAB3-0 setup time before falling edge of HSTRDN or HSTCSN	5 ns	
t3	HSTRDN or HSTCSN inactive to data out tri-state (output disable delay)		30 ns
t4	HSTRDN or HSTCSN positive edge to Status Ready clear		MAINCLOCKP
t5	HSTRDN or HSTCSN width	2 * MAINCLOCKP	
t6	HSTAB3-0 hold time after positive edge of HSTRDN or HSTCSN	2 ns	
t7	Recovery time between Host Accesses	2 * MAINCLOCKP	

Notes:

1. **Internal DSP *write* to Software Status Register (or Aux Software Status Register) sets Status Ready bit in Host Hardware Status Register.**
2. **IRQN asserted to Host assumes that the appropriate IE bit is set in the Host Hardware Control Register.**
3. **Host *read* of Software Status Register most significant byte clears Status Ready bit, de-asserts IRQN. The Status Ready bit illustrated is the bit that is visible to the Host in the Hardware Status Register.**
4. **t4 may be negative.**

10.3 Host Write to Host Transmit Data Buffer Access Port

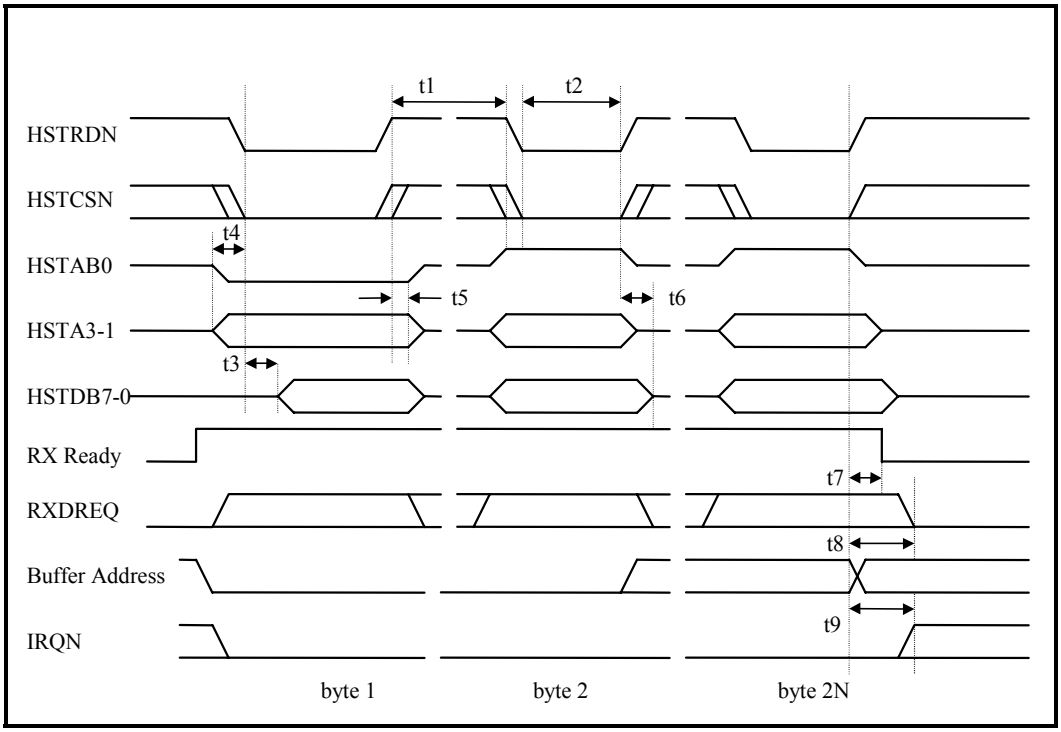


Parameter	Description	Min	Max
t1	HSTAB0-3 hold time after rising edge of HSTWRN or HSTCSN	2 ns	
t2	Recovery time between Host accesses	2 * MAINCLOCKP	
t3	HSTDB7-0 setup time before rising edge of HSTWRN or HSTCSN	20 ns	
t4	HSTDB7-0 hold time after rising edge of HSTWRN or HSTCSN	5 ns	
t5	Final rising edge of HSTWRN to TX Ready cleared		MAINCLOCKP
t6	Final rising edge of HSTWRN to TXDREQ cleared		MAINCLOCKP
t7	HSTWRN width	2 * MAINCLOCKP	
t8	Final rising edge of HSTWRN to IRQN de-asserted		MAINCLOCKP
t9	HSTAB3-0 valid before HSTWRN asserted	5 ns	

Notes:

1. **Internal Buffer Address cleared by transition of TX Ready bit from 0 to 1.**
2. **Internal Buffer Address increments on rising edge of HSTWRN only if HSTAB0 = 1.**
3. **TX Ready bit clears on final HSTWRN after N access with HSTAB0 =1, where N is the Frame Size value (word count).**
4. **TXDREQ asserted if TX DMA Enable bit is set in the Hardware Control Register.**
5. **TXDREQ may operate in Burst Mode or Single Cycle Mode.**
6. **IRQN driven by TX Ready if TX Ready IE bit set in Host Hardware Control Register.**
7. **t5, t6 and t8 may be negative.**

10.4 Host Read From Host Receive Data Buffer Access Port

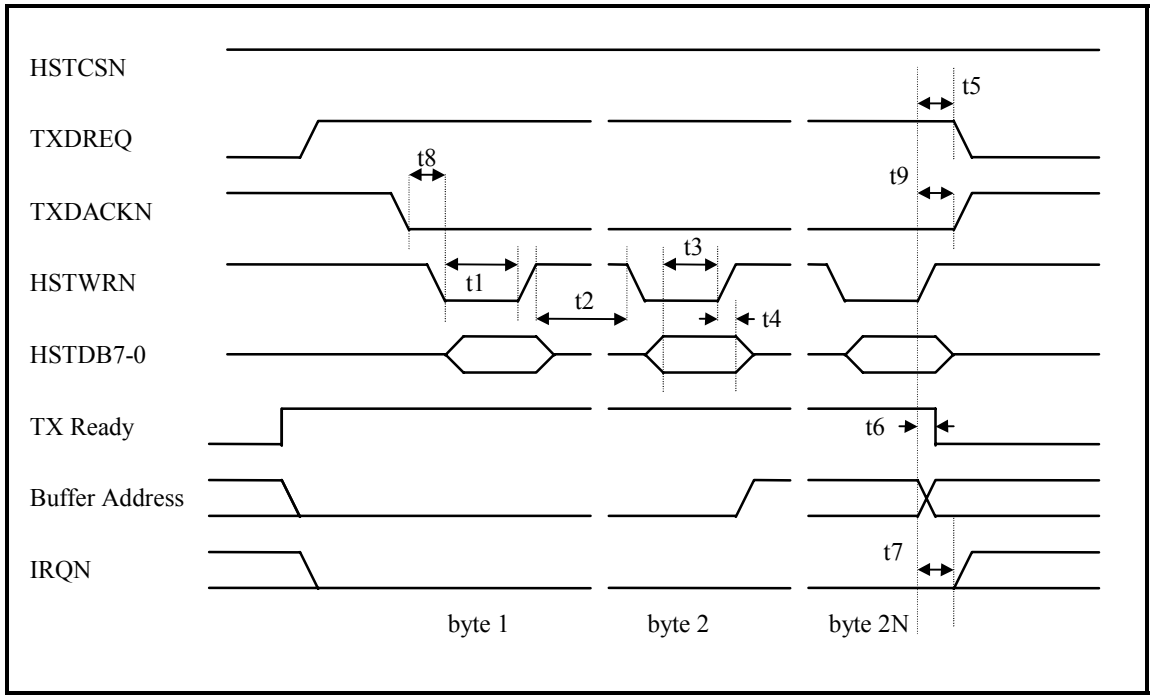


Parameter	Description	Min	Max
t1	Recovery time between Host accesses	2 * MAINCLOCKP	
t2	HSTRDN width	2 * MAINCLOCKP	
t3	HSTRDN or HSTCSN to data out valid		30 ns
t4	HSTAB3-0 setup time prior to falling edge of HSTRDN or HSTCSN	5 ns	
t5	HSTAB3-0 hold time after positive edge of HSTRDN or HSTCSN	2 ns	
t6	HSTRDN or HSTCSN inactive to data out tri-state (output disable delay)		30 ns
t7	Final rising edge of HSTRDN to RX Ready cleared		MAINCLOCKP
t8	Final rising edge of HSTRDN to RXDREQ cleared		MAINCLOCKP
t9	Final rising edge of HSTRDN to IRQN de-asserted		MAINCLOCKP

Notes:

1. **Internal Buffer Address cleared by transition of RX Ready bit from 0 to 1.**
2. **Internal Buffer Address increments on HSTRDN only if HSTAB0 = 1.**
3. **RX Ready bit clears on final HSTRDN after N accesses with HSTAB0=1, where N is the Frame Size value (word count).**
4. **RXDREQ asserted if DMA enable bit is set in the Hardware Control Register.**
5. **RXDREQ may operate in Burst Mode or Single Cycle Mode.**
6. **IRQN driven by RX Ready if RX Ready IE bit is set in the Host Hardware Control Register.**
7. **t7, t8, t9 may be negative.**

10.5 DMA Write to Host Transmit Data Buffer Access Port (Burst Mode)

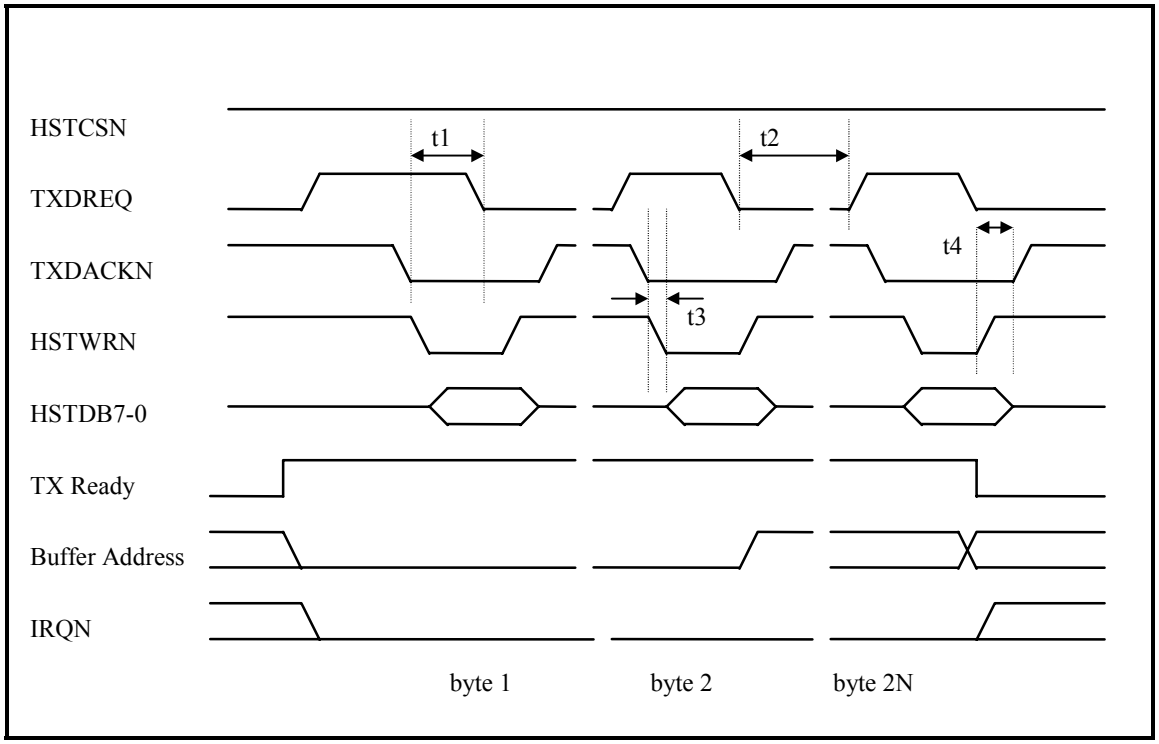


Parameter	Description	Min	Max
t1	HSTWRN width	2 * MAINCLOCKP	
t2	Recovery time between Host accesses	2 * MAINCLOCKP	
t3	HSTDB7-0 setup time before rising edge of HSTWRN	20 ns	
t4	HSTDB7-0 hold time after rising edge of HSTWRN	5 ns	
t5	TXDREQ de-asserted after final rising edge of HSTWRN		MAINCLOCKP
t6	Final rising edge of HSTWRN to TX Ready cleared		MAINCLOCKP
t7	Final rising edge of HSTWRN to IRQN cleared		MAINCLOCKP
t8	TXDACKN asserted before HSTWRN	5 ns	
t9	TXDACKN hold time after rising edge of HSTWRN	2 ns	

Notes:

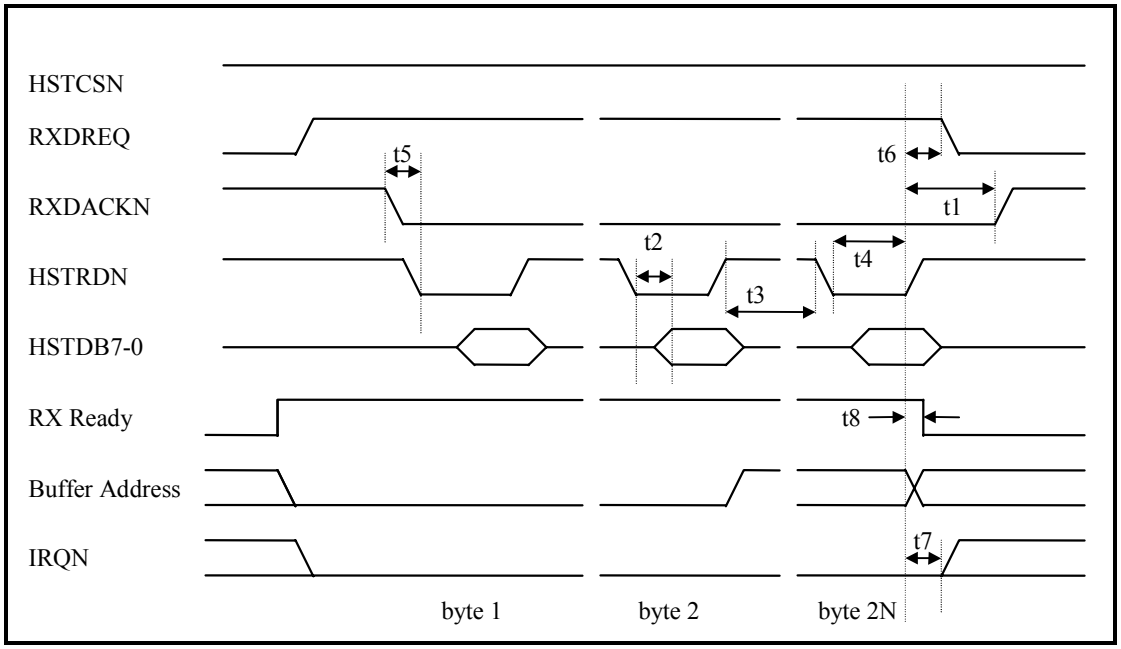
1. t5, t6, t7 may be negative.

10.6 DMA Write to Host Transmit Data Buffer Access Port (Single Cycle Mode)



Parameter	Description	Min	Max
t1	TXDACKN asserted to TXDREQ de-asserted response time		3 * MAINCLOCKP
t2	TXDREQ re-assertion delay	16 * MAINCLOCKP	
t3	TXDACKN setup time before falling edge of HSTWRN	5 ns	
t4	TXDACKN hold time after rising edge of HSTWRN	2 ns	

10.7 DMA Read from Host Receive Data Buffer Access Port (Burst Mode)

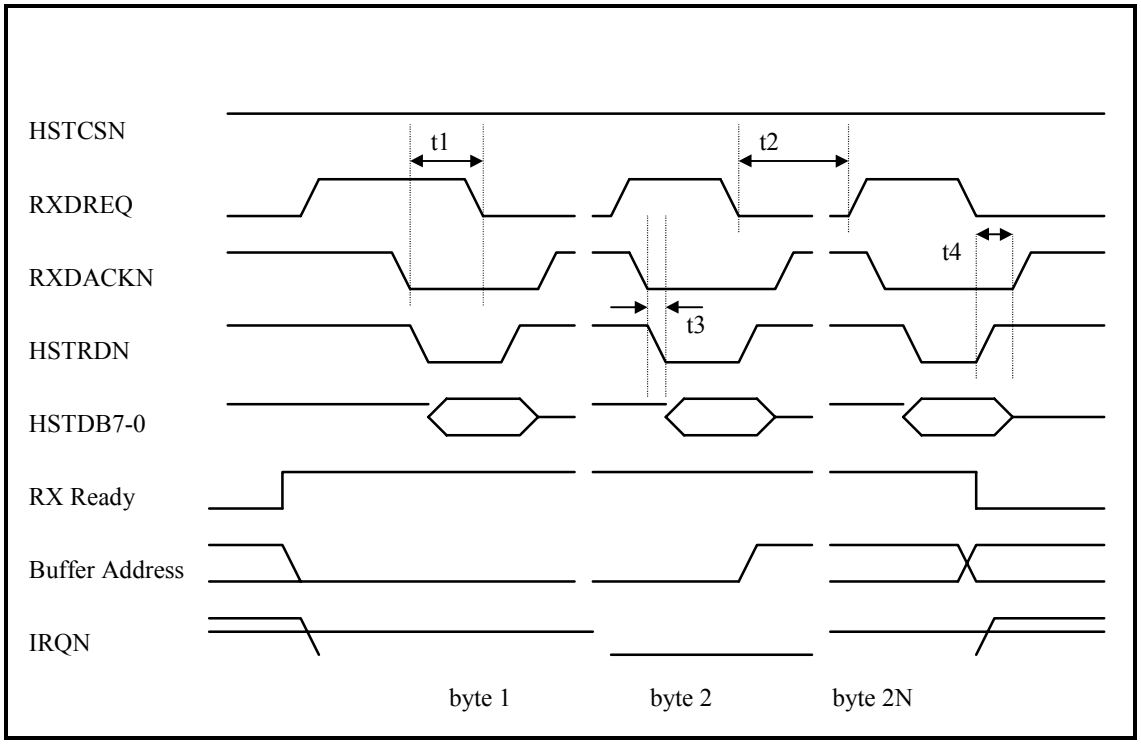


Parameter	Description	Min	Max
t1	RXDACKN hold time after rising edge of HSTRDN	2 ns	
t2	HSTRDN to data valid delay (access time)		30 ns
t3	Recovery time between DMA accesses	2 * MAINCLOCKP	
t4	HSTDRN width	2 * MAINCLOCKP	
t5	RXDACKN setup time before falling edge of HSTRDN	5 ns	
t6	Final rising edge of HSTRDN to RXDREQ de-assertion		MAINCLOCKP
t7	Final rising edge of HSTRDN to IRQN de-assertion		MAINCLOCKP
t8	Final rising edge of HSTDRN to RX Ready de-assertion		MAINCLOCKP

Notes:

1. t6, t7, t8 may be negative.

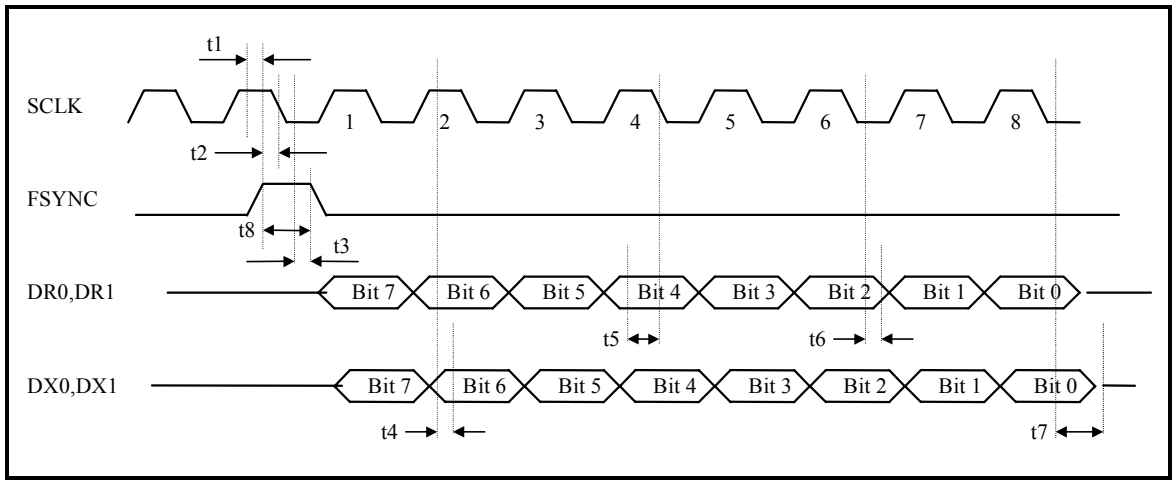
10.8 DMA Read from Host Receive Data Buffer Access Port (Single Cycle Mode)



Parameter	Description	Min	Max
t1	RXDACKN asserted to RXDREQ de-asserted response time		3 * MAINCLOCKP
t2	RXDREQ re-assertion delay	16 * MAINCLOCKP	
t3	RXDACKN setup before falling edge of HSTRDN	5 ns	
t4	RXDACKN hold time after rising edge of HSTRDN	2 ns	

11 CT8022 CODEC Interface Timing and AC Specification

11.1 Short Frame Sync

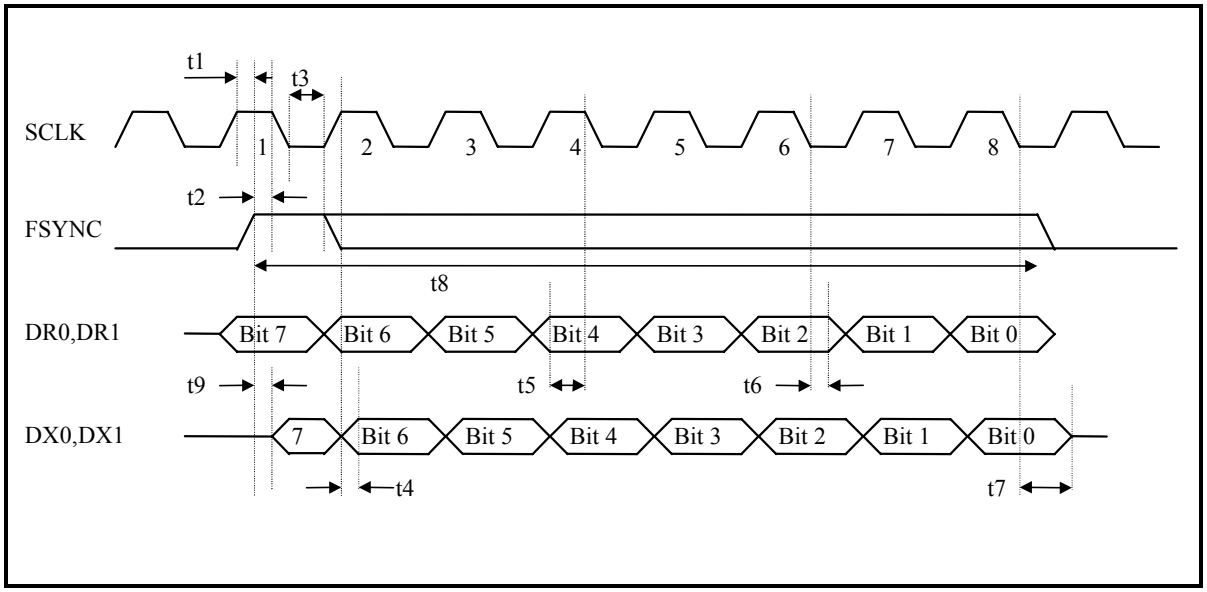


Parameter	Description	Min	Max
t1	Output delay from rising edge of SCLK to rising edge of FSYNC (master mode only)	0 ns	50 ns
t2	FSYNC setup time before falling edge of SCLK (slave mode only)	50 ns	
t3	FSYNC hold time after falling edge of SCLK. (slave mode only)	100 ns	
t4	SCLK rising edge to data output valid	0 ns	30 ns
t5	data in setup prior to falling edge of SCLK	30 ns	
t6	data in hold time after falling edge of SCLK	30 ns	
t7	data out tri-state after final falling edge of SCLK	0.25 * SCLKPERIOD (122 ns at 2.048 MHz)	0.5 * SCLKPERIOD (244 ns at 2.048 MHz)
t8	FSYNC width (master mode only)		1 SCLK period (nominal)
	SCLK duty cycle	45%	55%

Notes:

1. **SCLK is 2.048 MHz nominal; SCLKPERIOD is 488 ns nominal.**
2. **Timing diagram shows 8-bit mode only. In 16-bit mode, 16 bits of transmit data are shifted into and out of the CT8022. Bit 15 occurs first.**

11.2 Long Frame Sync



Parameter	Description	Min	Max
t1	Output delay from rising edge of SCLK to rising edge of FSYNC (master mode only)	0 ns	50 ns
t2	FSYNC setup time before falling edge of SCLK (slave mode only)	50 ns	
t3	FSYNC hold time after falling edge of SCLK. (slave mode only)	100 ns	
t4	SCLK rising edge to data output valid	0 ns	30 ns
t5	data in setup prior to falling edge of SCLK	30 ns	
t6	data in hold time after falling edge of SCLK	30 ns	
t7	data out tri-state after final falling edge of SCLK	0.25 * SCLKPERIOD (122 ns at 2.048 MHz)	0.5 * SCLKPERIOD (244 ns at 2.048 MHz)
t8	FSYNC width master mode slave mode	1 SCLK period	8 SCLK periods in 8-bit mode (nominal). 16 SCLK periods in 16-bit mode (nominal).
t9	ms data bit valid from rising edge of FSYNC. (slave mode only - output enable delay from FSYNC)	0 ns	30 ns
	SCLK duty cycle	45%	55%

Notes:

1. **SLCK is nominally 2.048 MHz.**
2. **Timing diagram shows 8-bit mode only. In 16-bit mode, 16 bits of data are shifted out of, or into the CT8022. Bit 15 is shifted first.**
3. **In master mode, FSYNC is 8 SCLK wide (8-bit mode) or 16 SCLK wide (16-bit mode).**
4. **In slave mode, FSYNC acts as an output enable for DX0,DX1 for the most signigicant data bit during the first SCLK period. (There is no internal synchronization delay on the first bit).**
5. **In slave mode, once the FSYNC signal has been present for one SCLK falling edge, the internal output enable for DX0 and DX1 is latched and remains active for the appropriate number of SCLK periods. The DX0 and DX1 outputs remain enabled, regardless of the state of FSYNC until after the final SCLK falling edge.**
6. **In master mode, where FSYNC is an output, it may be used as a tri-state control for gating the *receive* data. FSYNC will not be de-asserted by the CT8022 until the least significant *receive* data bit has been latched internally.**

12 Electrical Characteristics

Table 12-1: Absolute Maximum Ratings Over Specified Temperature Range

Supply voltage range, VCC	-0.3 V to 6 V
Input voltage range	-0.3 V to 6 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-55°C to 150°C

Table 12-2: Recommended Operating Conditions

PARAMETERS	MIN	TYP	MAX	UNIT
V_{CC} supply voltage	4.5	5	5.5	V
V_{SS} supply voltage		0		V
V_{IH} high-level input voltage (all digital input pins except RESET)	2			V
V_{IL} low-level input voltage (all digital input pins except RESET)			0.8	V
VT+ positive going RESET threshold (at VCC = 5.0 v)		3.35	4.6	V
VT- negative going RESET threshold	1.3	1.9		V
I_{OH} high level output current			+4	mA
I_{OL} low level output current			-4	mA
Oscillator crystal (100 PPM) Note: the exact 4.096 MHz crystal frequency used to generate the 45.056 main clock via the x11 PLL is required only if the CT8022 is to operate in CODEC master mode and generate a SCLK signal at exactly 2.048 MHz.		4.096	4.096	MHz
T_A operating free-air temperature	0		70	°C

The following circuit is recommended for driving the CT8022 RESET pin in order to meet the VIH spec for this pin:

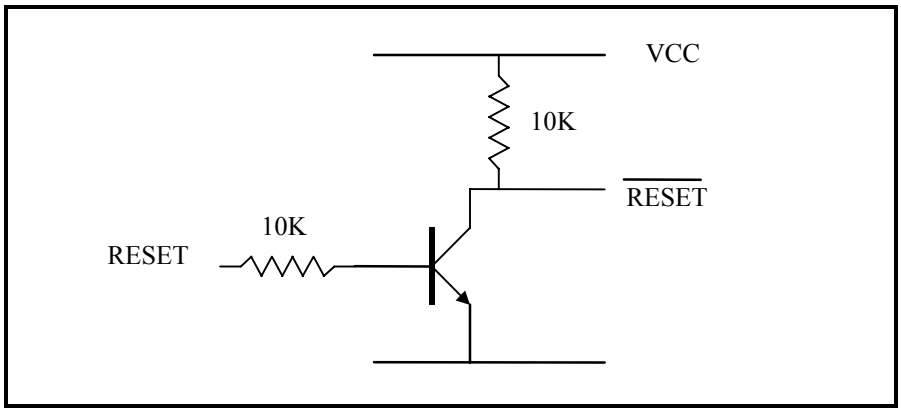


Table 12-3: Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} high level output voltage		VCC = 5V	2.4			V
V_{OL} low level output voltage					0.6	V
I_{OZ} off state output current		VCC = Max			20	µA
I_I input current (pins without pull down resistors)					±20	µA
I_I input current (pins with pull down resistors)					+20 -60	µA
ICC Supply Current	Operating Mode	f = 45.056 MIPS				mA
	Stop Device Mode	VCC = 5V		0.5	2	mA
	No Clock 25 °C all inputs GND all outputs NC	VCC = 5V		50		uA
CI Input capacitance					20	pF

Table 12-4: DTMF & Tone Generation Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
DTMF twist (high/low tone)		2	±8	dB
Tone generator frequency accuracy	-0.1		+0.1	%fc
Tone generator level*	-24		+6	dB0
Tone generator level accuracy	-0.5		+0.5	dB

*** 0 dB0 is 0.707 VRMs programmable with 2 dB resolution. Assumes FSYNC = 8.000 KHz**

Table 12-5: Acoustic Echo Canceller Performance

PARAMETER		NOTE
Acoustic Echo Cancellation	30 dB	1
Max echo delay	10ms	2, 3

Notes:

1. **The acoustic echo canceller achieves 30 dB of cancellation for white noise in less than 1.0 seconds with the speaker CODEC output connected to the microphone CODEC input via a 2:1 attenuator and an output level equivalent to -10 dBm0.**
2. **The acoustic echo canceller can cancell echos up to 10ms (approximately 3.4 meters or 11 feet in sound propagation.**
3. **Assumes operation of CODEC at 8.0 KHz sample rate.**

Table 12-6: Electrical Echo Canceller Performance

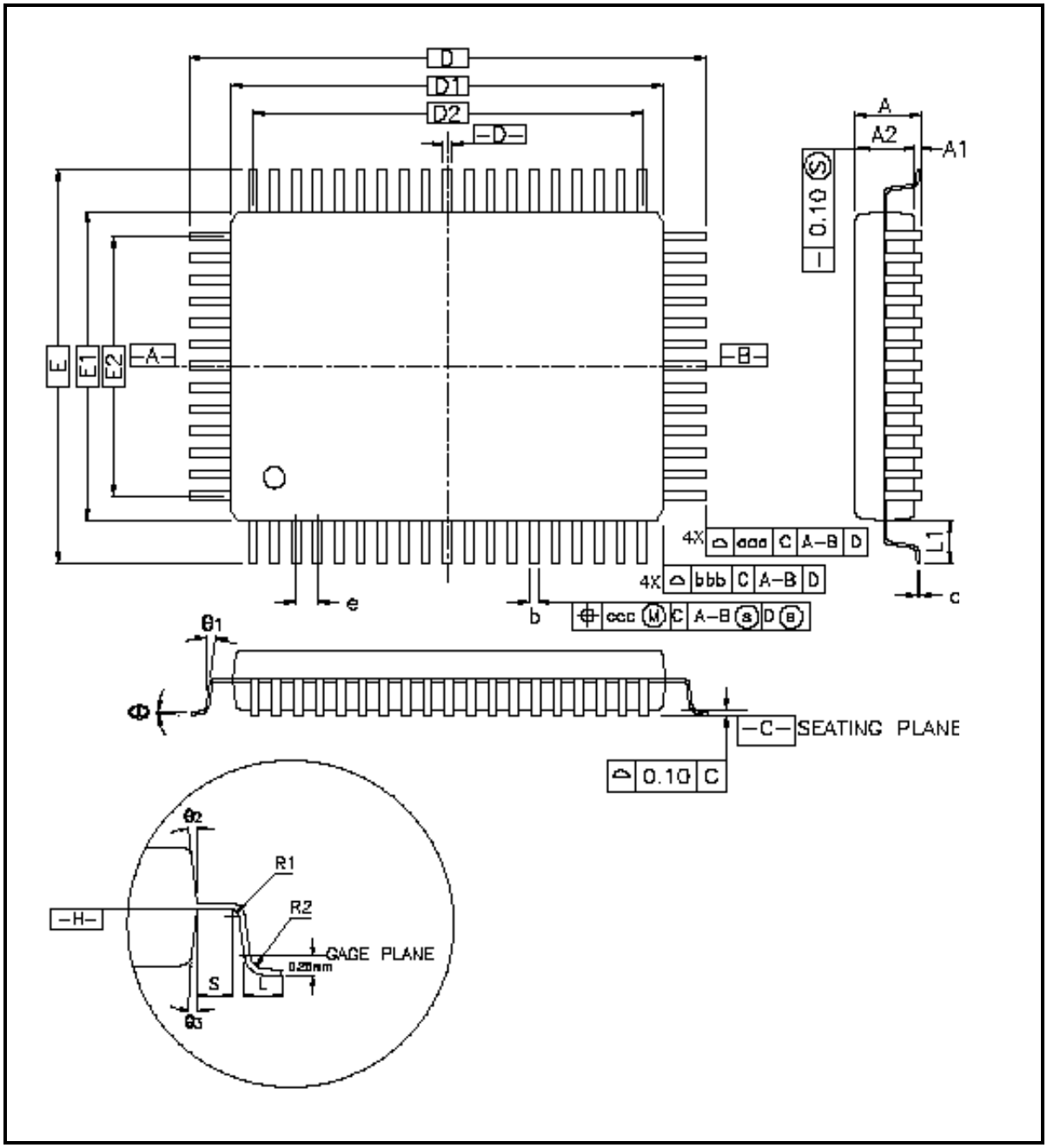
PARAMETER		NOTE
Training pulse duration	16ms	1
Echo duration	23.25ms	1
Canceller length	7.38ms	1,2
Training pulse peak amplitude	350 mV	3
Training pulse average peak amplitude	250 mV	3
Electrical echo cancellation	34 dB	4

Notes:

1. **Assumes operation of CODEC at 8.0 KHz sample rate.**
2. **The electrical echo canceller will model the impulse response of the attached line circuit for an impulse response up to this duration.**
3. **Measured at the CODEC output pin using a TP3054 Texas Instruments μ-law CODEC.**
4. **The electrical echo canceller will achieve 34 dB cancellation for white noise with the line CODEC output short circuit connected to the line CODEC input.**

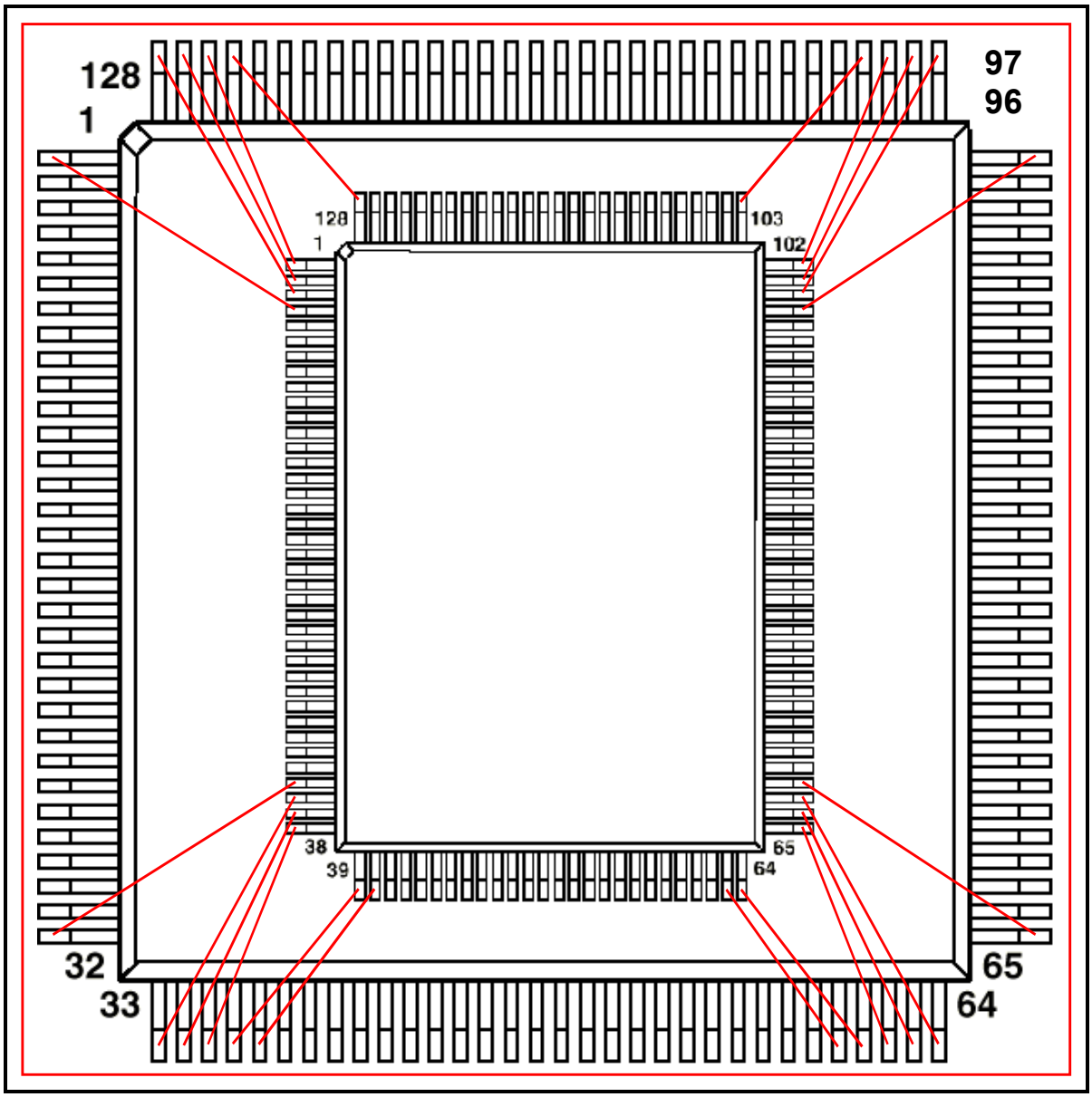
13 Mechanical Data - CT8022

13.1 PQFP Package 14x20mm



14 CT8020/1 Migration to CT8022

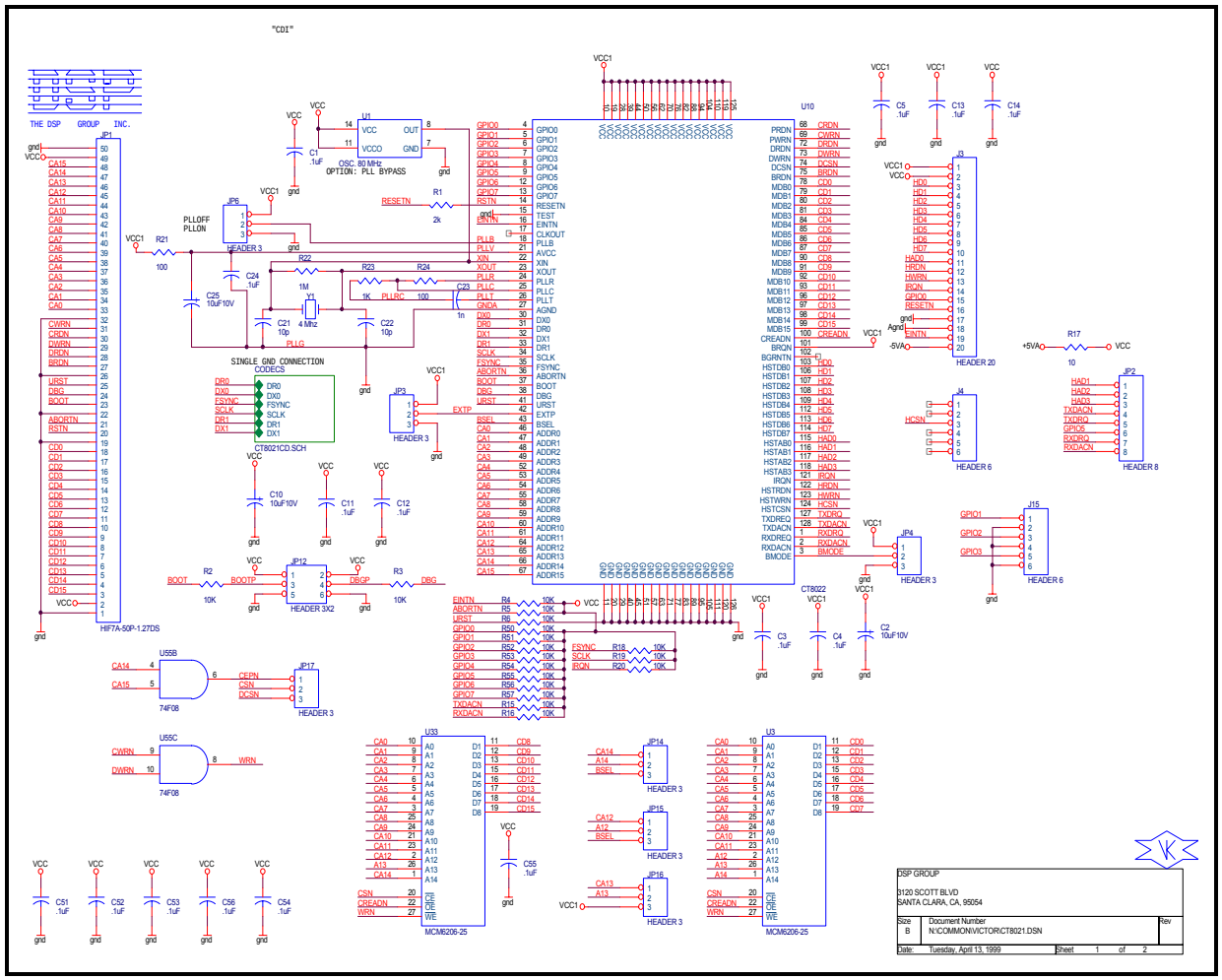
128-pin PQFP Package nesting: 14x20mm body built-in the 28x28mm body for direct replacement of CT8020/1 with CT8022 on the same PCB.



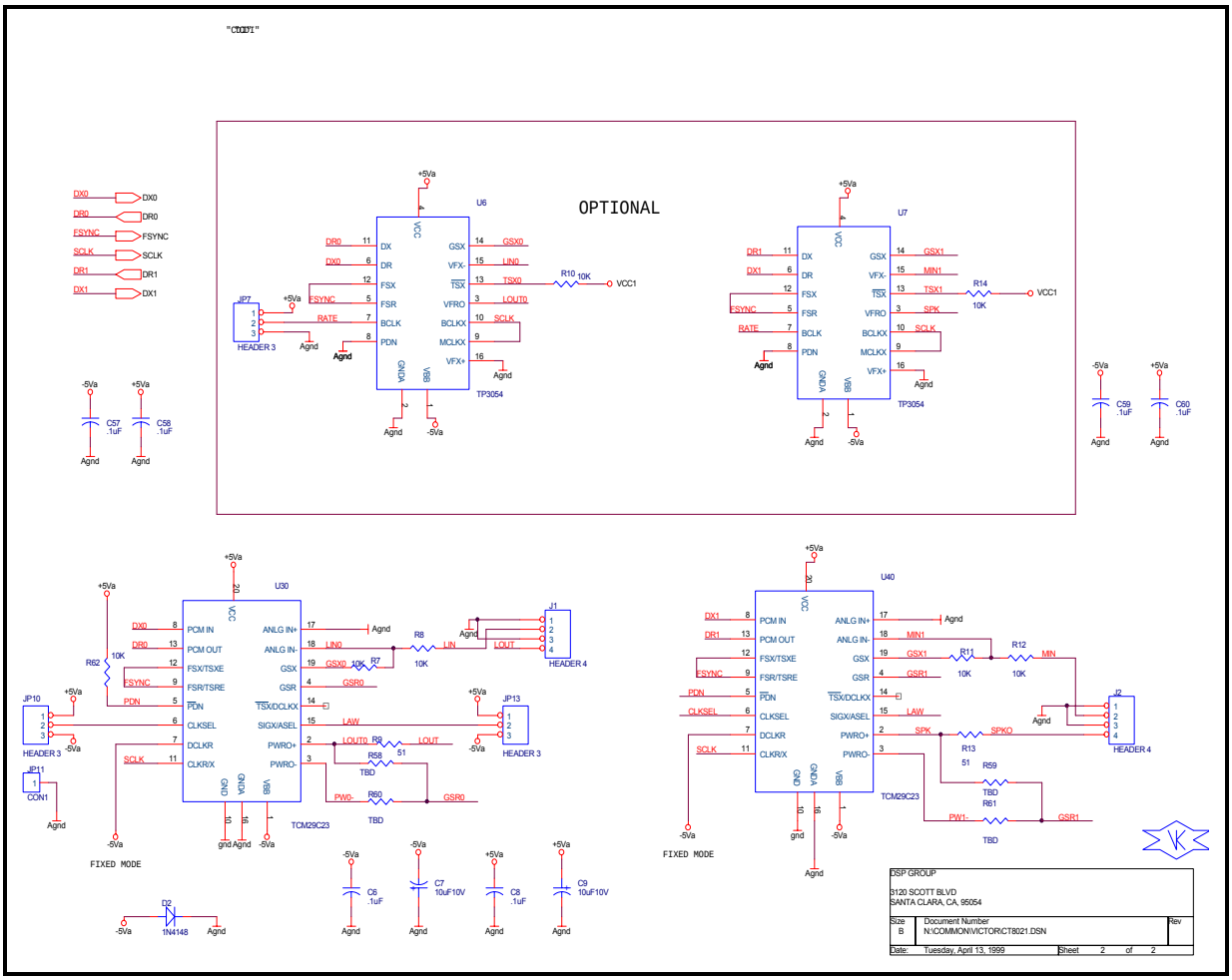
15 CT8022 EVB Schematic

15.1 CT8022 EVB

CT8022 EVB is intended for functionality evaluation and SW development. It is suitable for the entire CT802x family, and can accommodate CT8020, CT8021 and CT8022.



15.2 CT8022 EVB CODECs



Appendices

A Speakerphone Theory Of Operation

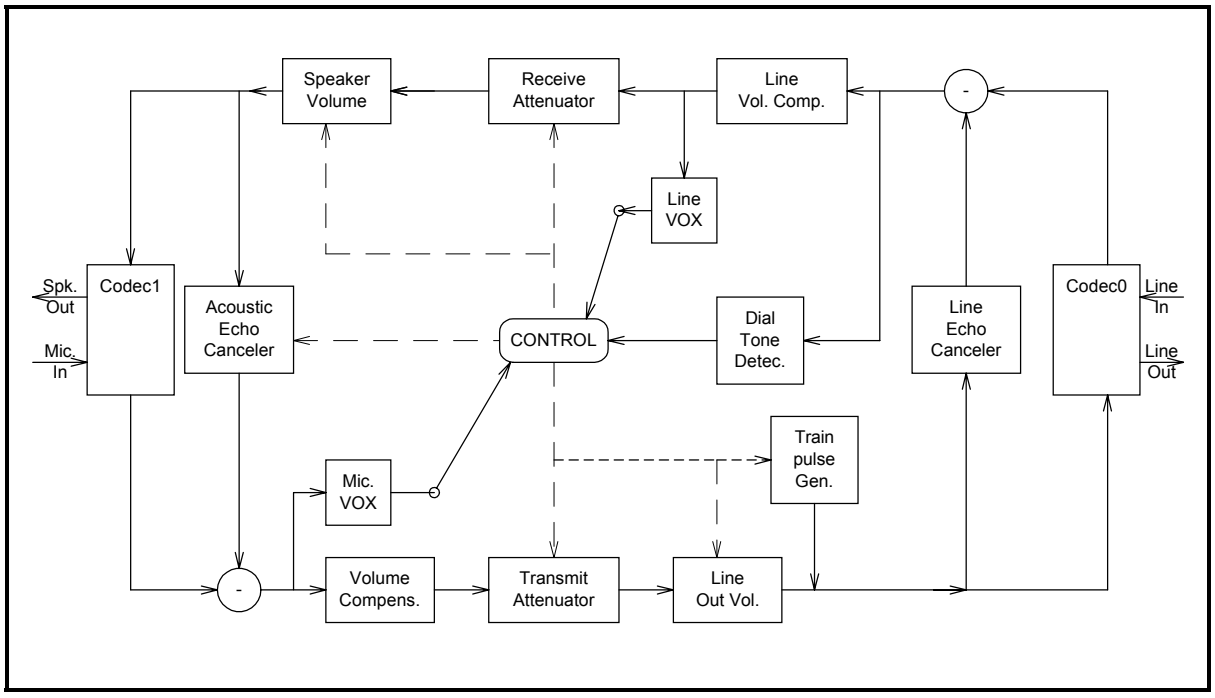


Figure A-1: SpeakerPhone – Digital Part

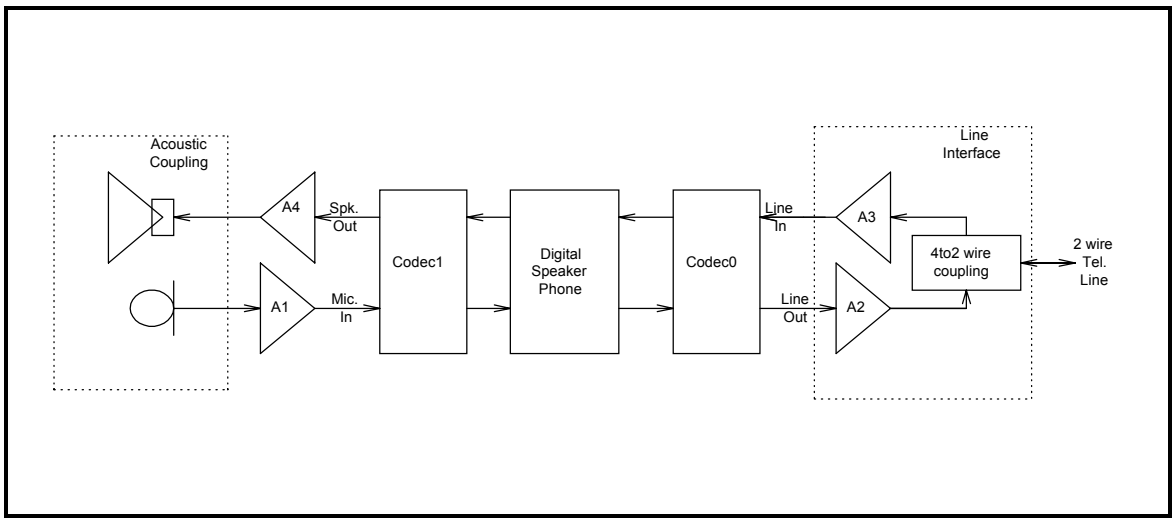


Figure A-2: SpeakerPhone – Acoustic and Analog Parts

A.1 Introduction

Implementation of a speakerphone system involves three primary sections:

- external analog circuitry
- physical acoustic devices
- digital canceller (provided by the CT8022)

Optimum speakerphone performance can only be achieved by the correct design and use of all three sections.

A.2 Analog Circuitry

The CT8022 interacts with the external physical system via two CODECs. CODEC0 connects to the telephone line, and CODEC1 connects to the microphone and speaker of the speakerphone. The input/output amplifiers (A1-A4 in Figure A) should be configured to make best use of the CODECs dynamic range without introducing distortion or clipping of the input/output signals. Care should be exercised in the design of the external circuits to avoid undesirable cross talk between the various sections. The 4-to-2 wire coupling circuitry at the telephone line interface should be designed to minimize the amount of the outgoing (*to line*) signal reflected (or *echoed*) back into the incoming signal (from *line*). The amount of gain within the loop formed by the amplifiers A1-A4, the 4-to-2 wire coupling, and the microphone-speaker acoustic linkage should be minimized.

The amplifier gains must be selected so that, when the voice signal comes from the microphone (and the telephone line is silent), the signal level at the CODEC microphone input (CODEC1) is higher than the reflected signal level at the CODEC line input (CODEC0). Further, when the voice signal originates from the telephone line, the input signal at CODEC0 must be higher than the signal resulting from the acoustic echo present at the microphone CODEC1 input. This arrangement allows the CT8022 to determine at any time whether the microphone or line side is speaking. The acoustic echo canceller is adjusted only when the CT8022 determines that the dominant signal is coming from the telephone line side.

A.3 Acoustic System

The quality of the microphone and speaker has a direct effect on the attainable level of speakerphone performance. Speech transducers that behave in a non-linear fashion introduce distortions into the signal that are not easy to cancel out. The microphone and speaker should be operated within their linear ranges. Over-driving of either the microphone of speaker must be avoided. It is possible to achieve significantly improved performance by eliminating any physical coupling between the microphone and speaker. Ideally, the speaker and microphone should not be housed within the same physical enclosure. Use of a freestanding speaker or microphone, separate from the main system housing, is recommended. In a personal computer application, it is often possible to connect to the PC's existing sound system speakers via the auxiliary input of a sound card. Use of a freestanding external microphone is often more convenient from the user's point of view, since it allows more flexibility in positioning. Placing of the microphone and speaker such that they are directly facing each other is not recommended. If microphone and speaker are contained within the same physical housing, care should be taken to minimize the physical coupling between them using acoustic isolation materials. In this situation, the physical coupling caused by the housing often creates more feedback than the acoustic path. Physical enclosures often exhibit resonances at particular frequencies; these should be damped as much as possible. It is also possible to reduce the effect of these resonances by electrical filtering within the analog circuitry.

A.4 CT8022 Digital Canceller

The CT8022 SpeakerPhone system actually contains two digital cancellers:

- an adaptive acoustical canceller which cancels the acoustic echo between microphone and speaker
- an electrical canceller which cancels the echo caused by the 4-to-2 wire telephone line connection

The CT8022 can be operated in two distinct modes:

- half-duplex mode where only the acoustic canceller is used
- full-duplex mode in which both cancellers are active

A.4.1 Half-Duplex Mode

In this half-duplex mode, the loop attenuation selected must be at least 12 dB. In this mode the SpeakerPhone operates by dynamically distributing the loop attenuation selected between the receive and transmit attenuators (see figure 1a). The CT8022 makes a decision as to which direction is talking, and then rapidly shifts the attenuation to the opposite direction. The total attenuation in the loop (receive attenuation plus transmit attenuation) remains constant. The exception to this is when the CT8022 detects abnormal conditions and loop adjustment mode 01 or 10 is selected. Under these circumstances, the CT8022 can (temporarily) introduce an additional 12 dB of attenuation in order to prevent howling or feedback. Abnormal conditions exist when the CT8022 determines that it unable to cancel the acoustic echo by adjusting the echo canceller coefficients. If loop adjust mode 10 is selected, the CT8022 will attempt to restore the original loop attenuation selected by reducing the additional attenuation in steps of 4 dB once the abnormal circumstances are removed.

Half-duplex mode is the default mode selected when the SpeakerPhone operation is started, before the training pulse has been sent to the telephone line activating the electrical echo canceller. The SpeakerPhone should always be started with a loop attenuation of at least 12 dB. The CT8022 operating in half-duplex mode provides for Host selection of the loop attenuation. This gives the system designer some flexibility in design of the external analog circuit. It also provides a more natural sounding speakerphone since the non-talking direction is never entirely muted as with some other speakerphone implementations. Using the lower attenuation levels offered by the CT8022 avoids the unnatural abrupt switching between active directions, present with alternative implementations, which causes the user to experience break up of the conversation.

A.4.2 Full-Duplex Mode

In full-duplex mode, the electrical (*line-side*) echo canceller must be activated by the Host micro-controller. When instructed, the CT8022 sends a *training* pulse of short duration to the telephone line to measure the echo (*impulse*) response of the line. This pulse is audible to the user, but is of very short duration and is not intrusive. There should not be any incoming signal from the telephone line when the training pulse is sent. The Host micro-controller must determine via an algorithm the correct time to send the pulse. On an incoming call, the pulse should be sent 100-200 ms after answering the call (going *off-hook*). This delay allows time for telephone line conditions to stabilize and for the ringing signal to cease. On an outgoing call, the pulse should ideally be ideally around 50ms after dialing the second digit. Again, this allows time for line conditions to stabilize, and avoids interfering with digit detection by the local telephone exchange. Sending the training pulse at this time also helps ensure that the line is silent, since at this point no ring tone or busy signal is likely to be present. Sending the training pulse at the end of a speed-dial or re-dial sequence also works well, provided it is sent before a ringing tone is presented. Sending the pulse after the first digit is not recommended since sometimes a secondary dial tone is encountered (as in dialing '9' for an outside line). The Host can determine if training was successful by using the ***Get Electrical Echo Canceller Quality Factor*** command.

The value of this parameter indicates the degree of echo cancellation from the telephone line. The precise threshold value, which indicates success or failure, depends to an extent on the design and amount of gain of the external hardware. Once the electrical echo canceller has been successfully trained, the loop attenuation can be safely reduced to zero or one of the other full-duplex attenuation factors. Since it is difficult to anticipate all circumstances under which the speakerphone may be used, a facility for the user to manually send the pulse should be provided in addition to the automatic training pulse control logic described. The speakerphone system should provide a manual speakerphone reset push button that the user can press to activate full duplex mode if the automatic control logic fails for any reason.

A.5 Volume Control

The CT8022 includes volume control for both the line output level (8dB range) and speaker output level (28dB range). The volume should be adjusted using the CT8022 rather than by changing external physical gain. In this way, the CT8022 is aware of the change in loop gain directly and can internally compensate for it, instead of having to adaptively adjust for the change. The CT8022 also supports speaker and microphone mute.

A.6 Dial Tone Detection

The CT8022 includes special handling for constant-level tone signals, such as a dial tone. The voice detectors used for controlling the loop attenuation ignore signals of this nature. When a steady tone is detected for a period of approximately 1-second, priority (or minimum attenuation) is automatically switched to the line side so that the user will hear the dial tone at full volume. Without this special handling, the CT8022 would see that both the *receive* and *transmit* directions had constant signal energy, and would distribute the loop attenuation equally between the two directions. Under these circumstances, the dial tone level heard by the user would be attenuated.

A.7 Performance

The acoustical echo canceller can handle echo delays up to 10ms (approximately 3.4 meters or 11 feet in sound propagation). The canceller supplies 34dB cancellation for white noise in less than 0.5 seconds with the speaker CODEC output short circuit connected to the microphone CODEC input.

The electrical echo canceller generates a training pulse of 16ms duration with an instantaneous peak output voltage of 350mV. The maximum line echo duration that will be cancelled is 23ms. With the output CODEC signal short circuit connected to the input CODEC signal, the electrical echo canceller achieves 34 dB of cancellation (measured with white noise). In this test, the echo canceller performance is limited primarily by the quantization noise associated with the D-to-A and A-to-D translations performed by the μ-law CODEC.

A.8 Control Algorithm Example

We provide this example for illustrative purposes only; system designers are free to construct their own control algorithms as desired.

On detection of an incoming call (off-hook preceded by ringing signal), the Host controller should start the speakerphone in half-duplex mode. The Host should then wait around 200ms following the off-hook transition before sending the electrical echo canceller training pulse to allow the line conditions to stabilize. After the training pulse has been sent, the Host should query the CT8022 to determine if electrical echo canceller training was successful. If not, the Host should attempt re-training at 500ms intervals for a total of three attempts. If training is not successful after three attempts, the Host should continue to let the speakerphone operate in half-duplex mode. Training will only fail if there is excessive noise present on the telephone line at the instant that the CT8022 attempts to send the training pulse. As an option, the system designer can provide a manual training or ***reset*** button, so that the user can decide when to send the training pulse.

On an outgoing call (e.g. speed dial), the Host again starts the speakerphone in half-duplex mode. After dialing of the second digit, the Host should wait 50ms and then attempt to send the training pulse. Once the training pulse has been sent, the Host can check whether the training process succeeded, or not. If training fails, the Host can try to train the electrical echo canceller after the third and subsequent digits, until adequate training is achieved. In the event that training is not possible, the Host can allow the speakerphone to continue operation in half-duplex mode. Sending the training pulse after the second digit is recommended, since in many installations a secondary dial tone may be presented after dialing of the first digit (for example dialing 9 for an external (public network) line).

Training needs to be achieved successfully only once during a call, as long as the physical line conditions do not change. An example of a change that would require re-training is the situation where a second telephone goes off-hook and operates in parallel with the original telephone.

Note that true full duplex operation will only be achieved after the electrical echo canceller has successfully trained and the acoustic echo canceller has had time to self-adjust. The acoustic echo canceller is only updated when the telephone line side is talking and the microphone side is silent. This may require a few seconds. When operated in loop adjustment mode 10 (the recommended setting), the CT8022 compensates for the initial start-up conditions by inserting additional loop attenuation. Once the acoustic echo canceller has stabilized, the additional loop attenuation is reduced and then removed.

Note that in an implementation where the microphone and speaker are physically separate from each other (this is the preferred implementation), the user should be discouraged from moving either microphone or speaker during a call. When the microphone and speaker change relative positions, the acoustic echo canceller has to work harder to compensate for the changed acoustic echo path. Under these circumstances, in loop adjustment mode 10, the CT8022 may again introduce temporary extra loop attenuation until the situation re-stabilizes. In addition, if the user desires to change the loud speaker volume, this should be done via the CT8022 controls and not by changing the external speaker amplification.

B AEC Performance In DSVD Applications

The CT8022 operates the same AEC algorithm in DSVD mode as Speakerphone mode. Since the AEC canceller operates on the input signal from the microphone, the effect of the AEC is heard at the far-end, as opposed to near-end of the DSVD communication link. The echo path in a symmetrical CT8022 implementation is shown below:

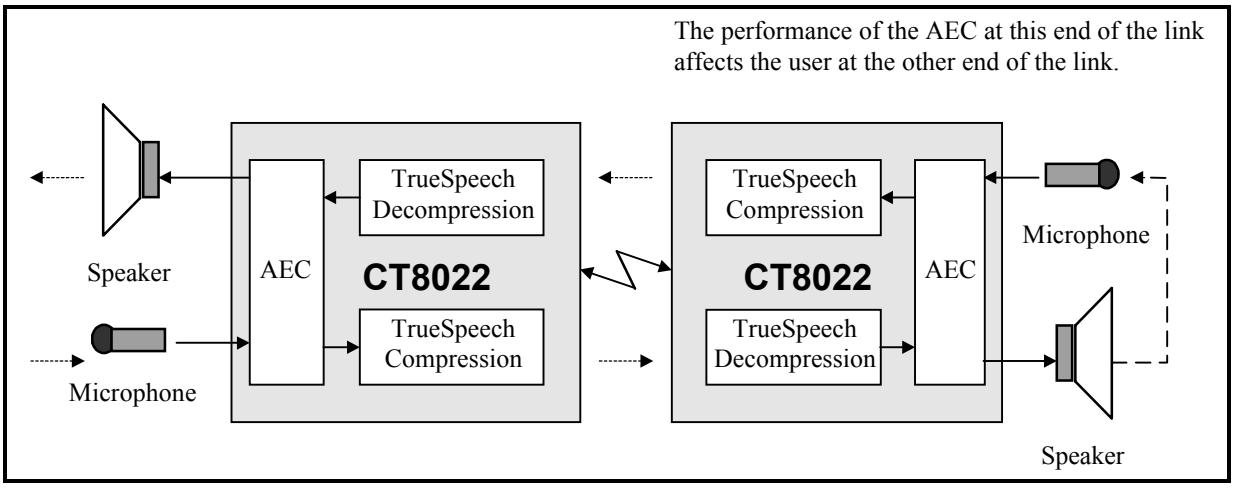


Figure B-1: CT8022s Connected via a Digital Link

Under ideal conditions, the AEC can achieve around 34dB of echo attenuation. With a symmetrical arrangement as shown above, this can produce up to 68dB of loop (or *round-trip*) attenuation. This is more than sufficient to ensure that acoustic feedback, howling or howl-round does not occur. However, the audible echo (attenuated by up to 34dB) may be overly annoying to users, due to the significant delay that is often present in this type of configuration. The key problem in this environment is the size of the delay, which may be several hundred milliseconds.

When the AEC is active in *speakerphone* mode, the primary consideration is to prevent *howling*. This condition is met, when the total loop gain in the system is less than 1.0. The round-trip delay in this mode is very short. With a short delay, the human ear is not able to perceive an echo with 34dB of attenuation except as a minor reverberation sound effect.

When the AEC is active in *DSVD* mode, since the delay is much greater, the *perceptual response to the same level echo is much greater*. The effect of a user hearing their own words echoed back to them with a 300-500ms delay is very distracting, even with 34dB of attenuation. To overcome this problem, it is necessary to introduce additional attenuation into the loop. To this end, it is recommended that the AEC be operated with at least 12dB of loop attenuation. While this precludes the possibility of operating in true full-duplex DSVD speakerphone mode, the additional 12dB of attenuation enable the CT8022 to achieve *near* full-duplex operation.

In this mode, the CT8022 monitors the *receive* and *transmit* directions in order to decide which direction is talking. It then attenuates the opposite direction by the selected amount of loop attenuation. The loop attenuation setting is programmable by the Host in 4dB increments from 0 to 28dB. The active switching of attenuation between the two speech directions is usually not noticeable to the user. The near full-duplex performance of the CT8022 in this mode still provides superior performance to comparable systems operating in half-duplex mode, where, at any time, one speech direction is completely muted. Also note that, without the active AEC in the illustrated situation, howling is extremely likely to occur, making the speech link unusable.

The CT8022 may be operated in DSVD mode without the AEC if a handset is used in place of a speaker-microphone arrangement.

C Wave File Format (.wav)

WAVE file format is actually a sub-format of RIFF (Resource Interchange File Format) and is as follows:

Example for 8/16 bit linear data (the byte offsets given are for illustration only; the byte offsets in a wave file are not absolute):

Byte Offset	Number of Bytes	Contents
0000H	4	"RIFF" = 52 49 46 46 (hex)
0004H	4	filesize -8 (the size of the waveform chunk)
0008H	4	"WAVE" = 57 41 56 45 (hex)
000CH	4	"fmt " = 66 6D 74 20 (hex)
0010H	4	format chunk size (16 for linear data)
0014H	2	wFormatTag = 1 (WAVE_FORMAT_PCM)
0016H	2	nChannels (number of channels 1:mono 2:stereo)
0018H	4	nSamplesPerSec (e.g. 8000)
001CH	4	nAvgBytesPerSec (.e.g. 8000, 16000)
0020H	2	nBlockAlign (block size in bytes 8-bit mono:1, 16 bit stereo:4)
0022H	2	wBitsPerSample (e.g. 8 or 16)
0024H	4	"data" = 64 61 74 61 (hex)
0028H	4	waveform data size (bytes)
002CH		start of actual waveform data

Example for TrueSpeech data (the byte offsets given are for illustration only; the byte offsets in a wave file are not absolute):

Byte Offset	Number of Bytes	Contents
0000H	4	"RIFF" = 52 49 46 46 (hex)
0004H	4	filesize -8 (the size of the waveform chunk)
0008H	4	"WAVE" = 57 41 56 45 (hex)
000CH	4	"fmt " = 66 6D 74 20 (hex)
0010H	4	format chunk size = 32H
0014H	2	wFormatTag = 22H (TrueSpeech tag value)
0016H	2	nChannels = 1
0018H	4	nSamplesPerSec = 8000
001CH	4	nAvgBytesPerSec = 1067 (used for buffer size estimation)
0020H	2	nBlockAlign = 20H
0022H	2	wBitsPerSample = 1
0024H	2	cbSize = 20H (size of extension area following)
0026H	2	wRevision = 1 (For TrueSpeech 8.5)
0028H	2	nSamplesPerBlock = 240
002AH	28	abReserved[28] (reserved area)
0042H	4	"fact" = 66 61 63 74
0046H	4	fact chunk size = 4
004AH	4	time length of data in sample units (e.g. 8000 = 1 sec)
004EH	4	"data" = 64 61 74 61 (hex)
0052H	4	waveform data size (bytes)
0056H		start of actual waveform data

Note: All wave formats except WAVE_FORMAT_PCM are required to include a *fact* chunk that gives the time length of the *data* chunk expressed in the samples.

The general format for wave files consists of a 4-byte ASCII tag for each chunk (“fmt”, “data”). This is followed by a 4-byte tag giving the length of the chunk (not including the 8-byte tag-length header), followed by the actual data for the chunk. A wave file can contain many chunks in any order. An application must search for the chunks it is interested in by skipping over other chunks that it does not understand. For example:

“RIFF”
“WAVE”
“test”
16
16 bytes of “test” chunk data
“fmt “
16
16 bytes of “fmt “ data
“data”
1024
1024 bytes of “data”
“more”
32
32 bytes of “more” data

Note: The case of the 4-byte ASCII tag is significant.

When an application encounters the tag “test”, it should read the next 4 bytes, which contain the length (16) of the “test” chunk. The application should then move forward through the file 16 bytes. This will position the file at the next chunk tag. The application should then read this tag and repeat the above process until it encounters the chunk that it is looking for.

To play back a wave file, the application should first find the “fmt “ chunk and determine if it can handle the wave format that it describes. Only then should the application search for the “data” chunk to obtain the actual waveform data.

D CT8022 Evaluation Board

The following diagram shows the layout of the CT8022. It indicates the positions of the main components and connectors. The actual EVB may contain locations for additional components. These additional components are not required for operation of the CT8022. They are intended to support operation of other devices in the CT8XXX family. Connector pins are on a pitch of 0.1 inch.

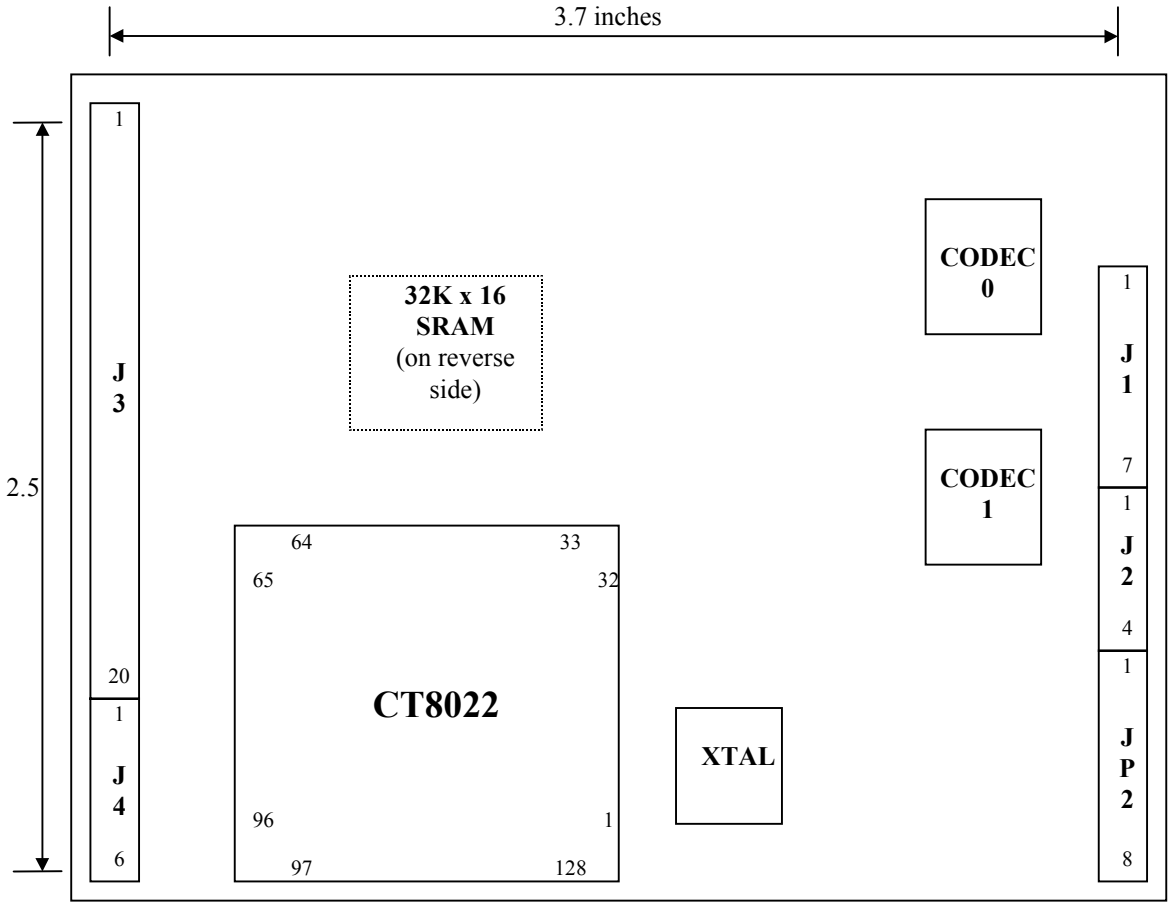


Figure C-1: CT8022 Family EVB

The following components, shown on the *full* EVB schematics, were used for development purposes *only* and are not required for normal operation of the CT8022:

- external program SRAMs MCM670R-6
- external EPROM 27010PLCC
- connector JP1

EVB boards normally supplied to customers do not include these additional components. The EVB contains options for several SRAM configurations. The minimum SRAM configuration for the CT8022 is 8K x 16, but 32K x 16 is recommend for future compatibility.

The jumper pin connection settings for normal operation are TBD.

D.1 CT8022 EVB Connector Pin Out

J1	
1	AGND
2	Line In
3	AGND
4	Line Out
5	(Line Out-)
6	AGND
7	(Speaker Out-)

J4	
1	
2	GPIO1
3	HSTCSN
4	
5	
6	

J2	
1	AGND
2	Mic In
3	AGND
4	Speaker Out

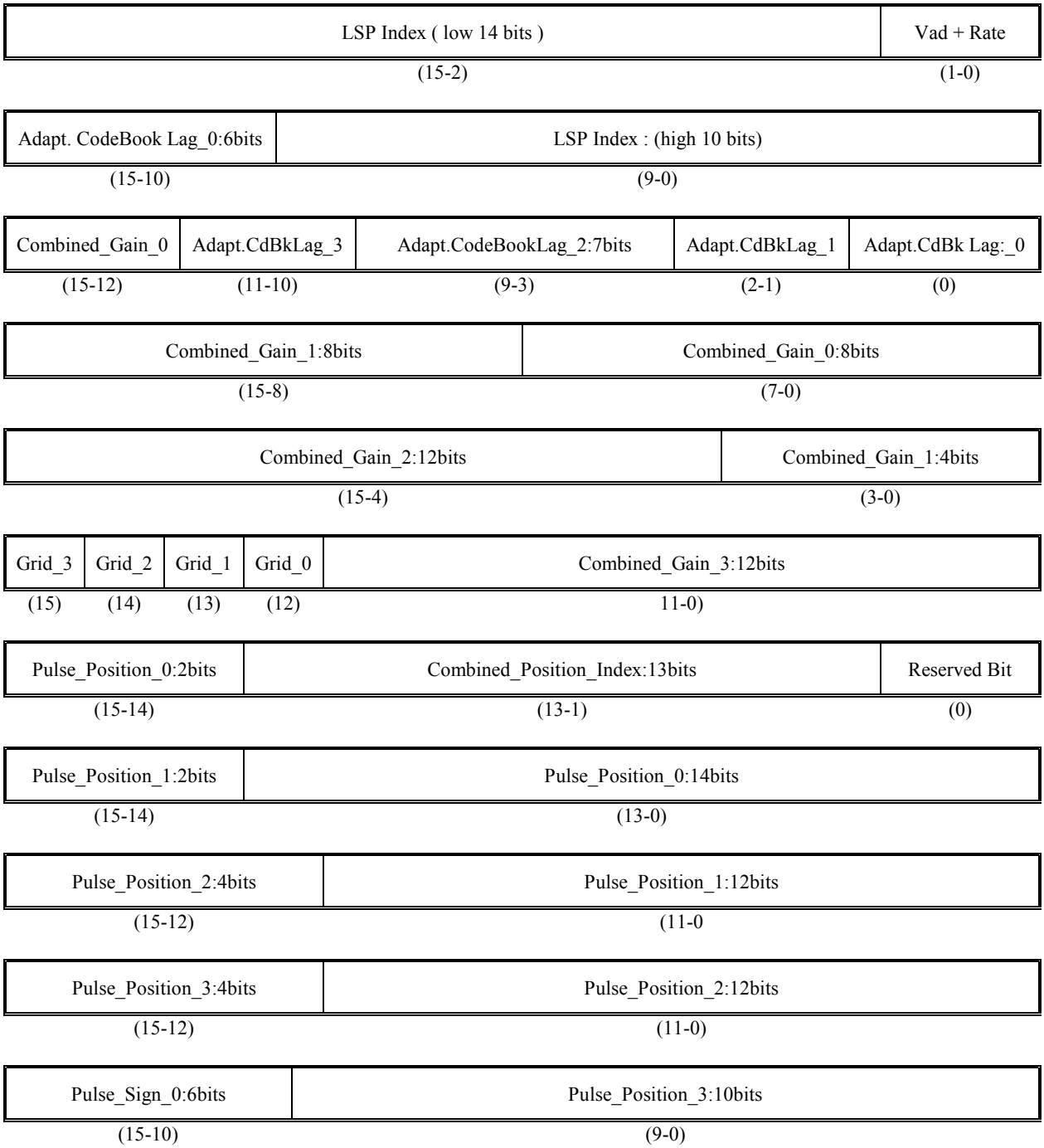
JP2	
1	HSTAB1
2	HSTAB2
3	HSTAB3
4	TXDACKN
5	TXDREQ
6	GPI05 / FRN
7	RXDREQ
8	RXDACKN

J3	
1	VCC +5V
2	VCC1 +5V
3	HSTDB0
4	HSTDB1
5	HSTDB2
6	HSTDB3
7	HSTDB4
8	HSTDB5
9	HSTDB6
10	HSTDB7
11	HSTAB0
12	HSTRD
13	HSTWR
14	IRQN
15	GPIO0 / DATAFLAGN
16	RESETN
17	GND
18	AGND
19	EXTINTN
20	-5V

E G.723.1 Frame Structure

This appendix shows the bit packing scheme used for compressed speech blocks for the G.723.1 6.3 and 5.3 bit rates. Note that the bit packing arrangement has changed from that used by the (pre-release) v3.0 of G.723.1, which was incorporated into the original CT8020A11AQC engineering samples and v4.0 in the CT8020A11BQC devices.

The following shows the bit packing used by all versions of the CT8022 and the CT8020D11AQC for the 6.3 data rate. The compressed speech frame consists of a block of 12 16-bit words. The least significant 2 bits indicate the type of compressed speech block.



Pulse_sign_3:5bits	Pulse_Sign_2:6bits	Pulse_Sign_1:5bits
(15-11	(10-5)	(4-0)

The following shows the bit packing used by the CT8020, CT8021, and CT8022 for the 5.3 data rate. The compressed speech frame consists of a block of 10 16-bit words. The least significant 2 bits indicate the type of compressed speech block.

LSP Index (low 14 bits)	Vad + Rate
(15-2)	(1-0)

Adapt. CodeBook Lag_0:6bits	LSP Index : (high 10 bits)
(15-10	(9-0)

Combined_Gain_0	Adapt.CdBkLag_3	Adapt.CodeBookLag_2:7bits	Adapt.CdBkLag_1	Adapt.CdBkLag:_0
(15-12)	(11-10)	(9-3)	(2-1)	(0)

Combined_Gain_1:8bits	Combined_Gain_0:8bits
(15-8_	(7-0)

Combined_Gain_2:12bits	Combined_Gain_1:4bits
(15-4)	(3-0)

Grid_3	Grid_2	Grid_1	Grid_0	Combined_Gain_3:12bits
(15)	(14)	(13)	(12)	(11-0)

Pulse_Position_1:4bits	Pulse_Position_0:12bits
(15-12)	(11-0)

Pulse_Position_2:8bits	Pulse_Position_1:8bits
(15-8	(7-0)

Pulse_Position_3:12bits	Pulse_Position_2:4bits
(15-4)	(3-0)

Pulse_Sign_3:4bits	Pulse_Sign_2:4bits	Pulse_Sign_1:4bits	Pulse_Sign_0:4bits
(15-12)	(11-8)	(7-4)	(3-0)

E.1 G.723.1 Version History

The CT8020D11AQC (firmware revision 0114) and all CT8021 and CT8022 versions implement (final-release) version 5.1 of G.723.1. Earlier versions of the CT8020 included pre-release versions of G.723.1, which are not directly compatible with the final v5.1 implementation. Transcoding between versions is possible using conversion software available from DSP Group. Following is a brief description of the G.723.1 revision history and its effect on the CT8020.

- v3.0, September 1995 - used in initial CT8020A11AQC engineering samples
- v4.0, January 1996 - almost the same as v3.0 but with different bit packing structure for the compressed speech frames. This version is included in the CT8020A11BQC devices.
- v4.1, April 1996 - fixed some instability problems in the G.723.1 algorithm encountered when pure sinewaves encoded.
- v5.0, May 1996 - added silence compression VAD/CNG as Annex A of G.723.1. VAD = voice activity detection. CNG = comfort noise generation. This creates 4 possible speech frame sizes:

  24-byte 6.3 Kbits/sec
  20-byte 5.3 Kbits/sec
  4-byte CNG frame
  1-byte silent frame
- v5.1, Oct/Nov 1996, minor bug fix release affecting only the VAD feature. This version is implemented in the CT8020D11AQC

The main coder/decoder in the v5.1, v5.0 and v4.1 revisions are identical. When use of the v5.1 coder with the VAD feature is disabled, the v5.1 and v4.1 encoders produce identical bit-streams. Therefore, inter-working between these versions of G.723.1 is straightforward.

It is possible to convert the compressed data between the various revisions so that, for example, chips of v3.0 can inter-work with v5.1. This requires software to run on the Host. This is simple code that re-packs bits and performs certain table look-up operations on some bit-fields. DSP Group provides ‘C’ reference source code for use with the CT8020. It is possible to freely incorporate this code into user software for use with CT8020 systems. DSP Group recommends incorporation of this code into all software that works with CT8020A11AQC and CT8020A11BQC devices to provide compatibility with the final G.723.1 v5.1 standard. Systems incorporating older versions of the G.723.1 standard should use the conversion software to promote to the final v5.1 G.723.1 version format.

The ITU-T has approved version 5.1 of G.723.1 as the final version. There will be no further changes to this standard.

The changes introduced by the ITU in version 4.1 of G.723.1 necessitated equivalent changes to the TrueSpeech 4.8 and 4.1 KBPS speech coders. Because of this conversion, software must be included in order to enable inter-working between the (DSP Group proprietary) 4.8/4.1 rates in the A11AQC/A11BQC chips and the final CT8020D11AQC silicon.

E.2 G.723.1 Control Bits

Following are the control bit assignments as implemented in the various G.723.1 (pre-release) revisions:

v3.0 (m.s. 2 bits of first 16-bit word) CT8020A11AQC

bit 15	bit 14	
0	0	(reserved for silence, but not implemented)
0	1	6.3 rate
1	0	5.3 rate
1	1	(reserved)

v4.0 (l.s. 2 bits of first 16-bit word) CT8020A11BQC

bit 1	bit 0	
0	0	(reserved for silence, but not implemented)
0	1	5.3 rate
1	0	6.3 rate
1	1	(reserved)

v4.1 and v5.1 (l.s. 2 bits of first 16-bit word) - final formal release CT8020D11AQC , all CT8021, and all CT8022

bit 1	bit 0	
0	0	6.3 rate
0	1	5.3 rate
1	0	4 byte silence frame (v5.1 only)
1	1	1 byte silence (not transmitted) frame (v5.1 only)

F Ordering Information

Use the following table for ordering part numbers:

CT8022A11AQC	128-pin 14x20x2.8mm PQFP package, 0-70°C temperature range
CT8022A11AQC-FWb	As CT8022A11AQC, with downloadable G.729AB CODER
CT8022A11ATC	128-pin 14x20x1.4mm Thin LQFP package, 0-70°C temperature range
CT8022A11ATC-FWb	As CT8022A11ALC, with downloadable G.729AB CODER

Pub: CT8022 Rev: **1** Amendment: **18**
Issue Date: **July, 2000**

All specifications are subject to change without prior notice