600 mA/1.25 MHz HIGH-EFFICIENCY STEP-DOWN CONVERTER

FEATURES

- **Up to 95% Conversion Efficiency**
- **Typical Quiescent Current: 18 µA**
- **Load Current: 600 mA**
- **Operating Input Voltage Range: 2.5 V to 6.0 V**
- **Switching Frequency: 1.25 MHz**
- **Adjustable and Fixed Output Voltage**
- **Power Save Mode Operation at Light load Currents**
- **Active-Low $\overline{\text{MODE}}$ pin on TPS62021**
- **100% Duty Cycle for Lowest Dropout**
- **Internal Softstart**
- **Dynamic Output Voltage Positioning**
- **Thermal Shutdown**
- **Short-Circuit Protection**
- **10 Pin MSOP PowerPad™ Package**
- **10 Pin QFN 3 X 3 mm Package**

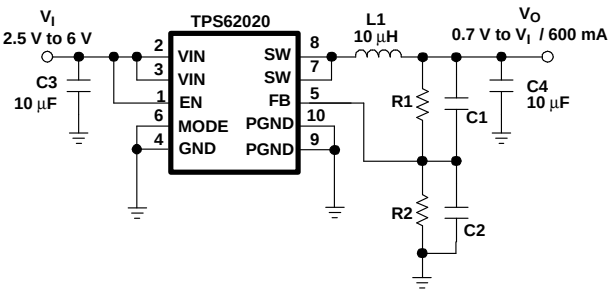
APPLICATIONS

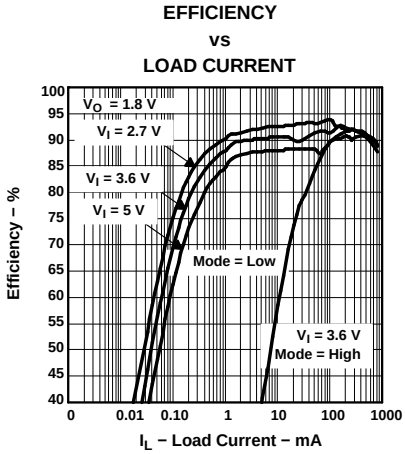
- **PDA, Pocket PC and Smart Phones**
- **USB Powered Modems**
- **CPUs and DSPs**
- **PC Cards and Notebooks**
- **xDSL Applications**
- **Standard 5-V to 3.3-V Conversion**

DESCRIPTION

The TPS6202x is a high efficiency synchronous step-down dc-dc converter optimized for battery powered portable applications. This device is ideal for portable applications powered by a single Li-Ion battery cell or by 3-cell NiMH/NiCd batteries. With an output voltage range from 6.0 V down to 0.7 V, the device supports low voltage DSPs and processors in PDAs, pocket PCs, as well as notebooks and subnotebook computers. The TPS6202x operates at a fixed switching frequency of 1.25 MHz and enters the power save mode operation at light load currents to maintain high efficiency over the entire load current range. For low noise applications, the device can be forced into fixed frequency PWM mode by pulling the MODE pin high. The difference between the TPS6202x and the TPS62021 is the logic level of the MODE pin. The TPS62021 has an active-low $\overline{\text{MODE}}$ pin. The TPS6202x supports up to 600-mA load current.

Typical Application Circuit (600-mA Output Current)





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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	MODE PIN LOGIC LEVEL	OUTPUT VOLTAGE	PACKAGE		PACKAGE MARKING	
			MSOP(1)	QFN(2)	MSOP	QFN
–40°C to 85°C	MODE	Adjustable	TPS62020DGQ	TPS62020DRC	BBK	BBJ
	$\overline{\text{MODE}}$	Adjustable	TPS62021DGQ	TPS62021DRC	ASH	ASJ
	MODE	3.3 V	TPS62026DGQ	TPS62026DRC	BKI	BKJ

(1) The DGQ package is available in tape and reel. Add R suffix (DGQR) to order quantities of 2500 parts per reel.
(2) The DRC package is available in tape and reel. Add R suffix (DRCR) to order quantities of 3000 parts per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	UNITS
Supply voltage VIN(2)	–0.3 V to 7 V
Voltages on EN, MODE, FB, SW(2)	–0.3 V to V_{CC} +0.3 V
Continuous power dissipation	See Dissipation Rating Table
Operating junction temperature range	–40°C to 150°C
Storage temperature range	–65°C to 150°C
Lead temperature (soldering, 10 sec)	260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

PACKAGE DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$(1)	$T_A \le 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
MSOP	60°C/W	1.67 W	917 mW	667 mW
QFN	48.7°C/W	2.05 W	1.13 W	821 mW

(1) The thermal resistance, $R_{\theta JA}$ is based on a soldered PowerPAD using thermal vias.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_I	Supply voltage	2.5		6.0	V
V_O	Output voltage range for adjustable output voltage version	0.7		V_I	V
I_O	Output current			600	mA
L	Inductor(1)	3.3	10		µH
C_I	Input capacitor(1)		10		µF
C_O	Output capacitor(1)		10		µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) Refer to application section for further information

ELECTRICAL CHARACTERISTICS

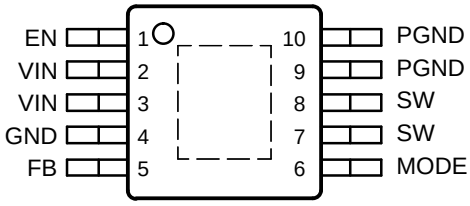
V_I = 3.6 V, V_O = 1.8 V, I_O = 600 mA, EN = VIN, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
V_I	Input voltage range			2.5		6.0	V
$I_{(Q)}$	Operating quiescent current		I_O = 0 mA, device is not switching		18	35	µA
I_{SD}	Shutdown supply current		EN = GND		0.1	1	µA
V_{UVLO}	Under-voltage lockout threshold			1.5		2.3	V
ENABLE AND MODE							
V_{EN}	EN high level input voltage			1.4			V
V_{EN}	EN low level input voltage					0.4	V
I_{EN}	EN input bias current		EN = GND or VIN		0.01	1.0	µA
$V_{(MODE)}$	MODE high level input voltage			1.4			V
$V_{(MODE)}$	MODE low level input voltage					0.4	V
$I_{(MODE)}$	MODE input bias current		MODE = GND or VIN		0.01	1.0	µA
POWER SWITCH							
$r_{DS(ON)}$	P-channel MOSFET on-resistance		$V_I = V_{GS}$ = 3.6 V		115	210	mΩ
	P-channel MOSFET on-resistance		$V_I = V_{GS}$ = 2.5 V		145	270	mΩ
$I_{lkg(P)}$	P-channel leakage current		V_{DS} = 6.0 V			1	µA
$r_{DS(ON)}$	N-channel MOSFET on-resistance		$V_I = V_{GS}$ = 3.6 V		85	200	mΩ
	N-channel MOSFET on-resistance		$V_I = V_{GS}$ = 2.5 V		115	280	mΩ
$I_{lkg(N)}$	N-channel leakage current		V_{DS} = 6.0 V			1	µA
I_L	P-channel current limit		2.5 V < V_I < 6.0 V	0.9	1.1	1.3	A
	Thermal shutdown				150		°C
OSCILLATOR							
f_S	Oscillator frequency		V_{FB}= 0.5 V	1	1.25	1.5	MHz
			V_{FB} = 0 V		625		kHz
OUTPUT							
V_O	Adjustable output voltage range	TPS62020, TPS62021		0.7		V_{IN}	V
V_{ref}	Reference voltage				0.5		V
V_{FB}	Feedback voltage	TPS62020, TPS62021 Adjustable	V_I = 2.5 V to 6.0 V; I_O = 0 mA	0%		3%	V
			V_I = 2.5 V to 6.0 V; 0 mA ≤ I_O ≤ 600 mA	–3%		3%	
V_O	Fixed output voltage	TPS62026 3.3 V	V_I = 3.6 V to 6.0 V; I_O = 0 mA	0%		3%	V
			V_I = 3.6 V to 6.0 V; 0 mA ≤ I_O ≤ 600 mA	–3%		3%	
	Line regulation(1)		$V_I = V_O$ + 0.5 V (min 2.5 V) to 6.0 V, I_O = 10 mA		0		%/V
	Load regulation(1)		I_O = 10 mA to 600 mA		0		%/mA
$I_{lkg(SW)}$	Leakage current into SW pin		$V_I > V_O$, 0 V≤ $V_{SW} \le V_I$		0.1	1	µA
	Reverse leakage current into pin SW		V_I = open; EN = GND; V_{SW} = 6.0 V		0.1	1	µA
f	Short circuit switching frequency		V_{FB} = 0 V		625		kHz

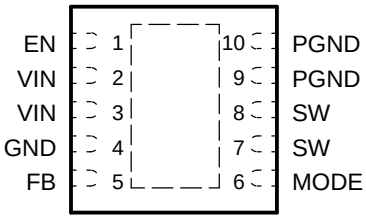
(1) The line and load regulations are digitally controlled to assure an output voltage accuracy of ±3%.

PIN ASSIGNMENTS

DGQ PACKAGE
(TOP VIEW)



DRC PACKAGE
(TOP VIEW)

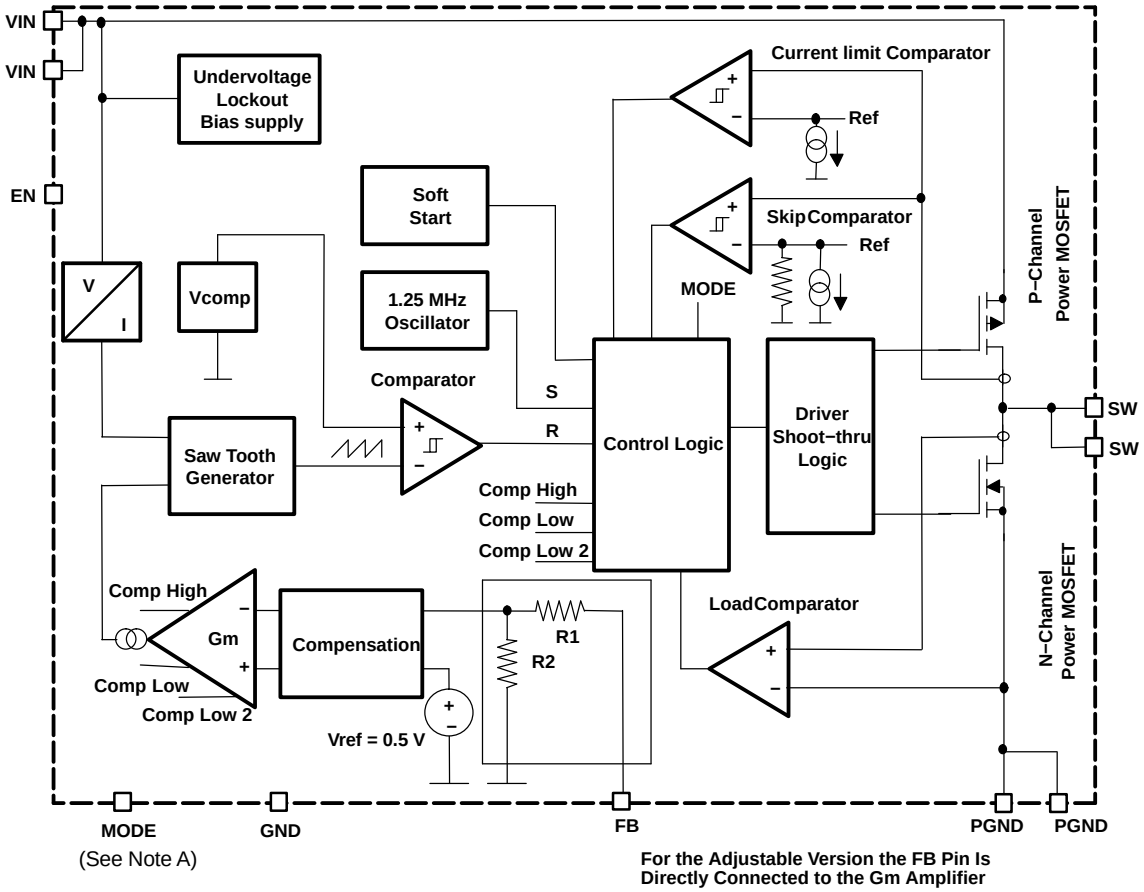


NOTE: The PowerPAD must be connected to GND.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
EN	1	I	Enable. Pulling EN to ground forces the device into shutdown mode. Pulling EN to V_I enables the device. EN should not be left floating and must be terminated.
VIN	2, 3	I	Supply voltage input
GND	4		Analog ground
FB	5	I	Feedback. Connect an external resistor divider to this pin. If a fixed-output-voltage device is ued, connect FB directly to the output.
MODE $\overline{\text{MODE}}$	6	I	The difference between TPS6202x and TPS62021 is the logic level of the MODE pin. The TPS62021 has an active-low $\overline{\text{MODE}}$ pin. The TPS6202x is forced into fixed-frequency PWM mode by pulling the MODE pin high. Pulling the MODE pin low enables the Power Save Mode, operating in PFM mode (Pulse frequency modulation) at light load current, and in fixed frequency PWM at medimum to heavy load currents. In contrast, the TPS62021 is forced into PWM mode by pulling the $\overline{\text{MODE}}$ pin low.
SW	7, 8	I/O	This is the switch pin of the converter and connected to the drain of the internal power MOSFETs
PGND	9, 10		Power ground

FUNCTIONAL BLOCK DIAGRAM



NOTE A: The TPS6202x has an active-high MODE pin. The TPS62021 has an active-low $\overline{\text{MODE}}$ pin.

NOTE B: The resistor network R1 and R2 is only integrated in fixed-output devices.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs Load current	1, 2, 3
η	Efficiency	vs Input voltage	4
I_Q	No load quiescent current	vs Input voltage	5, 6
f_s	Switching frequency	vs Input voltage	7
$r_{DS(on)}$	P-Channel switch $r_{DS(on)}$	vs Input voltage	8
$r_{DS(on)}$	N-Channel rectifier switch $r_{DS(on)}$	vs Input voltage	9
	Load transient response		10
	PWM operation		11
	Power save mode operation		12
	Start-up		13

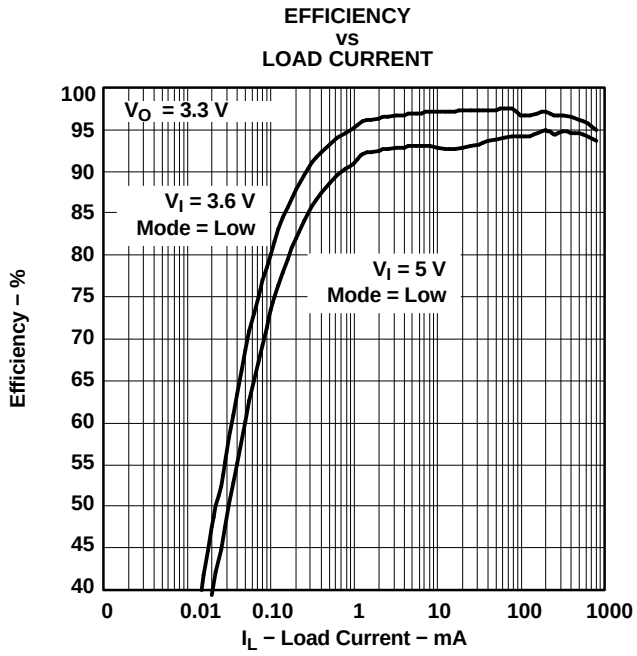


Figure 1.

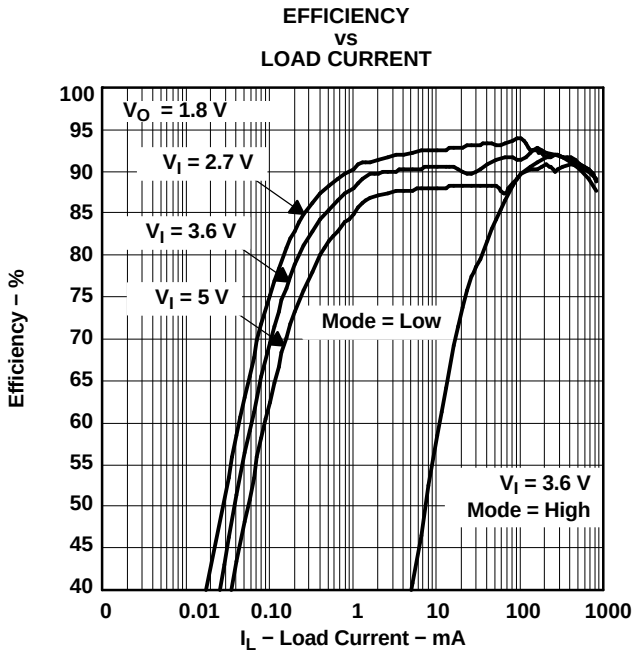


Figure 2.

EFFICIENCY
vs
LOAD CURRENT

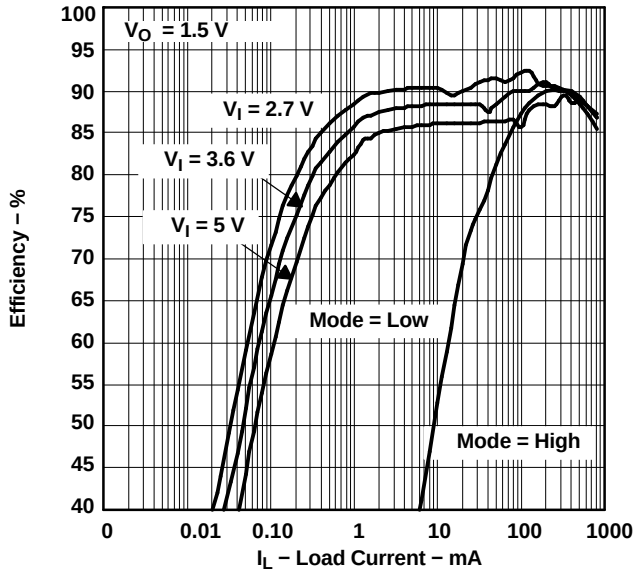


Figure 3.

EFFICIENCY
vs
INPUT VOLTAGE

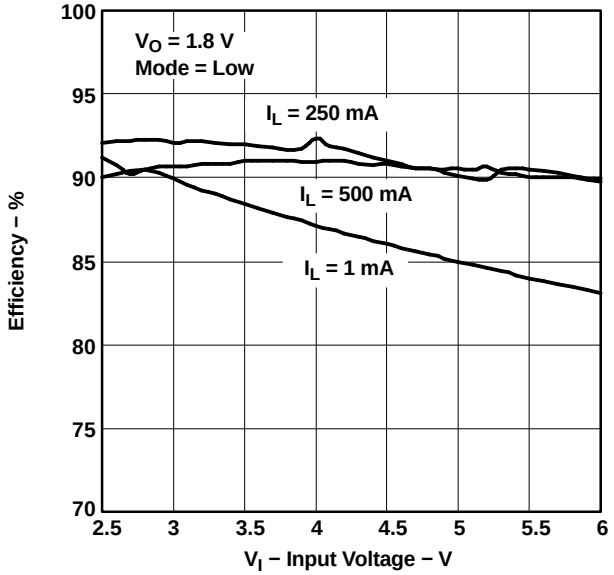


Figure 4.

QUIESCENT CURRENT
vs
INPUT VOLTAGE

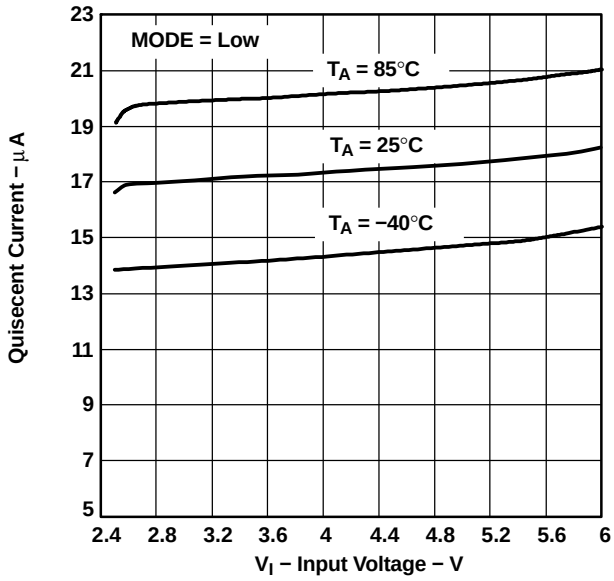


Figure 5.

QUIESCENT CURRENT
vs
INPUT VOLTAGE

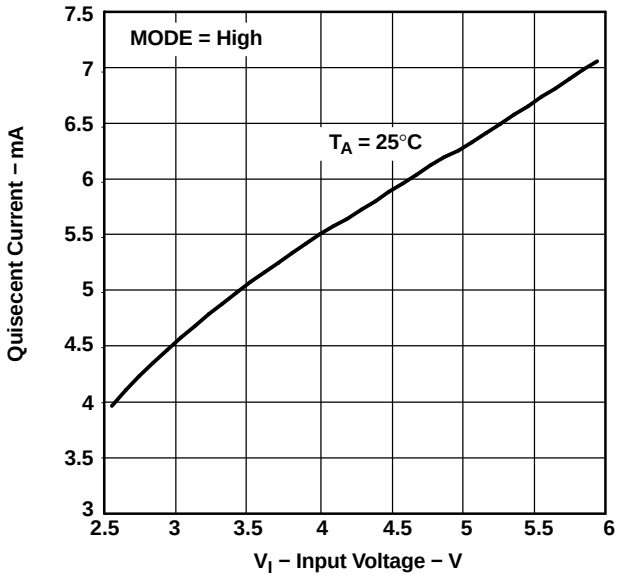


Figure 6.

SWITCHING FREQUENCY vs INPUT VOLTAGE

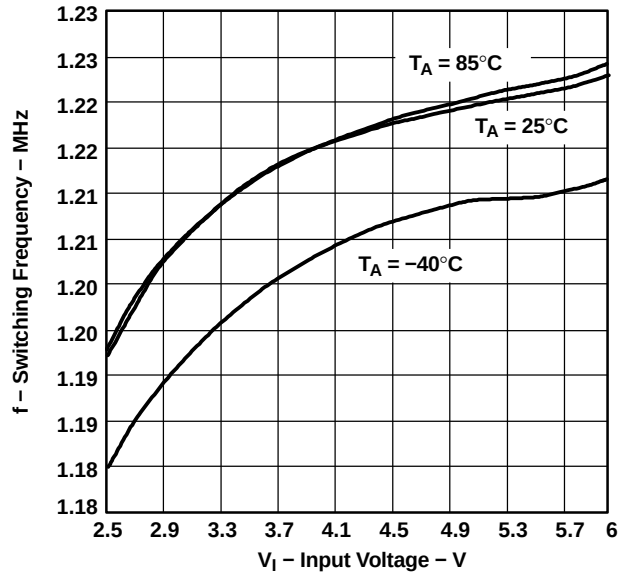


Figure 7.

P-CHANNEL $r_{DS(on)}$ vs INPUT VOLTAGE

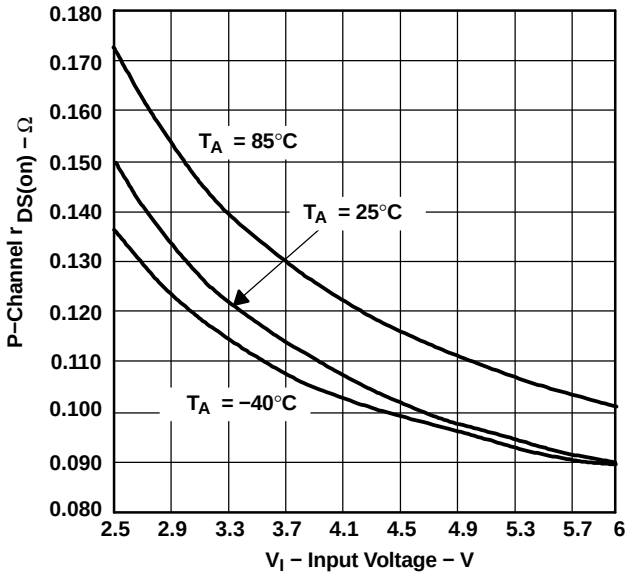


Figure 8.

N-CHANNEL RECTIFIER $r_{DS(on)}$ vs INPUT VOLTAGE

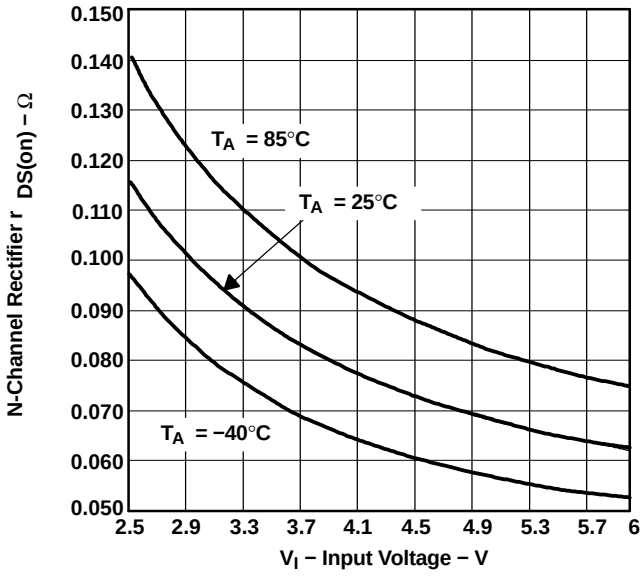


Figure 9.

LOAD TRANSIENT RESPONSE

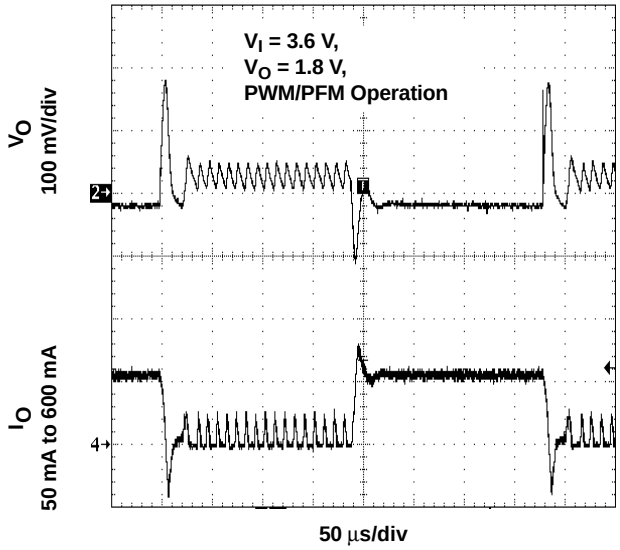


Figure 10.

PWM OPERATION

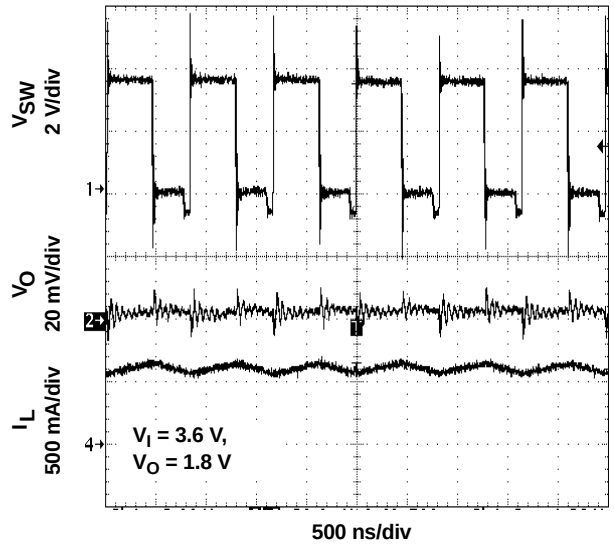


Figure 11.

POWER SAVE MODE OPERATION

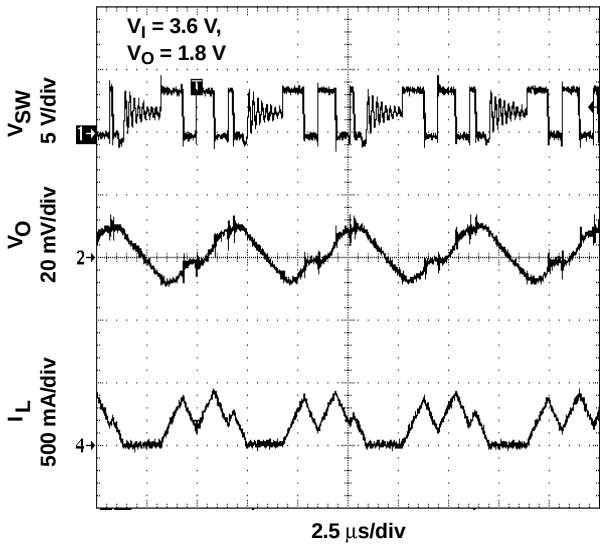


Figure 12.

START-UP

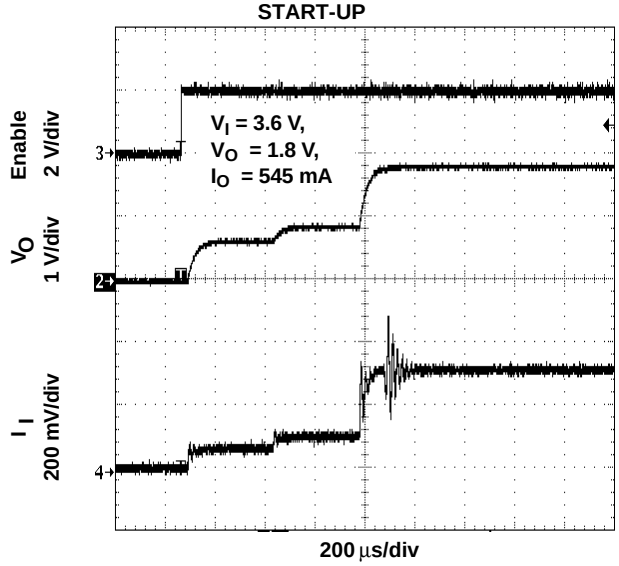


Figure 13.

DETAILED DESCRIPTION

OPERATION

The TPS6202x is a synchronous step-down converter that typically operates at a 1.25-MHz fixed frequency. At moderate to heavy load currents the device operates in pulse-width modulation (PWM), and at light load currents the device enters power-save mode operation using pulse-requency modulation (PFM). When operating in PWM mode, the typical switching frequency is 1.25 MHz with a minimum switching frequency of 1 MHz. This makes the device suitable for xDSL applications, minimizing RF (radio frequency) interference.

During PWM operation the converter uses a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal (S) the P-channel MOSFET switch turns on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch in case the current limit of the P-channel switch is exceeded. After the dead time preventing current shoot through, the N-channel MOSFET rectifier is turned on and the inductor current ramps down. The next cycle is initiated by the clock signal, again turning off the N-channel rectifier and turning on the P-channel switch.

The Gm amplifier as well as the input voltage determines the rise time of the saw tooth generator, and therefore, any change in input voltage or output voltage directly controls the duty cycle of the converter, giving a very good line and load transient regulation.

POWER SAVE MODE OPERATION

As the load current decreases, the converter enters power save mode operation. During power save mode the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current maintaining high efficiency.

The converter monitors the average inductor current and the device enters power save mode when the average inductor current is below the threshold. The transition point between PWM and power save mode is given by the transition current with the following equation:

$$I_{transition} = \frac{V_I}{18.66\ \Omega} \quad (1)$$

During power save mode the output voltage is monitored with the comparator by the threshold's comp low and comp high. As the output voltage falls below the comp low threshold set to typically 0.8% above the nominal output voltage, the P-channel switch turns on. The P-channel switch remains on until the transition current Equation 1 is reached. Then the N-channel switch turns on completing the first cycle. The converter continues to switch with its normal duty cycle determined by the input and output voltage but with half the nominal switching frequency of 625-kHz typ. Thus the output voltage rises and, as soon as the output voltage reaches the comp high threshold of 1.6%, the converter stops switching. Depending on the load current, the converter switches for a longer or shorter period of time in order to deliver the energy to the output. If the load current increases and the output voltage can not be maintained with the transition current Equation 1, the converter enters PWM again. See Figure 11 and Figure 12 under the typical graphs section and Figure 14 for power save mode operation. Among other techniques this advanced power save mode method allows high efficiency over the entire load current range and a small output ripple of typically 1% of the nominal output voltage.

Setting the power save mode thresholds to typically 0.8% and 1.6% above the nominal output voltage at light load current results in a dynamic voltage positioning achieving lower absolute voltage drops during heavy load transient changes. This allows the converter to operate with small output capacitors like 10 µF or 22 µF and still having a low absolute voltage drop during heavy load transient. Refer to Figure 14 as well for detailed operation of the power save mode.

DETAILED DESCRIPTION (continued)

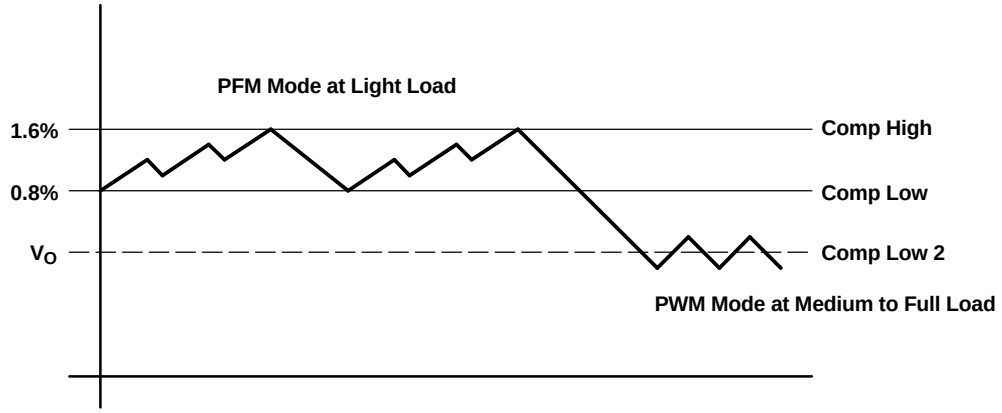


Figure 14. Power Save Mode Thresholds and Dynamic Voltage Positioning

The converter enters the fixed frequency PWM mode as soon as the output voltage falls below the comp low 2 threshold.

DYNAMIC VOLTAGE POSITIONING

As described in the power save mode operation sections before and as detailed in Figure 14 the output voltage is typically 0.8% (i.e., 1% on average) above the nominal output voltage at light load currents, as the device is in power save mode. This gives additional headroom for the voltage drop during a load transient from light load to full load. In the other direction during a load transient from full load to light load the voltage overshoot is also minimized by turning on the N-Channel rectifier switch to pull the output voltage actively down.

MODE (AUTOMATIC PWM/PFM OPERATION AND FORCED PWM OPERATION)

Connecting the MODE pin of the TPS6202x to GND enables the automatic PWM and power save mode operation. The converter operates in fixed frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, maintaining high efficiency over a wide load current range.

Pulling the TPS6202x MODE pin high forces the converter to operate constantly in the PWM mode even at light load currents. The advantage is the converter operates with a fixed switching frequency that allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads (see Figure 1 to Figure 3). For additional flexibility it is possible to switch from power save mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the TPS6202x to the specific system requirements.

The difference between the TPS6202x and the TPS62021 is the logic level of the MODE pin. The TPS62021 has an active-low $\overline{\text{MODE}}$ pin. Pulling the TPS62021 $\overline{\text{MODE}}$ pin high enables the automatic PWM and Power Save Mode.

100% DUTY CYCLE LOW DROPOUT OPERATION

The TPS6202x offers a low input to output voltage difference while still maintaining regulation with the use of the 100% duty cycle mode. In this mode, the P-Channel switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. i.e. The minimum input voltage to maintain regulation depends on the load current and output voltage and can be calculated as:

$$V_I\,\text{min} = V_O\,\text{max} + I_O\,\text{max} \times \left(r_{DS(on)}\,\text{max} + R_L\right) \quad (2)$$

with:

- $I_{O(max)}$ = maximum output current plus inductor ripple current
- $r_{DS(on)}$max = maximum P-channel switch $t_{DS(on)}$.

DETAILED DESCRIPTION (continued)

- R_L = DC resistance of the inductor
- $V_O$max = nominal output voltage plus maximum output voltage tolerance

SOFTSTART

The TPS6202x series has an internal softstart circuit that limits the inrush current during start-up. This prevents possible voltage drops of the input voltage in case a battery or a high impedance power source is connected to the input of the TPS6202x.

The softstart is implemented with a digital circuit increasing the switch current in steps of typically $I_{LIM}/8$, $I_{LIM}/4$, $I_{LIM}/2$ and then the typical switch current limit of 1.1 A as specified in the electrical parameter table. The start-up time mainly depends on the output capacitor and load current, see Figure 13.

SHORT-CIRCUIT PROTECTION

As soon as the output voltage falls below 50% of the nominal output voltage, the converter switching frequency as well as the current limit is reduced to 50% of the nominal value. Since the short-circuit protection is enabled during start up the device does not deliver more than half of its nominal current limit until the output voltage exceeds 50% of the nominal output voltage. This needs to be considered in case a load acting as a current sink is connected to the output of the converter.

THERMAL SHUTDOWN

As soon as the junction temperature of typically 150°C is exceeded the device goes into thermal shutdown. In this mode, the P-Channel switch and N-Channel rectifier are turned off. The device continues its operation when the junction temperature falls below typically 150°C again.

ENABLE

Pulling the EN low forces the part into shutdown mode, with a shutdown current of typically 0.1 µA. In this mode, the P-Channel switch and N-Channel rectifier are turned off and the whole device is in shut down. If an output voltage is present during shut down, which could be an external voltage source or super cap, the reverse leakage current is specified under electrical parameter table. For proper operation the enable (EN) pin must be terminated and should not be left floating.

Pulling EN high starts up the device with the softstart as described under the section Softstart.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit prevents device misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET with undefined conditions.

APPLICATION INFORMATION

ADJUSTABLE OUTPUT VOLTAGE VERSION

When the adjustable output voltage version TPS6202x is used, the output voltage is set by the external resistor divider. See Figure 15.

The output voltage is calculated as:

$$V_O = 0.5\ V \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

with R1 + R2 ≤ 1 MΩ and internal reference voltage V_{ref} typical = 0.5 V

R1 + R2 should not be greater than 1 MΩ because of stability reasons. To keep the operating quiescent current to a minimum, the feedback resistor divider should have high impedance with R1+R2≤1 MΩ. Due to this and the low reference voltage of V_{ref} = 0.5 V, the noise on the feedback pin (FB) needs to be minimized. Using a capacitive divider C1 and C2 across the feedback resistors minimizes the noise at the feedback, without degrading the line or load transient performance.

C1 and C2 should be selected as:

$$C1 = \frac{1}{2 \times \pi \times 10\ kHz \times R1} \quad (4)$$

with:

- R1 = upper resistor of voltage divider
- C1 = upper capacitor of voltage divider

For C1 a value should be chosen that comes closest to the calculated result.

$$C2 = \frac{R1}{R2} \times C1 \quad (5)$$

with:

- R2 = lower resistor of voltage divider
- C2 = lower capacitor of voltage divider

For C2, the selected capacitor value should always be selected larger than the calculated result. For example, in Figure 15 for C2 100 pF are selected for a calculated result of C2 = 88.42 pF.

If quiescent current is not a key design parameter C1 and C2 can be omitted, and a low impedance feedback divider has to be used with R1 + R2 < 100 kΩ. This reduces the noise available on the feedback pin (FB) as well but increases the overall quiescent current during operation. The higher the programmed output voltage the lower the feedback impedance has to be for best operation when not using C1 and C2.

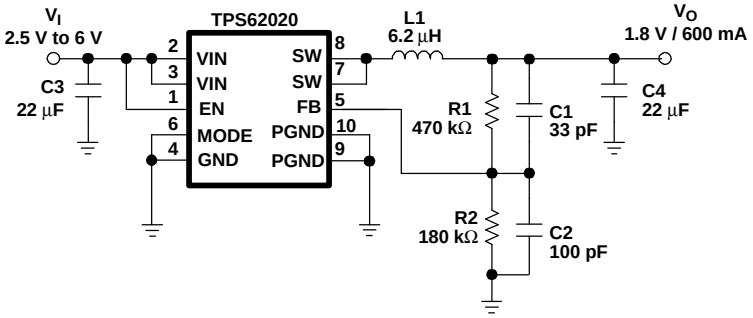


Figure 15. Adjustable Output Voltage Version

Inductor Selection

The TPS6202x uses typically a 10-µH output inductor. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. When changing inductor values, the product of the inductor value times output-capacitor value (L×C) should stay constant. For example, when reducing the

APPLICATION INFORMATION (continued)

inductor value, increase the output capacitor accordingly. See the application circuits in Figure 17, Figure 18, and Figure 19. The selected inductor has to be rated for its dc resistance and saturation current. The dc resistance of the inductance directly influences the efficiency of the converter. Therefore an inductor with the lowest dc resistance should be selected for highest efficiency. Formula Equation 7 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with formula Equation 7. This is needed because during heavy load transient the inductor current rises above the value calculated under Equation 7.

$$\Delta I_L = V_O \times \frac{1-\frac{V_O}{V_I}}{L \times f} \quad (6)$$

$$I_L\,max = I_O\,max + \frac{\Delta I_L}{2} \quad (7)$$

with:

- 7 = Switching frequency (1.25 MHz typical)
- L = Inductor value
- ΔI_L= Peak-to-peak inductor ripple current
- $I_L$max = Maximum inductor current

The highest inductor current occurs at maximum V_I.

Open core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor. A more conservative approach is to select the inductor current rating for the maximum switch current of 1.3 A for the TPS6202x. Keep in mind that core material differs from inductor to inductor, and this impacts efficiency, especially at high switching frequencies. Refer to Table 1 and the typical applications and inductors selection.

Table 1. Inductor Selection

INDUCTOR VALUE	DIMENSIONS	COMPONENT SUPPLIER
10 µH	6,6 mm × 4,75 mm × 2,92 mm	Coilcraft DO1608C-103
10 µH	5,0 mm × 5,0 mm × 3,0 mm	Sumida CDRH4D28-100
3.3 µH	5,0 mm × 5,0 mm × 2,4 mm	Sumida CDRH4D22 3R3
6.8 µH	5,8 mm × 7,4 mm × 1,5 mm	Sumida CMD5D13 6R8

Output Capacitor Selection

The advanced, fast-response voltage-mode control scheme of the TPS6202x allows the use of small ceramic capacitors with a typical value of 10 µF and 22 µF without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. Refer to Table 2 for component selection. If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. Just for completeness the RMS ripple current is calculated as:

$$I_{RMSCout} = V_O \times \frac{1-\frac{V_O}{V_I}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (8)$$

At nominal load current the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_O = V_O \times \frac{1-\frac{V_O}{V_I}}{L \times f} \times \left(\frac{1}{8 \times C_O \times f} + ESR \right) \quad (9)$$

Where the highest output voltage ripple occurs at the highest input voltage, V_I.

At light load currents, the device operates in power save mode and the output voltage ripple is independent of the output capacitor value. The output voltage ripple is set by the internal comparator thresholds. The typical output voltage ripple is 1% of the nominal output voltage.

Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. The input capacitor should have a minimum value of 10 µF for the TPS6202x. The input capacitor can be increased without any limit for better input voltage filtering.

Table 2. Input and Output Capacitor Selection

CAPACITOR VALUE	CASE SIZE	COMPONENT SUPPLIER	COMMENTS
10 µF	0805	Taiyo Yuden JMK212BJ106MG TDK C12012X5ROJ106K	Ceramic Ceramic
10 µF	1206	Taiyo Yuden JMK316BJ106KL TDK C3216X5ROJ106M	Ceramic
22 µF	1206	Taiyo Yuden JMK316BJ226ML	Ceramic
22 µF	1210	Taiyo Yuden JMK325BJ226MM	Ceramic

Layout Considerations

For all switching power supplies, the layout is an important step in the design especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current paths as indicated in bold in Figure 16. These traces should be routed first. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. The feedback resistor network should be routed away from the inductor and switch node to minimize noise and magnetic interference. To further minimize noise from coupling into the feedback network and feedback pin, the ground plane or ground traces should be used for shielding. A common ground plane or a star ground as shown below should be used. This becomes very important especially at high switching frequencies of 1.25 MHz.

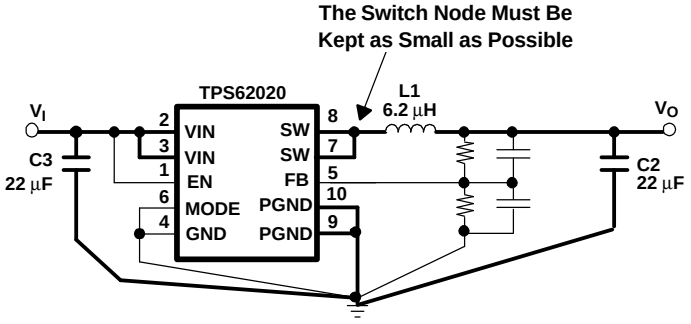


Figure 16. Layout Diagram

THERMAL INFORMATION

One of the most influential components on the thermal performance of a package is board design. In order to take full advantage of the heat dissipating abilities of the PowerPAD™ packages, a board should be used that acts similar to a heat sink and allows for the use of the exposed (and solderable), deep downset pad. For further information please refer to Texas Instruments application note (SLMA002) *PowerPAD Thermally Enhanced Package*.

The PowerPAD™ of the 10-pin MSOP package has an area of 1,52 mm × 1,79 mm (±0,05 mm) and must be soldered to the PCB to lower the thermal resistance. Thermal vias to the next layer further reduce the thermal resistance.

TYPICAL APPLICATIONS

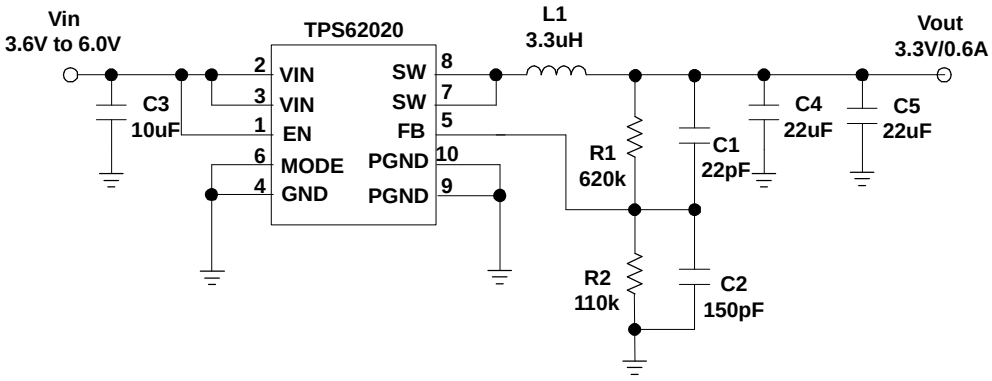


Figure 17. Li-Ion to 3.3 V With Improved Load Transient Response

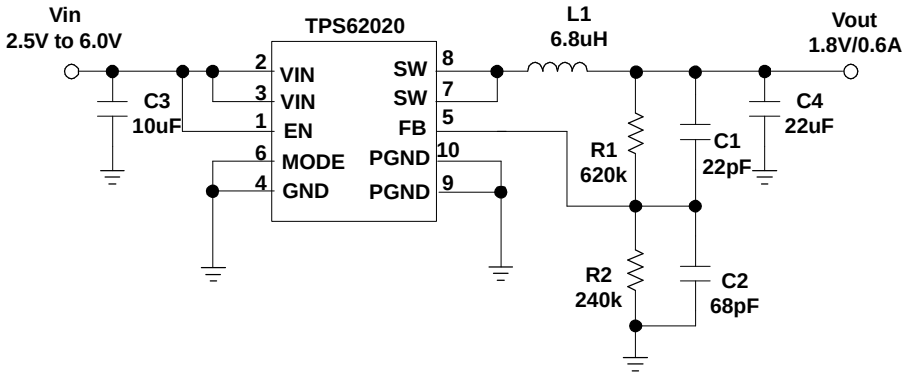


Figure 18. 1.8 V Output Using 6.8 µH Inductor

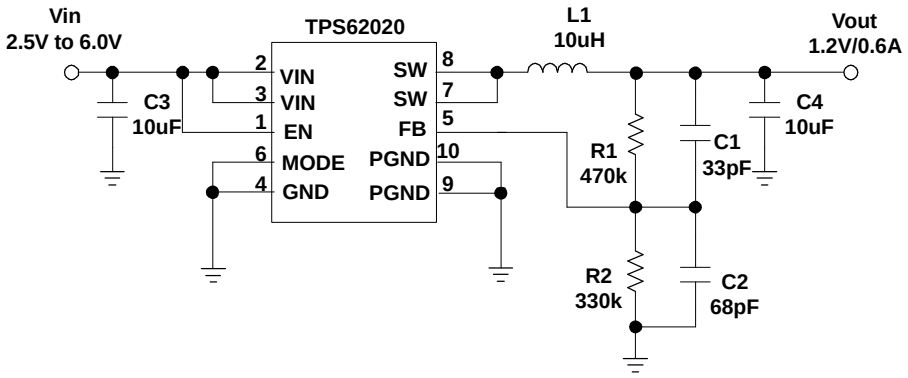


Figure 19. 1.2 V Output Using 10 µH Inductor

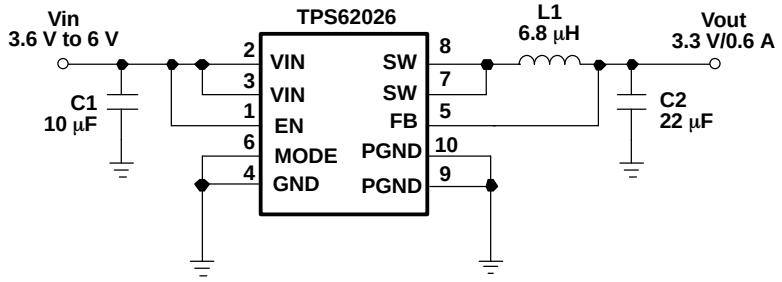


Figure 20. TPS62026 Fixed 3.3 V Output Using 6.8 µH inductor

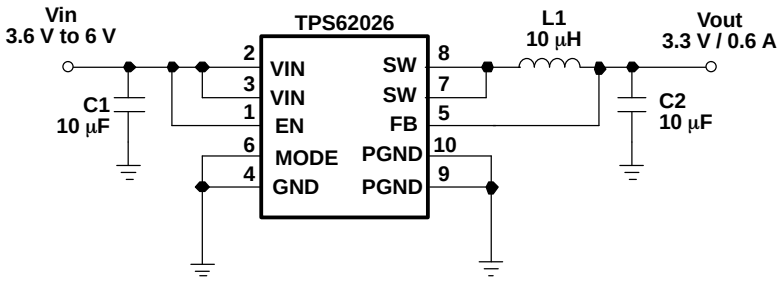


Figure 21. TPS62026 Fixed 3.3 V Output Using 10 µH inductor

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62020DGQ	ACTIVE	MSOP-PowerPAD	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BBK	Samples
TPS62020DGQG4	ACTIVE	MSOP-PowerPAD	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BBK	Samples
TPS62020DGQR	ACTIVE	MSOP-PowerPAD	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BBK	Samples
TPS62020DGQRG4	ACTIVE	MSOP-PowerPAD	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BBK	Samples
TPS62020DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BBJ	Samples
TPS62021DGQ	PREVIEW	MSOP-PowerPAD	DGQ	10		TBD	Call TI	Call TI	-40 to 85		
TPS62021DGQR	OBSOLETE	MSOP-PowerPAD	DGQ	10		TBD	Call TI	Call TI	-40 to 85	ASH	
TPS62021DGQRG4	OBSOLETE	MSOP-PowerPAD	DGQ	10		TBD	Call TI	Call TI	-40 to 85		
TPS62021DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ASJ	Samples
TPS62021DRCRG4	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ASJ	Samples
TPS62026DGQ	ACTIVE	MSOP-PowerPAD	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BKI	Samples
TPS62026DGQG4	ACTIVE	MSOP-PowerPAD	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BKI	Samples
TPS62026DGQR	ACTIVE	MSOP-PowerPAD	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BKI	Samples
TPS62026DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BKJ	Samples
TPS62026DRCRG4	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BKJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

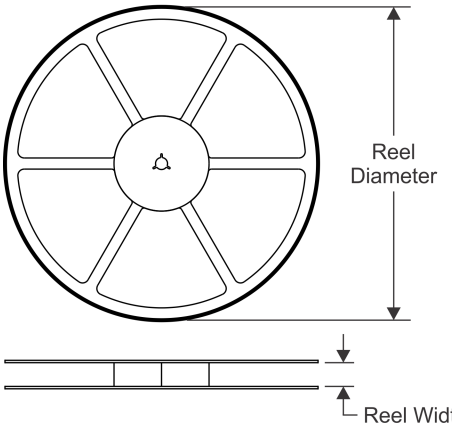
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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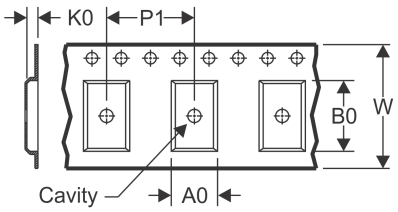
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

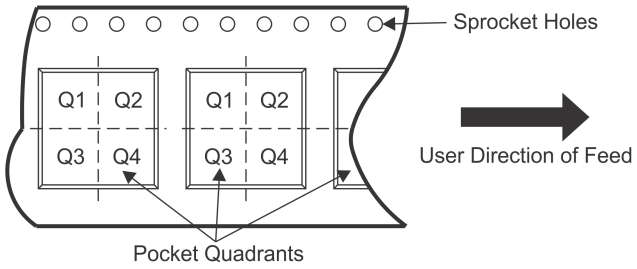


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

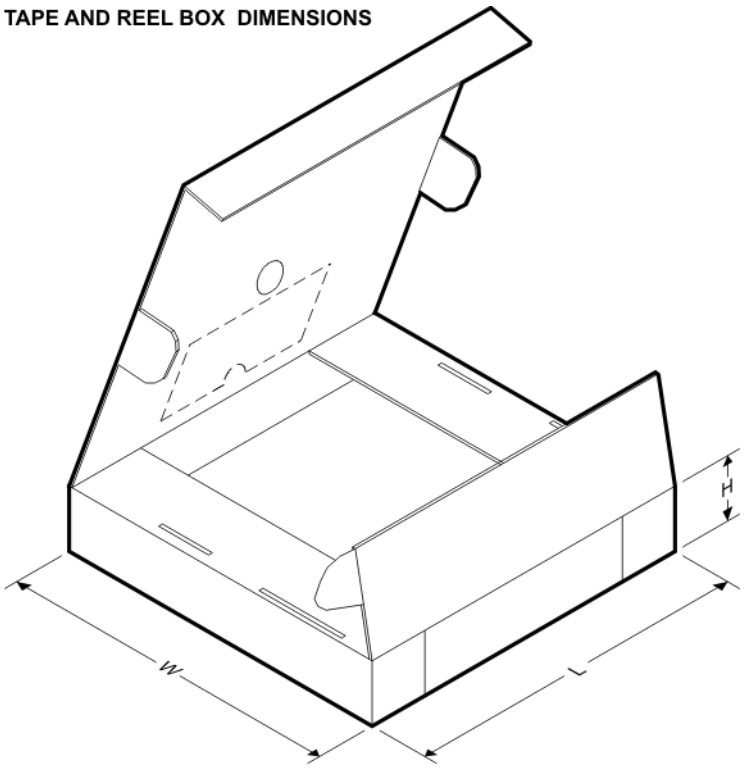
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62020DGQR	MSOP-Power PAD	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS62020DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62021DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS62021DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62026DGQR	MSOP-Power PAD	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS62026DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

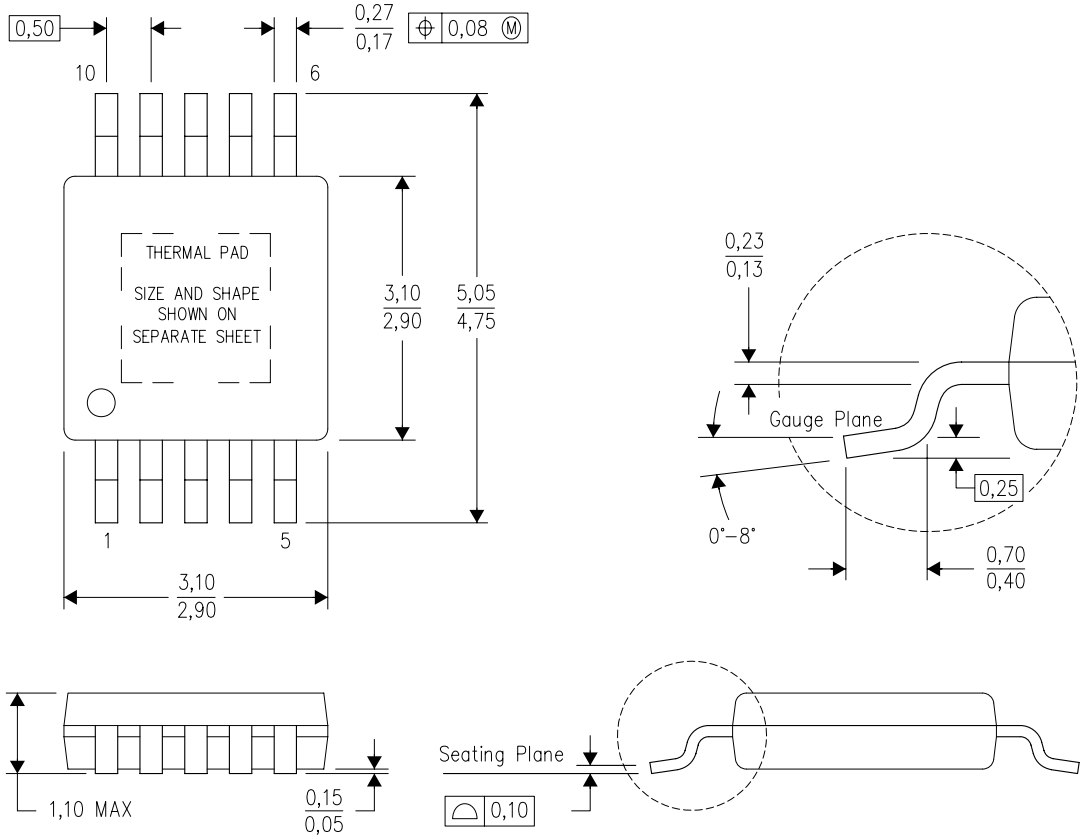
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62020DGQR	MSOP-PowerPAD	DGQ	10	2500	364.0	364.0	27.0
TPS62020DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS62021DRCR	VSON	DRC	10	3000	370.0	355.0	55.0
TPS62021DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS62026DGQR	MSOP-PowerPAD	DGQ	10	2500	364.0	364.0	27.0
TPS62026DRCR	VSON	DRC	10	3000	367.0	367.0	35.0

DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE



4073273/F 11/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation BA–T.

PowerPAD is a trademark of Texas Instruments.

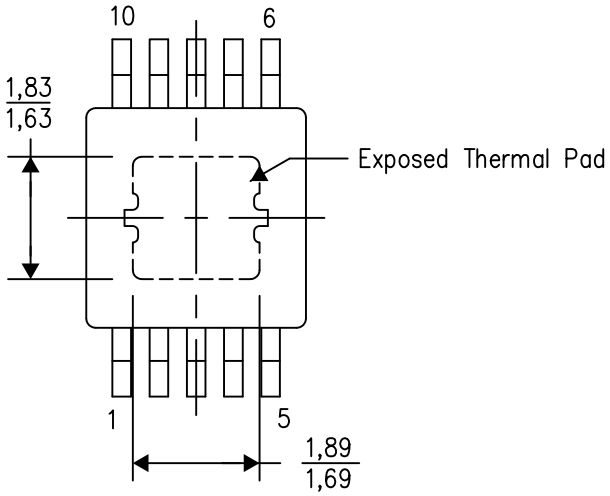
DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

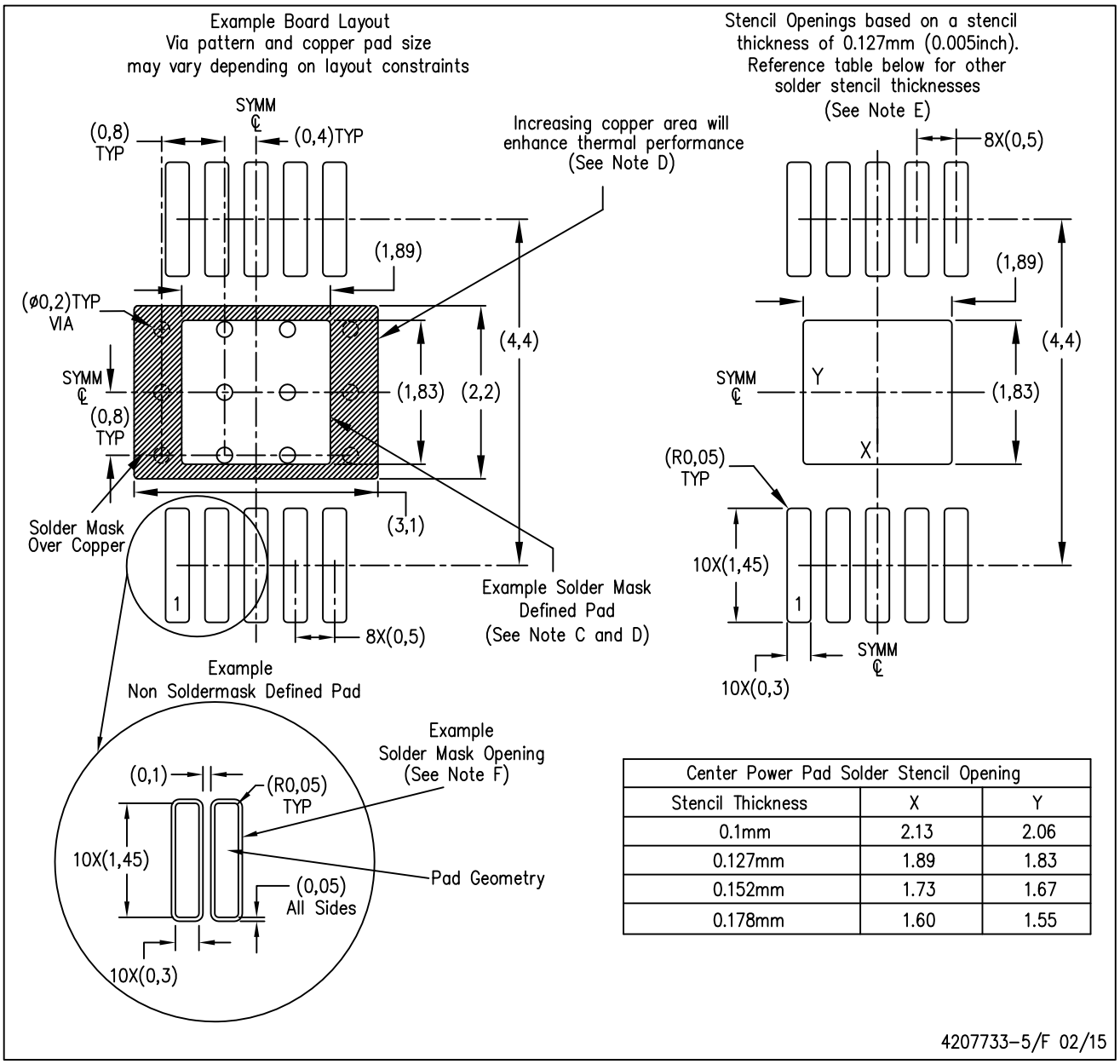
Exposed Thermal Pad Dimensions

4206324–7/H 12/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE

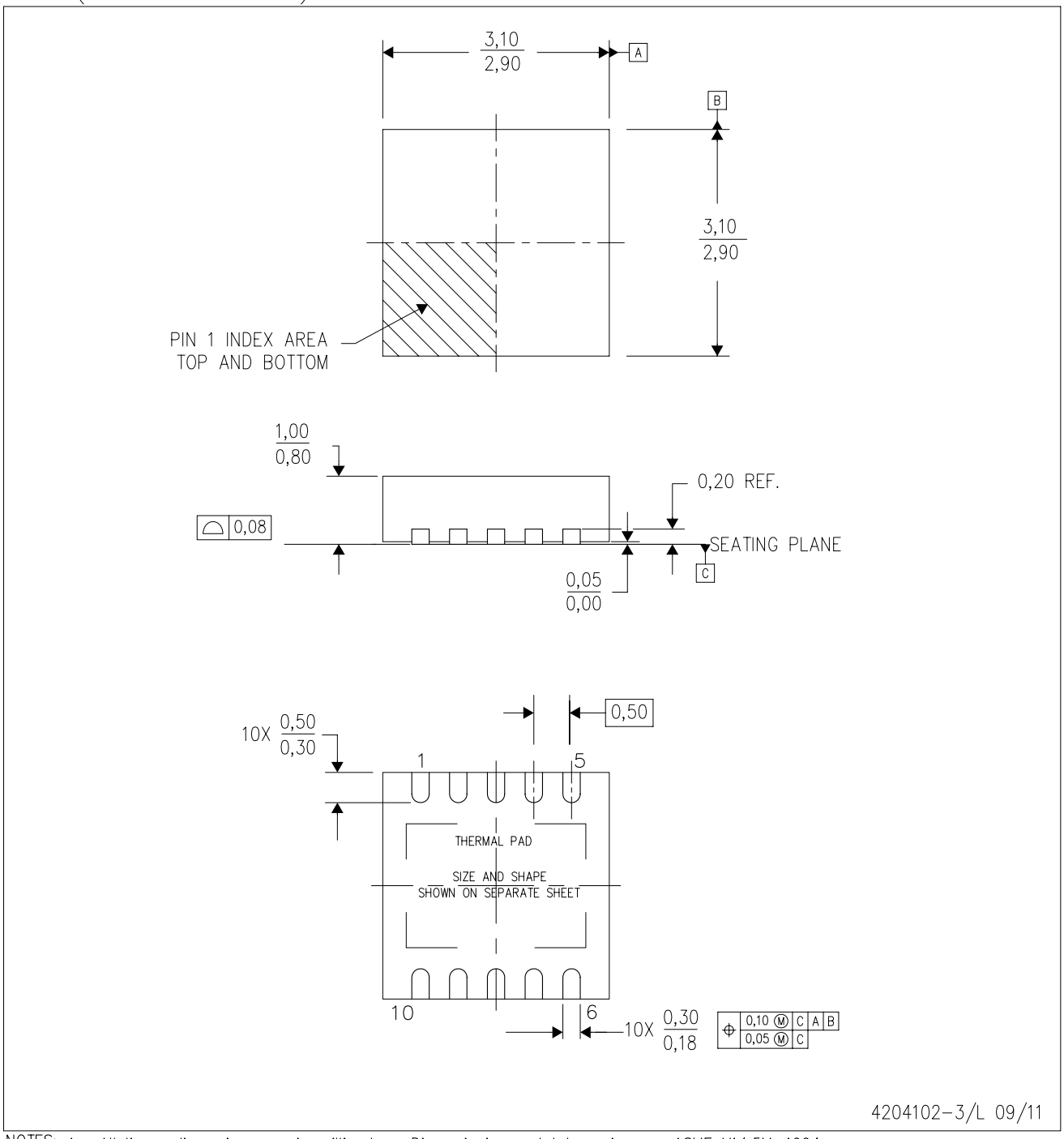


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.13	2.06
0.127mm	1.89	1.83
0.152mm	1.73	1.67
0.178mm	1.60	1.55

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

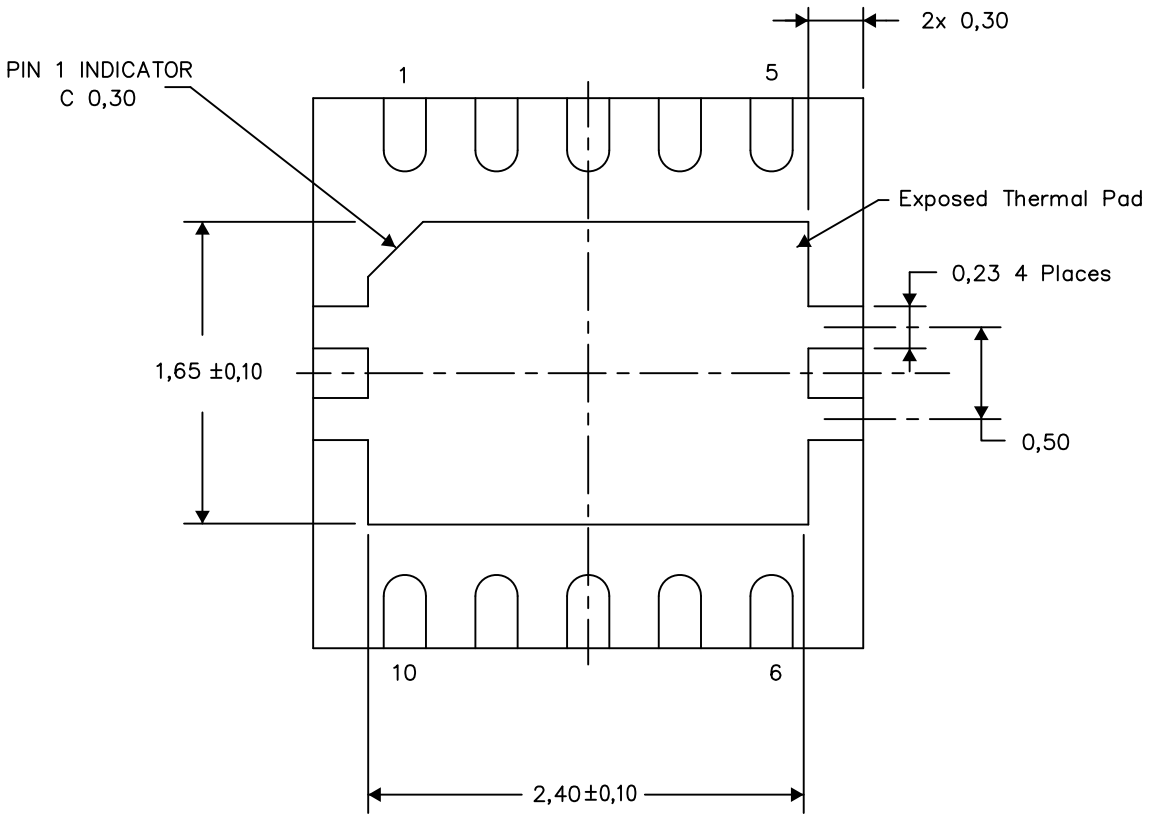
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



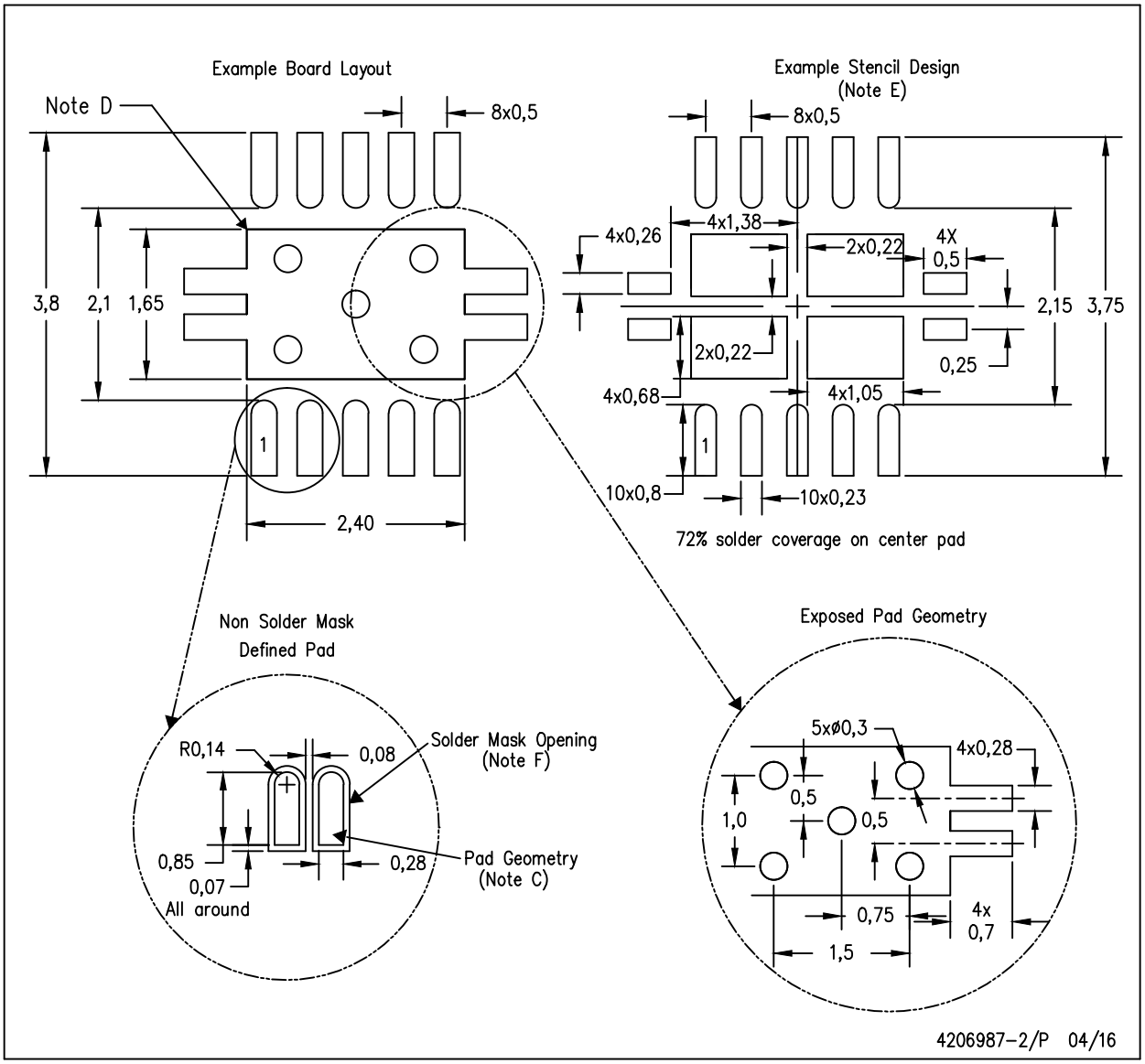
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/Y 08/15

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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