Integrated Device Technology, Inc.

16 x 16 PARALLEL CMOS MULTIPLIERS

IDT7216L
IDT7217L

FEATURES:

- 16 x 16 parallel multiplier with double precision product
- 16ns clocked multiply time
- Low power consumption: 120mA
- Produced with advanced submicron CMOS high performance technology
- IDT7216L is pin- and function compatible with TRW MPY016H/K and AMD Am29516
- IDT7217L requires a single clock with register enables making it pin- and function compatible with AMD Am29517
- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round control for rounding the MSP
- Input and output directly TTL-compatible
- Three-state output
- Available in Top Braze, DIP, PLCC, Flatpack and Pin Grid Array
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-86873 is listed on this function for IDT7216 and Standard Military Drawing #5962-87686 is listed for this function for IDT7217.
- Speeds available: Commercial: L16/20/25/35/45/55/65
  Military: L20/25/30/40/55/65/75

DESCRIPTION:

The IDT7216/IDT7217 are high-speed, low-power 16 x 16-bit multipliers ideal for fast, real time digital signal processing applications. Utilization of a modified Booths algorithm and IDT's high-performance, submicron CMOS technology, has achieved speeds comparable to bipolar (20ns max.), at 1/10 the power consumption.

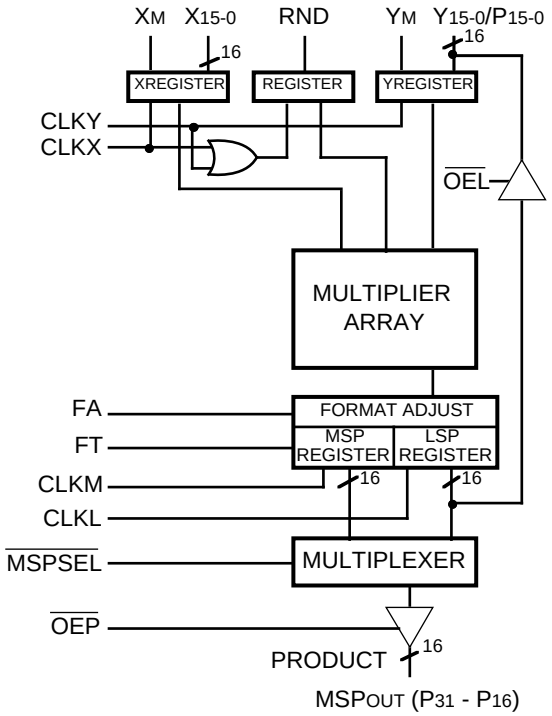
The IDT7216/IDT7217 are ideal for applications requiring high-speed multiplication such as fast Fourier transform analysis, digital filtering, graphic display systems, speech synthesis and recognition and in any system requirement where multiplication speeds of a mini/microcomputer are inadequate.

All input registers, as well as LSP and MSP output registers, use the same positive edge-triggered D-type flip-flop. In the IDT7216, there are independent clocks (CLKX, CLKY, CLKM, CLKL) associated with each of these registers. The IDT7217 has only a single clock input (CLK) and three register enables. $\overline{ENX}$ and $\overline{ENY}$ control the two input registers, while $\overline{ENP}$ controls the entire product.

The IDT7216/IDT7217 offer additional flexibility with the FA control and $\overline{MSPSEL}$ functions. The FA control formats the output for two's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP. The

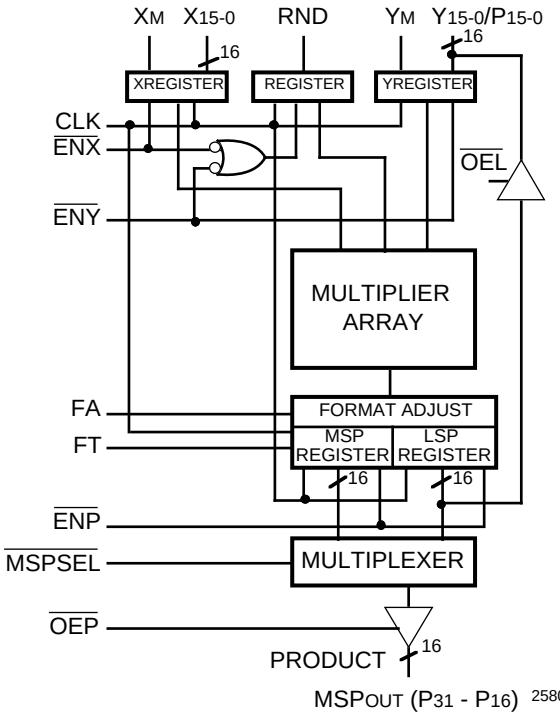
FUNCTIONAL BLOCK DIAGRAMS

IDT7216



2580 drw 01

IDT7217



2580 drw 02

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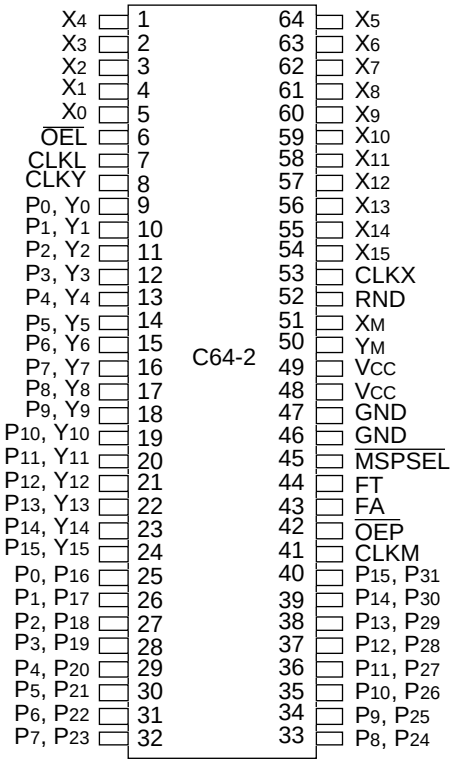
DESCRIPTION (Cont'd.)

$\overline{\text{MSPSEL}}$ low selects the MSP to be available at the product output port, while a high selects the LSP to be available. Keeping this pin low will ensure compatibility with the TRW MPY016H.

The IDT7216/IDT7217 multipliers are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS

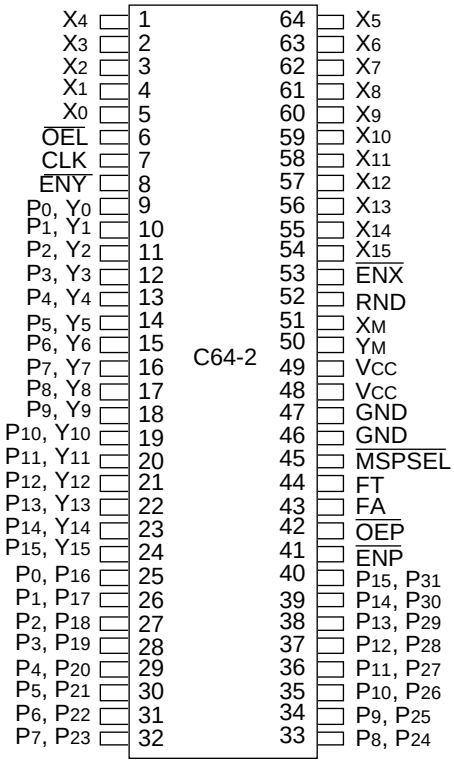
IDT7216



2580 drw 03

64-PIN DIP
TOP VIEW

IDT7217

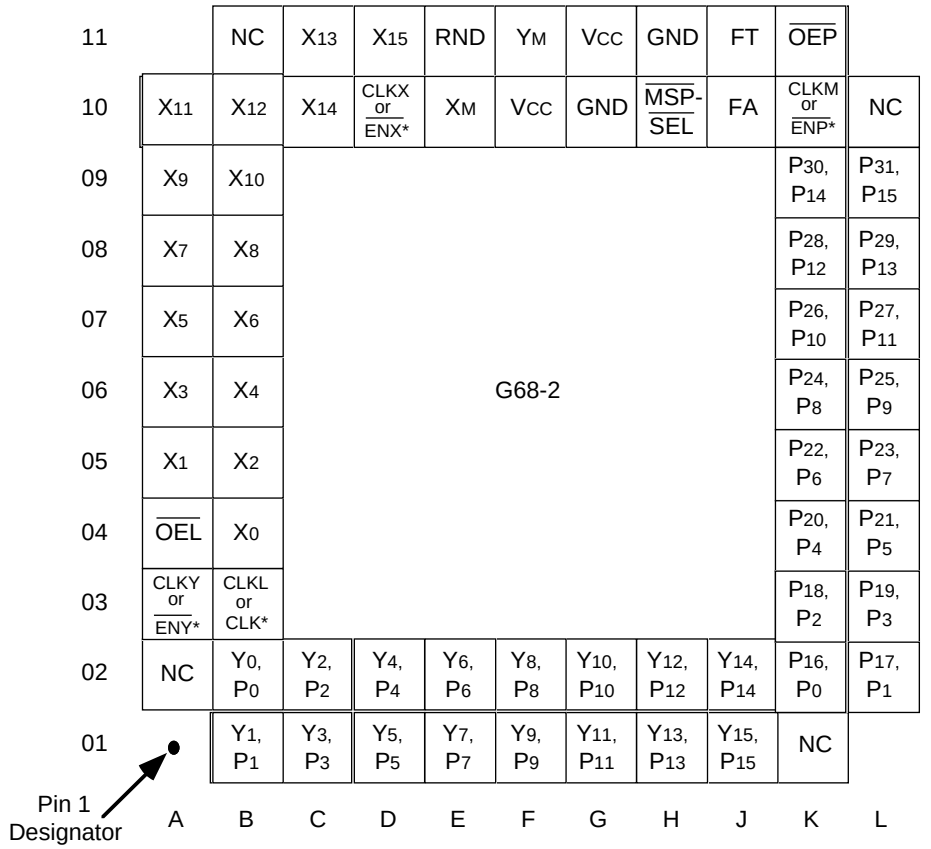


2580 drw 04

64-PIN DIP
TOP VIEW

PIN CONFIGURATIONS (Cont'd.)

IDT7216/IDT7217



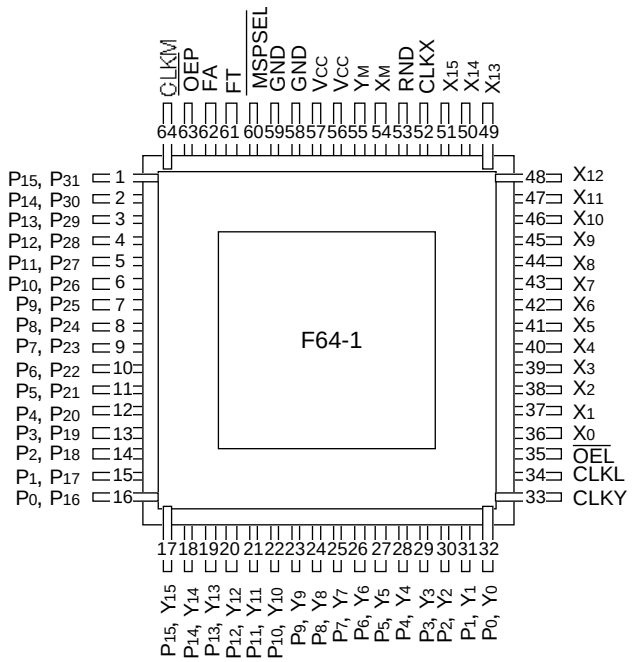
*Pin designation for IDT7217

2580 drw 05

PGA
TOP VIEW

PIN CONFIGURATIONS (Cont'd.)

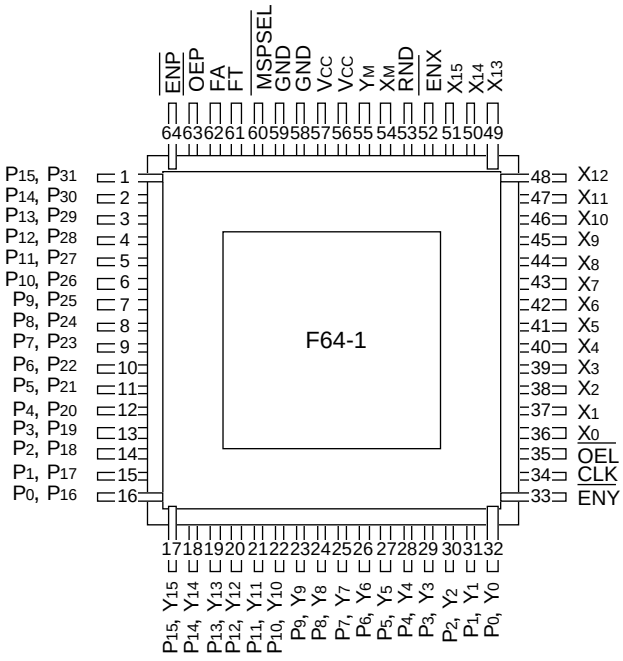
IDT7216



2580 drw 06

64-LEAD FLATPACK
TOP VIEW

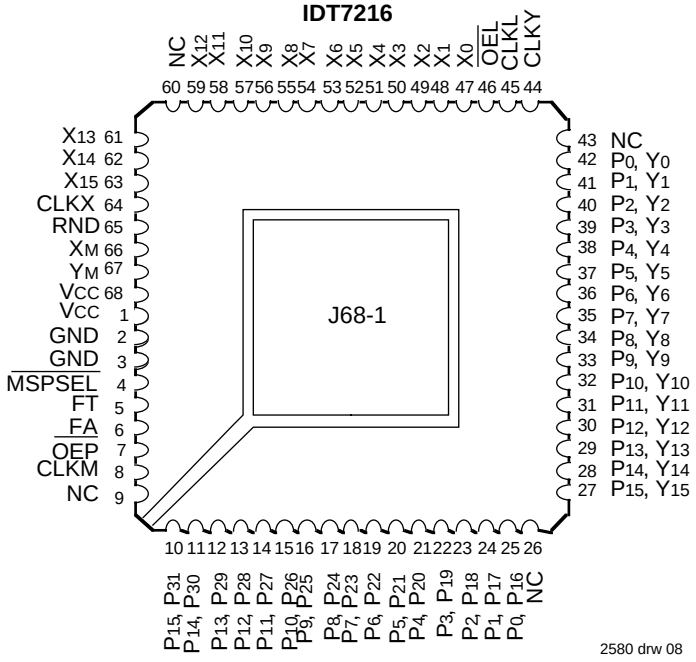
IDT7217



2580 drw 07

64-LEAD FLATPACK
TOP VIEW

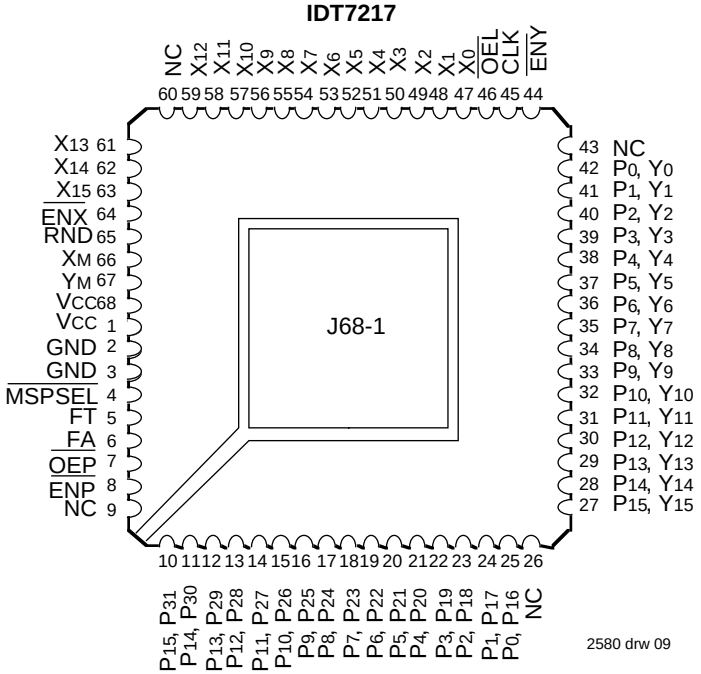
IDT7216



2580 drw 08

PLCC
TOP VIEW

IDT7217



2580 drw 09

PLCC
TOP VIEW

PIN DESCRIPTIONS

Pin Name	I/O	Description
X_0 - X_{15}	I	Data Inputs
Y_0 - Y_{15}/ P_0 - P_{15}	I/O	Y_0 - Y_{15} are data inputs P_0 - P_{15} are LSP register output, enabled when $\overline{OEL}$ = 0
P_{16} - P_{31}	O	Data Output (LSP or MSP)
$\overline{OEL}$	I	Output enable control for LSP (least significant product). When low enables P_0 - P_{15}. When high P_0 - P_{15} tristated.
$\overline{OEP}$	I	Output enable control for MSP (most significant product). When low enables P_{16} - P_{31}. When high P_{16} - P_{31} tristated.
X_M, Y_M	I	Mode control for each data word. Low designates unsigned data input and high designates two's complement.
RND	I	"Round" control for rounding of MSP. When high, 1 is added to the most significant bit of LSP. This signal is affected by the state of FA pin. When FA = 1 and RND = 1, 1 is added to the 2^{-15} bit (P_{15}). When RND = 1 and FA = 0, 1 is added to the 2^{-16} bit (P_{14}). The RND input is registered. It is clocked on the rising edge of the logical OR of CLKX and CLKY in the 7216 and on the rising edge of CLK in the 7217. Rounding always occurs in the positive direction which may introduce a systematic bias.
$\overline{MSPSEL}$	I	When low, MSP is output on P_{16} - P_{31} lines. When high, LSP is output on P_{16} - P_{31}.
FA	I	Format adjust control. When high, a full 32 bit product is selected. When low, a left shifted 31 bit product is selected with the sign bit replicated in the LSP. FA is normally high, except for certain fractional two's complement applications (see multiplier input / output formats).
FT	I	Flow through control. When high, both MSP and LSP registers are by-passed.
CLK	I	7217 X, Y, RND, LSP and MSP register clock input.
CLKX	I	7216 X register clock input. Also clocks RND register.
CLKY	I	7216 Y register clock input. Also clocks RND register.
CLKL	I	7216 LSP register clock input.
CLKM	I	7216 MSP register clock input.
$\overline{ENX}$	I	7217 X register clock enable. Also enables RND register clock.
$\overline{ENY}$	I	7217 Y register clock enable. Also enables RND register clock.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to GND	V_{CC} + 0.5	V_{CC} + 0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2580 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2580 tbl 04

1. This parameter is measured at characterization and not tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	Test Conditions[1]	Commercial			Military			Unit
			Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.	
V_{IH}	Input High Voltage	Guaranteed Logic High Level	2.0	—	—	2.0	—	—	V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level	—	—	0.8	—	—	0.8	V
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	10	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{OE}$ = 2.0V V_{OUT} = 0 to V_{CC}	—	—	10	—	—	10	µA
I_{CC}	Operating Power Supply Current	V_{CC} = Max., Outputs Disabled f = 10MHz[2]	—	40	80	—	40	100	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	40	—	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ – 0.2V, $V_{IN} \leq$ 0.2V	—	4	20	—	4	25	mA
I_{CC}/f[2,3]	Increase in Power Supply Current	V_{CC} = Max., Outputs Disabled	—	—	4	—	—	6	mA/ MHz
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}[4]	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_O = GND	-20	—	-120	-20	—	-120	mA

NOTES:

2580 tbl 03

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = 0 to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 80+ 4(f –10)mA; for the military range, I_{CC} = 100 + 6(f –10). f = operating frequency in MHz, f = 1/t_{MUC} for IDT7216 and f = 1/t_{MC} for IDT7217.
3. For frequencies greater than 10MHz, guaranteed by design, not production tested.
4. I_{OL} = 4mA for t_{MC} >65ns.

AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ± 10%, T_A = 0° to +70°C)

Symbol	Parameter	7216L16[5] 7217L16		7216L20 7217L20		7216L25 7217L25		7216L35 7217L35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{MUC}	Unclocked Multiply Time[4]	2	25	2	30	2	38	2	55	ns
t_{MC}	Clocked Multiply Time[4]	2	16	2	20	2	25	2	35	ns
t_S	X, Y, RND Set-up Time	10	—	11	—	12	—	12	—	ns
t_H	X, Y, RND Hold Time	1	—	1	—	2	—	3	—	ns
t_{PWH}	Clock Pulse Width High	7	—	9	—	10	—	10	—	ns
t_{PWL}	Clock Pulse Width Low	7	—	9	—	10	—	10	—	ns
t_{PDSEL}	$\overline{\text{MSPSEL}}$ to Product Out[4]	2	15	2	18	2	20	2	25	ns
t_{PDP}	Output Clock to P[4]	2	15	2	18	2	20	2	25	ns
t_{PDY}	Output Clock to Y[4]	2	15	2	18	2	20	2	25	ns
t_{ENA}	3-State Enable Time	—	15	—	18	—	20	—	25	ns
t_{DIS}	3-State Disable Time[2]	—	15	—	18	—	20	—	22	ns
t_S	Clock Enable Set-up Time (IDT7217 only)	9	—	10	—	10	—	10	—	ns
t_H	Clock Enable Hold Time (IDT7217 only)	0	—	0	—	2	—	3	—	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (IDT7216 only)[1,3]	0	—	0	—	0	—	0	—	ns

Symbol	Parameter	7216L45 7217L45		7216L55 7217L55		7216L65 7217L65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{MUC}	Unclocked Multiply Time[4]	2	65	2	75	2	85	ns
t_{MC}	Clocked Multiply Time[4]	2	45	2	55	2	65	ns
t_S	X, Y, RND Set-up Time	15	—	20	—	20	—	ns
t_H	X, Y, RND Hold Time	3	—	3	—	3	—	ns
t_{PWH}	Clock Pulse Width High	15	—	15	—	15	—	ns
t_{PWL}	Clock Pulse Width Low	15	—	20	—	20	—	ns
t_{PDSEL}	$\overline{\text{MSPSEL}}$ to Product Out[4]	2	25	2	25	2	30	ns
t_{PDP}	Output Clock to P[4]	2	25	2	30	2	30	ns
t_{PDY}	Output Clock to Y[4]	2	25	2	30	2	30	ns
t_{ENA}	3-State Enable Time	—	25	—	30	—	35	ns
t_{DIS}	3-State Disable Time[2]	—	22	—	25	—	25	ns
t_S	Clock Enable Set-up Time (IDT7217 only)	10	—	10	—	10	—	ns
t_H	Clock Enable Hold Time (IDT7217 only)	3	—	3	—	3	—	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (IDT7216 only)[1,3]	0	—	0	—	0	—	ns

NOTES:

2580 tbl 06

1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured ±500mV from steady state voltage.
3. Guaranteed by design, not production tested.
4. Minimum propagation delay times are guaranteed, not production tested.
5. This speed is available in PGA and PLCC packages only.

AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ± 10%, T_A = –55° to +125°C)

Symbol	Parameter	7216L20[5] 7217L20		7216L25 7217L25		7216L30 7217L30		7216L40 7217L40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{MUC}	Unclocked Multiply Time[4]	2	30	2	38	2	43	2	60	ns
t_{MC}	Clocked Multiply Time[4]	2	30	2	25	2	30	2	40	ns
t_S	X, Y, RND Set-up Time	11	—	12	—	12	—	15	—	ns
t_H	X, Y, RND Hold Time	1	—	2	—	2	—	3	—	ns
t_{PWH}	Clock Pulse Width High	9	—	10	—	10	—	15	—	ns
t_{PWL}	Clock Pulse Width Low	9	—	10	—	10	—	15	—	ns
t_{PDSEL}	$\overline{\text{MSPSEL}}$ to Product Out[4]	2	18	2	20	2	20	2	25	ns
t_{PDP}	Output Clock to P[4]	2	18	2	20	2	20	2	25	ns
t_{PDY}	Output Clock to Y[4]	2	18	2	20	2	20	2	25	ns
t_{ENA}	3-State Enable Time	—	18	—	20	—	20	—	25	ns
t_{DIS}	3-State Disable Time[2]	—	20	—	22	—	22	—	25	ns
t_S	Clock Enable Set-up Time (IDT7217 only)	10	—	10	—	10	—	12	—	ns
t_H	Clock Enable Hold Time (IDT7217 only)	0	—	2	—	2	—	3	—	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (IDT7216 only)[1,3]	0	—	0	—	0	—	0	—	ns

Symbol	Parameter	7216L55 7217L55		7216L65 7217L65		7216L75 7217L75		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{MUC}	Unclocked Multiply Time[4]	2	75	2	85	2	95	ns
t_{MC}	Clocked Multiply Time[4]	2	55	2	65	2	75	ns
t_S	X, Y, RND Set-up Time	20	—	25	—	25	—	ns
t_H	X, Y, RND Hold Time	3	—	3	—	3	—	ns
t_{PWH}	Clock Pulse Width High	15	—	15	—	15	—	ns
t_{PWL}	Clock Pulse Width Low	15	—	15	—	15	—	ns
t_{PDSEL}	$\overline{\text{MSPSEL}}$ to Product Out[4]	2	30	2	35	2	35	ns
t_{PDP}	Output Clock to P[4]	2	30	2	30	2	35	ns
t_{PDY}	Output Clock to Y[4]	2	30	2	30	2	35	ns
t_{ENA}	3-State Enable Time	—	25	—	35	—	40	ns
t_{DIS}	3-State Disable Time[2]	—	25	—	25	—	25	ns
t_S	Clock Enable Set-up Time (IDT7217 only)	15	—	15	—	15	—	ns
t_H	Clock Enable Hold Time (IDT7217 only)	3	—	3	—	3	—	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (IDT7216 only)[1,3]	0	—	0	—	0	—	ns

NOTES:

2580 tbl 07

1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured ±500mV from steady state voltage.
3. Guaranteed by design, not production tested.
4. Minimum propagation delay times are guaranteed, not production tested.
5. This speed is available in PGA and Flatpack packages only.

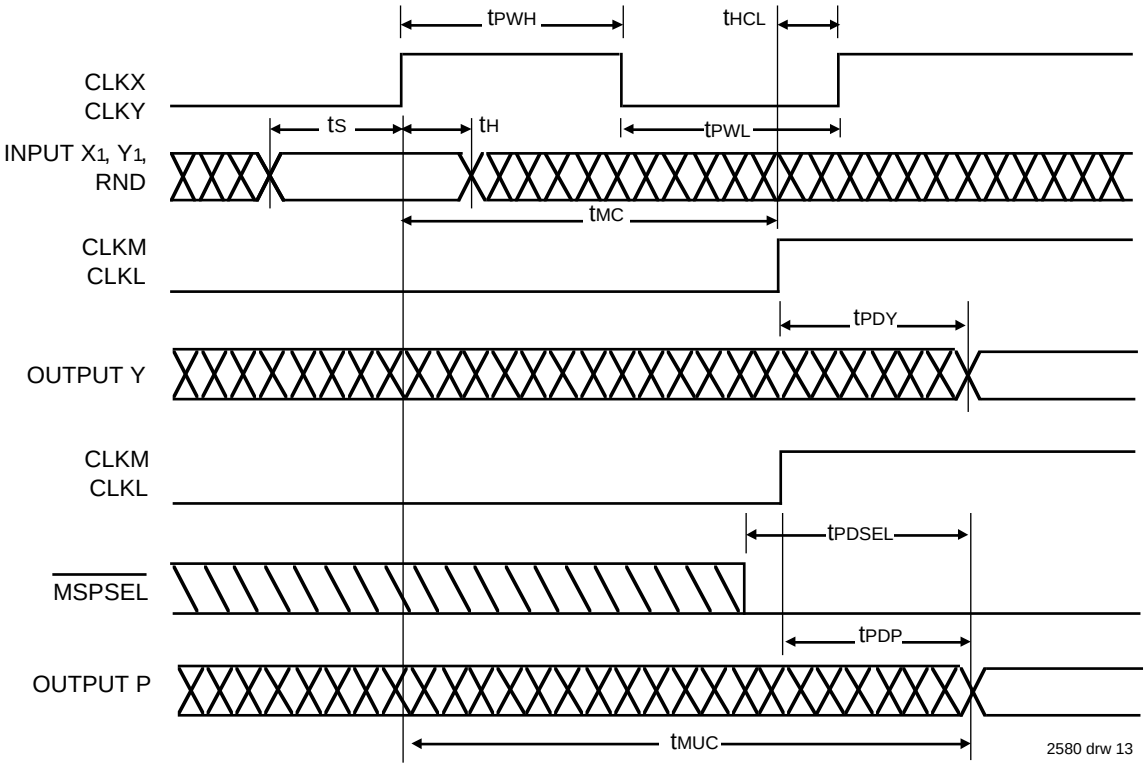


Figure 4. IDT7216 Timing Diagram

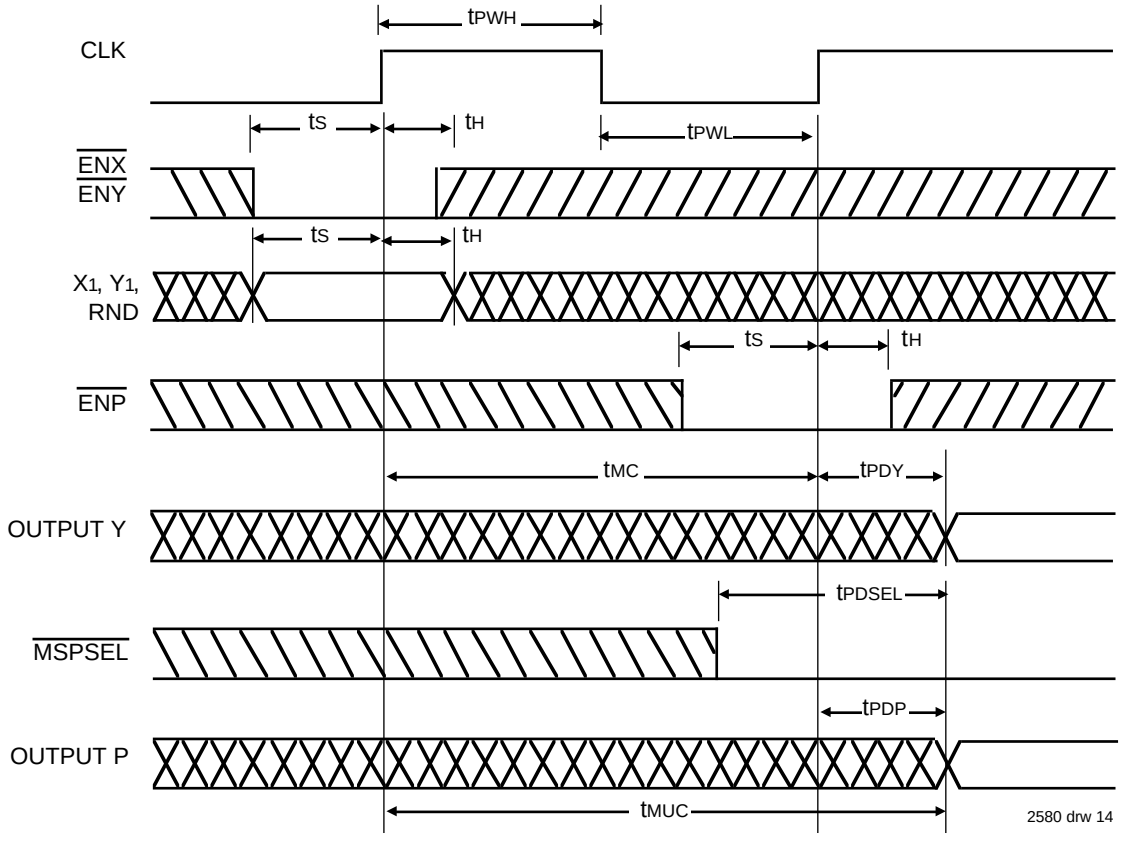


Figure 5. IDT7217 Timing Diagram

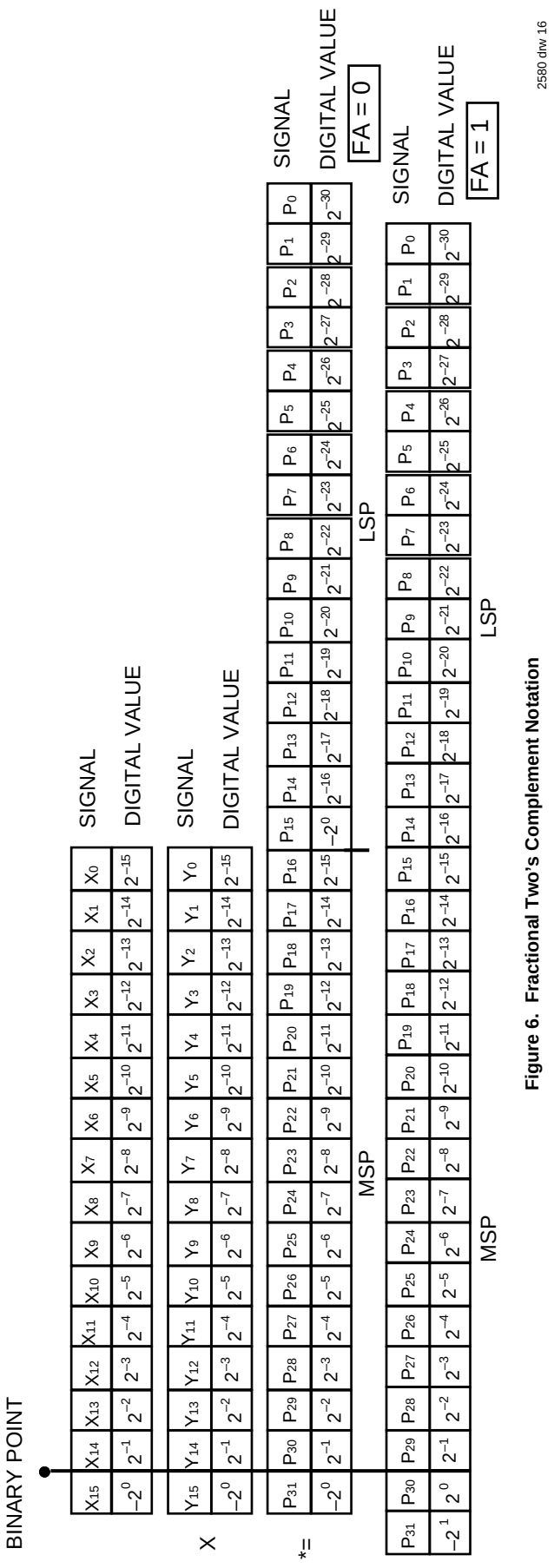


Figure 6. Fractional Two's Complement Notation

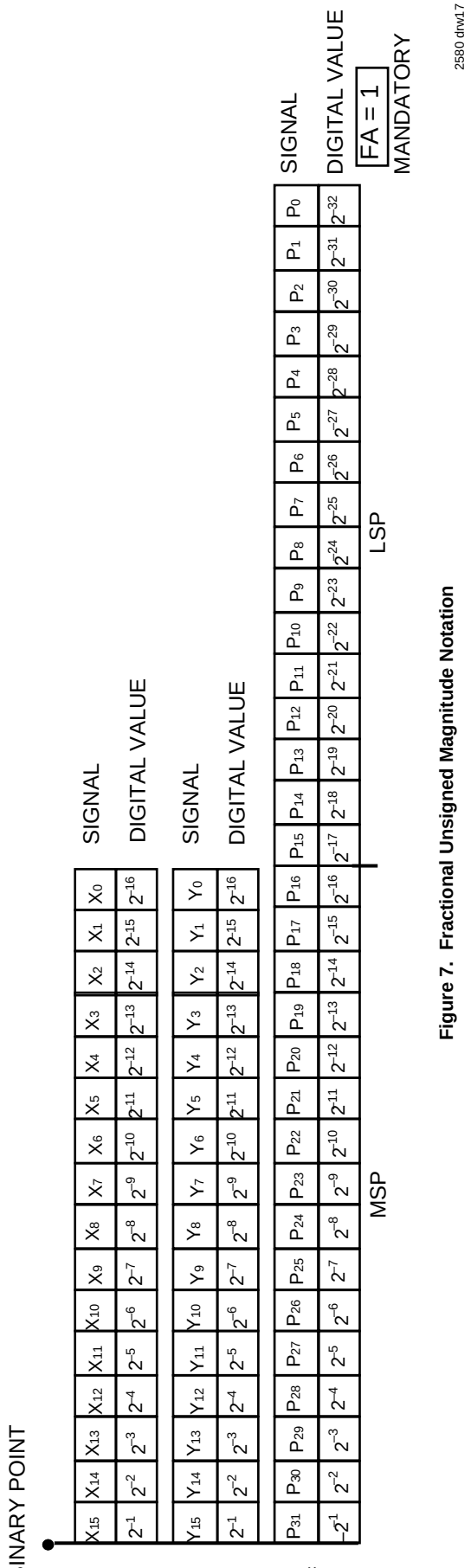


Figure 7. Fractional Unsigned Magnitude Notation

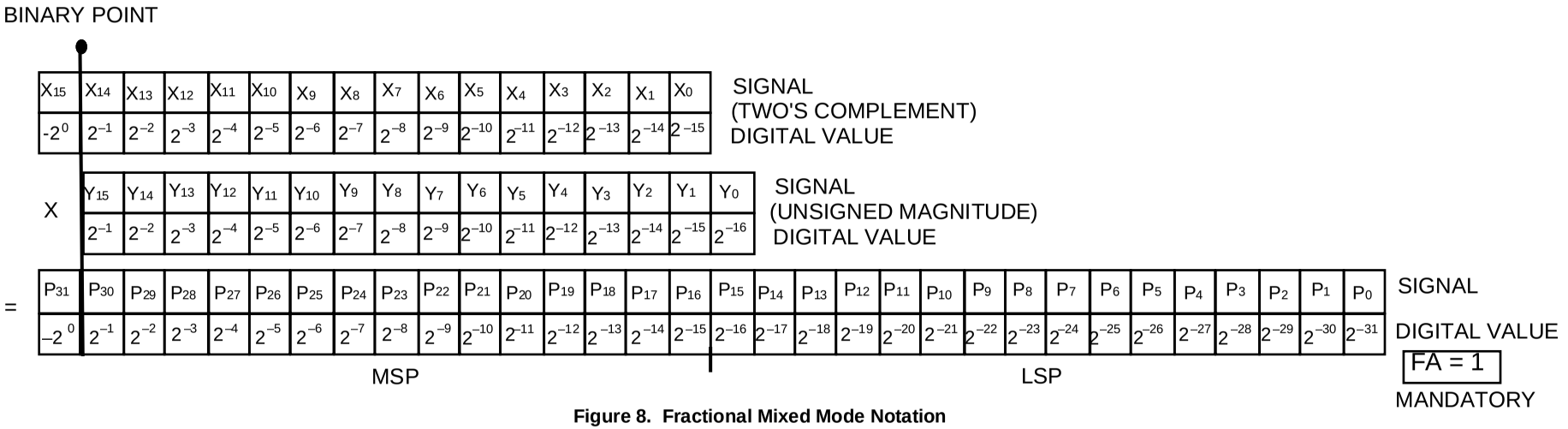


Figure 8. Fractional Mixed Mode Notation

2580 drw 18

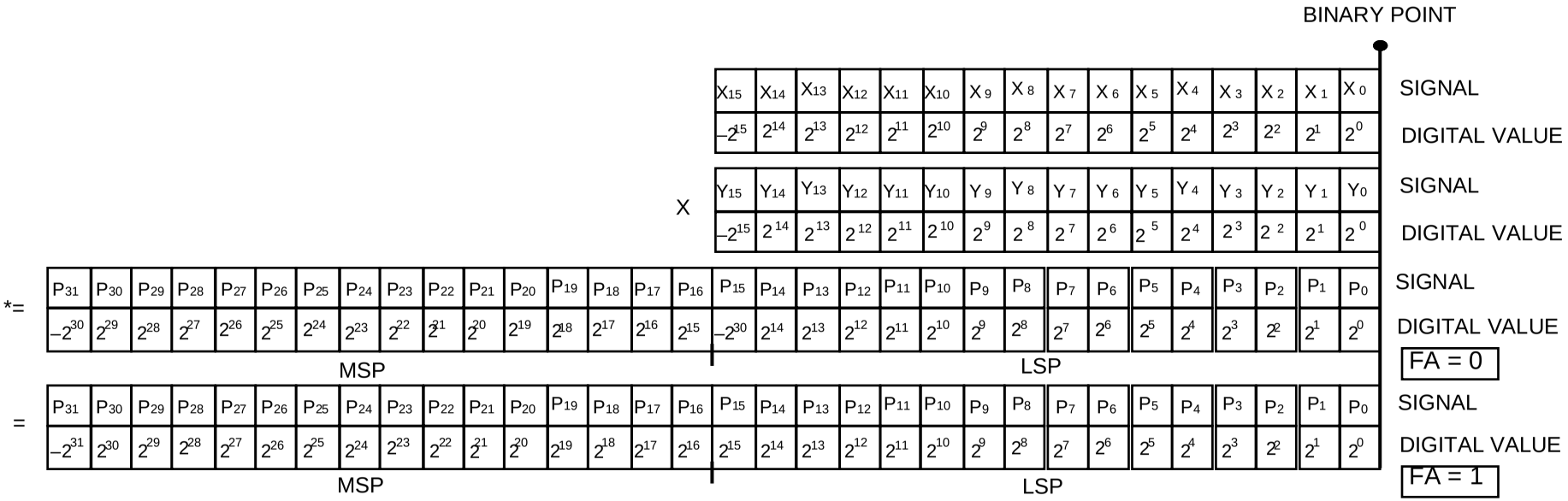


Figure 9. Integer Two's Complement Notation

2580 drw 19

* In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000 . . . 0 with 1,000.0 yielding an erroneous product of –1 in the fraction case and -2^{30} in the integer case.

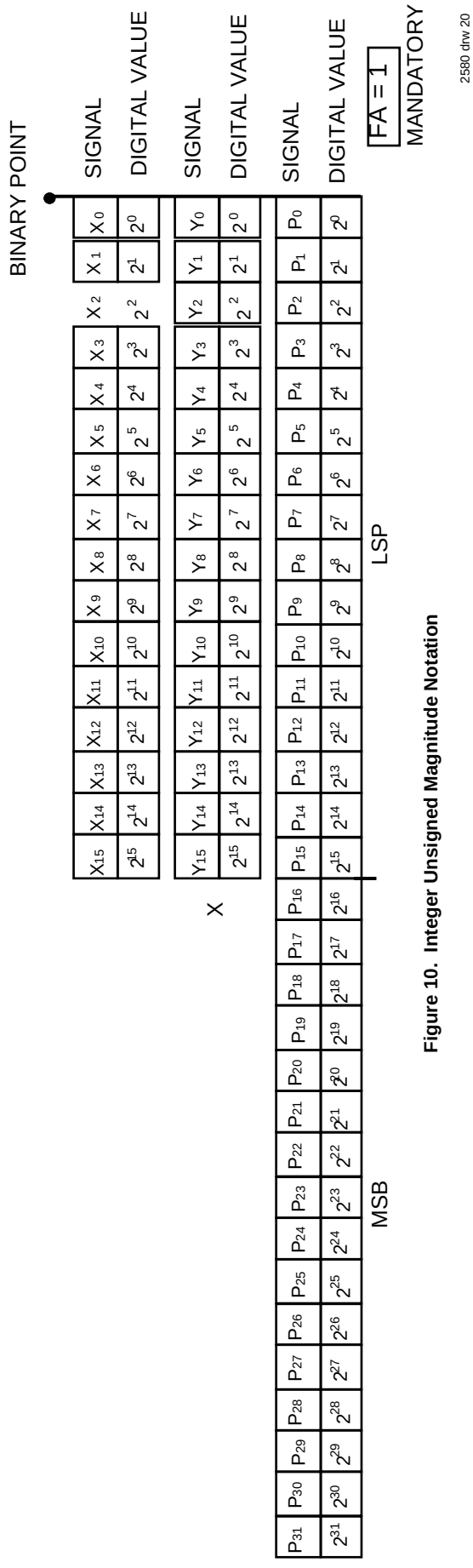


Figure 10. Integer Unsigned Magnitude Notation

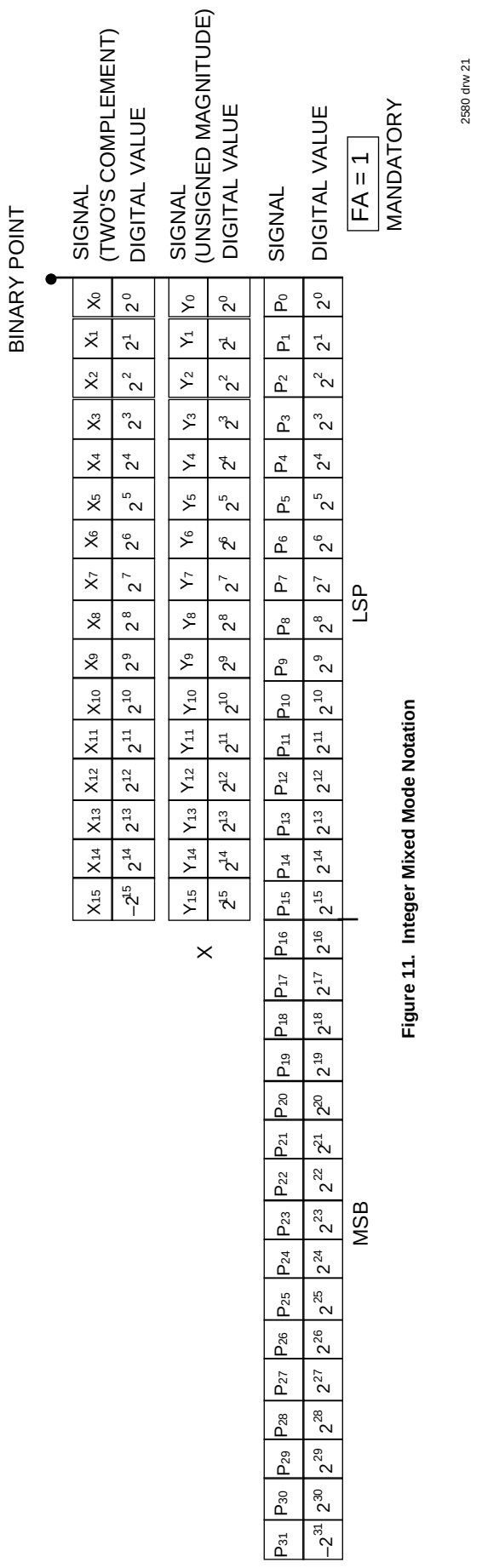


Figure 11. Integer Mixed Mode Notation

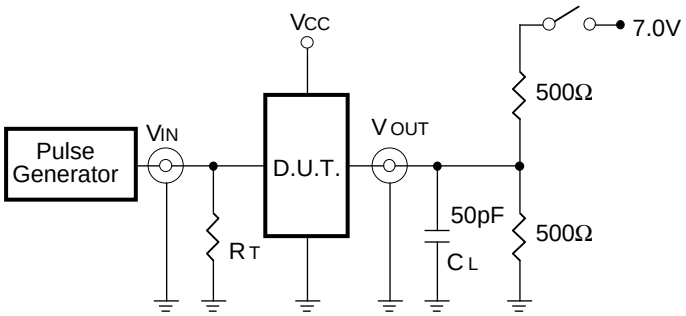


Figure 12. AC Test Load Circuit

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2580 tbl 08

SWITCH POSITION

Test	Switch
Disable Low Enable Low	Closed
All Other Tests	Open

2580 tbl 09

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

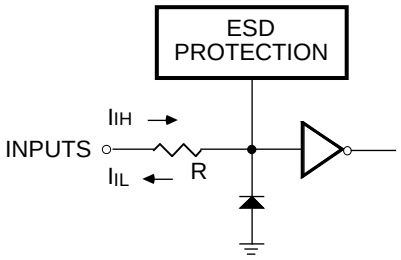


Figure 13. Input Interface Circuit

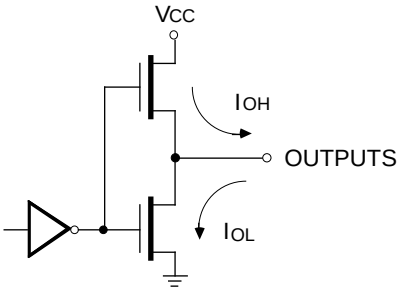
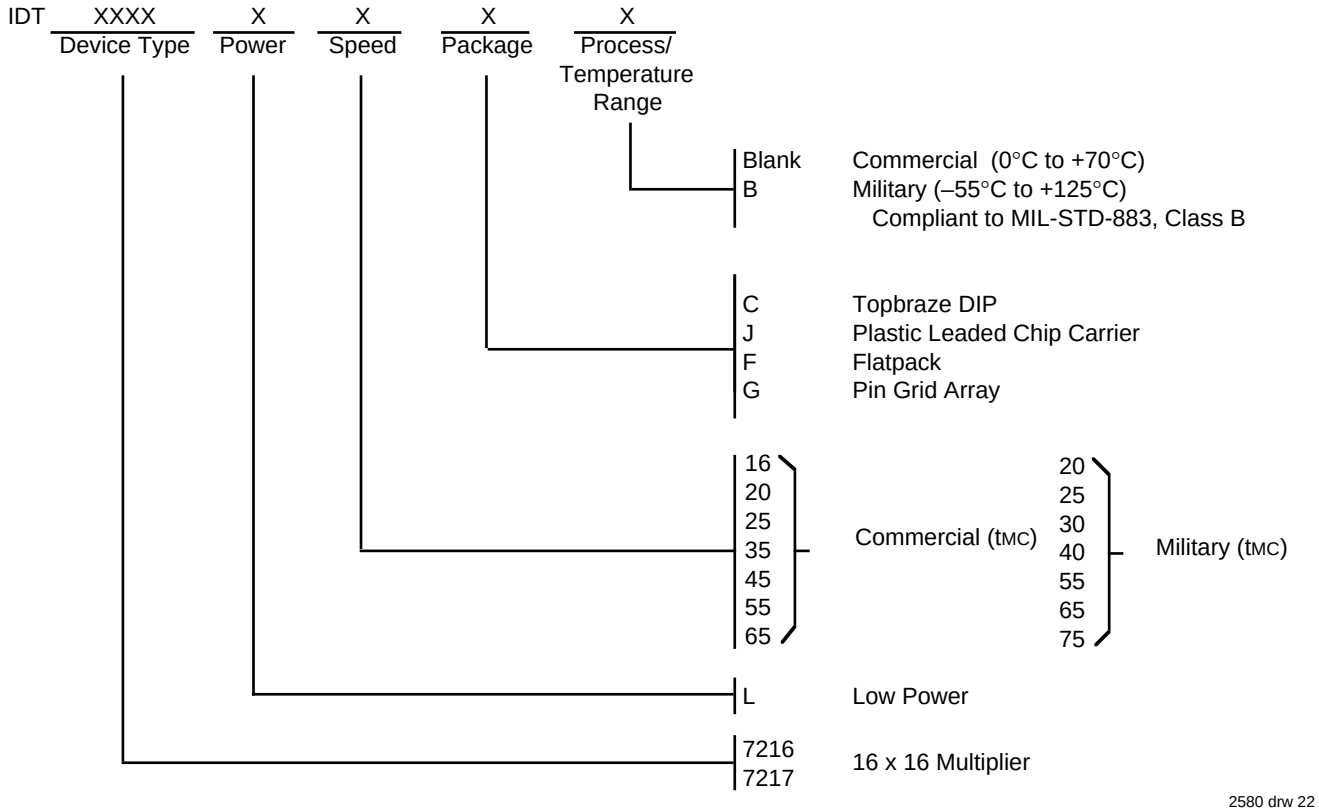


Figure 14. Output Interface Circuit

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