MX23L1614

16M-BIT MASK ROM

FEATURES

- Bit organization
  - 1Mb x 16 (word mode only)
- Fast access time
  - Random access:70ns(max.)
- Current
  - Operating:15mA
  - Standby:15uA(max.)
- Supply voltage
  - VCC : 2.7 ~ 3.6V
  - VCCQ : 2.7 ~ 3.6V
- Package
  - 48 pin TSOP (12mm X 20mm)
  - 48 ball mini BGA (8.0mm X 6.0mm, ball pitch 0.75mm)
- Temperature
  - -40~85° C

PIN DESCRIPTION

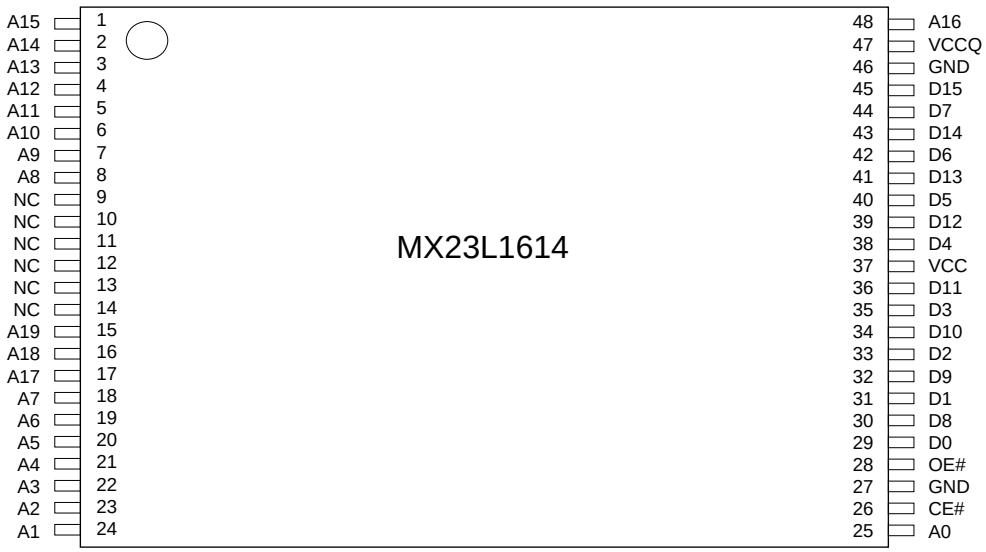
Symbol	Pin Function
A0~A19	Address Inputs
D0~D15	Data Outputs
CE#	Chip Enable Input
OE#	Output Enable Input
VCC	Power Supply Pin
VCCQ	Output VCC Pin
GND	Ground Pin
NC	No Connection

MODE SELECTION

CE#	OE#	D0~D15	Power
H	X	High Z	Stand-by
L	H	High Z	Active
L	L	D0~D15	Active

PIN CONFIGURATION

48 TSOP (Top View)



48 Mini BGA (Top View, Ball Down)



ORDER INFORMATION

Part No.	Speed	Package	Grade
MX23L1614TI-70	70ns	48 pin TSOP	Industrial
MX23L1614TI-90	90ns	48 pin TSOP	Industrial
MX23L1614TI-10	100ns	48 pin TSOP	Industrial
MX23L1614XI-70	70ns	48 ball mini BGA	Industrial
MX23L1614XI-90	90ns	48 ball mini BGA	Industrial
MX23L1614XI-10	100ns	48 ball mini BGA	Industrial

Note: Industrial grade temperature: -40 ~ 85° C
Commercial grade temperature: 0 ~ 70° C

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-0.3V to 3.9V
Ambient Operating Temperature	Topr	-40° C to 85° C
Storage Temperature	Tstg	-65° C to 125° C

DC CHARACTERISTICS (Ta = -40° C ~ 85° C, VCC = 2.7V~3.6V)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -400uA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.2V	VCCQ+0.3V	
Input Low Voltage	VIL	-0.4V	0.4V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC	-	15mA	f=5MHz, CE#=VIL, OE#=VIH all output open
Standby Current (CMOS)	ISTB	-	15uA	CE#>VCC-0.2V
Input Capacitance	CIN	-	10pF	Ta = 25° C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25° C, f = 1MHZ

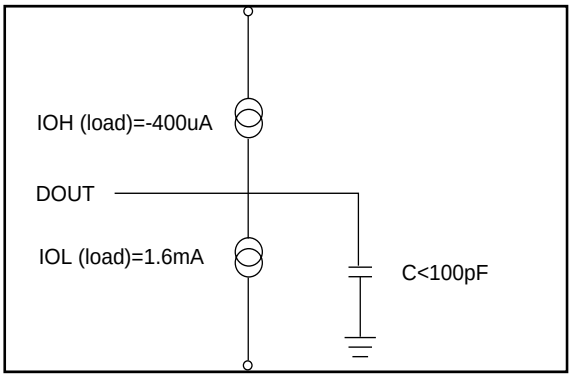
AC CHARACTERISTICS (Ta = -40° C ~ 85° C, VCC = 2.7V~3.6V)

Item	Symbol	MX23L1614-70		MX23L1614-90		MX23L1614-10	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	70ns	-	90ns	-	100ns	-
Address Access Time	tAA	-	70ns	-	90ns	-	100ns
Chip Enable Access Time	tACE	-	70ns	-	90ns	-	100ns
Output Enable Time	tOE	-	20ns	-	20ns	-	30ns
Output Hold After Address	tOH	0ns	-	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns	-	20ns

Note:Output high-impedance delay (tHZ) is measured from OE# or CE# going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

AC Test Conditions

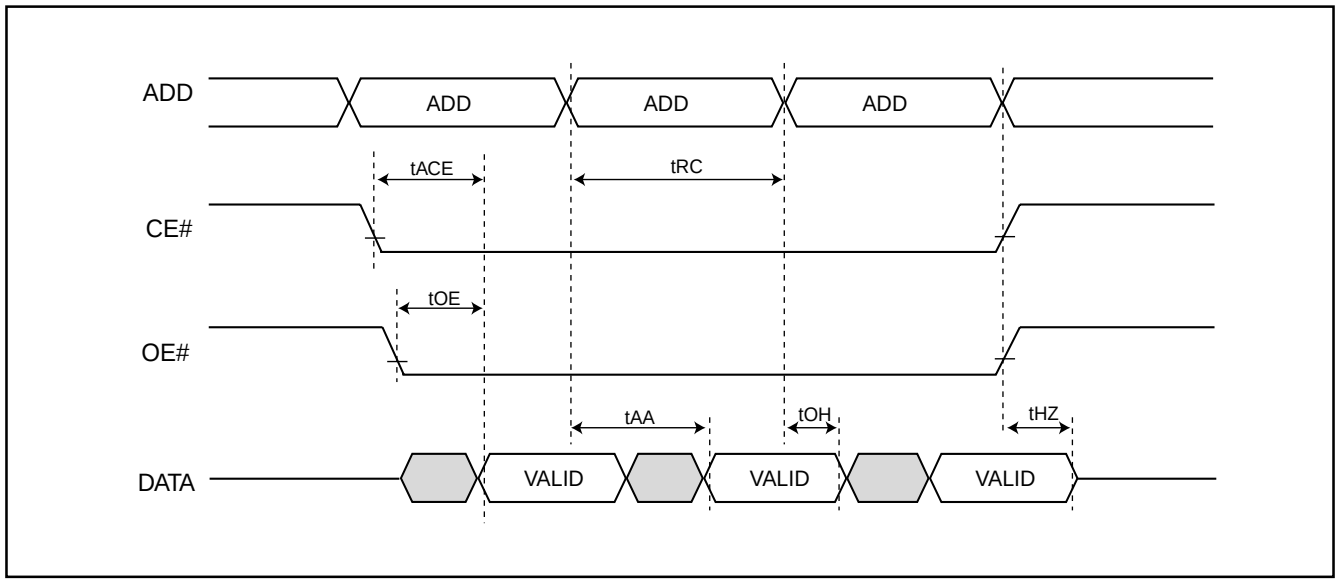
Input Pulse Levels	0.4V~2.4V
Input Rise and Fall Times	5ns
Input Timing Level	1.5V
Output Timing Level	1.5V
Output Load	See Figure 100pF output load capacitance



Note:No output loading is present in tester load board.
Active loading is used and under software programming control.
Output loading capacitance includes load board's and all stray capacitance.

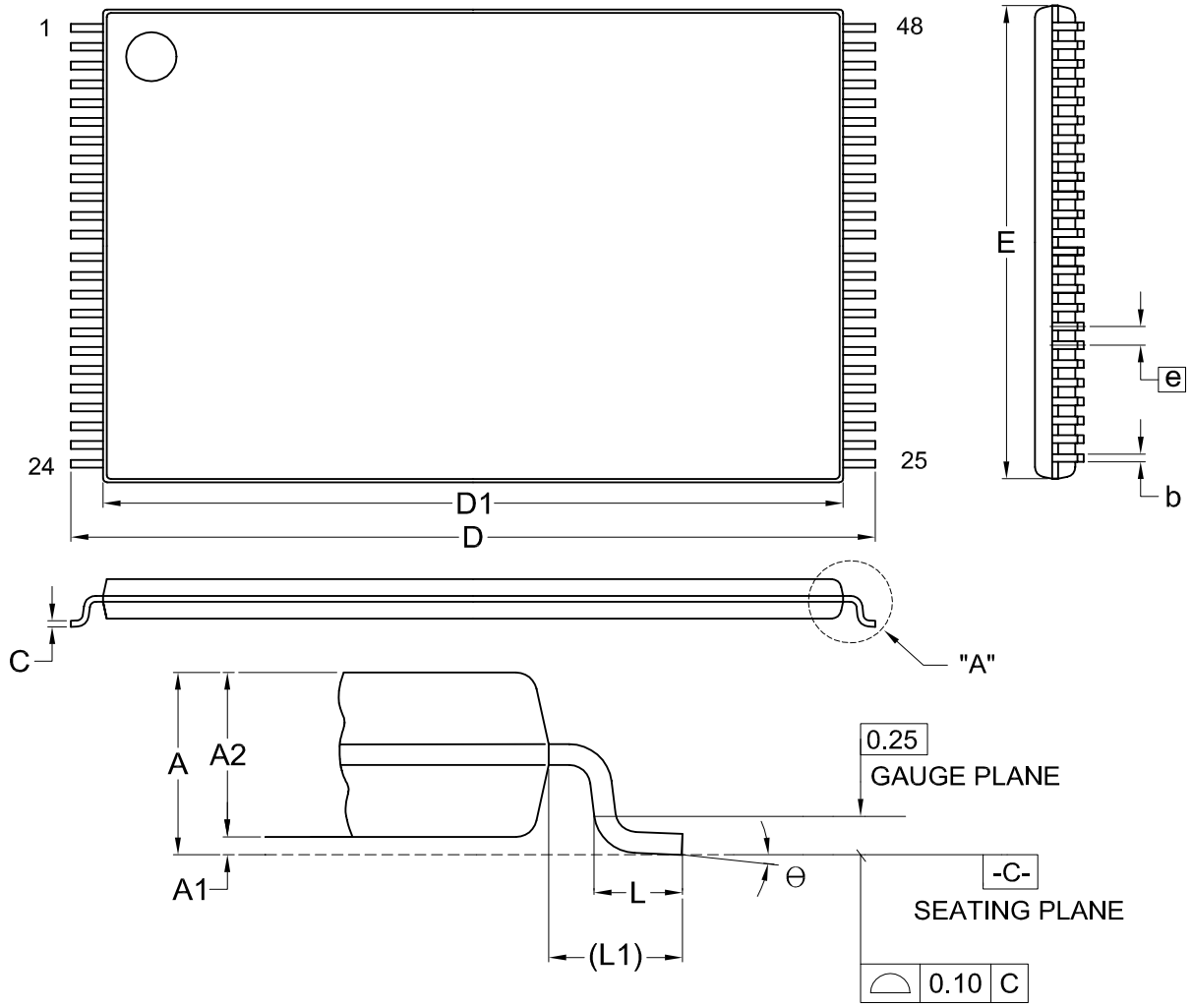
TIMING DIAGRAM

RANDOM READ



PACKAGE INFORMATION

Title: **Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM**



DETAIL"A"

Dimensions (inch dimensions are derived from the original mm dimensions)

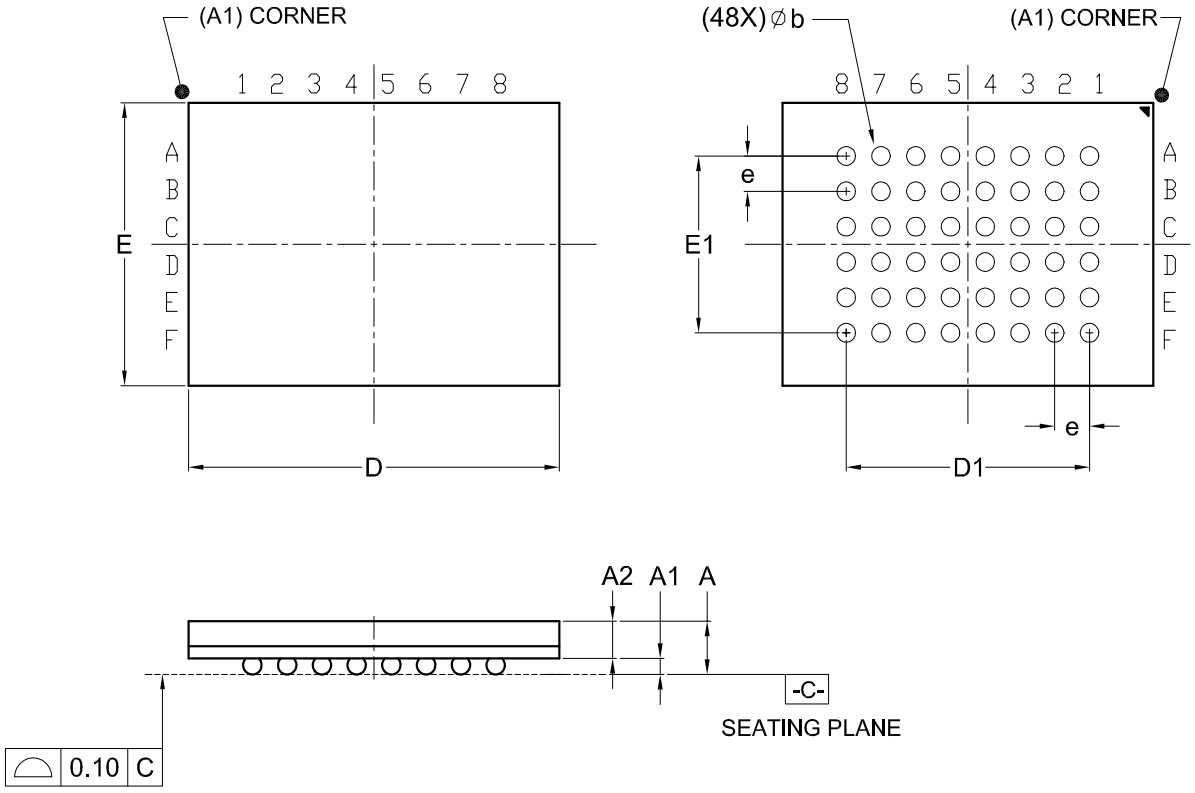
SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607	7	MO-142			12-01-'03

Title: **Package Outline for CSP 48BALL(8X6X1.2MM,BALL PITCH 0.75MM,BALL DIAMETER 0.35MM)**

TOP VIEW

BOTTOM VIEW



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.22	0.65	0.30	7.90		5.90		
	Nom.	---	0.27	---	0.35	8.00	5.25	6.00	3.75	0.75
	Max.	1.20	0.32	---	0.40	8.10		6.10		
Inch	Min.	---	0.009	0.026	0.012	0.311		0.232		
	Nom.	---	0.011	---	0.014	0.315	0.207	0.236	0.148	0.030
	Max.	0.047	0.013	---	0.016	0.319		0.240		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4208	4	MO-207			12-15-'05

REVISION HISTORY

Revision	Description	Page	Date
1.1	Modify Standby Current 7uA-->15uA	P1,2	AUG/08/2000
	Modify Operating Current 18mA-->15mA	P1,2	
	Modify Pin Description/Pin Configuration VSS-->GND	P1,2	
	Modify Random Access:90ns-->110ns	P1	
1.2	Add Pin Configuration--48 Mini BGA	P1	OCT/17/2000
	Add AC Characteristics--MX23L1614-80/90/100	P2	
1.3	Modify Package-48 ball mini BGA(8mm x 10mm)-->(6.0mm x 8.0mm)	P1	NOV/24/2000
	Modify 48-pin PIN Configuration	P2	
1.4	Modify Mode Selection--> L, H, High Z, Active	P1	DEC/19/2000
1.5	Modify Fast Access Time:80ns-->70ns(max.)	P1,2	JAN/18/2001
1.6	Modify Pin Configuration--48 mini BGA	P1	JUN/29/2001
	Add Package Information	P5,6	
1.7	Added Order Information	P2	JUL/10/2001
1.8	1.Modify DC Characteristics--VOH:VCCQ-0.1V-->2.4V, IOH=-100uA--> -400uA, VOL:0.1V-->0.4V, IOL:100uA-->1.6mA, VIH:VCCQ-0.4V-->2.2V	P3	SEP/10/2001
	2.Modify AC Test Conditions--Input Pulse Levels:0~VCCQ-->0.4V~2.4V, Input/Output Timing Level:VCCQx0.5-->1.5V, Output Load:50pF--> 100pF output load capacitance	P4	
1.9	Add CE#=VIL, OE#=VIH in DC Characteristics's ICC	P3	SEP/28/2001
2.0	Modify 48-Ball BAG Package Information	P6	MAR/12/2002
2.1	1. To modify Package Information	P5,6	MAR/28/2003

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