DATA SHEET

TEA6824T
In Car Entertainment (ICE) car radio

Preliminary specification
Supersedes data of 1996 Nov 04
File under Integrated Circuits, IC01

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Philips
Semiconductors

PHILIPS

In Car Entertainment (ICE) car radio TEA6824T

FEATURES

- FM mixer for conversion from FM-IF_1 = 72.2 MHz to FM-IF_2 = 10.7 MHz
- AM mixer for conversion from AM-IF_1 = 10.7 MHz to AM-IF_2 = 450 kHz
- FM-IF gain stage
- Crystal oscillator providing mixer frequencies and references for IF-counter
- FM quadrature demodulator with automatic centre frequency adjustment and THD compensation
- AM-IF-amplifier and demodulator
- I^2C-bus transceiver with interface to enable direct data transfer to radio front-end
- IF-count for AM and FM
- Analog-to-digital conversion of level voltage and multi-path information
- Reference frequency generation for PLL synthesizer.

GENERAL DESCRIPTION

The TEA6824T together with the TEA6810T forms the receiver part of an AM/FM electronically tuned car radio providing FM MPX signal and AM AF signal for Car Digital Signal Processor (CDSP) applications.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6824T	VSO56	plastic very small outline package; 56 leads; face down	SOT190-2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA1}	analog supply voltage 1 (+5 V; pin 5)	note 1	4.5	5.0	5.5	V
		operating range	4.75	5.0	5.25	V
I_{DDA1}	analog supply current 1 (pin 5)	FM mode	17	21	25	mA
		AM mode	14	17	21	mA
$I_{19} + I_{20}$	total FM mixer output current (pins 19 and 20)		4.8	6.0	7.2	mA
$I_{22} + I_{23}$	total AM mixer output current (pins 22 and 23)		10	12	14	mA
V_{DDA2}	analog supply voltage 2 (pin 28)	note 1	7.0	8.5	10	V
		operating range	8.1	8.5	8.9	V
I_{DDA2}	analog supply current 2 (pin 28)	FM mode	2.4	3.0	3.6	mA
V_{DDA3}	analog supply voltage 3 (+8.5 V; pin 56)	note 1	7.0	8.5	10	V
		operating range	8.1	8.5	8.9	V
I_{DDA3}	analog supply current 3 (pin 56)	FM mode	19	25	31	mA
		AM mode	9.5	12	15	mA
V_{DDD}	digital supply voltage 1 (+5 V; pin 5)	note 1	4.5	5.0	5.5	V
		operating range	4.75	5.0	5.25	V
I_{DDD}	digital supply current (pin 52)	note 1	8	10	12	mA
$\frac{S+N}{N}$	signal plus noise-to-noise ratio	FM mode; Δf = 22.5 kHz at pin 47	66	75	–	dB
		AM mode; m = 0.3	54	60	–	dB
THD	total harmonic distortion	FM mode; Δf = 75 kHz	–	0.1	0.35	%
		AM mode	–	1.5	3.0	%
T_{amb}	operating ambient temperature		–40	–	+85	°C

Note

1. IC is operating; specified parameters may deviate from limits which are valid for operating range.

BLOCK DIAGRAM

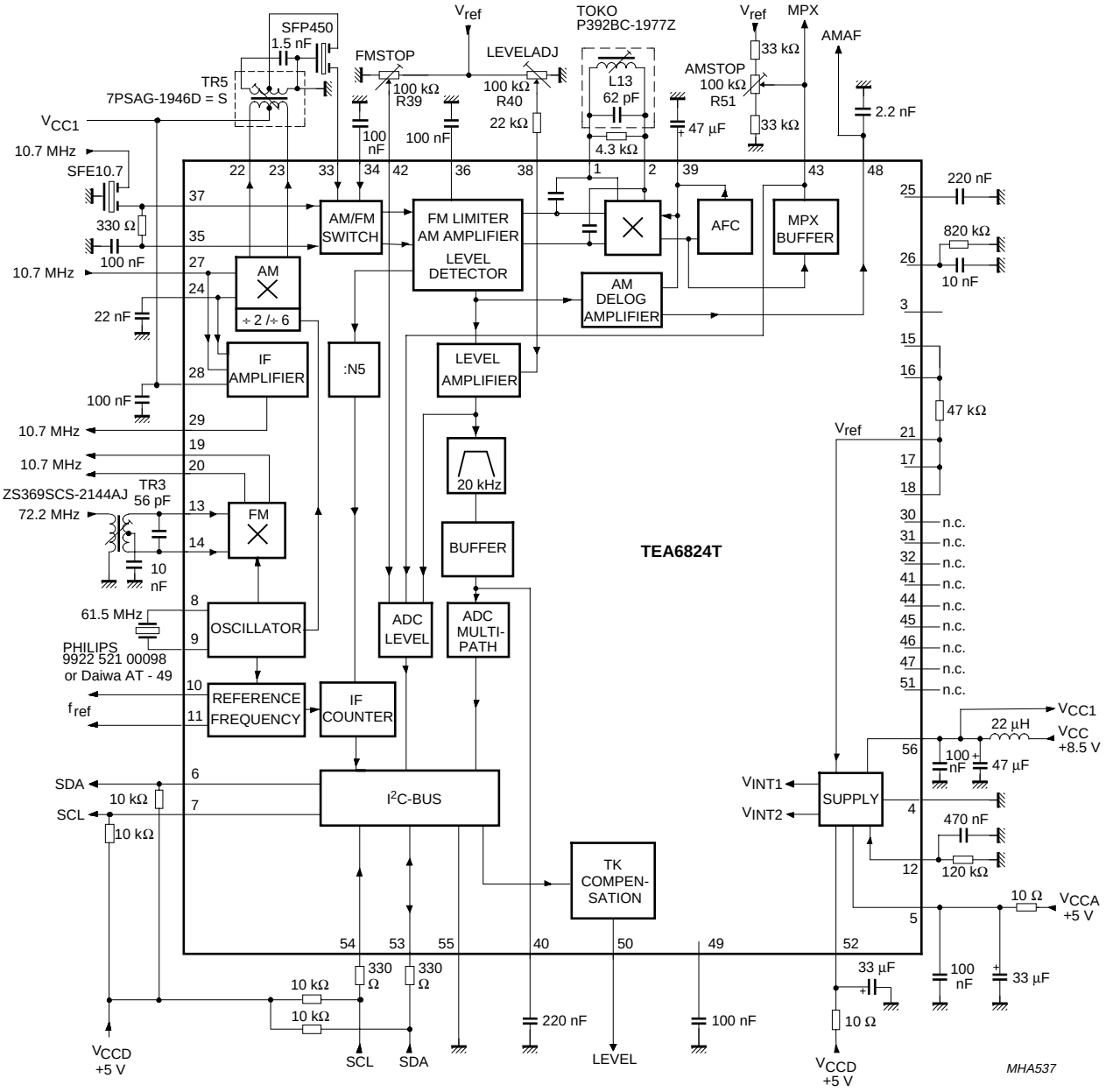


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
QDET1	1	demodulator tank 1
QDET2	2	demodulator tank 2
REFIN1	3	reference input 1
AGND	4	analog ground
V_{DDA1}	5	analog supply voltage 1 (+5 V)
HFBUS1	6	HF bus 1 output; pull-up to +5 V
HFBUS2	7	HF bus 2 output; pull-up to +5 V
XTAL1	8	crystal oscillator 1
XTAL2	9	crystal oscillator 2
$f_{ref(p)}$	10	PLL reference frequency output p
$f_{ref(n)}$	11	PLL reference frequency output n
I_{ref}	12	reference current input
FMIF1IN1	13	72 MHz FM-IF input 1
FMIF1IN2	14	72 MHz FM-IF input 2
REFIN2	15	reference input 2
REFIN3	16	reference input 3
REFIN4	17	reference input 4
REFIN5	18	reference input 5
FMIF2OUT1	19	FM mixer output 1
FMIF2OUT2	20	FM mixer output 2
V_{ref}	21	reference voltage input
AMIF2OUT1	22	AM mixer output 1
AMIF2OUT2	23	AM mixer output 2
FMAMDEC	24	FM/AM 10.7 MHz decoupling input
DEC1	25	decoupling 1
DEC2	26	decoupling 2
FMAM10.7	27	FM/AM 10.7 MHz input
V_{DDA2}	28	analog supply voltage 2

SYMBOL	PIN	DESCRIPTION
FMIFAMPOUT	29	FM-IF-amplifier output
n.c.	30	not connected
n.c.	31	not connected
n.c.	32	not connected
AMIF2IN1	33	AM-IF_2 input 1
AMIF2IN2	34	AM-IF_2 input 2
FMIN2	35	FM limiter input 2
DCFEED	36	DC feed FM limiter
FMIN1	37	FM limiter input 1
LEVELADJ	38	level adjustment
C_{AFC}	39	AFC capacitor
MPBUF	40	multi-path buffer time constant
n.c.	41	not connected
FMSTOP	42	FMSTOP adjustment
MPXOUT	43	FM demodulator MPX output
n.c.	44	not connected
n.c.	45	not connected
n.c.	46	not connected
n.c.	47	not connected
AMAFOUT	48	AM demodulator AF output
DEC3	49	decoupling 3
LEVELUNWEIG	50	level unweighted output
n.c.	51	not connected
V_{DDD}	52	digital supply voltage (+5 V)
SDA	53	serial data input/output; pull-up to +5 V; I^2C-bus
SCL	54	serial clock input; pull-up to +5 V; I^2C-bus
DGND	55	digital ground
V_{DDA3}	56	analog supply voltage 3 (+8.5 V)

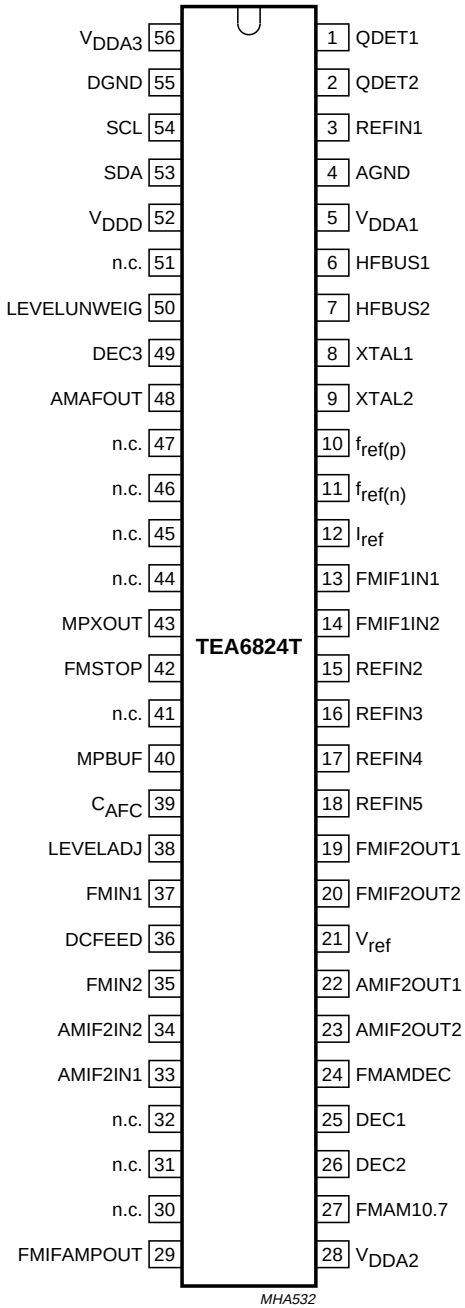


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA1}	analog supply voltage 1 (pin 5)		–0.3	+6.5	V
V_{DDA2}	analog supply voltage 2 (pin 28)		–0.3	+12	V
V_{DDA3}	analog supply voltage 3 (pin 56)		–0.3	+12	V
V_{DDD}	digital supply voltage (pin 52)		–0.3	+6.5	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es}	electrostatic handling	note 1			
	pins 8 and 9		–100	+100	V
	all other pins		–300	+300	V

Note

1. Charge device model class B: equivalent to discharging a 200 pF capacitor via a 0 Ω series resistor.

CHARACTERISTICS

$V_{DDA3} = V_{DDA2} = 8.5$ V (ref. AGND); $V_{DDA1} = 5$ V (ref. AGND); $V_{DDD} = 5$ V (ref. DGND); $T_{amb} = 25$ °C; $f_{mod} = 1$ kHz; $\Delta f = 22.5$ kHz; $R_g = 50$ Ω; $V_{37\text{-}35} = 10$ mV; with de-emphasis = 50 µs; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Current consumption						
I_{DDA1}	analog supply current 1 (pin 5)	FM mode	17	21	25	mA
		AM mode	14	17	21	mA
I_{DDA2}	analog supply current 2 (pin 28)	FM mode	2.4	3.0	3.6	mA
I_{DDA3}	analog supply current 3 (pin 56)	FM mode	19	25	31	mA
		AM mode	9.5	12	15	mA
I_{DDD}	digital supply current (pin 52)		8	10	12	mA
$I_{19} + I_{20}$	total FM mixer output current pins 19 and 20		4.8	6.0	7.2	mA
$I_{22} + I_{23}$	total AM mixer output current pins 22 and 23	AM mode	10	12	14	mA
FM-IF path; see Fig.3						
$V_{19\text{-}20max(p\text{-}p)}$	maximum output voltage pins 19 to 20 (peak-to-peak value)		12	14	–	V
$I_{bias(19\text{-}20)}$	mixer bias current pins 19 to 20		2.4	3.0	3.6	mA
$I_{LI(19\text{-}20)}$	mixer leakage current pins 19 to 20	in AM position	–	–	2	µA
$I_{19IF2}/V_{13\text{-}14IF1}$	conversion gain		1.65	1.9	2.2	mS
$R_{i(13\text{-}14)}$	input resistance between pins 13 and 14		5	7	–	kΩ
$C_{i(13\text{-}14)}$	input capacitance between pins 13 and 14		–	3	4.5	pF
R_{opt}	optimum generator resistance		–	1.2	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{o(19-20)}$	output resistance between pins 19 and 20		15	20	–	kΩ
$C_{o(19-4)}$; $C_{o(20-4)}$	output capacitance between pins 19 to 4 and pins 20 to 4		–	12	14	pF
IP3	third-order intermodulation		114	124	–	dBμV
Oscillator						
f_{osc}	oscillator frequency		–	61.5	–	MHz
Δf_{osc}	oscillator frequency spread		–	–	250	Hz
$\Delta f_{osc}/\Delta T$	temperature dependence of oscillator frequency	crystal type Philips 9922 521 00098	–	30×10^{-6}	–	K^{-1}
R_1	crystal motional resistance		–	–	70	Ω
C_0	crystal shunt capacitance		–	–	5	pF
FM-IF$_2$ amplifier						
$V_{27-24max(rms)}$	maximum input voltage for 1 dB compression point between pins 27 and 24 (RMS value)		80	110	–	mV
$V_{29-4max(rms)}$	maximum output voltage between pins 29 and 4 (RMS value)		220	320	–	mV
V_{29-4}/V_{27-24}	amplifier gain between pins 29 and 4 and between pins 27 and 24	loaded with 330 Ω; see Fig.4	9	12	15	dB
$\Delta V_{29-4}/V_{27-24}$	gain temperature dependence between pins 29 and 4 and between pins 27 and 24		–	0.05	–	dB/K
$R_{i(27-4)}$	input resistance between pins 27 and 4		300	330	360	Ω
$C_{i(27-4)}$	input capacitance between pins 27 and 4		–	–	5	pF
$R_{o(29-4)}$	output resistance between pins 29 and 4		300	330	360	Ω
$C_{o(29-4)}$	output capacitance between pins 29 and 4		–	–	5	pF
FM-IF$_2$ limiter						
$V_{o1-2(p-p)}$	limiter output voltage between pins 1 and 2 (peak-to-peak value)		500	700	–	mV
V_{1-2}/V_{37-35}	limiter gain between pins 1 and 2 and between pins 37 and 35	see Fig.5	–	80	–	dB
$C_{i(37-4)}$	input capacitance between pins 37 and 4		–	–	5	pF
$R_{o(1-2)}$	output resistance between pins 1 and 2		–	–	1.0	kΩ
$C_{o(1-2)}$	output capacitance between pins 1 and 2		10	15	20	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM demodulator						
$V_{43\text{-}4(rms)}$	MPX output voltage between pins 43 and 4 (RMS value)		160	200	240	mV
$V_{37\text{-}35(rms)}$	start of limiting voltage between pins 37 and 35 (RMS value)	α_{AF} = –3 dB	–	25	40	μV
$V_{37\text{-}35(rms)}$	input voltage for signal plus noise-to-noise ratio (RMS value)	see Fig.6;				
		$\frac{S+N}{N}$ = 26 dB	–	30	45	μV
		$\frac{S+N}{N}$ = 46 dB	–	70	100	μV
ΔV_{43DC}	residual DC-offset voltage pin 43	ΔL_{demod} = typical value;				
		10 μV < $V_{37\text{-}35}$ < 80 μV	–	100	1000	mV
		80 μV < $V_{37\text{-}35}$ < 800 mV	–	10	30	mV
V_{43FM}/V_{43AM}	AM suppression pin 43	Δf = 22.5 kHz; f_{modAM} = 1 kHz; m_{AM} = 30%; $V_{37\text{-}35}$ = 3 to 300 mV	50	60	–	dB
$\Delta V_{43\text{-}44AFCdis}$ /$\Delta V_{43\text{-}44AFCactive}$	demodulator frequency control voltage (AFC) efficiency between pins 43 and 44 at 100 kHz detune from exact tuning		28	32	–	dB
R_{o43}	output resistance pin 43		–	–	1.5	kΩ
B_{43}	AF bandwidth pin 43		200	–	–	kHz
$\frac{S+N}{N}$	signal plus noise-to-noise ratio		66	75	–	dB
THD	total harmonic distortion at pin 43	detuning ≤50 kHz; Δf = 75 kHz; f_{mod} = 1 kHz without de-emphasis; L_{demod} = typical value; $V_{37\text{-}35}$ = 300 μV to 800 mV	–	0.1	0.35	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Unweighted voltage level						
V_{50-4}	unweighted voltage level	see Fig.7; V_{38} = 2.52 V;				
		$V_{37-35} \leq 2.5$ μV	1.6	2.2	3.0	V
		V_{37-35} = 1.0 mV	2.7	3.4	4.7	V
$\Delta V_{50-4}/\Delta V_{37-35}$	slope of unweighted voltage level	100 μV ≤ $V_{37-35(rms)}$ < 300 mV;				
		temperature compensation off	0.75	0.9	1.05	V/20 dB
		temperature compensation on	0.6	0.75	0.9	V/20 dB
$\Delta V_{50-4}/(V_{50-4}\Delta T)$	temperature dependence	V_{37-35} = 1 mV;				
		temperature compensation off	–	5.0	–	mV/VK
		temperature compensation on	–	2.0	–	mV/VK
$I_{source(max)}$	maximum output source current pin 50		0.3	–	–	mA
$I_{sink(max)}$	maximum output sink current pin 50		–50	–	–	μA
R_{o50}	output resistance pin 50		–	–	300	Ω
ADJUSTMENT OF UNWEIGHTED VOLTAGE LEVEL AND V_{mutaml}; note 1						
ΔV_{50}	adjusting range voltage pin 50	$V_{37-35(rms)}$ = 10 mV	–1.8	–	+1.8	V
V_{38-4}	internal bias voltage		–	2.6	–	V
$\Delta V_{50-4}/\Delta V_{38-4}$	adjusting gain		–	–0.9	–	
R_{i38}	input resistance pin 38		–	80	–	kΩ
Multi-path detector						
f_{MP}	multi-path detector band-pass centre frequency		–	20	–	kHz
B_{MP}	band-pass bandwidth		7	–	–	kHz
Reference voltage						
$V_{o(21-4)}$	output voltage	I_{21} = –1 mA	4.5	5.1	5.7	V
$\Delta V_{21-4}/(V_{21-4}\Delta T)$	temperature dependence		–	3.3	–	mV/VK
I_{o21}	output current pin 21		–	–	1	mA
AM-IF path; see Fig.9 and notes 2 and 3						
$V_{22-23max(p-p)}$	maximum output voltage between pins 22 and 23 (peak-to-peak value)		12	15	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{bias(22-23)}$	mixer bias current pins 22 and 23		5	6	7	mA
$I_{LI(22-23)}$	mixer leakage current pins 22 and 23	in FM position	–	–	2	µA
$I_{22IF2}/V_{27-24IF1}$	conversion gain		2.2	2.7	3.4	mS
$R_{i(27-24)}$	input resistance between pins 27 and 24		300	330	360	Ω
$C_{i(27-24)}$	input capacitance between pins 27 and 24		–	5	8	pF
$R_{o(22-23)}$	output resistance between pins 22 and 23		10	20	–	kΩ
$C_{o(22-23)}$	output capacitance between pins 22 and 23		–	5	10	pF
IP3	third order intermodulation		–	137	–	dBµV
AM DETECTOR; see notes 4 and 5						
$V_{48-4(rms)}$	AF output level (RMS value)	R_{L48} > 500 kΩ; 100 µV ≤ V_{33-34} ≤ 300 mV	190	240	290	mV
$V_{33-34(rms)}$	sensitivity voltage (RMS value)	$\frac{S+N}{N}$ = 26 dB	–	50	75	µV
		$\frac{S+N}{N}$ = 46 dB	–	200	400	µV
	AM-IF_2 minimum input voltage (RMS value)	THD ≤ 5%; m = 0.8	–	–	100	µV
	AM-IF_2 maximum input voltage (RMS value)	THD ≤ 5%; m = 0.8	800	–	–	mV
$R_{i(33-34)}$	IF_2 input resistance between pins 33 and 34		1.8	2.0	2.2	kΩ
$C_{i(33-34)}$	IF_2 input capacitance between pins 33 and 34		–	10	15	pF
R_{o48}	output resistance pin 48		27	33	39	kΩ
C_{o48}	output capacitance pin 48		–	–	10	pF
$\frac{S+N}{N}$	signal-plus-noise-to-noise ratio		54	60	–	dB
THD	total harmonic distortion	m = 0.8; 300 µV ≤ V_{33-34} ≤ 200 mV	–	1.5	3.0	%

Notes to the Characteristics

1. For typical adjusting range see Fig.8.
2. f_{IF1} = 10.7 MHz; f_{IF2} = 450 kHz for AM mixer.
3. The AM oscillator signal is generated by division of the 61.5 MHz crystal oscillator. Two divider ratios programmable by the I^2C-bus: division by 6 (AM-IF_1 = 10.7 MHz); division by 2 (AM-IF_1 = 30 MHz).
4. For typical AM level curve see Fig.10.
5. For AM detector; f_{AMIF2} = 450 kHz; f_{mod} = 400 Hz; m = 30%.

ADCs CHARACTERISTICS FOR LEVEL AND MULTI-PATH VOLTAGES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADC for FM level information; note 1						
ΔV_{37-35}	analog-to-digital conversion step size for V_{37-35}		2	4	8	dB/step
ΔV_{37-35}	analog-to-digital conversion level range for V_{37-35}		43	56	69	dB
FM STOP						
ΔV_{stop}	variation of stop level as function of V_{42-4}		–	16	–	dB/V
ADC for AM level information; note 2						
ΔV_{33-34}	analog-to-digital conversion step size for V_{33-34}		2	4	8	dB/step
ΔV_{33-34}	analog-to-digital conversion level range for V_{33-34}		43	56	69	dB
AM STOP						
ΔV_{stop}	variation of stop level as a function of V_{43-4}		–	16	–	dB/V
ADC for multi-path information; note 3						
m	multi-path conversion	step 0	–	–	5	%
		step 1	–	15	–	%
		step 2	–	22	–	%
		step 3	–	28	–	%
		step 4	–	34	–	%
		step 5	–	40	–	%
		step 6	–	46	–	%
		step 7	–	52	–	%

Notes

1. The FM level information V_{50-3} is analog-to-digital converted with 4 bits.
2. The AM level information V_{49-4} is analog-to-digital converted with 4 bits.
3. The multi-path information V_{40-4} is analog-to-digital converted with 3 bits covering an IF_2 amplitude modulation range $m \leq 0.6$; f_{mod} = 20 kHz.

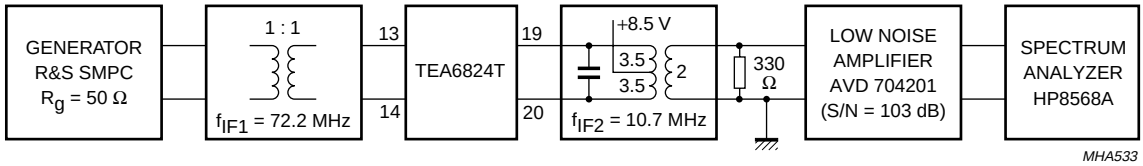


Fig.3 Test circuit FM mixer.

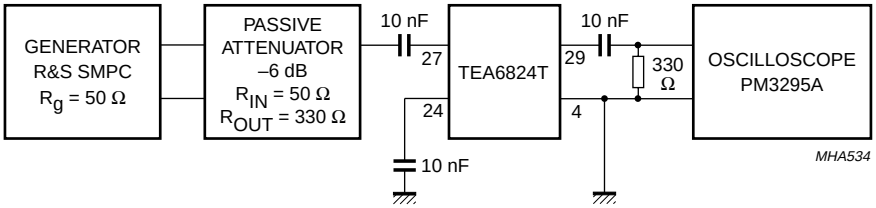


Fig.4 Test circuit IF-amplifier.

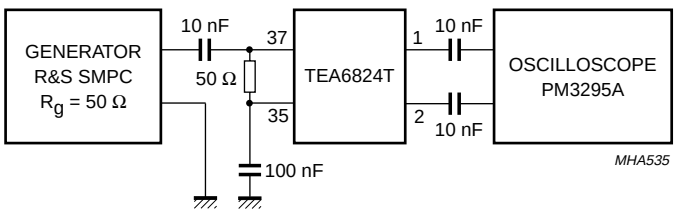
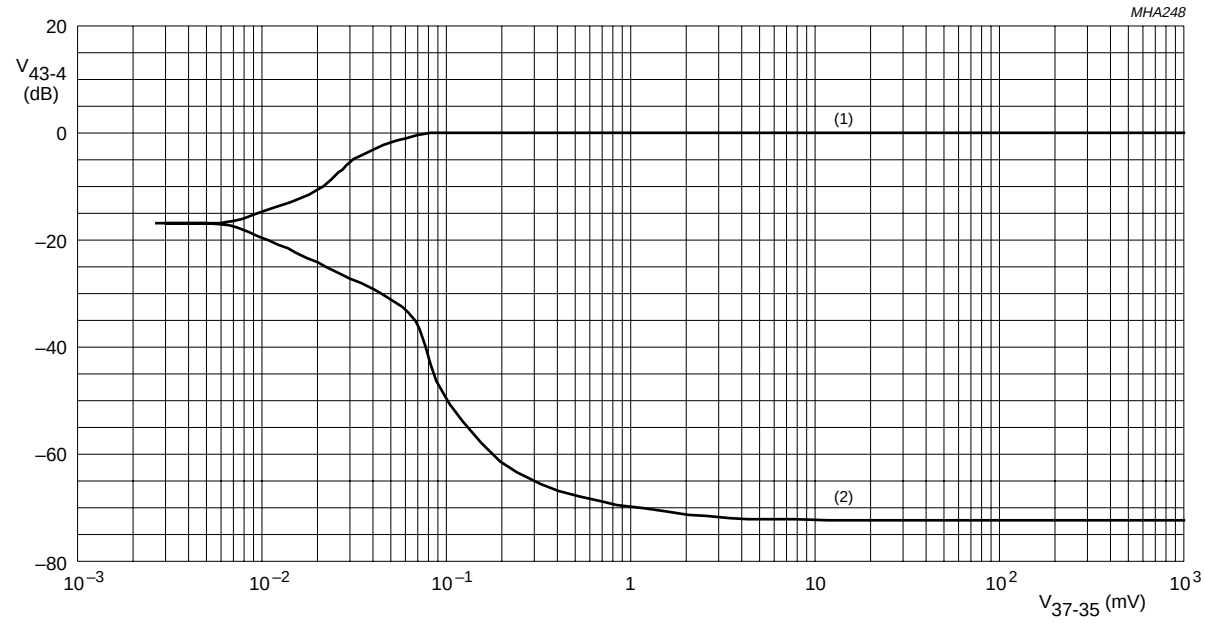
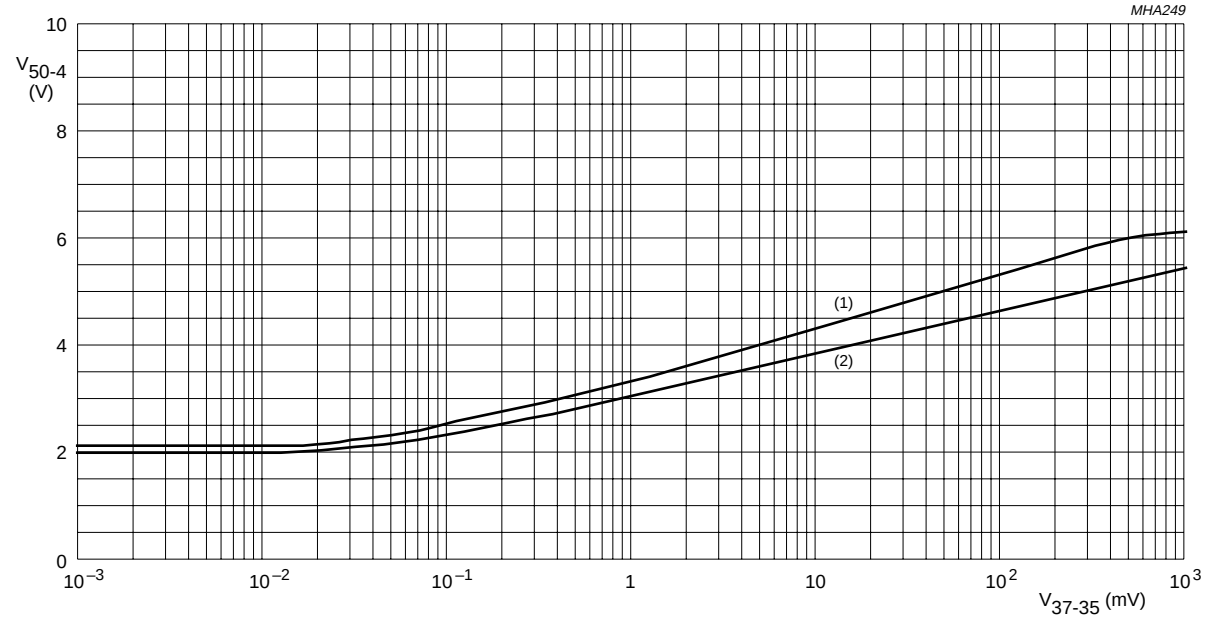


Fig.5 Test circuit limiter gain.



(1) AF: f_{IF} = 10.7 MHz; deviation = 22.5 kHz; f_{mod} = 1 kHz.
(2) Noise: unweighted B = 250 Hz to 15 kHz with de-emphasis 50 μs.

Fig.6 Signal and noise of unmuted MPX voltage.



(1) Temperature compensation off.
(2) Temperature compensation on.

Fig.7 Unweighted voltage level (typical curve).

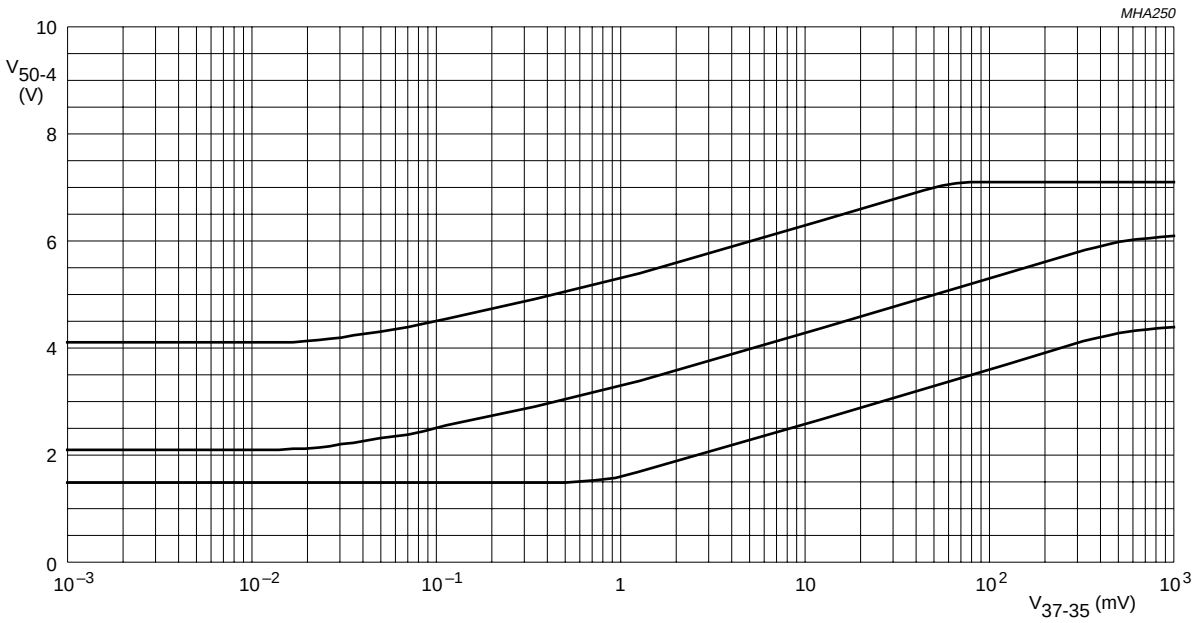


Fig.8 Adjustment range of unweighted voltage level.

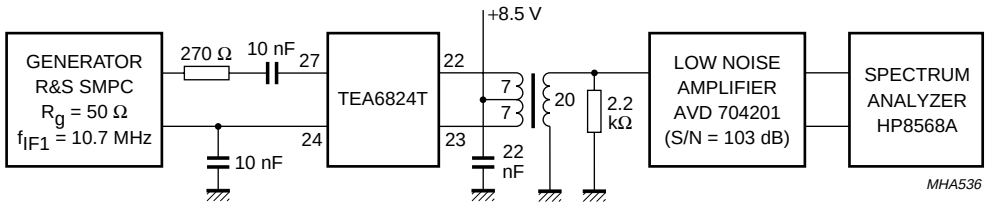
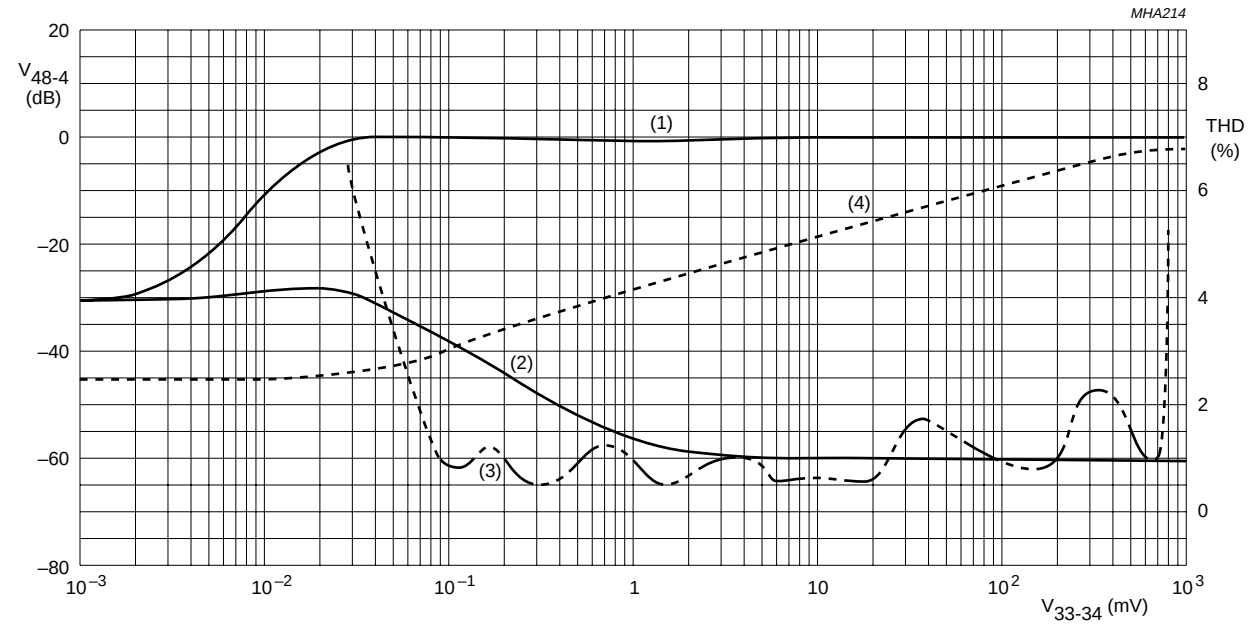


Fig.9 Test circuit AM mixer.



(1) AF: f = 450 kHz; m = 30%; f_{mod} = 400 Hz. (2) Noise: unweighted B = 250 Hz to 15 kHz.
(3) THD m = 80%. (4) AM level voltage.

Fig.10 Signal, noise and distortion of AM AF output voltage and AM voltage level (typical curve).

I²C-BUS AND I²C-BUS CONTROLLED FUNCTIONS

I²C- bus specification

The standard I²C-bus specification is expanded by the following definitions.

Structure of the I²C-bus logic: slave transceiver with auto increment and expansion to switch a direct transfer of all transmissions to an output for the radio front-end IC TEA6810T.

Sub-addresses are not used.

DATA TRANSFER FOR THE TEA6824T

Data sequence:

- Address
- Byte 1
- Byte 2.

The data transfer may only be in this order. The transfer direction of the data bytes is defined by the LSB of the address.

The data becomes valid at the output of the internal latches with the acknowledge of each byte. A STOP condition after any byte can shorten transmission times.

When writing to the transceiver by using the STOP condition before completion of the whole transfer:

- The remaining bytes will contain the old information
- If the transfer of a byte was not completed, this byte is lost and the previous information is available.

DATA TRANSFER TO AN OUTPUT OF THE FRONT-END IC

A data bit in the transceiver of the TEA6824T enables or disables a direct transfer of all transmissions to an interface stage for the front-end IC.

For a transmission to the front-end IC the address and the data format of the front-end IC has to be used.

Remark: The pull-up resistors for the front-end interface (pins 6 and 7) should not be connected to the +5 V supply voltage of the front-end IC, otherwise a bus pull-down (pin 53) can occur during switching off the front-end supply when the interface stage is enabled.

DATA TRANSFER TO THE IF IC

Data transfer to the IF IC (TEA6824T) is independent of the state of interface stage for the front-end IC.

Table 1 Structure of the I²C-bus

DESCRIPTION	SPECIFICATION
Bus address of the TEA6824T	1100001X
Subaddress	not used
Hardware (pin) programmable address bits	not available
Default settings by power-on reset	data byte 1 bits 4 to 7 are set to logic 0; all other bits are random

Table 2 Data to be received by the IC for data byte 1

BIT	DESCRIPTION	RESULT
0	not used	–
1	LSB reference frequency for synthesizer	–
2	reference frequency for synthesizer	–
3	MSB reference frequency for synthesizer	–
4	not used	–
5	not used	–
6	not used	–
7	I²C-bus to front-end ENABLED	bit 7 = 1
	I²C-bus to front-end DISABLED	bit 7 = 0

Table 3 Reference frequency setting in byte 1; see Table 1

BIT 3	BIT 2	BIT 1	FREQUENCY SETTING
0	0	0	3 kHz
0	0	1	5 kHz
0	1	0	10 kHz
0	1	1	15 kHz
1	0	0	25 kHz
1	0	1	50 kHz
1	1	0	not defined
1	1	1	not defined

Table 4 Data to be received by the IC for data byte 2

BIT	DESCRIPTION	RESULT
0	AM/FM; AM mode	bit 0 = 0
	AM/FM; FM mode	bit 0 = 1
1	divider for AM mixer; divide-by-2	bit 1 = 0
	divider for AM mixer; divide-by-6	bit 1 = 1
2	measure time IF-count; 40 ms	bit 2 = 0
	measure time IF-count; 4 ms	bit 2 = 1
3	not used	
4	IF-prescaler division rate; divide-by-200	bit 4 = 0
	IF-prescaler division rate; divide-by-25	bit 4 = 1
5	not used	
6	temperature compensation of unweighted voltage level; temperature coefficient as specified in Chapter “Characteristics”	
	temperature compensation off	bit 6 = 0
	temperature compensation on	bit 6 = 1
7	not used	

Table 5 Data to be transmitted by the IC for data byte 1; note 1

BIT	DESCRIPTION
0	bit 1 level information
1	bit 2 level information
2	MSB (bit 3) level information
3	LSB multi-path information
4	multi-path information
5	MSB multi-path information
6	not used
7	LSB (bit 0) level information

Note

1. The analog-to-digital conversion for multi-path and level will be performed during a transmission of any address to the I²C-bus.

Table 6 Data to be transmitted by the IC for data byte 2

BIT	DESCRIPTION
0	LSB of the IF-counter
1	IF-counter
2	IF-counter
3	IF-counter
4	IF-counter
5	IF-counter
6	IF-counter
7	MSB of the IF-counter

REFERENCED FREQUENCY GENERATION

Table 7 Division ratios

DIVISION RATIO	REFERENCE FREQUENCY (kHz)(1)
20500	3
12300	5
6150	10
4100	15
2460	25
1230	50

Note

1. All specified frequencies are valid for a crystal oscillator frequency of 61.5 MHz.

Table 8 Output signal of reference frequency divider

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{10\text{-}11(p\text{-}p)}$	differential output voltage between pins 10 and 11 (peak-to-peak value)	0.3	0.4	0.5	V
$V_{10\text{-}4(p\text{-}p)}$; $V_{11\text{-}4(p\text{-}p)}$	single-ended output voltage between pins 10 and 4 and between pins 11 and 4 (peak-to-peak value)	0.15	0.2	0.3	V
$C_{10\text{-}4}$; $C_{11\text{-}4}$	output capacitance between pins 10 and 4 and between pins 11 and 4	–	–	4	pF
$R_{10\text{-}52}$; $R_{11\text{-}52}$	output resistance between pins 10 and 52 and between pins 11 and 52	800	1000	1200	Ω

IF-COUNTER

Table 9 IF-counter sensitivity

SYMBOL	PARAMETER	CONDITIONS	MIN.	UNIT
$V_{33\text{-}34}$	IF-counter sensitivity	AM mode; m = 0	200	μV
$V_{37\text{-}35}$	IF-counter sensitivity	FM mode	200	μV

AM and FM counting windows are 4 or 40 ms. AM counting resolution is 250 or 25 Hz. FM counting resolution is 5 kHz, 625 Hz, 50 kHz or 6.25 kHz. AM-IF-prescaler is divisible by 1. FM-IF-prescaler is divisible by 25 or 200.

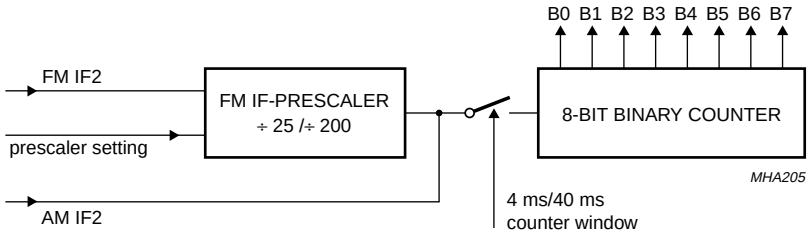


Fig.11 IF-counter structure.

IF-counter read out

IF-counter read out as a function of FM or AM position, counter window and prescaler setting

FM/AM	PRESCALER RATIO	WINDOW (ms)	f_{IF} (kHz)	READ OUT	RESOLUTION (Hz/count)	RANGE (kHz)	
						MIN.	MAX.
FM	200	4	10700	D6H	50000	4300	17050
FM	200	40	10700	5CH	5000	10065	11335
FM	25	4	10700	B0H	6250	9906.25	11493.75
FM(1)	25	40	10700	E0H	625	10620.63	10779.38
AM	1	4	450	08H	250	418.25	481.75
AM(1)	1	40	450	50H	25	446.83	453.18

Note

1. In position FM with a prescaler ratio of 25, counter window of 40 ms and in position AM with 40 ms counter window ambiguous counting results within the IF filter bandwidth are obtained. The counting range is 127 counts above and 127 counts below the nominal IF of 10.7 MHz for FM and 450 kHz for AM.

The IF-count windows are valid for a crystal oscillator frequency of 61.5 MHz.

The FM/AM switching is carried out by bit 0 of byte 2 of the received data of the IC.

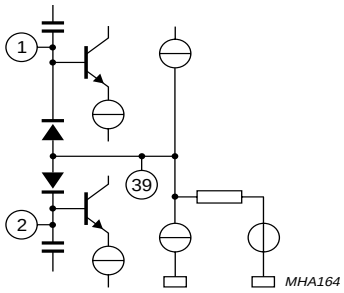
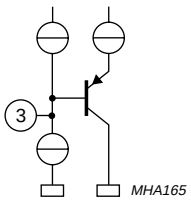
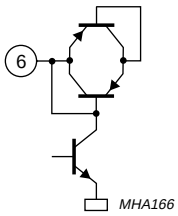
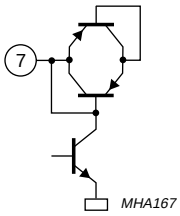
The IF-counter operates continuously.

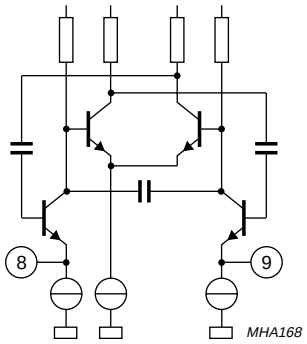
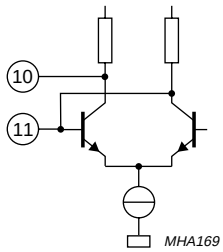
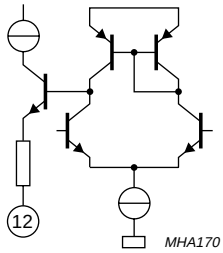
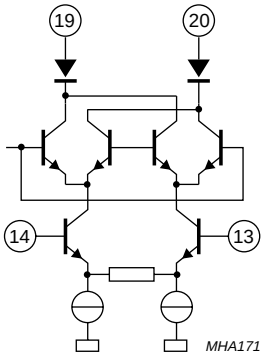
The IF-counter and window counter will be reset when the I^2C-bus logic detects the address of the IC. This disables changes in the latches for the IF-counter, while reading this value. If the transmission to the front-end IC is disabled after the synthesizer loop of the TEA6810T front-end IC has locked to a new frequency, the IF-counter will be available after the set measuring time.

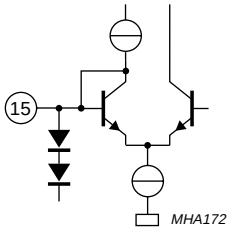
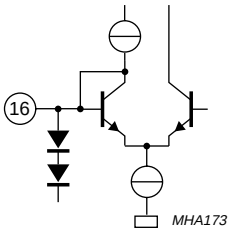
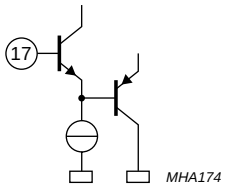
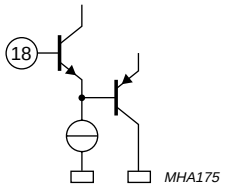
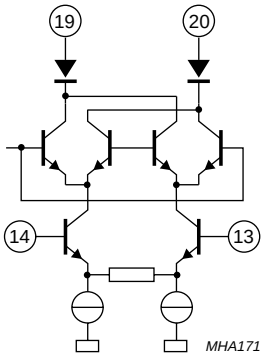
The IF-counter starts at 0. The IF-counter output are the 8 least significant bits of the counting result.

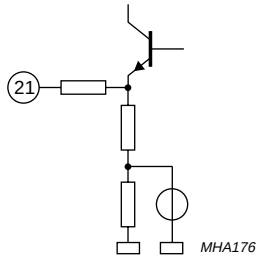
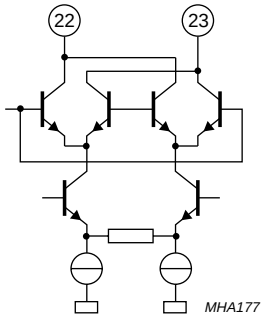
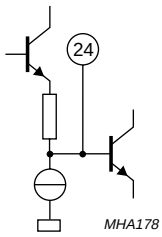
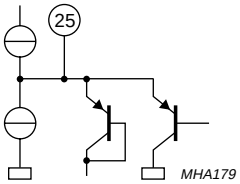
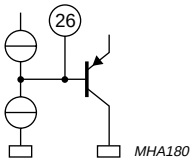
INTERNAL CIRCUITRY

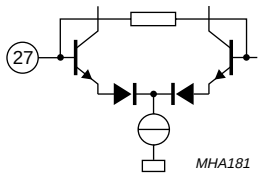
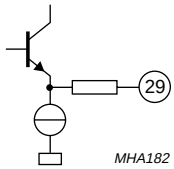
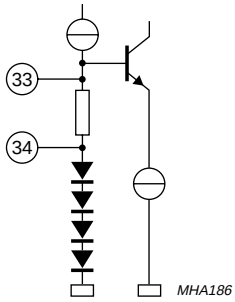
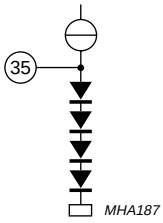
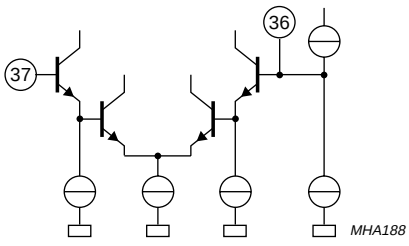
Table 10 Equivalent pin circuits and pin voltages

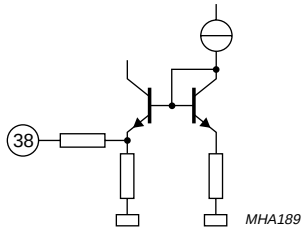
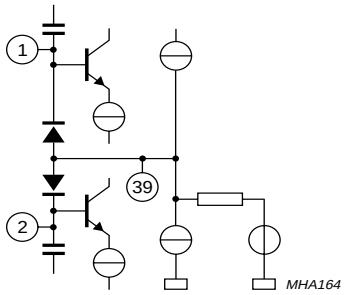
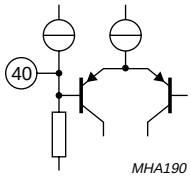
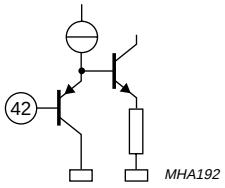
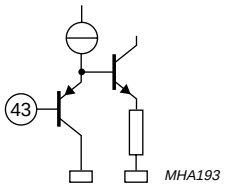
PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
1	QDET1	4.0	4.0	
2	QDET2	4.0	4.0	
3	REFIN1	0	0	
4	AGND	–	–	
5	V_{DDA1}	5.0	5.0	
6	HFBUS1	5.0	5.0	
7	HFBUS2	5.0	5.0	

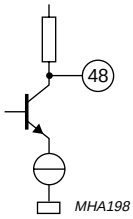
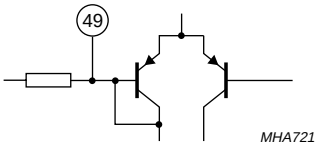
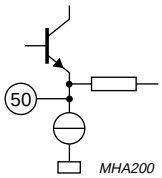
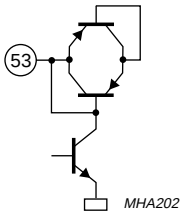
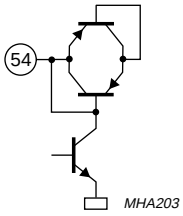
PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
8	XTAL1	4.1	4.1	
9	XTAL2	4.1	4.1	
10	$f_{ref(p)}$	4.9	4.9	
11	$f_{ref(n)}$	4.9	4.9	
12	I_{ref}	4.3	4.3	
13	FMIF1IN1	2.3	2.3	
14	FMIF1IN2	2.3	2.3	

PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
15	REFIN2	4.9	4.9	
16	REFIN3	4.9	4.9	
17	REFIN4	4.9	4.9	
18	REFIN5	4.9	4.9	
19	FMIF2OUT1	8.5	8.5	
20	FMIF2OUT2	8.5	8.5	

PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
21	V_{ref}	5.1	5.1	
22	AMIF2OUT1	8.5	8.5	
23	AMIF2OUT2	8.5	8.5	
24	FMAMDEC	3.0	2.5	
25	DEC1	2.8 to 7.0	2.8 to 7.2	
26	DEC2	0.4	0.4 to 7.0	

PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
27	FMAM10.7	3.0	2.5	
28	V_{DDA2}	8.5	8.5	
29	FMIFAMPOUT	6.0	6.0	
30	n.c.			
31	n.c.			
32	n.c.			
33	AMIF2IN1	2.7	0.7	
34	AMIF2IN2	2.7	0.7	
35	FMIN2	0.7	2.7	
36	DCFEED	2.7	2.7	
37	FMIN1	0.7	2.7	

PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
38	LEVELADJ	2.6	2.6	
39	C_{AFC}	1.0 to 2.2	1.0 to 7.0	
40	MPBUF	0.7 to 6.0	0.7 to 6.0	
41	n.c.			
42	FMSTOP	0 to 5.2	0 to 5.2	
43	MPXOUT	0 to 5.2	3.0	
44	n.c.			
45	n.c.			
46	n.c.			
47	n.c.			

PIN	SYMBOL	DC VOLTAGE (V)		EQUIVALENT CIRCUIT
		AM	FM	
48	AMAFOUT	3.7	4.8	
49	DEC3	1.0 to 5.5	1.0 to 5.5	
50	LEVELUNWEIG	1.0 to 7.0	1.0 to 7.0	
51	n.c.			
52	V_{DDD}	5.0	5.0	
53	SDA	5.0	5.0	
54	SCL	5.0	5.0	
55	DGND	0	0	
56	V_{DDA3}	8.5	8.5	

APPLICATION INFORMATION

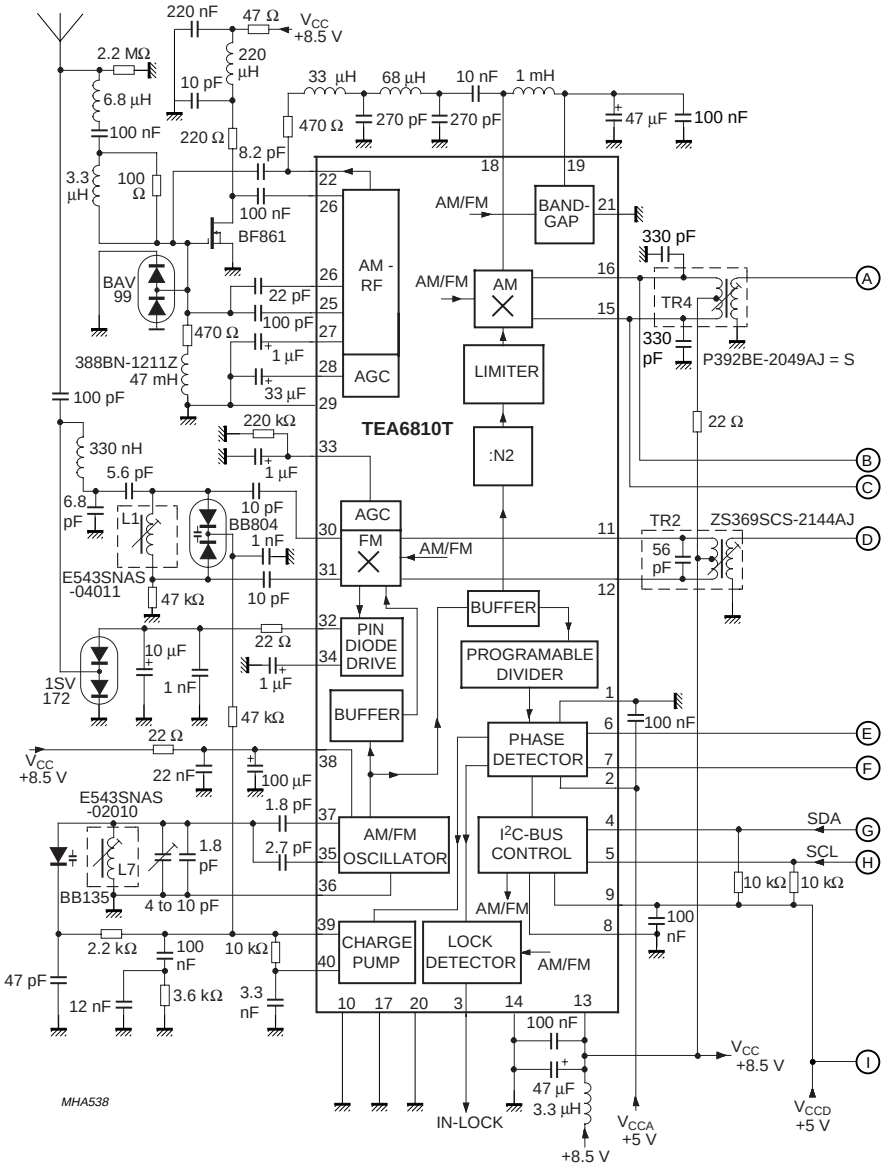


Fig.12 Application diagram (continued in Fig.13).

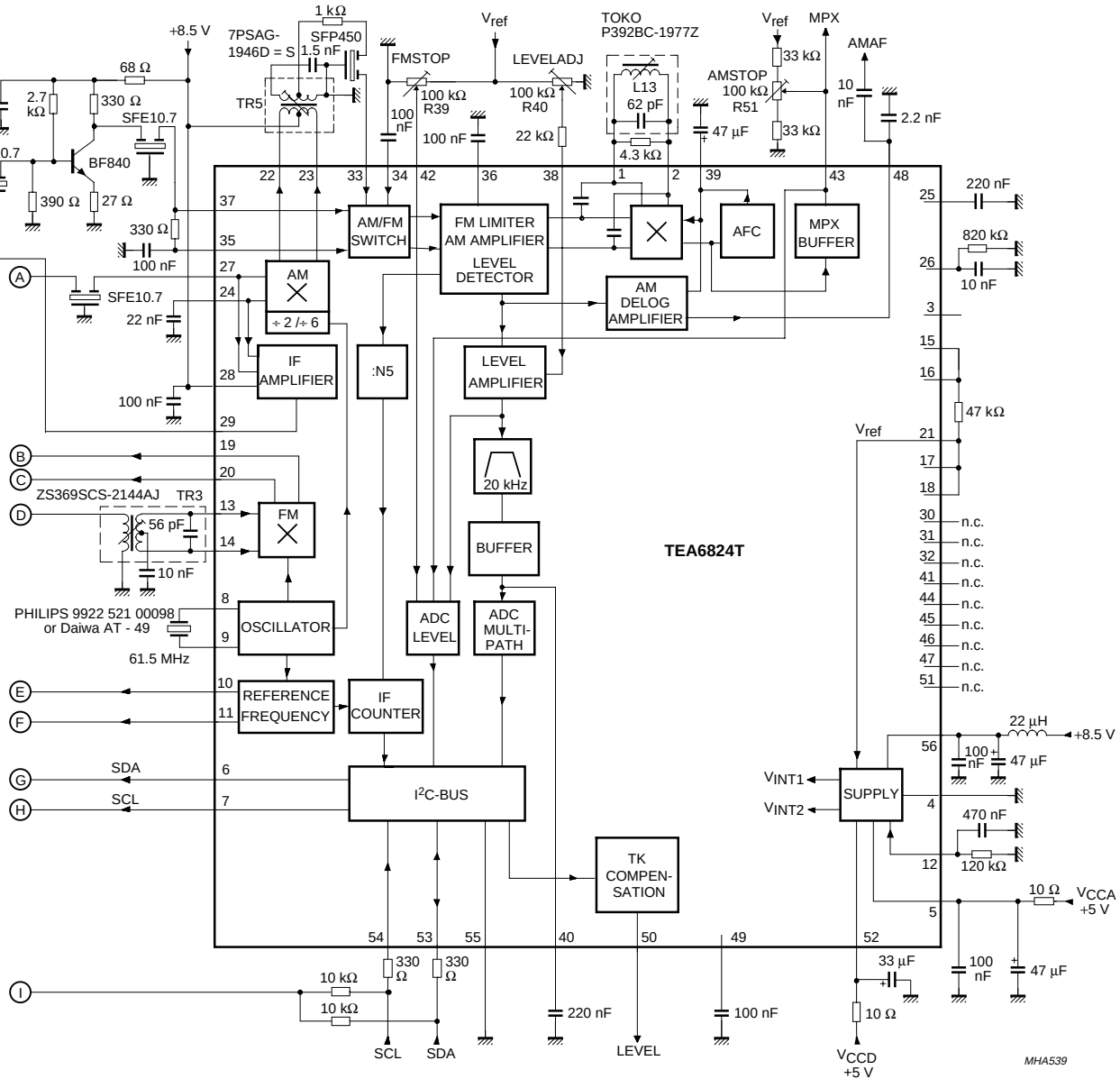


Fig.13 Application diagram (continued from Fig.12).

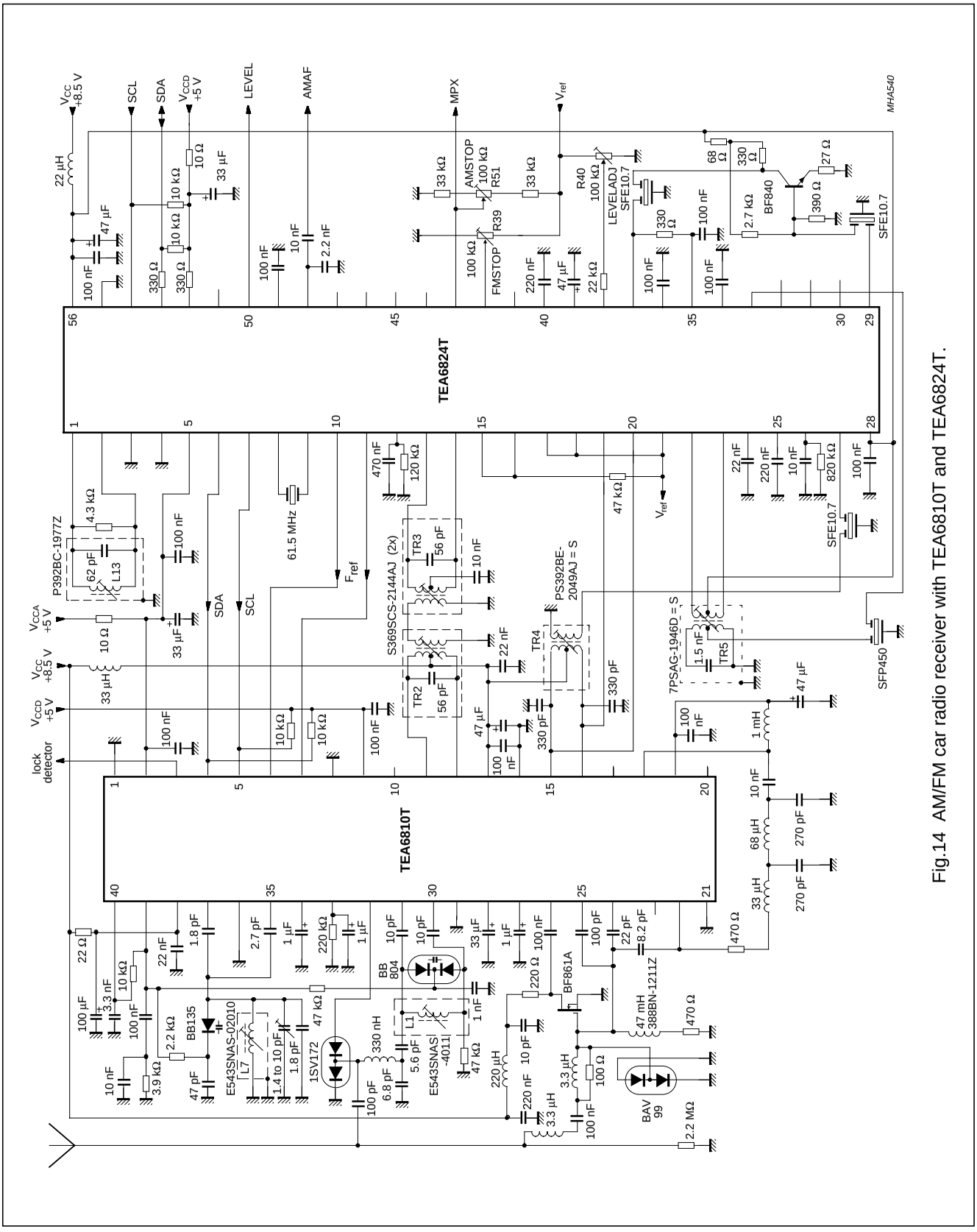
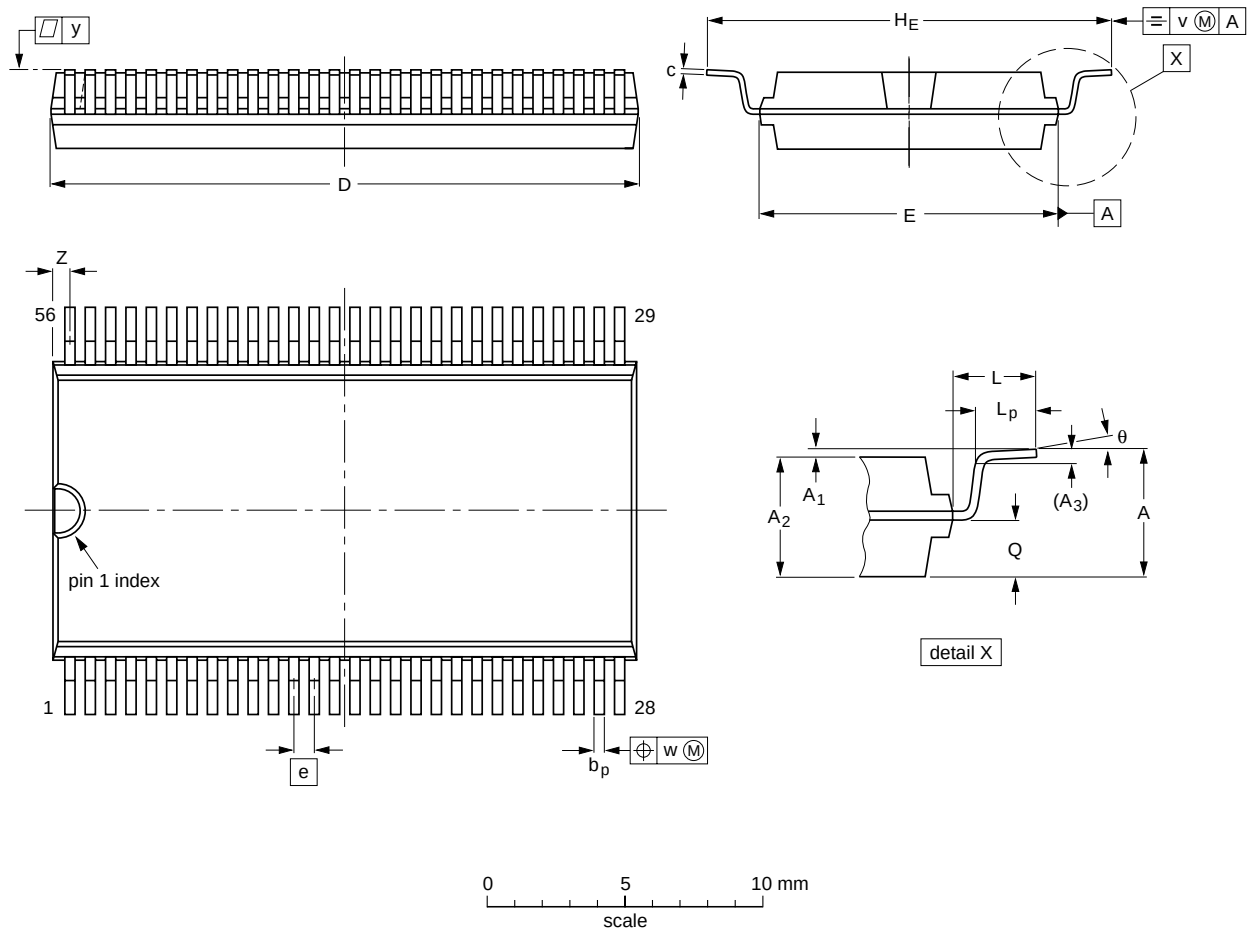


Fig.14 AM/FM car radio receiver with TEA6810T and TEA6824T.

PACKAGE OUTLINE

VSO56: plastic very small outline package; 56 leads; face down **SOT190-2**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	3.3	0.3 0.1	3.0 2.8	0.25	0.42 0.30	0.22 0.14	21.65 21.35	11.1 11.0	0.75	15.8 15.2	2.25	1.6 1.4	1.45 1.30	0.2	0.1	0.1	0.90 0.55	7^o 0^o
inches	0.13	0.012 0.004	0.12 0.11	0.01	0.017 0.012	0.0087 0.0055	0.85 0.84	0.44 0.43	0.0295	0.62 0.60	0.089	0.063 0.055	0.057 0.051	0.008	0.004	0.004	0.035 0.022	

Note

1. Plastic or metal protrusions of 0.3 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT190-2						~~96-04-02~~ 97-08-11

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all VSO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all VSO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

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