



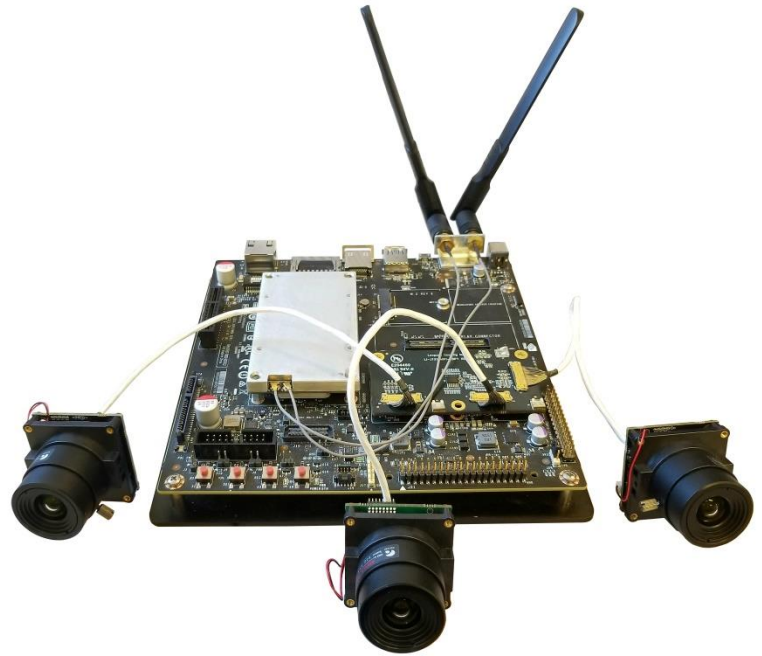
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LI-JETSON-KIT- RAA462113CS-X Data Sheet

Key Features

- Compatible with Nvidia® Jetson™ TX1/TX2 Developer Kit
- MIPI CSI-2 interface
- Support up to three cameras
- Renesas 8MP CMOS Image Sensor RAA462113
- Effective pixels: 3872H x 2192V
- Pixel size: 1.85 um x 1.85 um
- Color camera
- High sensitivity
- Low noise
- Length of the I-PEX cable: 300mm
- Support multiple length cables
- Support CS lens (Lens not included)
- 650 nm IR cut filter included
- Provide customization services
- Part#:

- (1 cam) **LI-JETSON-KIT-RAA462113CS**
- (2 cam) **LI-JETSON-KIT-RAA462113CS-D**
- (3 cam) **LI-JETSON-KIT-RAA462113CS-T**



BOM

Nvidia TX1/TX2 Development Kit not included
CS lens not included

#	Items	QTY
1	LI-JTX1-MIPI-ADPT	1
2	LI-RAA462113-MIPI-CS	1,2 or 3
3	FAW-1233-03 cable	1,2 or 3



Leopard Imaging Inc.

48820 Kato Road, Suite 100B, Fremont, CA 94538, USA
Phone: +1-408-263-0988
Fax: +1-408-217-1960
Email: sales@leopardimaging.com
Website: www.leopardimaging.com

LI-JETSON-KIT- RAA462113CS

BOM

#	Items	QTY
1	LI-JTX1-MIPI-ADPT	1
2	LI- RAA462113-MIPI-CS	1
3	FAW-1233-03 cable	1



LI-JETSON-KIT- RAA462113CS-D

BOM

#	Items	QTY
1	LI-JTX1-MIPI-ADPT	1
2	LI- RAA462113-MIPI-CS	2
3	FAW-1233-03 cable	2



LI-JETSON-KIT- RAA462113CS-T

BOM

#	Items	QTY
1	LI-JTX1-MIPI-ADPT	1
2	LI-RAA462113-MIPI-CS	3
3	FAW-1233-03 cable	3

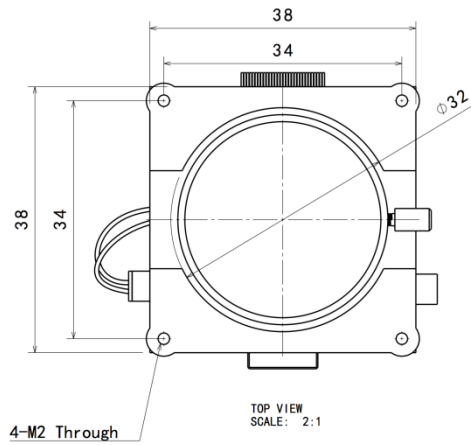


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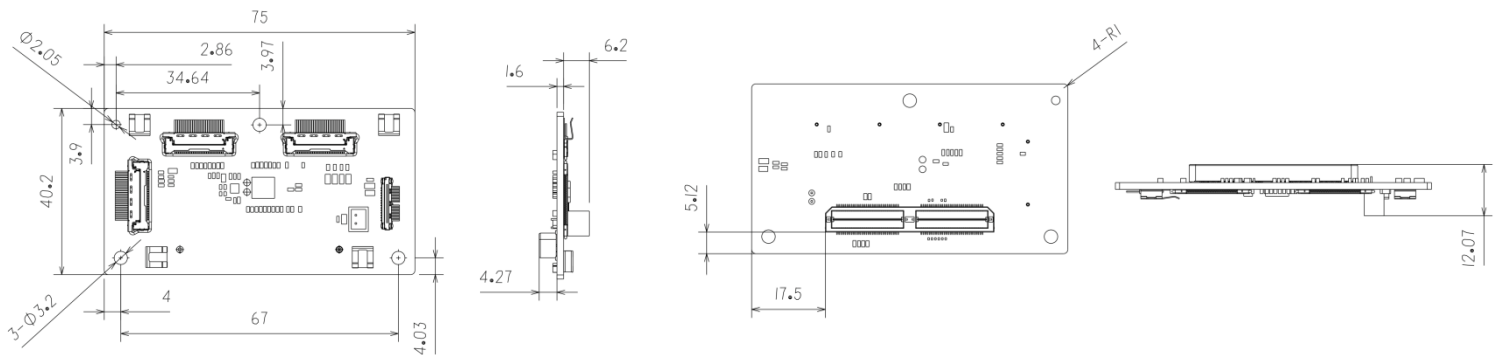
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Dimensions

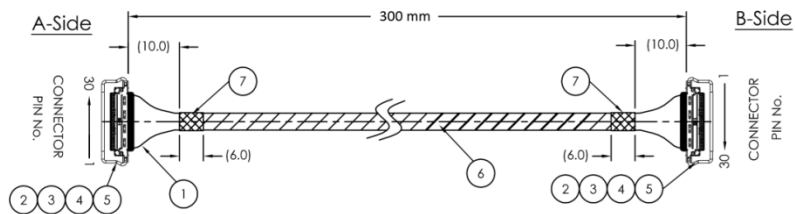
LI-RAA462113-MIPI-CS



LI-JTX1-MIPI-ADPT



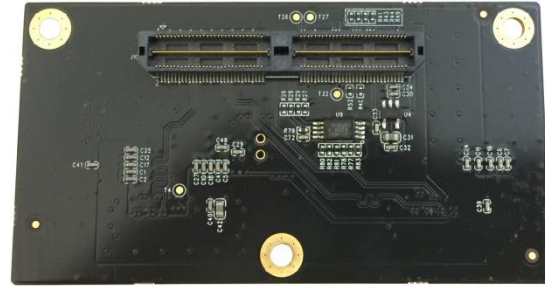
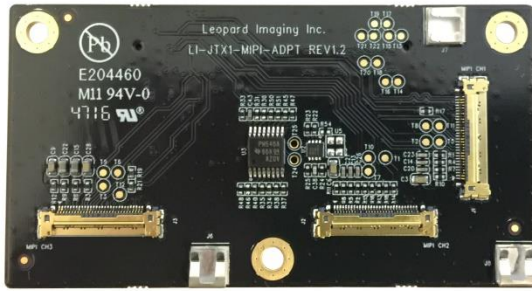
FAW-1233-03



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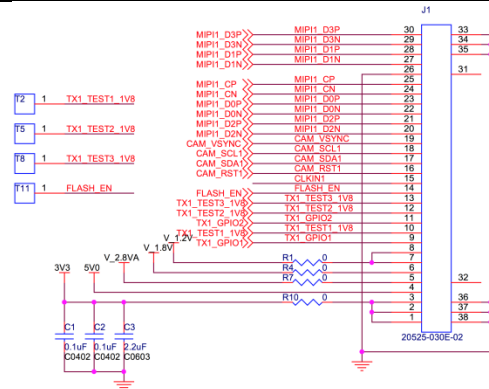
LI-JTX1-MIPI-ADPT



Interfaces

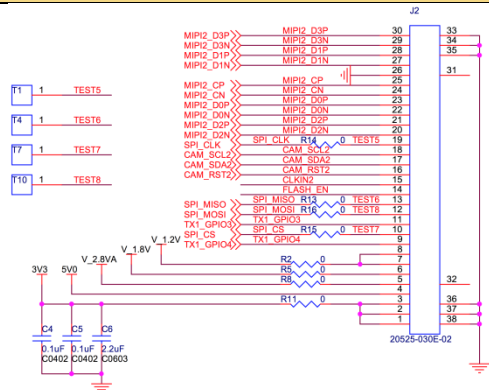
Interface J1

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



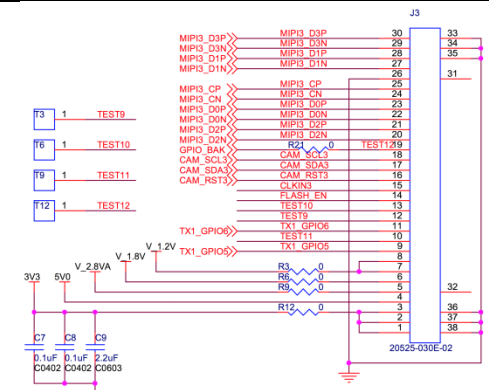
Interface J2

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



Interface J3

- Part#: 20525-030E-02C
- Number of Positions: 30
- Pitch: 0.4mm
- Mating I-PEX cable: FAW-1233-03 (300mm)



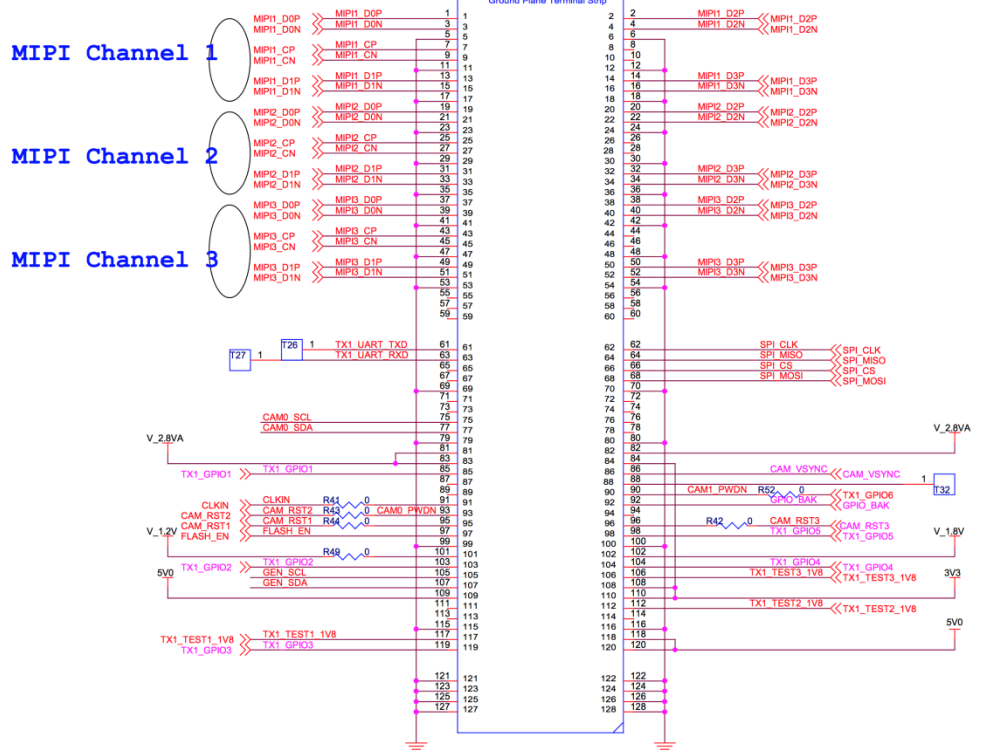
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Interface J10

- Part#: QTH-060-01-L-D-A
- Number of Positions: 120
- Number of Rows: 2
- Pitch: 0.5 mm

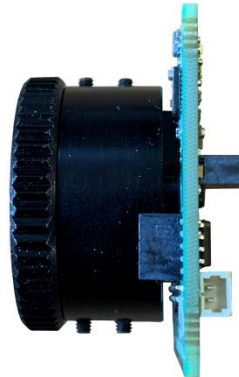
Vertical Mating connector of Jetson TX1 J22 QTH-060-01-D-A



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LI-RAA462113-MIPI-CS



Camera Spec	
Image Sensor	Renesas 8MP CMOS Image Sensor RAA462113
Optical format	1/1.9"
Number of effective pixels	3872 (H) x 2192 (V)
Pixel size	1.85um (H) x 1.85um (V)
Color or Mono	Color
Interface	MIPI interface
Lens mount	CS (lens not included)
Weight (without lens)	20 g
Interfaces	
Interface J4: <ul style="list-style-type: none"> Part#: 20525-030E-02C Number of Positions: 30 Pitch: 0.4mm Mating I-PEX cable: FAW-1233-03 (300mm) 	
Interface J8: <ul style="list-style-type: none"> Part#: 1734829-2 Number of Positions: 2 Pitch: 1.25mm 	
Interface J2: <ul style="list-style-type: none"> Part#: 20021321-00010C4LF Number of Positions: 10 Pitch: 1.27mm 	



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Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit
VDD_PX, VDD_RG, VDD_AD_N, VDD_AD_S, VDD_AD_V VDD_AD_C, VDD_AN, VCAP_VTXH, VREF, IREF, VCAP_VDRS VCAP_PX_N, VCAP_PX_, VDD_IO_N, VDD_IO_I2C SDA, SCL, SCE, SCK, SDI, CM4W, CMHP, CMHV CLK_RF1, RSTN, TRIG, SDO, SACK, SYNC ATEST_VDC, ATEST_VWC, ATEST_VGC, ATEST_DAC DTEST_ED, SCAN_MODE, CLK_RF2, DTEST_M1, DTEST_M2 TEST_NC1, TEST_NC2, TEST_NC3	AVH	-0.3	3.6V	V
VCAP_VTXL	AVN	-0.9	0.3	V
VDD_DG, VDD_DG_PL1, VDD_DG_PL2, VDD_DG_SL D*P, D*N, {*: Lane Number (1-8)}, CK1P, CK1N, CK2P, CK2N	AVL	-0.3	1.32	V
Storage temperature	Tstg	-20	110	°C
Operating temperature	Ta	-20	85	°C
Storage and operating humidity	-	No condensation		%

Power supply voltage

Item	Symbol	Min	Typ	Max	Unit	Condition
2.8V power supply (analog) VDD_PX, VDD_RG VDD_AD_N, VDD_AD_S VDD_AD_V, VDD_AD_C VDD_AN, VCAP_VTXH	VDA28	2.66	2.80	2.94	V	
1.8V power supply (digital) VDD_IO_N, VDD_IO_I2C	VDD18	1.71	1.80	1.89	V	
1.8V power supply (analog) VREF	VDA18	1.71	1.80	1.89	V	
1.2V power supply (digital) VDD_DG	VDD12	1.14	1.20	1.26	V	
1.2V power supply (analog) VDD_DG_PL1, VDD_DG_PL2 VDD_DG_SL	VDA12	1.14	1.20	1.26	V	

Current consumption

Ta=25°C, power supply voltage: typical if not specified

Item	Symbol	Min	Typ	Max	Unit	Condition
2.8V power supply (analog) VDD_PX, VDD_RG VDD_AD_N, VDD_AD_S VDD_AD_V, VDD_AD_C VDD_AN, VCAP_VTXH	IVDA28	-	220	300	mA	
1.8V power supply (digital) VDD_IO_N, VDD_IO_I2C	IVDD18	-	0.1	4	mA	
1.8V power supply (analog) VREF	IVDA18	-	0.1	1	mA	
1.2V power supply (digital) VDD_DG	IVDD12	-	610	900	mA	
1.2V power supply (analog) VDD_DG_PL1, VDD_DG_PL2 VDD_DG_SL	IVDA12	-	12	20	mA	

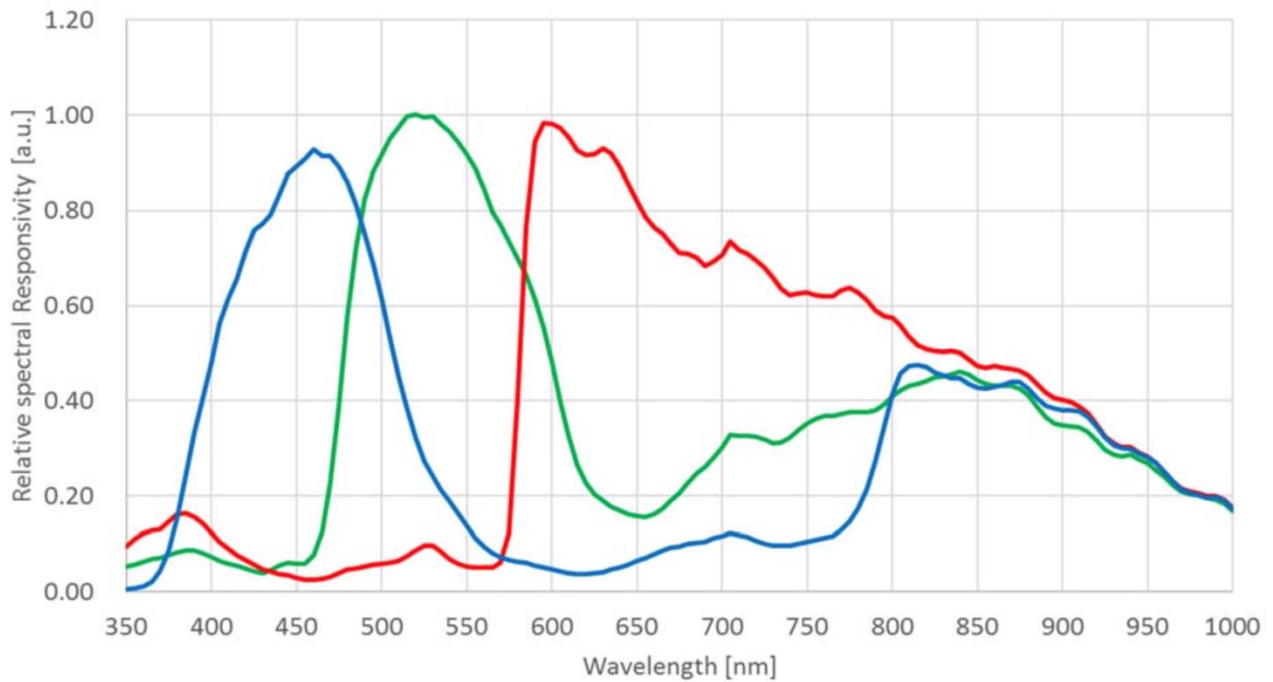


Image Sensor Characteristics

Tj=60C, power supply voltage: typical if not specified

Item	Symbol	Min	Typ	Max	Unit	Condition
Sensitivity		(2100)*	-	-	LSB	
Sensitivity ratio R/G		-	(45)	-	%	
Sensitivity ratio B/G		-	(73)	-	%	
Maximum output		(4000)	-	-	LSB	
Dark Shading		-	-	(17)*	LSB	
Shine shot detect at Dark		-	-	3996	pixel	
Shine shot detect at Bright		-	-	3996	pixel	
Total spot defect		-	-	3996	pixel	
pixel defect pattern		-	-	0	pixel	

* The values given in parentheses are supposed to change w/o notice. (These values shall be determined at ES)



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DC Characteristics

Digital input pin: CLK_RF1, RSTN, TRIG, CM4W, CMHP, CMHV

Digital output pin: SYNC, SACK

Ta=25°C, power supply voltage: typical if not specified

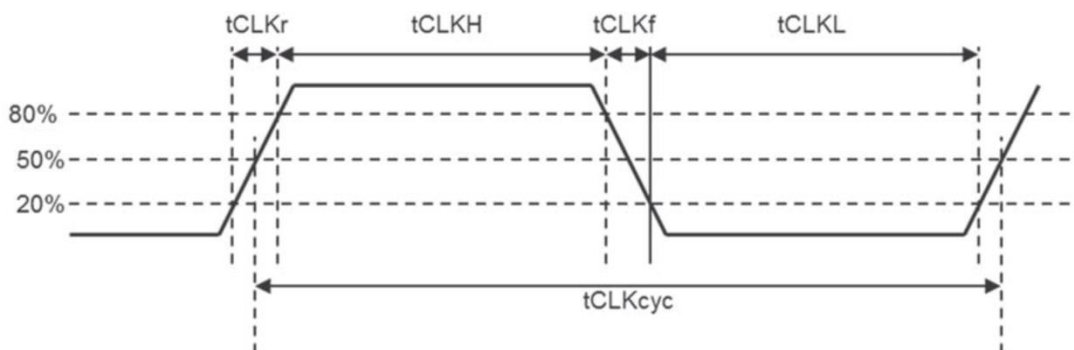
Item	Symbol	Min	Typ	Max	Unit	Condition
Digital Input Voltage at High	VIH	VDD18 x0.7		VDD18 +0.2	V	
Digital Input Voltage at Low	VIL	-0.2		VDD18 x0.2	V	
Digital Output Voltage at High	VOH	VDD18 -0.2		-	V	IOH=1mA
Digital Output Voltage at Low	VOL	-		0.20	V	IOL=1mA

AC characteristics (Clock)

Clock: CLK_RF1

Ta=25°C, power supply voltage: typical if not specified

Item	Symbol	Min	Typ	Max	Unit	Condition
Cycle time	tCLKcyc	typ -20ppm	1/27M	typ +20ppm	s	
High level pulse width	tCLKH	tCLKcyc x0.42		tCLKcyc x0.58	s	
Low level pulse width	tCLKL	tCLKcyc x0.42		tCLKcyc x0.58	s	
Clock rise time	tCLKr			1	ns	
Clock fall time	tCLKf			1	ns	
Clock jitter	tCLKj	-15		15	ps	



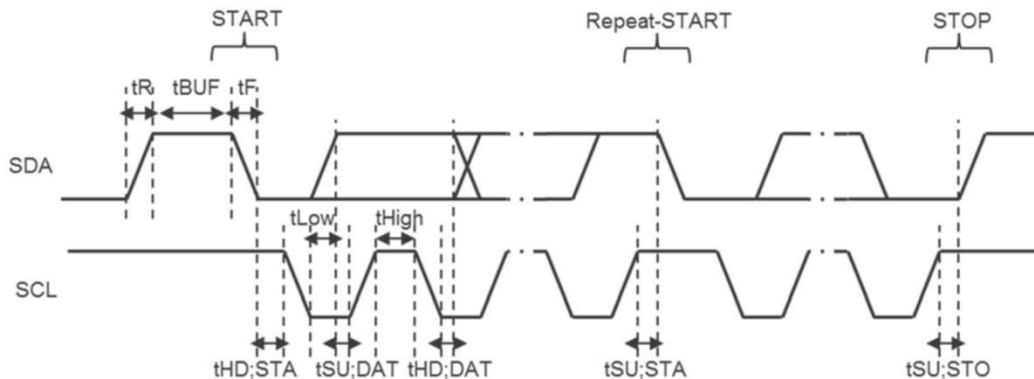
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I2C bus timing characteristics

Ta=25°C, power supply voltage: typical if not specified

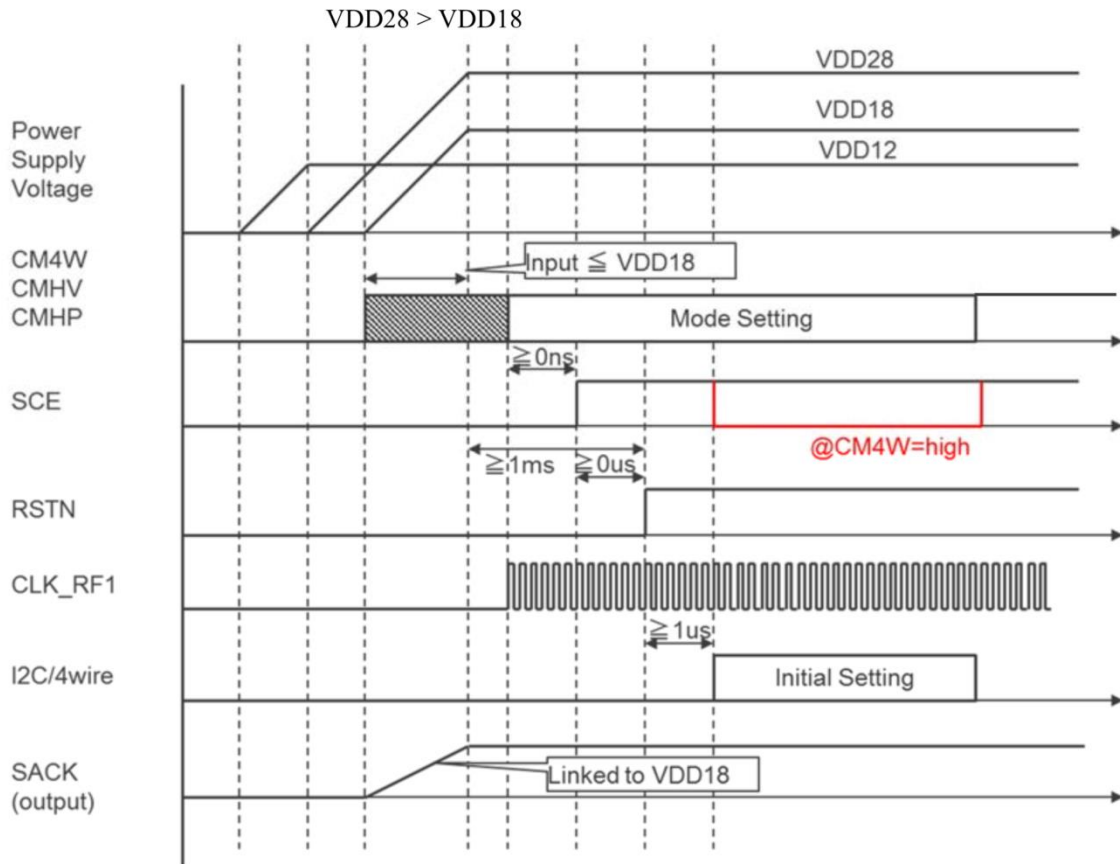
Item	Symbol	Min	Typ	Max	Unit	Condition
SCL clock frequency	fSCL	0	-	400	kHz	fast mode
		0	-	1000		fast mode plus
Hold time (repeated) START condition. After this period, the first clock pulse is generated	tHD;STA	0.6	-	-	us	fast mode
		0.26	-	-		fast mode plus
LOW period of the SCL clock	tLOW	1.3	-	-	us	fast mode
		0.5	-	-		fast mode plus
HIGH period of the SCL clock	tHIGH	0.6	-	-	us	fast mode
		0.26	-	-		fast mode plus
Setup time for a repeated START condition	tSU;STA	0.6	-	-	us	fast mode
		0.26	-	-		fast mode plus
Data hold time	tHD;DAT	0	-	0.9	us	fast mode
		0	-	0.45		fast mode plus
Data set-up time	tSU;DAT	100	-	-	ns	fast mode
		50	-	-		fast mode plus
Rise time of both SDA and SCL signals (CB=total capacitance of one bus line in pF)	tR	20	-	300	ns	fast mode
		-	-	120		fast mode plus
Fall time of both SDA and SCL signals (CB=total capacitance of one bus line in pF)	tF	VDI *20 /5.5	-	300	ns	fast mode
		VDI *20 /5.5	-	120		fast mode plus
Set-up time for STOP condition	tSU;STO	0.6	-	-	us	fast mode
		0.26	-	-		fast mode plus
Bus free time between a STOP and START condition	tBUF	1.3	-	-	us	fast mode
		0.5	-	-		fast mode plus
Capacitive load for each bus line	CB	10	-	400	pF	fast mode
		10	-	550		fast mode plus
Noise margin at the LOW level for each connected device (including hysteresis)	VnL	0.18	-	-	V	



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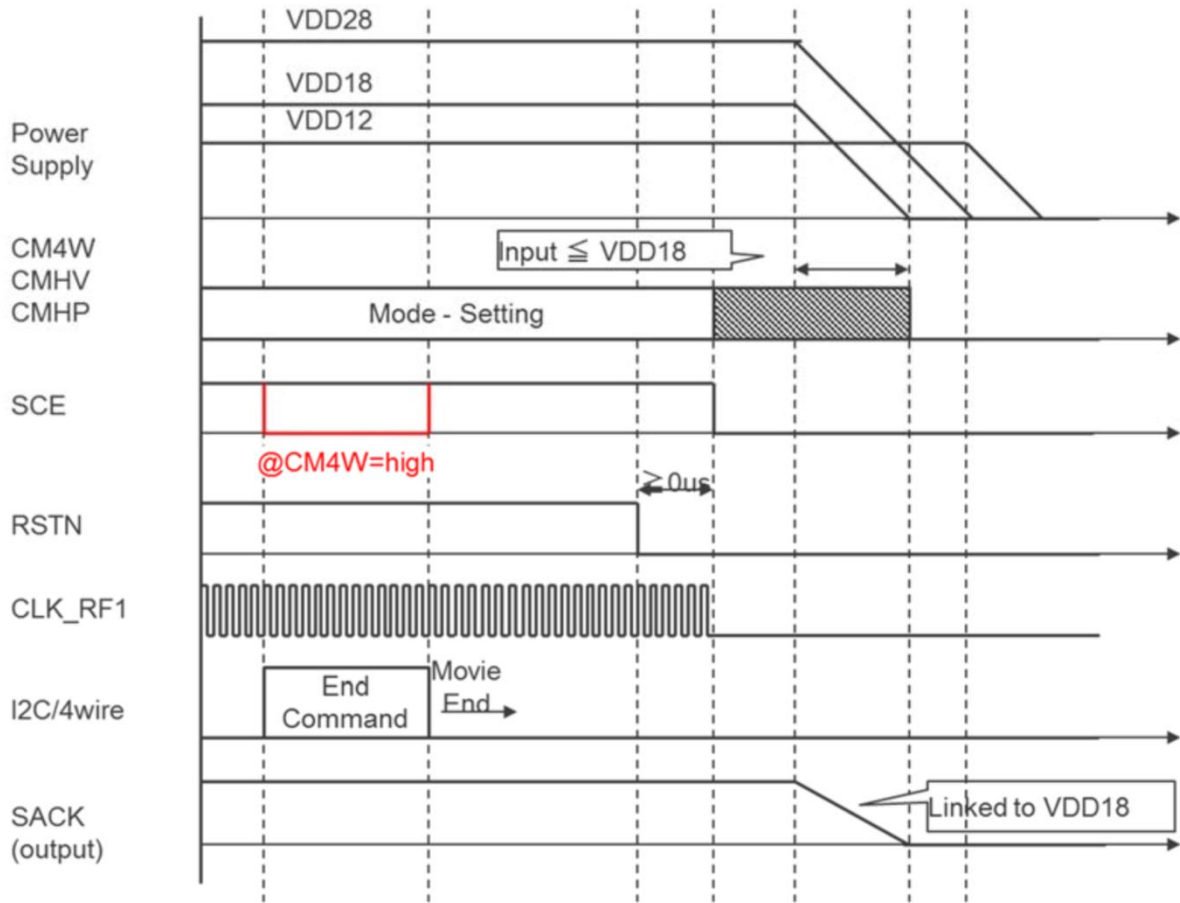
Power-on Sequence



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Power-off Sequence



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Revision History

Revision	Description	Release Date
1.0	First Release	28. Apr. 2019



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