



ON Semiconductor®

<http://onsemi.com>

# LV5744V

Bi-CMOS LSI

## 2-channel Step-down Switching Regulator

### Overview

The LV5744V is a 2-channel step-down switching regulator.

### Features

- Provides dual switching regulator control circuits integrated on the chip.
- Output-stage push-pull structure enabling high efficient operation.
- Provides power supply ( $V_{CC}-5V$ ) for protecting the external P channel MOS gate.
- Built-in timer latch type SCP (short-circuit protection circuit)
- Built-in UVLO (Low voltage malfunction prevention circuit)
- Built-in reference voltage circuit
- Max\_On\_Duty is adjustable.

### Specifications

**Absolute Maximum Ratings** at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}$ max		35	V
Output voltage	$V_O$ max		33	V
Allowable power dissipation	$P_d$ max	Mounted on a specified board *	0.74	W
Operating temperature	$T_{opr}$		-40 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$
Allowable pin voltage				
1	CT, NON1, NON2, INV1, INV2, FB1, FB2, DT1, DT2, SCP, VREF		7	V
2	$V_{CC}-5V$		30	V
3	GND, OUT1, OUT2, $V_{CC}$		35	V

\* : Specified board : 114.3×76.1×1.6mm<sup>3</sup>, glass epoxy board

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

# LV5744V

## Allowable Operating Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}$		8 to 33	V
Error amplifier input voltage	$V_{IN}$		0 to 3.3	V
Timing capacitance	$C_{CT}$		50 to 5000	pF
Oscillation frequency	$F_{CT}$		20k to 1M	Hz

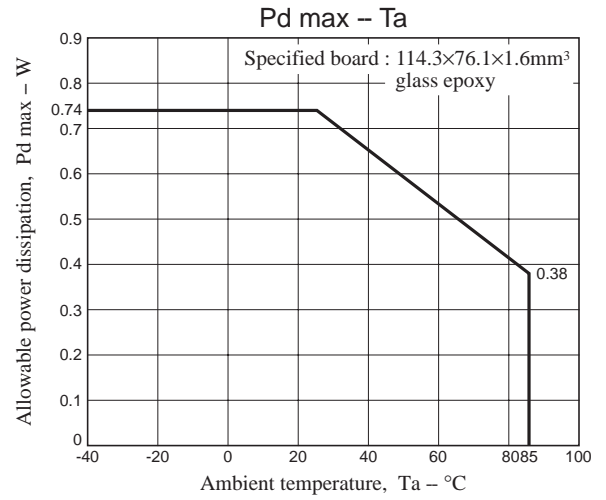
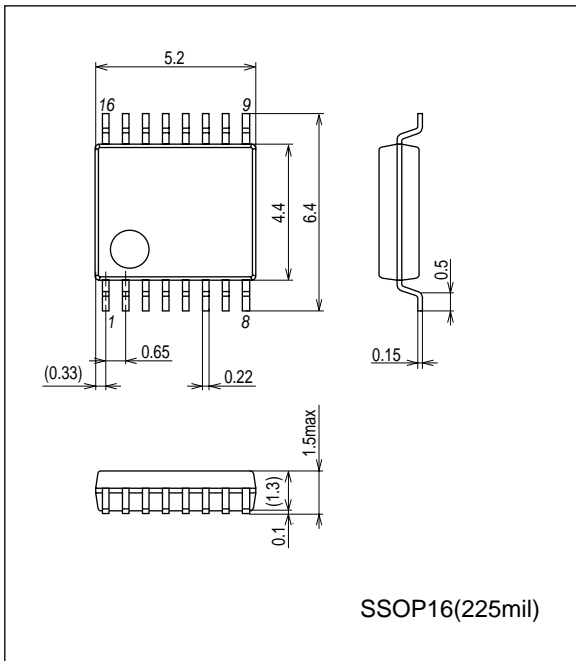
## Electrical Characteristics at $T_a = 25^\circ\text{C}$ , $V_{CC} = 12\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
<b>Reference voltage block</b>						
Output voltage	$V_{ref}$	$I_{ref} = 1\text{mA}$	2.4948	2.520	2.5452	V
Input stability	$V_{DLI}$	$V_{CC} = 8 \text{ to } 33\text{V}$		1	10	mV
Load stability	$V_{DLO}$	$I_{ref} = 0 \text{ to } 5\text{mA}$		1	10	mV
$V_{IN}$ -5V supply voltage	$V_{N5}$	$I_{OUT} = -5\text{mA}$	$V_{CC}-5.5$	$V_{CC}-5.0$	$V_{CC}-4.5$	V
<b>Triangular wave oscillator block</b>						
Oscillation frequency	$F_{OSC}$	$C_{CT} = 220\text{pF}$	320	400	480	kHz
Frequency fluctuation	$F_{DV}$	$V_{CC} = 8 \text{ to } 33\text{V}$		1		%
<b>Protection circuit block</b>						
Threshold voltage	$V_{IT}$		1.5	1.7	1.9	V
Standby voltage	$V_{STB}$			50	100	mV
Latch voltage	$V_{LT}$			30	100	mV
Source current	$I_{SCP}$		1.6	2.1	2.6	$\mu\text{A}$
Comparator threshold voltage	$V_{CT}$		1.4	1.5	1.6	V
<b>Quiescent time adjustment circuit block</b>						
Input threshold voltage ( $f_{osc} = 20\text{kHz}$ )	$V_{t0}$	Duty cycle = 0%	0.45	0.5	0.55	V
	$V_{t100}$	Duty cycle = 100%	0.95	1.0	1.05	V
Input bias current	$I_{BDT}$	$DT1, DT2 = 0\text{V}$		0.1	1	$\mu\text{A}$
<b>Low voltage malfunction prevention circuit block</b>						
Threshold voltage	$V_{UT}$		6.5	7	7.5	V
<b>Error amplifier</b>						
Input offset voltage	$V_{IO}$				6	mV
Input offset current	$I_{IO}$				30	nA
Input bias current	$I_{IB}$			15	100	nA
Open gain	$A_V$			85		dB
Common mode input voltage range	$V_{OM}$	$V_{CC} = 8 \text{ to } 33\text{V}$	0		3.3	V
Common mode rejection ratio	$CMRR$			80		dB
Maximum output voltage	$V_{OH}$			2.6		V
Minimum output voltage	$V_{OL}$			0.2	0.4	V
Output sink current	$I_{OI}$	$FB = 1.25\text{V}$		1		mA
Output source current	$I_{OO}$	$FB = 1.25\text{V}$		85		$\mu\text{A}$
<b>PWM comparator</b>						
Input threshold voltage ( $f_{osc} = 20\text{kHz}$ )	$V_{t0}$	Duty cycle = 0%	0.45	0.5	0.55	V
	$V_{t100}$	Duty cycle = 100%	0.95	1.0	1.05	V
<b>Output block</b>						
Output stage on resistance (upper)	$R_{ONH}$			7		$\Omega$
Output stage on resistance (lower)	$R_{ONL}$			2		$\Omega$
<b>Overall device characteristics</b>						
Standby current	$I_{CCS}$	When output is off			10	mA

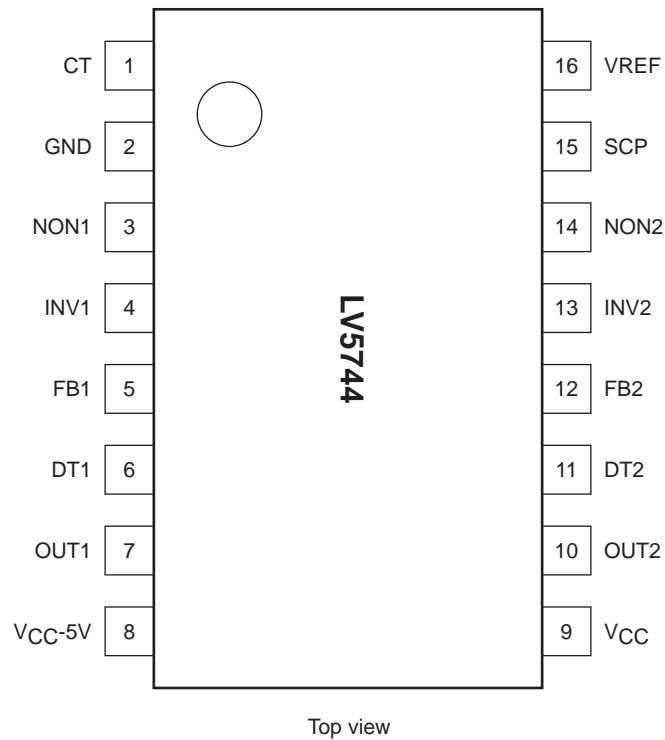
# LV5744V

## Package Dimensions

unit : mm (typ)  
3178B



## Pin Assignment

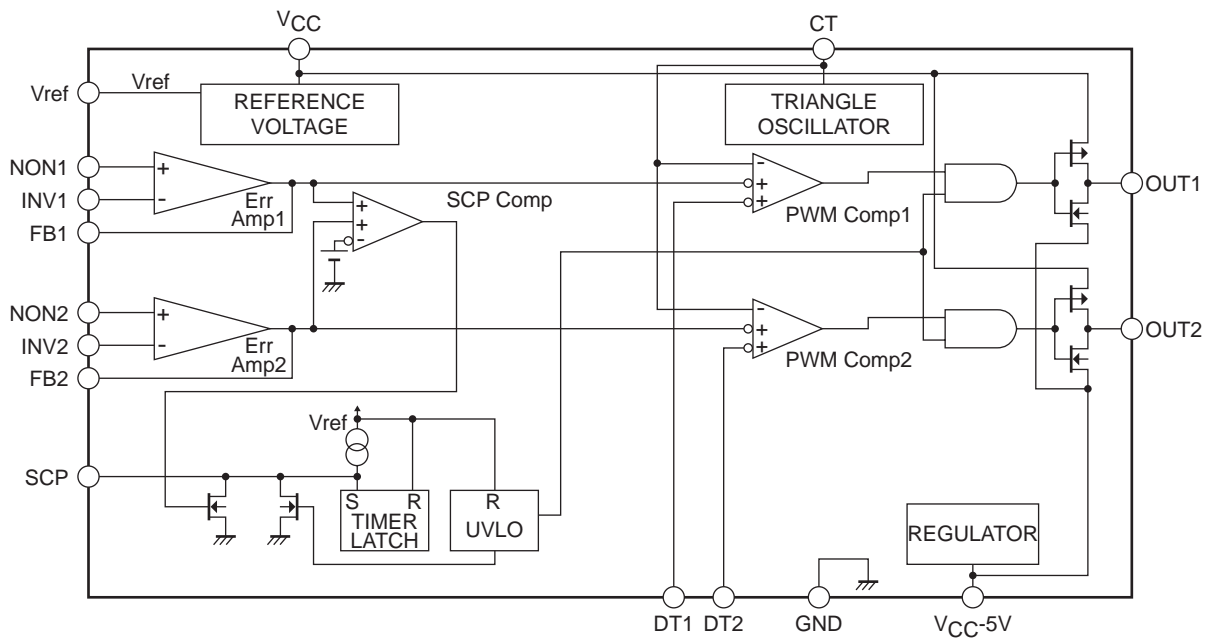


# LV5744V

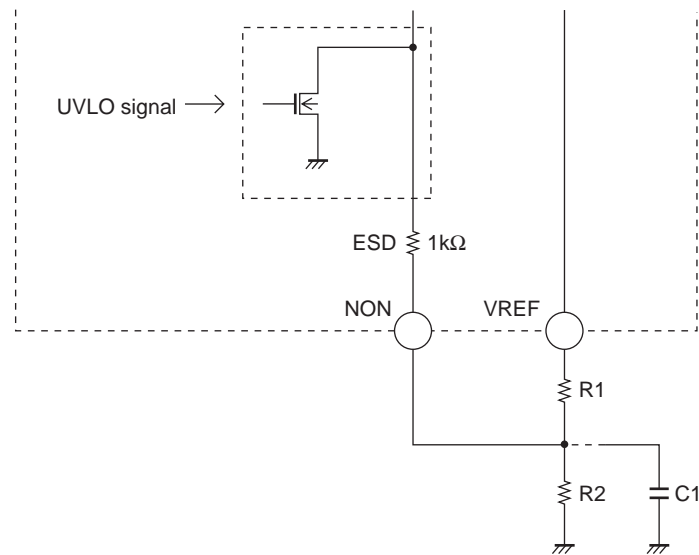
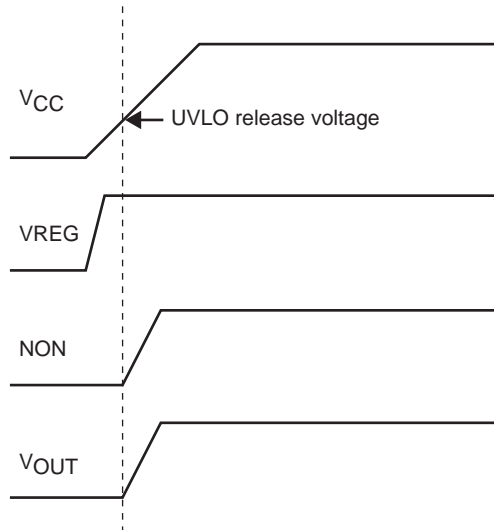
## Pin Function

Pin No.	Pin Name	Description
1	CT	External timing capacitor connection pin
2	GND	Ground
3	NON1	Error amplifier 1 input (+)
4	INV1	Error amplifier 1 input (-)
5	FB1	Error amplifier 1 output
6	DT1	Output 1 maximum duty setting
7	OUT1	Output 1
8	V <sub>CC-5V</sub>	Power supply for output stage drive
9	V <sub>CC</sub>	Power supply
10	OUT2	Output 2
11	DT2	Output 2 maximum duty setting
12	FB2	Error amplifier 2 input (+)
13	INV2	Error amplifier 2 input (-)
14	NON2	Error amplifier 2 output
15	SCP	Timer latch setting
16	VREF	Reference voltage output

## Block Diagram

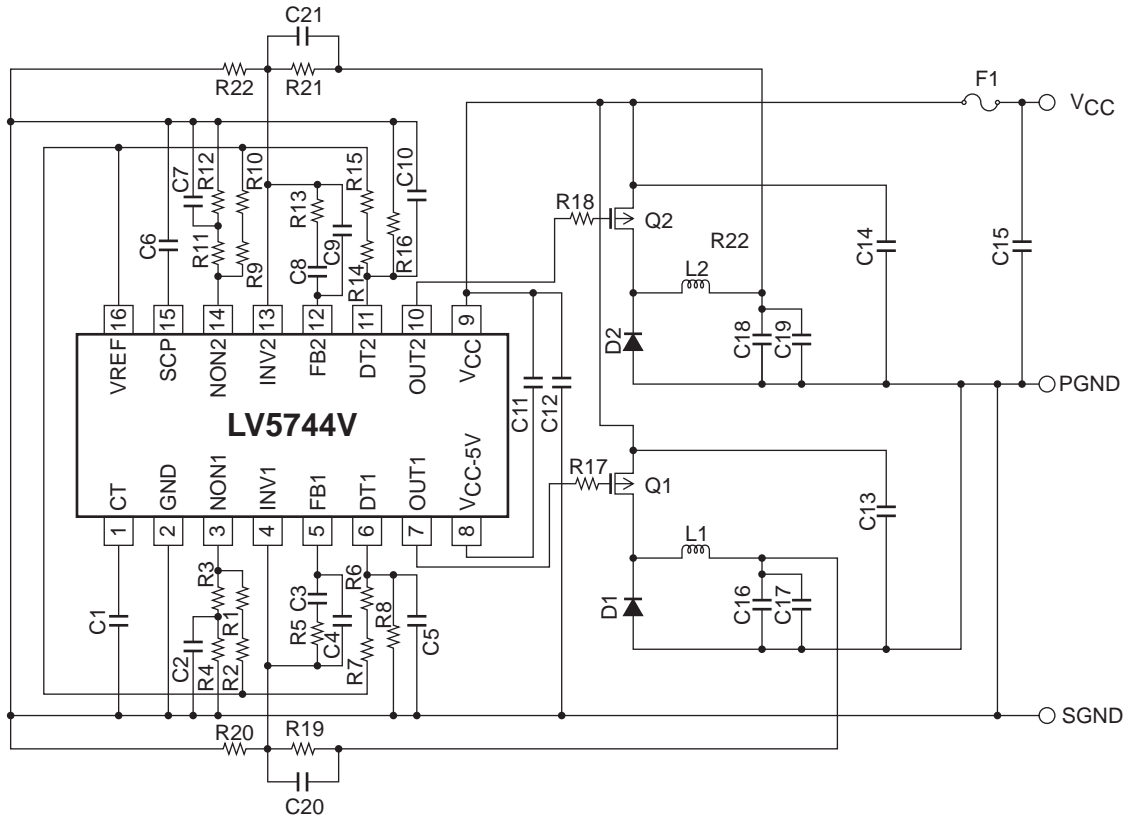


## Timing Chart



\* The voltage at the NON pin is  $\{VREF/(R1+1k)\} \times 1k$  in UVLO mode.

Application Circuit Example



ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.