Ordering number : ENA1241

LV5744V

Bi-CMOS LSI

2-channel Step-down Switching Regulator

ON Semiconductor®

http://onsemi.com

Overview

The LV5744V is a 2-channel step-down switching regulator.

Features

- Provides dual switching regulator control circuits integrated on the chip.
- Output-stage push-pull structure enabling high efficient operation.
- Provides power supply (V_{CC}-5V) for protecting the external P channel MOS gate.
- Built-in timer latch type SCP (short-circuit protection circuit)
- Built-in UVLO (Low voltage malfunction prevention circuit)
- Built-in reference voltage circuit
- Max_On_Duty is adjustable.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter		Symbol	Conditions	Ratings	Unit
Maximum supply voltage		V_{CC} max		35	V
Output voltage		V_O max		33	V
Allowable power dissipation		Pd max	Mounted on a specified board *	0.74	W
Operating temperature		Topr		-40 to +85	°C
Storage temperature		Tstg		-55 to +150	°C
Allowable pin voltage					
1	CT, NON1, NON2, INV1, INV2, FB1, FB2, DT1, DT2, SCP, VREF			7	V
2	V_{CC}-5V			30	V
3	GND, OUT1, OUT2, V_{CC}			35	V

* : Specified board : 114.3×76.1×1.6mm³, glass epoxy board

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		8 to 33	V
Error amplifier input voltage	V_{IN}		0 to 3.3	V
Timing capacitance	C_{CT}		50 to 5000	pF
Oscillation frequency	F_{CT}		20k to 1M	Hz

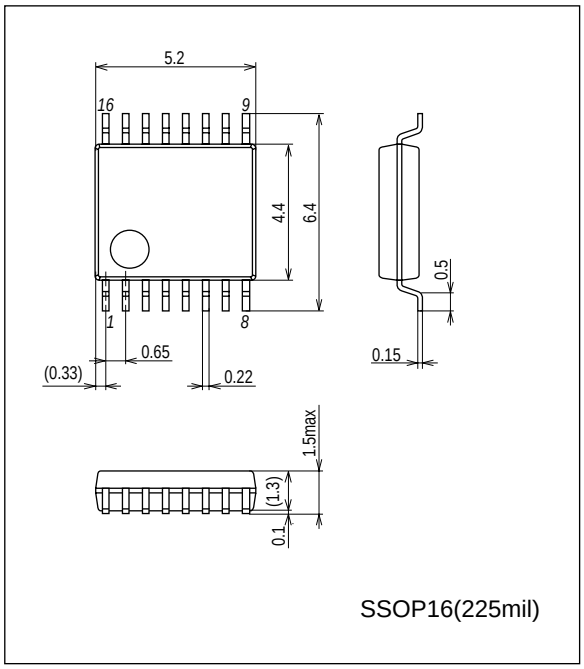
Electrical Characteristics at Ta = 25°C, V_{CC} = 12V

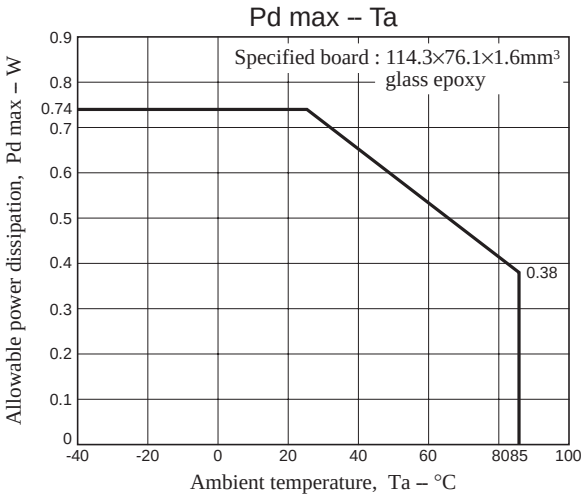
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Reference voltage block						
Output voltage	Vref	Iref = 1mA	2.4948	2.520	2.5452	V
Input stability	V_{DLI}	V_{CC} = 8 to 33V		1	10	mV
Load stability	V_{DLO}	Iref = 0 to 5mA		1	10	mV
V_{IN}-5V supply voltage	V_{N5}	I_{OUT} = -5mA	V_{CC}-5.5	V_{CC}-5.0	V_{CC}-4.5	V
Triangular wave oscillator block						
Oscillation frequency	F_{OSC}	C_{CT} = 220pF	320	400	480	kHz
Frequency fluctuation	F_{DV}	V_{CC} = 8 to 33V		1		%
Protection circuit block						
Threshold voltage	V_{IT}		1.5	1.7	1.9	V
Standby voltage	V_{STB}			50	100	mV
Latch voltage	V_{LT}			30	100	mV
Source current	I_{SCP}		1.6	2.1	2.6	µA
Comparator threshold voltage	V_{CT}		1.4	1.5	1.6	V
Quiescent time adjustment circuit block						
Input threshold voltage (fosc = 20kHz)	Vt0	Duty cycle = 0%	0.45	0.5	0.55	V
	Vt100	Duty cycle = 100%	0.95	1.0	1.05	V
Input bias current	I_{BDT}	DT1, DT2 = 0V		0.1	1	µA
Low voltage malfunction prevention circuit block						
Threshold voltage	V_{UT}		6.5	7	7.5	V
Error amplifier						
Input offset voltage	V_{IO}				6	mV
Input offset current	I_{IO}				30	nA
Input bias current	I_{IB}			15	100	nA
Open gain	AV			85		dB
Common mode input voltage range	V_{OM}	V_{CC} = 8 to 33V	0		3.3	V
Common mode rejection ratio	CMRR			80		dB
Maximum output voltage	V_{OH}			2.6		V
Minimum output voltage	V_{OL}			0.2	0.4	V
Output sink current	I_{OI}	FB = 1.25V		1		mA
Output source current	I_{OO}	FB = 1.25V		85		µA
PWM comparator						
Input threshold voltage (fosc = 20kHz)	Vt0	Duty cycle = 0%	0.45	0.5	0.55	V
	Vt100	Duty cycle = 100%	0.95	1.0	1.05	V
Output block						
Output stage on resistance (upper)	R_{ONH}			7		Ω
Output stage on resistance (lower)	R_{ONL}			2		Ω
Overall device characteristics						
Standby current	I_{CCS}	When output is off			10	mA

Package Dimensions

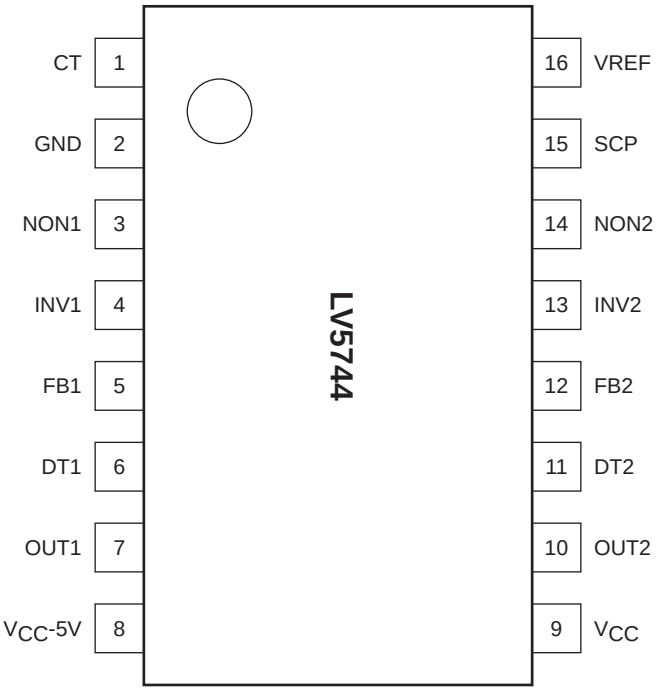
unit : mm (typ)

3178B





Pin Assignment

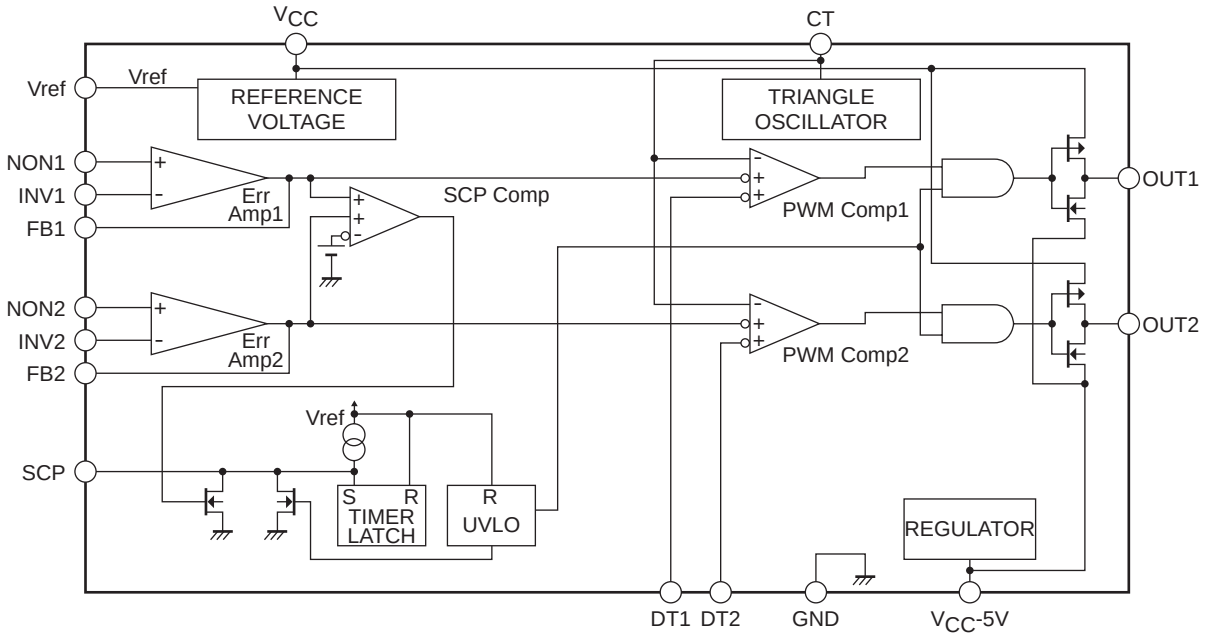


Top view

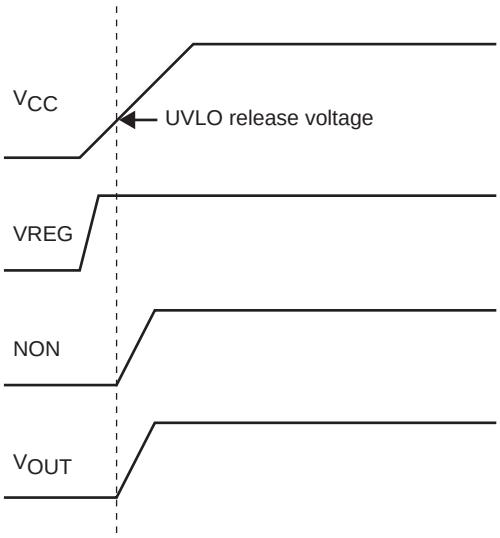
Pin Function

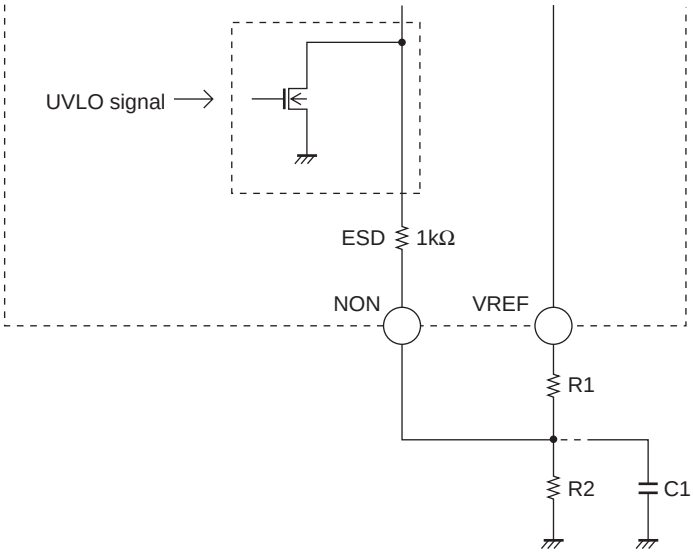
Pin No.	Pin Name	Description
1	CT	External timing capacitor connection pin
2	GND	Ground
3	NON1	Error amplifier 1 input (+)
4	INV1	Error amplifier 1 input (-)
5	FB1	Error amplifier 1 output
6	DT1	Output 1 maximum duty setting
7	OUT1	Output 1
8	V_{CC}-5V	Power supply for output stage drive
9	V_{CC}	Power supply
10	OUT2	Output 2
11	DT2	Output 2 maximum duty setting
12	FB2	Error amplifier 2 input (+)
13	INV2	Error amplifier 2 input (-)
14	NON2	Error amplifier 2 output
15	SCP	Timer latch setting
16	VREF	Reference voltage output

Block Diagram



Timing Chart





* The voltage at the NON pin is {VREF/(R1+1k)} × 1k in UVLO mode.

Application Circuit Example