bq27742-G1 Single-Cell Li-Ion Battery Fuel Gauge with Programmable Hardware Protection

1 Features

- Battery Fuel Gauge and Protector for Single-Cell Li-Ion Applications
- Microcontroller Peripheral Provides:
  - Precision 16-Bit, High-Side Coulomb Counter with Low-Value Sense Resistor (5 mΩ to 20 mΩ)
  - External and Internal Temperature Sensors for Battery Temperature Reporting
  - Lifetime and Current Data Logging
  - 64 Bytes of Non-Volatile Scratch Pad Flash
  - SHA-1 Authentication Capability
- Battery Fuel Gauging Based on Patented Impedance Track™ Technology
  - Models Battery Discharge Curve for Accurate Time-To-Empty Predictions
  - Automatically Adjusts for Aging, Self-Discharge, and Temperature- and Rate-Induced Effects on Battery
- Integrated High-side NMOS Protection FET Drive
- Hardware-based Safety and Protection:
  - Overvoltage (OVP)
  - Undervoltage (UVP)
  - Overcurrent in Charge (OCC)
  - Overcurrent in Discharge (OCD)
  - Short-Circuit in Discharge (SCD)
- I^2C™ and HDQ Interface Formats for Communication with Host System
- Ultra-Compact, 15-Ball NanoFree™ DSBGA

2 Applications

- Smartphones
- Tablets
- Handheld Terminals
- MP3 and Multimedia Players
- Portable Gaming

3 Description

The Texas Instruments bq27742-G1 is a fuel gauge for single-cell Li-Ion battery packs that uses patented Impedance Track™ technology to deliver rate-, temperature-, and aging-compensated predictions of remaining battery capacity and system runtime with highest accuracy. The device also includes a fully integrated high-side protector that eliminates the need for a separate Li-Ion protection circuit and provides a full suite of high-accuracy fault detections for overvoltage, undervoltage, overcurrent in charge, overcurrent in discharge, and short-circuit in discharge conditions. The hardware protection functions offer built-in data flash-based programmability, allowing simple reconfiguration of existing devices for varying end equipment needs.

The fuel gauge provides information such as remaining battery capacity (mAh), state-of-charge (%), runtime to empty (minutes), voltage (mV), current (mA), and temperature (°C), as well as recording vital parameters throughout the lifetime of the battery. The device also supports interrupts to the host to indicate detection of a variety of important battery conditions to the system.

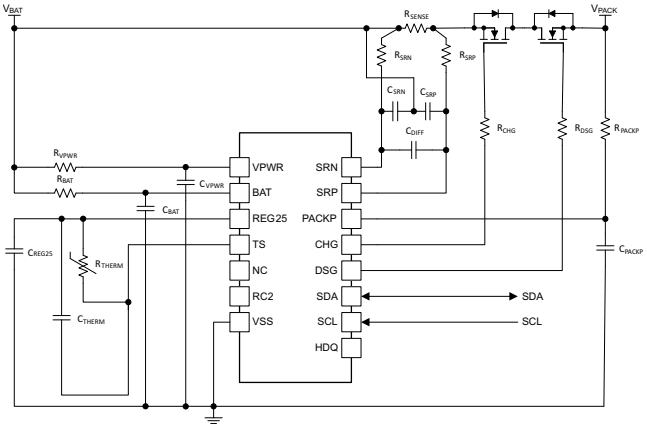
The DSBGA is a 15-ball package (2.78 mm × 1.96 mm) that is ideal for space-constrained applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
BQ27742YZFR-G1	YZF (15)	2.78 mm × 1.96 mm
BQ27742YZFT-G1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2015) to Revision C — **Page**

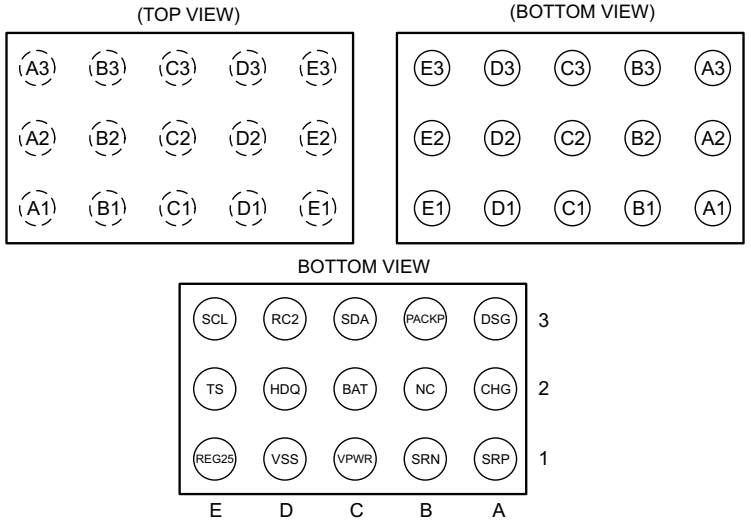
- Changed occurrences of the package label "CSP" to "DSBGA" ... 1
- Changed *Integrating ADC (Coulomb Counter) Characteristics* ... 11

Changes from Revision A (December 2014) to Revision B — **Page**

- Added minor editorial and formatting updates ... 1
- Changed Pin Functions ... 3
- Changed *Absolute Maximum Ratings* ... 6
- Changed *Recommended Operating Conditions* ... 7
- Changed *Functional Block Diagram* ... 17
- Changed V_{VPWR} to V_{BAT} in Figure 15 ... 21
- Changed "V_{PWR}" to "V_{BAT}" in the *OVERVOLTAGE Mode* section ... 22
- Changed "V_{PWR}" to "V_{BAT}" in the *UNDERVOLTAGE Mode* section ... 22
- Added *Community Resources* ... 40

5 Pin Configuration and Functions

bq27742-G1 Pin Diagram
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
SRP	A1	I	Analog input pin connected to the internal coulomb counter where SRP is nearest the PACK+ connection. Connect to sense resistor.
CHG	A2	O	External high side N-channel charge FET driver.
DSG	A3	O	External high side N-channel discharge FET driver.
SRN	B1	I	Analog input pin connected to the internal coulomb counter where SRN is nearest the CELL+ connection. Connect to sense resistor.
NC	B2	IO	Not used. Reserved for future GPIO. Recommended to connect to GND.
PACKP	B3	I	Pack voltage measurement input for protector operation.
VPWR	C1	—	Power input. Decouple with 0.1-µF ceramic capacitor to V_{SS}.
BAT	C2	I	Cell-voltage measurement input. ADC input.
SDA	C3	IO	Slave I^2C serial communications data line for communication with system. Open-drain I/O. Use with 10-kΩ pullup resistor (typical).
VSS	D1	—	Device ground.
HDQ	D2	I/O	HDQ serial communications line. Open-drain.
RC2	D3	IO	General purpose IO. Push-pull output.
REG25	E1	—	Regulator output and bq27742-G1 processor power. Decouple with 1.0-µF ceramic capacitor to V_{SS}.
TS	E2	I	Pack thermistor voltage sense (use 103AT-type thermistor). ADC input.
SCL	E3	IO	Slave I^2C serial communications clock input line for communication with system. Use with 10-kΩ pullup resistor (typical).

Table 1. Hardware Protection Thresholds(1)

OVERVOLTAGE PROTECTION (V_{OVP})	UNDERVOLTAGE PROTECTION (V_{UVP})	OVERCURRENT IN CHARGE (V_{OCC})	OVERCURRENT IN DISCHARGE (V_{OCD})	SHORT-CIRCUIT IN DISCHARGE (V_{SCD})
4.450 V	2.438 V	6 mV	14 mV	73 mV
			24 mV	
		13 mV	34 mV	
			44 mV	
		18 mV	53 mV	148 mV
			63 mV	
		28 mV	73 mV	
			83 mV	
4.425 V	2.422 V	6 mV	13 mV	73 mV
			23 mV	
		13 mV	33 mV	
			43 mV	
		18 mV	53 mV	148 mV
			63 mV	
		28 mV	72 mV	
			83 mV	
4.400 V	2.409 V	6 mV	13 mV	72 mV
			23 mV	
		13 mV	33 mV	
			43 mV	
		18 mV	52 mV	147 mV
			62 mV	
		28 mV	72 mV	
			82 mV	
4.375 V	2.395 V	6 mV	13 mV	72 mV
			23 mV	
		13 mV	33 mV	
			42 mV	
		18 mV	52 mV	146 mV
			62 mV	
		28 mV	72 mV	
			82 mV	
4.350 V	2.381 V	6 mV	13 mV	71 mV
			23 mV	
		13 mV	32 mV	
			42 mV	
		18 mV	52 mV	145 mV
			62 mV	
		28 mV	71 mV	
			81 mV	

(1) Production tested in the following configuration: V_{OVP} = 4.450 V, V_{UVP} = 2.438 V, V_{OCC} = 28 mV, V_{OCD} = 83 mV, and V_{SCD} = 148 mV.

Table 1. Hardware Protection Thresholds(1) (continued)

OVERVOLTAGE PROTECTION (V_{OVP})	UNDERVOLTAGE PROTECTION (V_{UVP})	OVERCURRENT IN CHARGE (V_{OCC})	OVERCURRENT IN DISCHARGE (V_{OCD})	SHORT-CIRCUIT IN DISCHARGE (V_{SCD})
4.325 V	2.368 V	6 mV	13 mV	71 mV
			22 mV	
		13 mV	32 mV	
			42 mV	
		18 mV	52 mV	144 mV
			61 mV	
		27 mV	71 mV	
			81 mV	
4.300 V	2.354 V	6 mV	13 mV	71 mV
			22 mV	
		13 mV	32 mV	
			42 mV	
		18 mV	51 mV	143 mV
			61 mV	
		27 mV	70 mV	
			80 mV	
4.275 V	2.340 V	6 mV	13 mV	70 mV
			22 mV	
		13 mV	32 mV	
			41 mV	
		18 mV	51 mV	143 mV
			60 mV	
		27 mV	70 mV	
			80 mV	

Table 2. Hardware Protection Delays

OVERVOLTAGE PROTECTION DELAY (t_{OVP})	UNDERVOLTAGE PROTECTION DELAY (t_{UVP})	OVERCURRENT IN CHARGE DELAY (t_{OCC})	OVERCURRENT IN DISCHARGE DELAY (t_{OCD})	SHORT-CIRCUIT IN DISCHARGE DELAY (t_{SCD})
1.00 s	31.25 ms	7.81 ms	31.25 ms	312.50 µs

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{VPWR}	Power input range	–0.3	5.5	V
V_{REG25}	Supply voltage range	–0.3	2.75	V
V_{PACKP}	PACKP input pin	–0.3	5.5	V
	PACK+ input when external 2-kΩ resistor is in series with PACKP input pin (see Figure 19 and Figure 20)	–0.3	28	V
V_{OUT}	Voltage output pins (DSG, CHG)	–0.3	10	V
V_{IOD1}	Push-pull IO pins (RC2)	–0.3	2.75	V
V_{IOD2}	Open-drain IO pins (SDA, SCL, HDQ, NC)	–0.3	5.5	V
V_{BAT}	BAT input pin	–0.3	5.5	V
V_I	Input voltage range to all other pins (SRP, SRN)	–0.3	5.5	V
V_{TS}	Input voltage range for TS	–0.3	2.75	V
T_A	Operating free-air temperature	–40	85	°C
T_F	Functional temperature	–40	100	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process..

6.3 Recommended Operating Conditions

T_A = 25°C, C_{REG25} = 1.0 µF, and V_{VPWR} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
V_{VPWR}	Supply voltage	No operating restrictions	2.8		5.0	V
		No FLASH writes	2.45		2.8	
C_{VPWR}	External input capacitor for internal LDO between VPWR and V_{SS}	Nominal capacitor values specified. Recommend a 5% ceramic X5R type capacitor located close to the device.		0.1		µF
C_{REG25}	External output capacitor for internal LDO between REG25 and V_{SS}		0.47	1.0		µF
I_{CC}	NORMAL operating mode current(1)(2) (VPWR)	Fuel gauge in NORMAL mode I_{LOAD} > ***Sleep Current*** with charge pumps on (FETs on)		167		µA
I_{SLP}	SLEEP mode current(1)(2) (VPWR)	Fuel gauge in SLEEP+ mode. I_{LOAD} < ***Sleep Current*** with charge pumps on (FETs on)		88		µA
$I_{FULLSLP}$	FULLSLEEP mode current(1)(2) (VPWR)	Fuel gauge in SLEEP mode. I_{LOAD} < ***Sleep Current*** with charge pumps on (FETs on)		40		µA
$I_{SHUTDOWN}$	SHUTDOWN mode current(1)(2) (VPWR)	Fuel gauge in SHUTDOWN mode. UVP tripped with fuel gauge and protector turned off (FETs off) V_{VPWR} = 2.5 V T_A = 25°C		0.1	0.2	µA
		T_A = –40°C to 85°C			0.5	µA
V_{OL}	Output voltage low (SCL, SDA, HDQ, NC, RC2)	I_{OL} = 1 mA			0.4	V
$V_{OH(OD)}$	Output voltage high (SDA, SCL, HDQ, NC, RC2)	External pullup resistor connected to V_{REG25}	V_{REG25} – 0.5			V
V_{IL}	Input voltage low (SDA, SCL, HDQ, NC)		–0.3		0.6	V
$V_{IH(OD)}$	Input voltage high (SDA, SCL, HDQ, NC)		1.2		5.5	V
V_{A1}	Input voltage range (TS)		V_{SS} – 0.125		2	V
V_{A2}	Input voltage range (BAT)		V_{SS} – 0.125		5	V
V_{A3}	Input voltage range (SRP, SRN)		V_{VPWR} – 0.125		V_{VPWR} + 0.125	V
I_{lkg}	Input leakage current (I/O pins)				0.3	µA
t_{PUCD}	Power-up communication delay			250		ms

(1) All currents are specified with charge pump on (FETs on).
(2) All currents are continuous average over 5-second period.

6.4 Thermal Information

THERMAL METRIC(1)		bq27742-G1 YZF (DSBGA) 15 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	17	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

6.5 Power-On Reset

T_A = 25°C, C_{REG25} = 1.0 µF, and V_{VPWR} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Increasing battery voltage input at V_{REG25}		2.09	2.20	2.31	V
V_{HYS}	Power-on reset hysteresis		45	115	185	mV

6.6 2.5-V LDO Regulator(1)

T_A = 25°C, C_{REG25} = 1.0 µF, and V_{VPWR} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REG25}	Regulator output voltage	2.8 V ≤ V_{VPWR} ≤ 4.5 V, I_{OUT}(1) ≤ 16 mA	T_A = –40°C to 85°C	2.3	2.5	2.6	V
		2.45 V ≤ V_{VPWR} < 2.8 V (low battery), I_{OUT}(1) ≤ 3 mA		2.3			V
I_{SHORT}(2)	Short-circuit current limit	V_{REG25} = 0 V	T_A = –40°C to 85°C			250	mA

(1) LDO output current, I_{OUT}, is the sum of internal and external load currents.
(2) Assured by characterization. Not production tested.

6.7 Charger Attachment and Removal Detection

T_A = 25°C, C_{REG25} = 1.0 µF, and V_{VPWR} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CHGATT}	Voltage threshold for charger attachment detection			2.7	3.0	V
V_{CHGREM}	Voltage threshold for charger removal detection		0.5	1.0		V

6.8 CHG and DSG FET Drive

T_A = 25°C, C_{REG25} = 1.0 µF, and V_{VPWR} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FETON}	CHG and DSG FETs on	I_L = 1 µA, T_A = –40°C to 85°C	2 × V_{VPWR} – 0.4	2 × V_{VPWR} – 0.2	2 × V_{VPWR}	V
V_{FETOFF}	CHG and DSG FETs off	T_A = –40°C to 85°C			0.2	V
$V_{FETRIPPLE}$(1)	CHG and DSG FETs on	I_L = 1 µA, T_A = –40°C to 85°C			0.1	V_{PP}
t_{FETON}	FET gate rise time (10% to 90%)	C_L = 4 nF, T_A = –40°C to 85°C, No series resistance	67	140	218	µs
t_{FETOFF}	FET gate fall time (90% to 10%)	C_L = 4 nF, T_A = –40°C to 85°C, No series resistance	10	30	60	µs

(1) Assured by characterization. Not production tested.

6.9 Overvoltage Protection (OVP)

T_A = 25°C and C_{REG25} = 1.0 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP}	OVP detection voltage threshold	T_A = 25°C	V_{OVP} – 0.016	V_{OVP}	V_{OVP} + 0.016	V
		T_A = 0°C to 25°C	V_{OVP} – 0.033	V_{OVP}	V_{OVP} + 0.030	
		T_A = 25°C to 50°C	V_{OVP} – 0.028	V_{OVP}	V_{OVP} + 0.024	
		T_A = –40°C to 85°C	V_{OVP} – 0.063	V_{OVP}	V_{OVP} + 0.045	
V_{OVPREL}	OVP release voltage	T_A = 25°C	V_{OVPREL} – 0.022	V_{OVP} – 0.215	V_{OVPREL} + 0.022	V
		T_A = 0°C to 25°C	V_{OVPREL} – 0.033	V_{OVP} – 0.215	V_{OVPREL} + 0.030	
		T_A = 25°C to 50°C	V_{OVPREL} – 0.028	V_{OVP} – 0.215	V_{OVPREL} + 0.024	
		T_A = –40°C to 85°C	V_{OVPREL} – 0.063	V_{OVP} – 0.215	V_{OVPREL} + 0.045	
t_{OVP}	OVP delay time	T_A = –40°C to 85°C	t_{OVP} – 5%	t_{OVP}	t_{OVP} + 5%	s

6.10 Undervoltage Protection (UVP)

T_A = 25°C and C_{REG25} = 1.0 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVP}	UVP detection voltage threshold	T_A = 25°C	V_{UVP} – 0.022	V_{UVP}	V_{UVP} + 0.022	V
		T_A = –5°C to 50°C	V_{UVP} – 0.030	V_{UVP}	V_{UVP} + 0.030	
		T_A = –40°C to 85°C	V_{UVP} – 0.050	V_{UVP}	V_{UVP} + 0.050	
V_{UVPREL}	UVP release voltage	T_A = 25°C	V_{UVPREL} – 0.022	V_{UVP} + 0.105	V_{UVPREL} + 0.022	V
		T_A = –5°C to 50°C	V_{UVPREL} – 0.030	V_{UVP} + 0.105	V_{UVPREL} + 0.030	
		T_A = –40°C to 85°C	V_{UVPREL} – 0.050	V_{UVP} + 0.105	V_{UVPREL} + 0.050	
t_{UVP}	UVP delay time	T_A = –40°C to 85°C	t_{UVP} – 5%	t_{UVP}	t_{UVP} + 5%	ms

6.11 Overcurrent in Discharge (OCD)

T_A = 25°C, C_{REG25} = 1.0 µF, and V_{VPWR} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OCD}	OCD detection voltage threshold	T_A = 25°C $V_{SRN} – V_{SRP}$	V_{OCD} – 3	V_{OCD}	V_{OCD} + 3	mV
		T_A = –20°C to 60°C $V_{SRN} – V_{SRP}$	0.98 * V_{OCD} – 3.125	V_{OCD}	1.02 * V_{OCD} + 3.125	
		T_A = –40°C to 85°C $V_{SRN} – V_{SRP}$	0.98 * V_{OCD} – 3.5	V_{OCD}	1.02 * V_{OCD} + 3.5	
t_{OCD}	OCD delay time	T_A = –40°C to 85°C	t_{OCD} – 5%	t_{OCD}	t_{OCD} + 5%	ms

6.12 Overcurrent in Charge (OCC)

T_A = 25°C, C_{REG25} = 1.0 µF, and V_{VPWR} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OCC}	OCC detection voltage threshold	T_A = 25°C $V_{SRP} – V_{SRN}$	V_{OCC} – 3	V_{OCC}	V_{OCC} + 3	mV
		T_A = –20°C to 60°C $V_{SRP} – V_{SRN}$	0.98 * V_{OCC} – 3.125	V_{OCC}	1.02 * V_{OCC} + 3.125	
		T_A = –40°C to 85°C $V_{SRP} – V_{SRN}$	0.98 * V_{OCC} – 3.5	V_{OCC}	1.02 * V_{OCC} + 3.5	
t_{OCC}	OCC delay time	T_A = –40°C to 85°C	t_{OCC} – 5%	t_{OCC}	t_{OCC} + 5%	ms

6.13 Short-Circuit in Discharge (SCD)

T_A = 25°C, C_{REG25} = 1.0 µF, and V_{VPWR} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SCD}	SCD detection voltage threshold	T_A = 25°C $V_{SRN} - V_{SRP}$	V_{SCD} – 3	V_{SCD}	V_{SCD} + 3	mV
		T_A = –20°C to 60°C $V_{SRN} - V_{SRP}$	0.98 * V_{SCD} – 3.125	V_{SCD}	1.02 * V_{SCD} + 3.125	
		T_A = –40°C to 85°C $V_{SRN} - V_{SRP}$	0.98 * V_{SCD} – 3.5	V_{SCD}	1.02 * V_{SCD} + 3.5	
t_{SCD}	SCD delay time	T_A = –40°C to 85°C	t_{SCD} – 30%	t_{SCD}	t_{SCD} + 30%	µs

6.14 Low Voltage Charging

T_A = 25°C, C_{REG25} = 1.0 µF, and V_{VPWR} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LVDET}	Voltage threshold for low-voltage charging detection	T_A = –40°C to 85°C	1.4	1.55	1.7	V

6.15 Internal Temperature Sensor Characteristics

T_A = –40°C to 85°C, 2.4 V < V_{REG25} < 2.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$G_{(TEMP)}$	Temperature sensor voltage gain			–2		mV/°C

6.16 High-Frequency Oscillator

2.4 V < V_{REG25} < 2.6 V; typical values at T_A = 25°C and V_{REG25} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Operating frequency			8.389		MHz
f_{EIO}	Frequency error(1) (2)	T_A = 0°C to 60°C	–2.0%	0.38%	2.0%	
		T_A = –20°C to 70°C	–3.0%	0.38%	3.0%	
		T_A = –40°C to 85°C	-4.5%	0.38%	4.5%	
t_{SXO}	Start-up time(3)	T_A = –40°C to 85°C		2.5	5	ms

(1) The frequency error is measured from 2.097 MHz.
(2) The frequency drift is included and measured from the trimmed frequency at V_{REG25} = 2.5 V, T_A = 25°C.
(3) The startup time is defined as the time it takes for the oscillator output frequency to be ±3% of the typical oscillator frequency.

6.17 Low-Frequency Oscillator

2.4 V < V_{REG25} < 2.6 V; typical values at T_A = 25°C and V_{REG25} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(LOSC)}$	Operating frequency			32.768		kHz
$f_{(LEIO)}$	Frequency error(1) (2)	T_A = 0°C to 60°C	–1.5%	0.25%	1.5%	
		T_A = –20°C to 70°C	–2.5%	0.25%	2.5%	
		T_A = –40°C to 85°C	-4.0%	0.25%	4.0%	
$t_{(LSXO)}$	Start-up time(3)	T_A = –40°C to 85°C		500		µs

(1) The frequency drift is included and measured from the trimmed frequency at V_{REG25} = 2.5 V, T_A = 25°C.
(2) The frequency error is measured from 32.768 kHz.
(3) The startup time is defined as the time it takes for the oscillator output frequency to be ±3% of the typical oscillator frequency.

6.18 Integrating ADC (Coulomb Counter) Characteristics

T_A = –40°C to 85°C, 2.4 V < V_{REG25} < 2.6 V; typical values at T_A = 25°C and V_{REG25} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SR_IN}	Input voltage range, V_{SRN} and V_{SRP}	$V_{SR} = V_{SRP} – V_{SRN}$	V_{VPWR} – 0.125		V_{VPWR} + 0.125	V
t_{SR_CONV}	Conversion time	Single conversion		1		s
	Resolution		14		15	bits
V_{SR_OS}	Input offset			10		µV
INL	Integral nonlinearity error			±0.007%	±0.034%	FSR
Z_{SR_IN}	Effective input resistance(1)		7			MΩ
I_{SR_LKG}	Input leakage current(1)				0.3	µA

(1) Assured by design. Not production tested.

6.19 ADC (Temperature and Cell Voltage) Characteristics

T_A = –40°C to 85°C, 2.4 V < V_{REG25} < 2.6 V; typical values at T_A = 25°C and V_{REG25} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ADC_IN}	Input voltage range (V_{BAT} channel)		V_{SS} – 0.125		5	V
	Input voltage range (other channels)		V_{SS} – 0.125		1	V
t_{ADC_CONV}	Conversion time				125	ms
	Resolution		14		15	bits
V_{ADC_OS}	Input offset			1		mV
Z_{ADC1}	Effective input resistance (TS) (1)		55			MΩ
Z_{ADC2}	Effective input resistance (BAT)(1)	Not measuring cell voltage	55			MΩ
		Measuring cell voltage		100		kΩ
I_{ADC_LKG}	Input leakage current(1)				0.3	µA

(1) Assured by design. Not production tested.

6.20 Data Flash Memory Characteristics

T_A = –40°C to 85°C, 2.4 V < V_{REG25} < 2.6 V; typical values at T_A = 25°C and V_{REG25} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Data retention(1)		10			years
	Flash programming write-cycles (1)		20,000			cycles
$t_{WORDPROG}$	Word programming time(1)				2	ms
I_{CCPROG}	Flash-write supply current(1)			5	10	mA

(1) Assured by design. Not production tested.

6.21 Timing Requirements

T_A = –40°C to 85°C, 2.4 V < V_{REG25} < 2.6 V; typical values at T_A = 25°C and V_{REG25} = 2.5 V (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I²C-Compatible Interface Timing Characteristics (see Figure 1)					
t_R	SCL or SDA rise time			300	ns
t_F	SCL or SDA fall time			300	ns
$t_{w(H)}$	SCL pulse width (high)	600			ns
$t_{w(L)}$	SCL pulse width (low)	1.3			µs
$t_{su(STA)}$	Setup for repeated start	600			ns
$t_{d(STA)}$	Start to first falling edge of SCL	600			ns
$t_{su(DAT)}$	Data setup time	100			ns
$t_{h(DAT)}$	Data hold time	0			ns
$t_{su(STOP)}$	Setup time for stop	600			ns
t_{BUF}	Bus free time between stop and start	66			µs
f_{SCL}	Clock frequency			400	kHz
HDQ Communication Timing Characteristics (see Figure 2)					
$t_{(CYCH)}$	Cycle time, host to fuel gauge	190			µs
$t_{(CYCD)}$	Cycle time, fuel gauge to host	190	205	250	µs
$t_{(HW1)}$	Host sends 1 to fuel gauge	0.5		50	µs
$t_{(DW1)}$	Fuel gauge sends 1 to host	32		50	µs
$t_{(HW0)}$	Host sends 0 to fuel gauge	86		145	µs
$t_{(DW0)}$	Fuel gauge sends 0 to host	80		145	µs
$t_{(RSPS)}$	Response time, fuel gauge to host	190		950	µs
$t_{(B)}$	Break time	190			µs
$t_{(BR)}$	Break recovery time	40			µs
$t_{(RST)}$	HDQ reset	1.8		2.2	s
$t_{(RISE)}$	HDQ line rise time to logic 1 (1.2 V)			950	ns

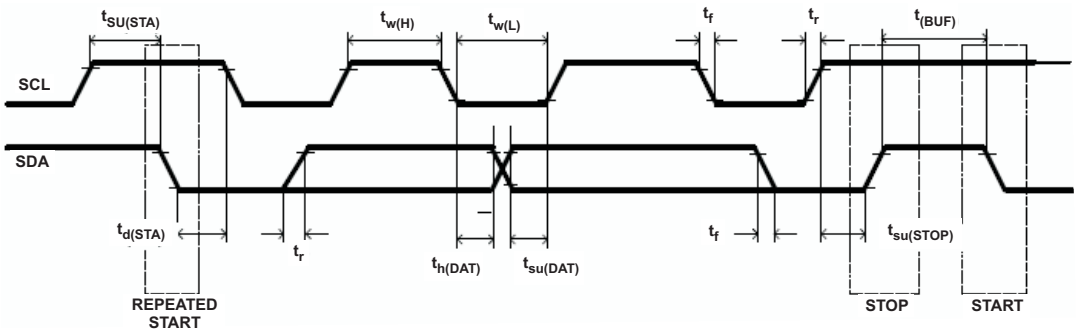
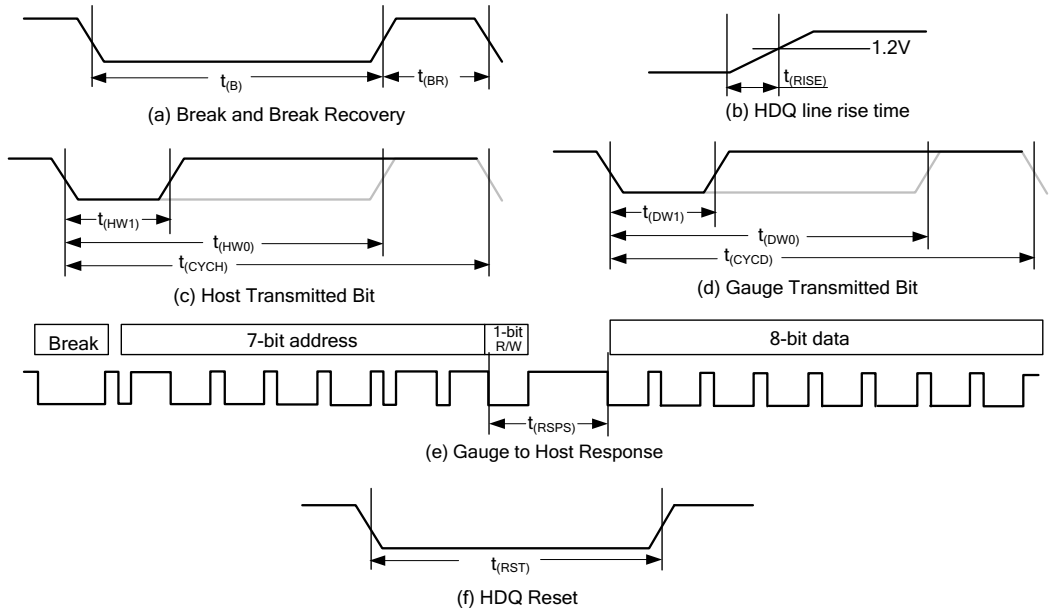


Figure 1. I²C-Compatible Interface Timing Diagrams



a. HDQ Breaking
b. Rise time of HDQ line
c. HDQ Host to fuel gauge communication
d. Fuel gauge to Host communication
e. Fuel gauge to Host response format
f. HDQ Host to fuel gauge

A. HDQ Breaking
B. Rise time of HDQ line
C. HDQ Host to fuel gauge communication
D. Fuel gauge to Host communication
E. Fuel gauge to Host response format
F. HDQ Host to fuel gauge reset

Figure 2. HDQ Communication Timing Diagrams

6.22 Typical Characteristics

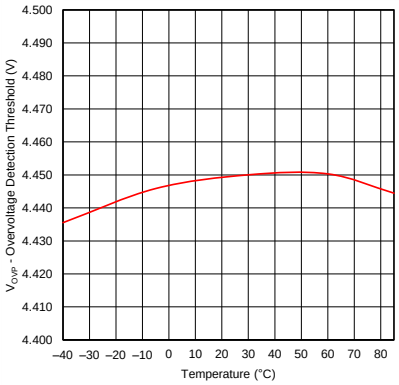
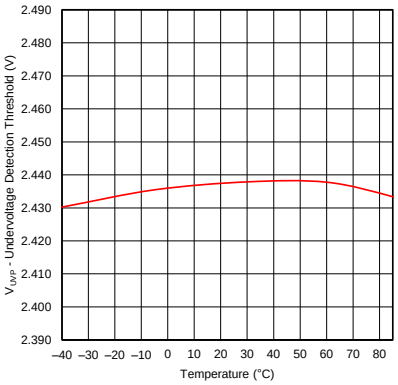
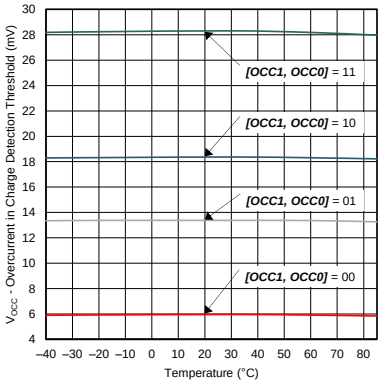


Figure 3. Overvoltage Detection Threshold vs Temperature



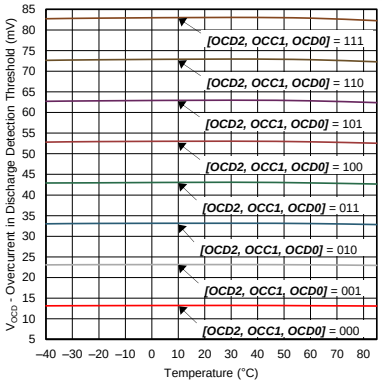
UVP threshold shown assumes an overvoltage setting of 4.450 V

Figure 4. Undervoltage Detection Threshold vs Temperature



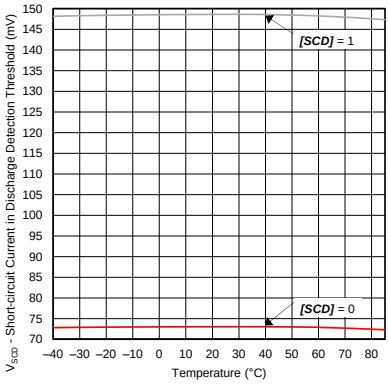
OCC thresholds shown assume an overvoltage setting of 4.450 V

Figure 5. Overcurrent in Charge Detection Threshold vs Temperature



OCD thresholds shown assume an overvoltage setting of 4.450 V

Figure 6. Overcurrent in Discharge Detection Threshold vs Temperature



SCD thresholds shown assume an overvoltage setting of 4.450 V

Figure 7. Short-Circuit in Discharge Detection Threshold vs Temperature

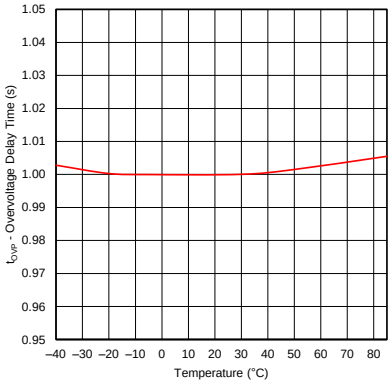


Figure 8. Overvoltage Delay Time

Typical Characteristics (continued)

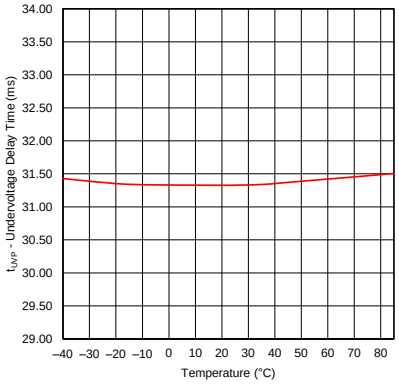


Figure 9. Undervoltage Delay Time

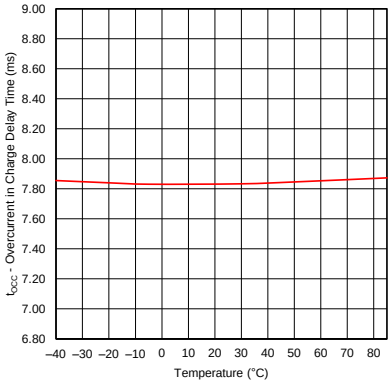


Figure 10. Overcurrent in Charge Delay Time vs Temperature

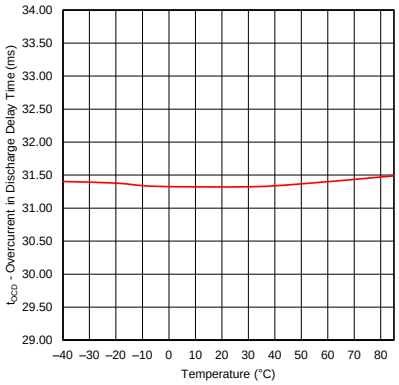


Figure 11. Overcurrent in Discharge Delay vs Temperature

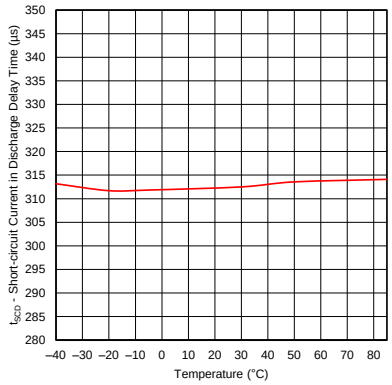
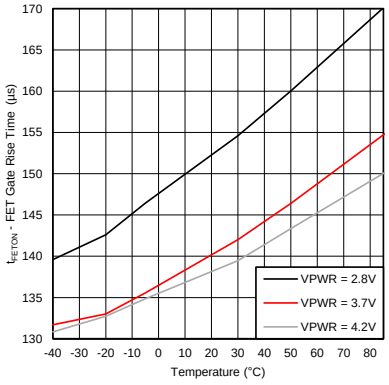
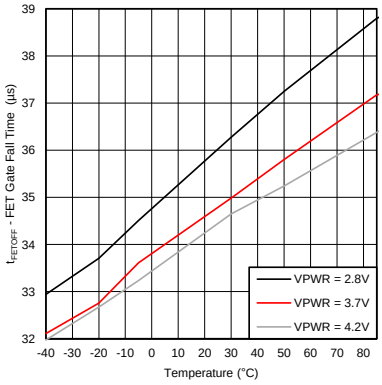


Figure 12. Short-Circuit in Discharge Delay vs Temperature



Performance with C_L = 4 nF

Figure 13. FET Gate Rise Time vs Temperature



Performance with C_L = 4 nF

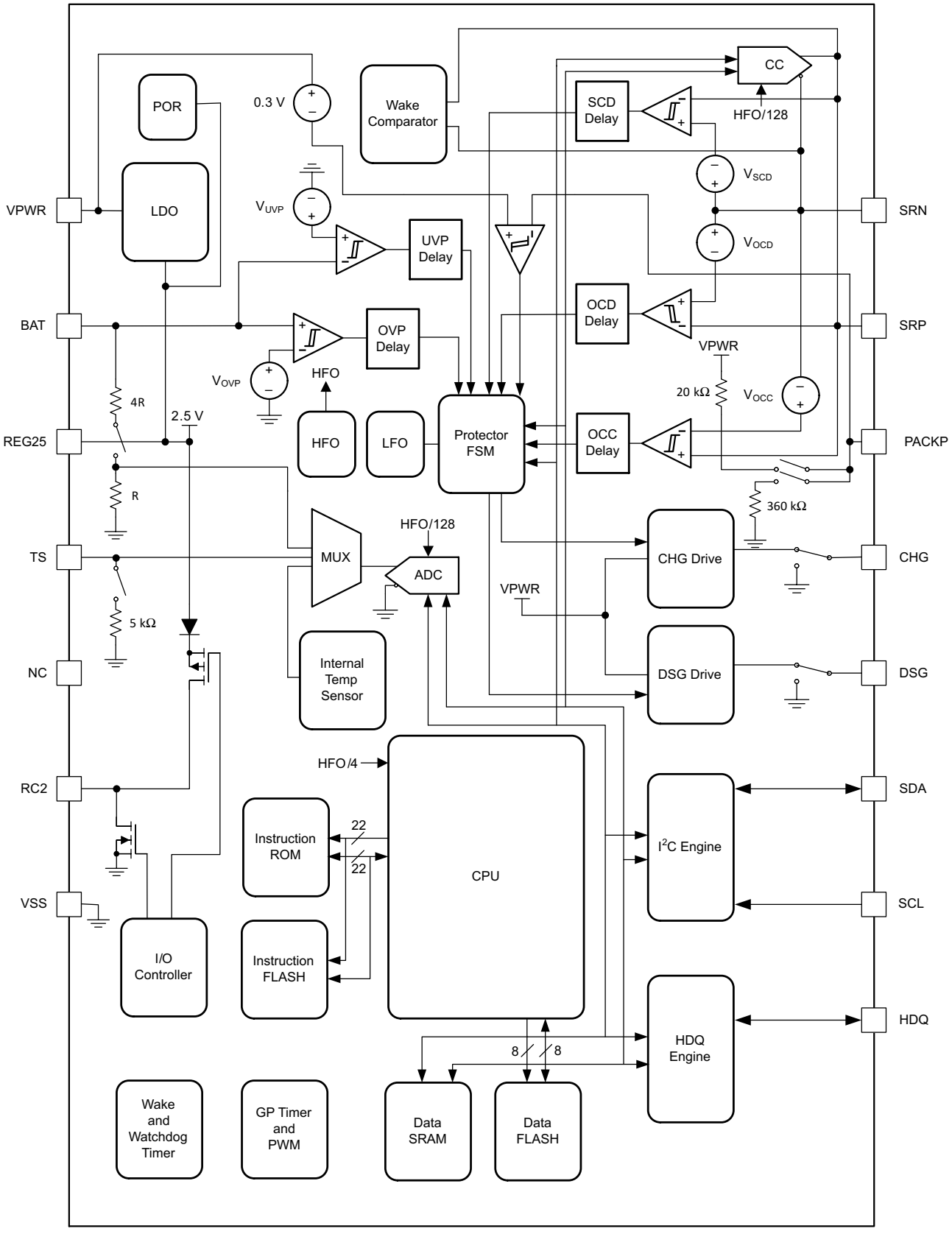
Figure 14. FET Gate Fall Time vs Temperature

7 Detailed Description

7.1 Overview

The bq27742-G1 fuel gauge accurately predicts the battery capacity and other operational characteristics of a single Li-based rechargeable cell. It can be interrogated by a system processor to provide cell information, such as state-of-charge (SOC), time-to-empty (TTE), and time-to-full (TTF).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Configuration

Cell information is stored in the fuel gauge in non-volatile flash memory. Many of these data flash locations are accessible during application development. They cannot, generally, be accessed directly during end-equipment operation. Access to these locations is achieved by either use of the companion evaluation software, through individual commands, or through a sequence of data-flash-access commands. To access a desired data flash location, the correct data flash subclass and offset must be known.

The fuel gauge provides 64 bytes of user-programmable data flash memory, partitioned into two 32-byte blocks: ***Manufacturer Info Block A*** and ***Manufacturer Info Block B***. This data space is accessed through a data flash interface.

7.3.2 Fuel Gauging

The key to the high-accuracy gas gauging prediction is Texas Instruments proprietary Impedance Track™ algorithm. This algorithm uses cell measurements, characteristics, and properties to create state-of-charge predictions that can achieve less than 1% error across a wide variety of operating conditions and over the lifetime of the battery.

See *Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm Application Note* (SLUA364) for further details.

7.3.3 Power Modes

To minimize power consumption, the fuel gauge has different power modes: NORMAL, SLEEP, and FULLSLEEP. The fuel gauge passes automatically between these modes, depending upon the occurrence of specific events, though a system processor can initiate some of these modes directly.

7.3.3.1 NORMAL Mode

The fuel gauge is in NORMAL mode when not in any other power mode. During this mode, *AverageCurrent()*, *Voltage()*, and *Temperature()* measurements are taken, and the interface data set is updated. Decisions to change states are also made. This mode is exited by activating a different power mode.

Because the fuel gauge consumes the most power in NORMAL mode, the Impedance Track™ algorithm minimizes the time the fuel gauge remains in this mode.

7.3.3.2 SLEEP Mode

SLEEP mode performs *AverageCurrent()*, *Voltage()*, and *Temperature()* less frequently which results in reduced power consumption. SLEEP mode is entered automatically if the feature is enabled (***Pack Configuration [SLEEP]*** = 1) and *AverageCurrent()* is below the programmable level ***Sleep Current***. Once entry into SLEEP mode has been qualified, but prior to entering it, the fuel gauge performs an ADC autocalibration to minimize offset.

During the SLEEP mode, the fuel gauge periodically takes data measurements and updates its data set. However, a majority of its time is spent in an idle condition.

The fuel gauge exits SLEEP if any entry condition is broken, specifically when either:

- *AverageCurrent()* rises above ***Sleep Current***, or
- A current in excess of I_{WAKE} through R_{SENSE} is detected.

Feature Description (continued)

7.3.3.3 FULLSLEEP Mode

FULLSLEEP mode turns off the high-frequency oscillator and performs *AverageCurrent()*, *Voltage()*, and *Temperature()* less frequently which results in power consumption that is lower than that of the SLEEP mode.

FULLSLEEP mode can be enabled by two methods:

- Setting the ***[FULLSLEEP]*** bit in the Control Status register using the FULL_SLEEP subcommand and ***Full Sleep Wait Time (FS Wait)*** in data flash is set as 0.
- Setting the ***Full Sleep Wait Time (FS Wait)*** in data flash to a number larger than 0. This method is disabled when the ***FS Wait*** is set as 0.

FULLSLEEP mode is entered automatically when it is enabled by one of the methods above. When the first method is used, the gauge enters the FULLSLEEP mode when the fuel gauge is in SLEEP mode. When the second method is used, the FULLSLEEP mode is entered when the fuel gauge is in SLEEP mode and the timer counts down to 0.

The fuel gauge exits the FULLSLEEP mode when there is any communication activity. Therefore, the execution of SET_FULLSLEEP sets the ***[FULLSLEEP]*** bit. The FULLSLEEP mode can be verified by measuring the current consumption of the gauge.

During FULLSLEEP mode, the fuel gauge periodically takes data measurements and updates its data set. However, a majority of its time is spent in an idle condition.

The fuel gauge exits SLEEP if any entry condition is broken, specifically when either:

- *AverageCurrent()* rises above ***Sleep Current***, or
- A current in excess of I_{WAKE} through R_{SENSE} is detected.

While in FULLSLEEP mode, the fuel gauge can suspend serial communications by as much as 4 ms by holding the comm line(s) low. This delay is necessary to correctly process host communication, because the fuel gauge processor is mostly halted in SLEEP mode.

7.3.4 Li-Ion Battery Protector Description

The battery protector controls two external high-side N-channel FETs in a back-to-back configuration for battery protection. The protector uses two voltage doublers to drive the CHG and DSG FETs on.

7.3.4.1 High-Side NFET Charge and Discharge FET Drive

These FETs are automatically turned off by the protector based on the detected hardware protection faults or by the fuel gauge based on detected firmware protection faults. This enables the gauge to be configured with effectively two levels of safety: the first level employing conservative protection settings to keep the cell within a safe operating area and the second level set to act as a fail-safe measure to prevent cell damage. Once the protection fault(s) is deemed to be cleared, the protector or fuel gauge will re-enable the applicable FET(s). Additionally, the FET drivers can be manually tested at production using the *FETTest*(0x74/0x75) extended command if needed.

7.3.4.2 Protector Configuration

The integrated Li-Ion hardware protector includes full programmability of its fault detection thresholds, eliminating the need to order several part variants to accommodate different system safety threshold needs. Configuration of the thresholds is provided in the form of data flash parameters, ***Prot OV Config*** and ***Prot OC Config***, which are bit-mapped to two simple lookup tables that determine the protector safety thresholds. Table 3 through Table 6 detail the protection settings available for hardware overvoltage, overcurrent in charge, overcurrent in discharge, and short-circuit in discharge, respectively. An added degree of flexibility is made possible in combining the programmable thresholds with changes to the selected sense resistor value, enabling a wide variety of Li-Ion protection options in a single device.

Feature Description (continued)

Table 3. Hardware Overvoltage Protection Configuration

Prot OV Config			OVERVOLTAGE (V_{OVP}) SETTING
[OVP2]	*[OVP1]*	*[OVP0]*	
0	0	0	4.275 V
0	0	1	4.300 V
0	1	0	4.325 V
0	1	1	4.350 V
1	0	0	4.375 V
1	0	1	4.400 V
1	1	0	4.425 V
1	1	1	4.450 V (default)

Table 4. Hardware Overcurrent in Charge Configuration

Prot OC Config		OVERCURRENT IN CHARGE (V_{OCC}) SETTING
[OCC1]	*[OCC0]*	
0	0	6 mV
0	1	13 mV
1	0	18 mV (default)
1	1	28 mV

Table 5. Hardware Overcurrent in Discharge Configuration

Prot OC Config			OVERCURRENT IN DISCHARGE (V_{OCD}) SETTING
[OCD1]	*[OCD0]*	*[OCD0]*	
0	0	0	14 mV
0	0	1	24 mV
0	1	0	34 mV (default)
0	1	1	44 mV
1	0	0	53 mV
1	0	1	63 mV
1	1	0	73 mV
1	1	1	83 mV

Table 6. Hardware Short-Circuit in Discharge Configuration

Prot OC Config	SHORT-CIRCUIT IN DISCHARGE (V_{SCD}) SETTING
[SCD]	
0	73 mV (default)
1	148 mV

7.4 Device Functional Modes

7.4.1 Operating Modes

The battery protector has several operating modes depending on a variety of conditions. The various modes are described below:

- NORMAL Mode
- OVERVOLTAGE Mode
- UNDERVOLTAGE Mode
- OVERCURRENT IN DISCHARGE and SHORT-CIRCUIT IN DISCHARGE Mode
- Overcurrent in Charge Mode

Device Functional Modes (continued)

- SHUTDOWN WAIT Mode
  - ANALOG SHUTDOWN State
  - LOW VOLTAGE CHARGING State

The relationships among these modes are shown in Figure 15.

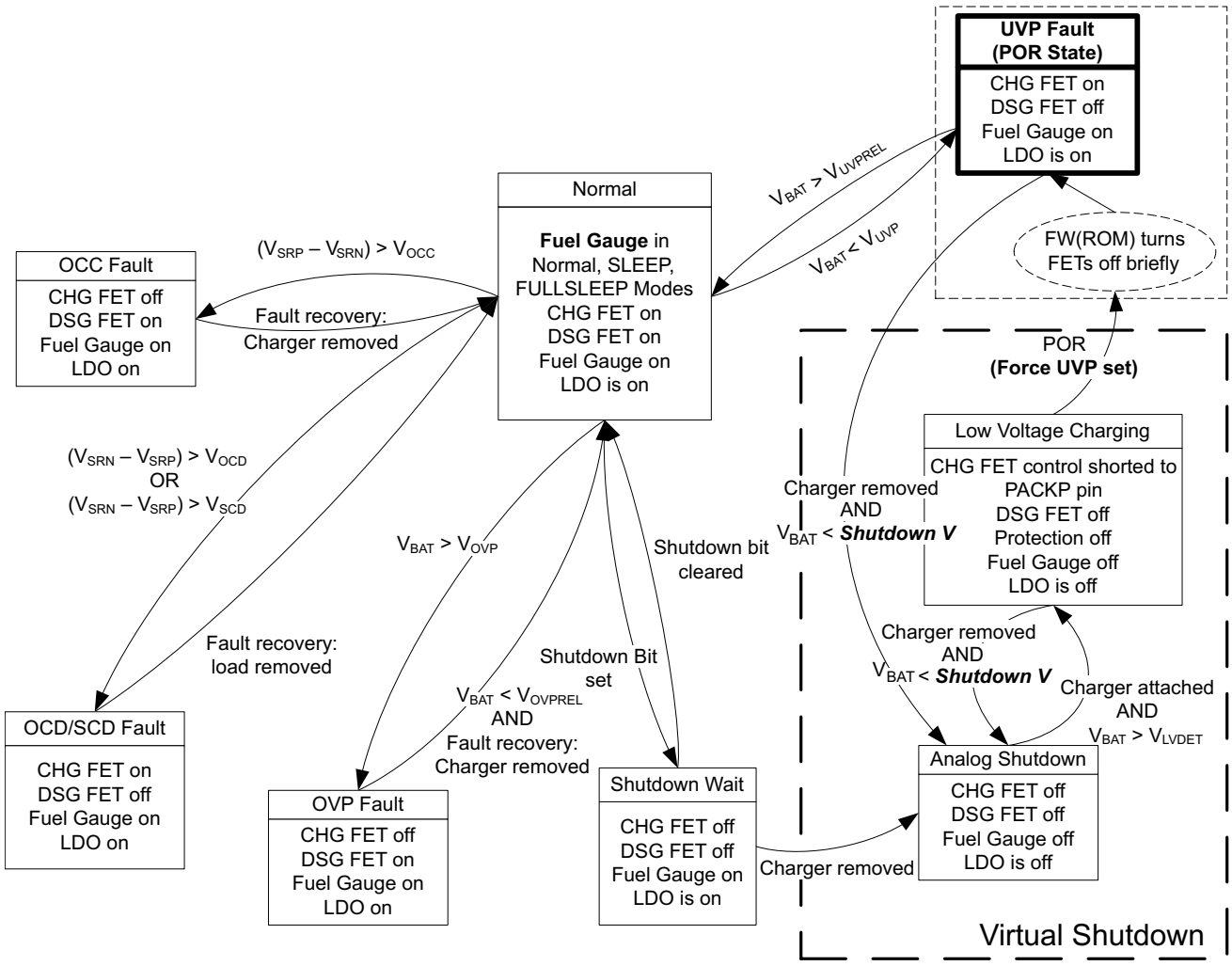


Figure 15. Operating Modes

7.4.1.1 NORMAL Mode

In this mode, the protector is fully powered and operational. Both CHG and DSG FETs are closed and the protector continuously checks for fault conditions.

FET enable override capability is available to the fuel gauge to force the CHG or DSG FET open based on firmware instruction. It is useful for firmware-defined safety features or other special functionality that requires one or both FETs to be opened based on specific conditions. It cannot, however, be used to enforce FET turn-on when the hardware protector is one of the protection fault modes, as the latter has ultimate authority over the FET drive control circuitry.

Firmware can also command the fuel gauge to go into SHUTDOWN mode based on a dedicated *Control()* subcommand from the host. In this case, firmware sets the Shutdown bit to indicate intent to go into SHUTDOWN mode. The fuel gauge then transitions to SHUTDOWN WAIT mode and waits for charger removal prior to disabling the internal LDO and fully powering down the entire device.

Device Functional Modes (continued)

7.4.1.2 OVERVOLTAGE Mode

In this mode, an overvoltage protection (OVP) fault mode is entered when the voltage on the V_{BAT} pin continuously exceeds the V_{OVP} threshold for longer than the t_{OVP} delay time. At this point, the fuel gauge enables the fault recovery detection circuitry, which monitors the PACKP pin for charger removal. The OVP fault is cleared once the pack voltage drops below the cell voltage by more than 300 mV and the cell voltage drops below V_{OVPREL}, which causes the fuel gauge to transition to NORMAL mode.

7.4.1.3 UNDERVOLTAGE Mode

In this mode, an undervoltage protection (UVP) fault mode is entered when the voltage on the V_{BAT} pin continuously falls below the V_{UVP} threshold for longer than the t_{UVP} delay time. The fuel gauge then enables the charger attach detection circuitry and, if no charger is found, sends the fuel gauge into ANALOG SHUTDOWN mode to minimize power consumption and avoid further discharge of the battery. The UVP fault is cleared once charger attach is detected and the cell voltage rises above V_{UVPREL}, which causes the fuel gauge to transition to NORMAL mode.

The fuel gauge can enter this mode from LOW VOLTAGE CHARGING mode when the battery pack is being charged from a deeply discharged state or from NORMAL mode when the battery pack is being discharged past the UVP threshold.

7.4.1.4 OVERCURRENT CHARGE Mode

In this mode, an overcurrent in charge (OCC) fault mode is entered when the voltage across the sense resistor continuously exceeds the V_{OCC} threshold for longer than the configured t_{OCC} delay time. Recovery occurs when the PACKP voltage drops to more than 300 mV below the cell voltage, indicating charger removal.

7.4.1.4.1 OVERCURRENT DISCHARGE and SHORT-CIRCUIT DISCHARGE Mode

In this mode, a short-circuit discharge (SCD) or overcurrent discharge (OCD) protection fault is detected when the voltage across the sense resistor continuously exceeds the V_{OCD} or V_{SCD} thresholds for longer than the t_{OCD} or t_{SCD}delay times. Recovery occurs when the PACKP voltage rises to within 300 mV of the cell voltage, indicating load removal.

7.4.1.5 SHUTDOWN WAIT Mode

A transition to this mode occurs when the host sends the SET_SHUTDOWN command and the fuel gauge subsequently initiated the shutdown sequence.

The shutdown sequence is as follows:

1. Open both CHG and DSG FETs.
2. Determine if any faults are set. If any faults are set, then go back to NORMAL mode.
3. Wait for charger removal. Once the charger is removed, turn off the LDO, which puts the fuel gauge into ANALOG SHUTDOWN mode.

7.4.1.5.1 ANALOG SHUTDOWN State

In this mode, the fuel gauge is completely powered down and no portions of the device are functional. Once the charger is connected, the fuel gauge will transition into either LOW VOLTAGE CHARGING mode (if below the power-on reset voltage) or NORMAL mode (if above the POR voltage and no faults are detected).

7.4.1.6 LOW VOLTAGE CHARGING State

In this mode, the fuel gauge shorts the CHG FET gate to PACKP pin if the cell voltage is above the V_{LVDET} threshold, allowing the battery to be trickle charged with the CHG FET biased in the ohmic region. If below the aforementioned threshold, low voltage charging is prohibited for safety reasons and the cell will likely be permanently unrecoverable due to being dangerously depleted.

7.4.2 Firmware Control of Protector

The firmware has control to open the CHG FET or DSG FET independently by overriding hardware control. However, it has no control to close the CHG FET or DSG FET and can only disable the FET override.

Device Functional Modes (continued)

7.4.3 OVERTEMPERATURE FAULT Mode

Gauging firmware monitors temperature every second and will open either the CHG FET if *Temperature()* > ***OT Chg*** for ***OT Chg Time*** in CHARGING mode or open the DSG FET if *Temperature()* > ***OT Dsg*** for ***OT Dsg Time*** in DISCHARGING mode. Gauge determination of charge or discharge mode is based on *Current()* > ***Chg Current Threshold*** for ***Quit Relax Time*** or *Current()* < ***Dsg Current Threshold*** for ***Quit Relax Time***. Recovery from the given overtemperature fault occurs when *Temperature()* < ***OT Chg Recovery*** or < ***OT Dsg Recovery***, depending on if a charge overtemperature or discharge overtemperature fault is present.

7.4.4 Wake-Up Comparator

The wake-up comparator indicates a change in cell current while the fuel gauge is in SLEEP mode. Wake comparator threshold can be configured in firmware and set to the thresholds in Table 7. An internal event is generated when the threshold is breached in either charge or discharge directions.

Table 7. I_{WAKE} Threshold Settings(1)

RSNS1	RSNS0	IWAKE	Vth(SRP-SRN)
0	0	0	Disabled
0	0	1	Disabled
0	1	0	1.0 mV or –1.0 mV
0	1	1	2.2 mV or –2.2 mV
1	0	0	2.2 mV or –2.2 mV
1	0	1	4.6 mV or –4.6 mV
1	1	0	4.6 mV or –4.6 mV
1	1	1	9.8 mV or –9.8 mV

(1) The actual resistance value versus the setting of the sense resistor is not important just the actual voltage threshold when calculating the configuration. The voltage thresholds are typical values under room temperature.

7.5 Battery Parameter Measurements

7.5.1 Charge and Discharge Counting

The integrating delta-sigma ADC measures the charge or discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SRP and SRN pins. The integrating ADC measures bipolar signals and detects charge activity when $V_{SR} = V_{SRP} – V_{SRN}$ is positive and discharge activity when $V_{SR} = V_{SRP} – V_{SRN}$ is negative. The fuel gauge continuously integrates the signal over time using an internal counter.

7.5.2 Voltage

The fuel gauge updates cell voltages at 1-second intervals when in NORMAL mode. The internal ADC of the fuel gauge measures the voltage, and scales and calibrates it appropriately. Voltage measurement is automatically compensated based on temperature. This data is also used to calculate the impedance of the cell for Impedance Track™ fuel gauging.

7.5.3 Current

The fuel gauge uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a 5-mΩ to 20-mΩ typical sense resistor.

7.5.4 Auto-Calibration

The fuel gauge provides an auto-calibration feature to cancel the voltage offset error across SRN and SRP for maximum charge measurement accuracy. The fuel gauge performs auto-calibration before entering the SLEEP mode.

Battery Parameter Measurements (continued)

7.5.5 Temperature

The fuel gauge external temperature sensing is optimized with the use of a high-accuracy negative temperature coefficient (NTC) thermistor with R25 = 10 kΩ ± 1% and B25/85 = 3435 kΩ ± 1% (such as Semitec 103AT for measurement). The fuel gauge can also be configured to use its internal temperature sensor. The fuel gauge uses temperature to monitor the battery-pack environment, which is used for fuel gauging and cell protection functionality.

NOTE

Formatting Conventions in This Document:

Commands: *italics* with parentheses and no breaking spaces, for example, *RemainingCapacity()*.

Data Flash: *italics*, **bold**, and breaking spaces, for example, ***Design Capacity***.

Register Bits and Flags: brackets only, for example, [TDA]

Data Flash Bits: *italic* and **bold**, for example, ***[XYZ1]***

Modes and states: ALL CAPITALS, for example, UNSEALED mode.

7.6 Communications

7.6.1 HDQ Single-Pin Serial Interface

The HDQ interface is an asynchronous return-to-one protocol where a processor sends the command code to the fuel gauge. With HDQ, the least significant bit (LSB) of a data byte (command) or word (data) is transmitted first. The DATA signal on pin 12 is open-drain and requires an external pullup resistor. The 8-bit command code consists of two fields: the 7-bit HDQ command code (bits 0 through 6) and the 1-bit RW field (MSB bit 7). The RW field directs the fuel gauge either to:

- Store the next 8 bits of data to a specified register, or
- Output 8 bits of data from the specified register

The HDQ peripheral can transmit and receive data as either an HDQ master or slave.

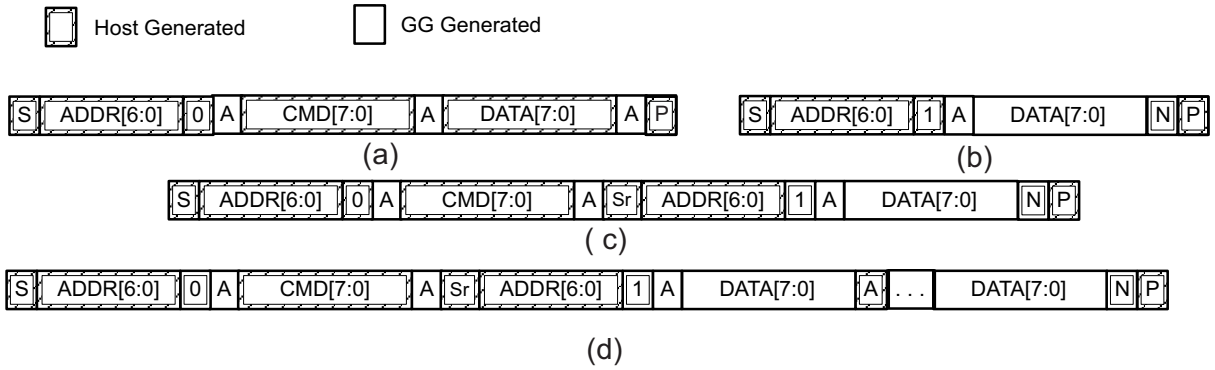
HDQ serial communication is normally initiated by the host processor sending a break command to the fuel gauge. A break is detected when the DATA pin is driven to a logic low state for a time $t_{(B)}$ or greater. The DATA pin then is returned to its normal ready logic high state for a time $t_{(BR)}$. The fuel gauge is now ready to receive information from the host processor.

The fuel gauge is shipped in the I^2C mode. TI provides tools to enable the HDQ peripheral.

7.6.2 I^2C Interface

The fuel gauge supports the standard I^2C read, incremental read, one-byte write quick read, and functions. The 7-bit device address (ADDR) is the most significant 7 bits of the hex address and is fixed as 1010101. The 8-bit device address is therefore 0xAA or 0xAB for write or read, respectively.

Communications (continued)

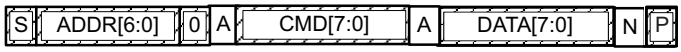


A. 1-byte write; b. Quick read; c. 1-byte read; Incremental read (S = Start, Sr = Repeated Start, A = Acknowledge, N = No Acknowledge, and P = Stop)

Figure 16. Supported I²C Formats

The quick read returns data at the address indicated by the address pointer. The address pointer, a register internal to the I²C communication engine, increments whenever data is acknowledged by the fuel gauge or the I²C master. Quick writes function in the same manner and are a convenient means of sending multiple bytes to consecutive command locations (such as two-byte commands that require two bytes of data).

Attempt to write a read-only address (NACK after data sent by master):



Attempt to read an address above 0x7F (NACK command):

Attempt at incremental writes (NACK all extra data bytes sent):

Incremental read at the maximum allowed read address:

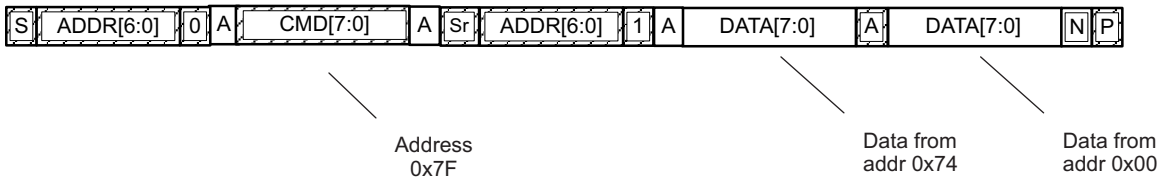


Figure 17. I²C Interfaces

The I²C engine releases both SDA and SCL if the I²C bus is held low for $t_{(BUSERR)}$. If the fuel gauge was holding the lines, releasing them frees the master to drive the lines. If an external condition is holding either of the lines low, the I²C engine enters the low-power SLEEP mode.

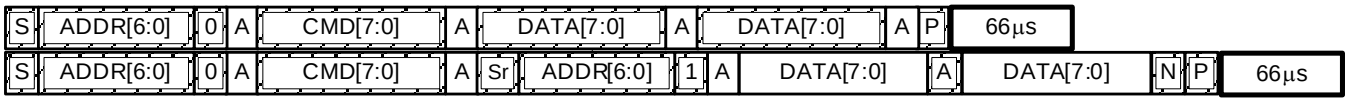
7.6.2.1 I²C Time Out

The I²C engine releases both SDA and SCL lines if the I²C bus is held low for about 2 seconds. If the fuel gauge was holding the lines, releasing them frees the master to drive the lines.

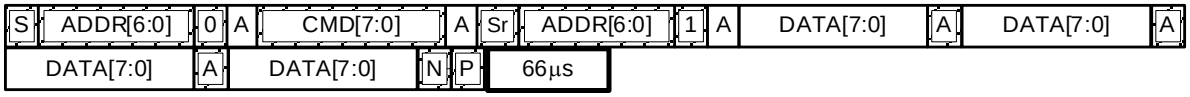
Communications (continued)

7.6.2.2 I²C Command Waiting Time

To ensure the correct results of a command with the 400-kHz I²C operation, a proper waiting time must be added between issuing a command and reading the results. For subcommands, the following diagram shows the waiting time required between issuing the control command and reading the status with the exception of the checksum command. A 100-ms waiting time is required between the checksum command and reading the result. For read-write standard commands, a minimum of 2 seconds is required to get the result updated. For read-only standard commands, there is no waiting time required, but the host must not issue any standard command more than two times per second. Otherwise, the gauge could result in a reset issue due to the expiration of the watchdog timer.



Waiting time between control subcommand and reading results



Waiting time between continuous reading results

Figure 18. I²C Command Waiting Time

The I²C clock stretch could happen in a typical application. A maximum 80-ms clock stretch could be observed during the flash updates. There is up to a 270-ms clock stretch after the OCV command is issued.

7.7 Standard Data Commands

The fuel gauge uses a series of 2-byte standard commands to enable system reading and writing of battery information. Each standard command has an associated command-code pair, as indicated in Table 8. Each protocol has specific means to access the data at each Command Code. Data RAM is updated and read by the gauge only once per second. Standard commands are accessible in NORMAL operation mode.

Table 8. Standard Commands

COMMAND NAME	COMMAND CODE	UNIT	SEALED ACCESS
Control()	0x00 and 0x01	—	RW
AtRate()	0x02 and 0x03	mA	RW
UnfilteredSOC()	0x04 and 0x05	%	R
Temperature()	0x06 and 0x07	0.1°K	R
Voltage()	0x08 and 0x09	mV	R
Flags()	0x0A and 0x0B	—	R
NomAvailableCapacity()	0x0C and 0x0D	mAh	R
FullAvailableCapacity()	0x0E and 0x0F	mAh	R
RemainingCapacity()	0x10 and 0x11	mAh	R
FullChargeCapacity()	0x12 and 0x13	mAh	R
AverageCurrent()	0x14 and 0x15	mA	R
TimeToEmpty()	0x16 and 0x17	min	R
FilteredFCC()	0x18 and 0x19	mAh	R
SafetyStatus()	0x1A and 0x1B	—	R
UnfilteredFCC()	0x1C and 0x1D	mAh	R
Imax()	0x1E and 0x1F	mA	R
UnfilteredRM()	0x20 and 0x21	mAh	R
FilteredRM()	0x22 and 0x23	mAh	R

Standard Data Commands (continued)

Table 8. Standard Commands (continued)

COMMAND NAME	COMMAND CODE	UNIT	SEALED ACCESS
BTPSOC1Set()	0x24 and 0x25	mAh	RW
BTPSOC1Clear()	0x26 and 0x27	mAh	RW
InternalTemperature()	0x28 and 0x29	0.1°K	R
CycleCount()	0x2A and 0x2B	Counts	R
StateofCharge()	0x2C and 0x2D	%	R
StateofHealth()	0x2E and 0x2F	%/num	R
ChargingVoltage()	0x30 and 0x31	mV	R
ChargingCurrent)	0x32 and 0x33	mA	R
PassedCharge()	0x34 and 0x35	mAh	R
DOD0()	0x36 and 0x37	hex	R
SelfDischargeCurrent()	0x34 and 0x35	mA	R

7.7.1 Control(): 0x00 and 0x01

Issuing a *Control()* command requires a subsequent 2-byte subcommand. These additional bytes specify the particular control function desired. The *Control()* command allows the system to control specific features of the fuel gauge during normal operation and additional features when the fuel gauge is in different access modes, as described in Table 9.

Table 9. *Control()* Subcommands

SUBCOMMAND NAME	SUBCOMMAND CODE	SEALED ACCESS	DESCRIPTION
CONTROL_STATUS	0x0000	Yes	Reports the status of DF Checksum, Impedance Track™, etc.
DEVICE_TYPE	0x0001	Yes	Reports the device type of 0x0742 (indicating bq27742-G1).
FW_VERSION	0x0002	Yes	Reports the firmware version on the device type.
HW_VERSION	0x0003	Yes	Reports the hardware version on the device type.
PROTECTOR_VERSION	0x0004	Yes	Reports the hardware protector version on the device type.
RESET_DATA	0x0005	Yes	Returns reset data.
PREV_MACWRITE	0x0007	Yes	Returns previous *Control()* subcommand code.
CHEM_ID	0x0008	Yes	Reports the chemical identifier of the Impedance Track™ configuration.
BOARD_OFFSET	0x0009	No	Forces the device to measure and store the board offset.
CC_OFFSET	0x000A	No	Forces the device to measure the CC offset.
DF_VERSION	0x000C	Yes	Reports the data flash version of the device.
SET_FULLSLEEP	0x0010	Yes	Sets the *CONTROL_STATUS[FULLSLEEP]* bit to 1.
SET_SHUTDOWN	0x0013	Yes	Sets the *CONTROL_STATUS[SHUTDWN]* bit to 1.
CLEAR_SHUTDOWN	0x0014	Yes	Clears the *CONTROL_STATUS[SHUTDWN]* bit to 1.
STATIC_CHEM_CHKSUM	0x0017	Yes	Calculates chemistry checksum.
ALL_DF_CHKSUM	0x0018	Yes	Reports checksum for all data flash excluding device specific variables.
STATIC_DF_CHKSUM	0x0019	Yes	Reports checksum for static data flash excluding device specific variables.
PROTECTOR_CHKSUM	0x001A	Yes	Reports checksum for protector configuration data flash excluding device specific variables.
SEALED	0x0020	No	Places the fuel gauge in SEALED access mode.
IT_ENABLE	0x0021	No	Enables the Impedance Track™ algorithm.
IMAX_INT_CLEAR	0x0023	Yes	Clears an Imax interrupt that is currently asserted on the RC2 pin.
START_FET_TEST	0x0024	No	Starts FET Test based on data entered in *FETTest()* register. Sets and clears the *[FETTST]* bit in *CONTROL_STATUS*.
CAL_ENABLE	0x002D	No	Toggle CALIBRATION mode.
RESET	0x0041	No	Forces a full reset of the fuel gauge.

Table 9. *Control()* Subcommands (continued)

SUBCOMMAND NAME	SUBCOMMAND CODE	SEALED ACCESS	DESCRIPTION
EXIT_CAL	0x0080	No	Exit CALIBRATION mode.
ENTER_CAL	0x0081	No	Enter CALIBRATION mode.
OFFSET_CAL	0x0082	No	Reports internal CC offset in CALIBRATION mode.

7.8 Extended Data Commands

Extended commands offer additional functionality beyond the standard set of commands. They are used in the same manner; however unlike standard commands, extended commands are not limited to 2-byte words. The number of command bytes for a given extended command ranges in size from single to multiple bytes, as specified in Table 10. For details on the SEALED and UNSEALED states, see the *Access Modes* section in the *bq27742-G1 Technical Reference Manual* (SLUUAX0).

Table 10. Extended Commands

NAME	COMMAND CODE	UNIT	SEALED ACCESS (1) (2)	UNSEALED ACCESS (1) (2)
PackConfiguration()	0x3A and 0x3B	Hex	R	R
DesignCapacity()	0x3C and 0x3D	mAh	R	R
DataFlashClass() (2)	0x3E	NA	NA	RW
DataFlashBlock() (2)	0x3F	NA	RW	RW
BlockData()/Authenticate() (3)	0x40 to 0x53	NA	RW	RW
BlockData()/AuthenticateCheckSum() (3)	0x54	NA	RW	RW
BlockData()	0x55 to 0x5F	NA	R	RW
BlockDataCheckSum()	0x60	NA	RW	RW
BlockDataControl()	0x61	NA	NA	RW
DODatEOC()	0x62 and 0x63	NA	R	R
Qstart()	0x64 and 0x65	mAh	R	R
FastQmax()	0x66 and 0x67	mAh	R	R
Reserved	0x68 to 0x6C	NA	R	R
ProtectorStatus()	0x6D	Hex	R	R
Reserved	0x6E and 0x6F	NA	R	R
SimultaneousCurrent()	0x70 and 0x71	mA	R	R
Reserved	0x72 and 0x73	NA	R	R
FETTest()	0x74 and 0x75	Hex	R	RW
AveragePower()	0x76 and 0x77	mW or cW	R	R
ProtectorState()	0x78	Hex	R	R
AN_COUNTER	0x79			
AN_CURRENT_LSB	0x7A			
AN_CURRENT_MSB	0x7B			
AN_VCELL_LSB	0x7C			
AN_VCELL_MSB	0x7D			
AN_TEMP_LSB	0x7E			
AN_TEMP_MSB	0x7F			

(1) SEALED and UNSEALED states are entered via commands to *Control()* 0x00 and 0x01
(2) In SEALED mode, data flash cannot be accessed through commands 0x3E and 0x3F.
(3) The *BlockData()* command area shares functionality for accessing general data flash and for using Authentication. See *Authentication* in the *bq27742-G1 Technical Reference Manual* (SLUUAX0) for more details.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The bq27742-G1 is a single-cell fuel gauge with integrated Li-Ion protection circuitry for highly accurate detection of overvoltage, undervoltage, overcurrent in charge, overcurrent in discharge, and short-circuit in discharge fault conditions. If the detected fault continues to be present for a specific delay time (pre-configured in the device), the protection front-end will disable the applicable charge pump circuit, resulting in opening of the FET until the provoking safety condition resolves. The integrated 16-bit delta-sigma converters provide accurate, high precision measurements for voltage, current, and temperature in order to accomplish effective battery monitoring, protection, and gauging. To allow for optimal performance in the end application, special considerations must be taken to ensure minimization of measurement error through proper printed circuit board (PCB) board layout and correct configuration of battery characteristics in the fuel gauge data flash. Such requirements are detailed in *Design Requirements*.

8.2 Typical Applications

8.2.1 Pack-Side, Single-Cell Li-Ion Fuel Gauge and Protector

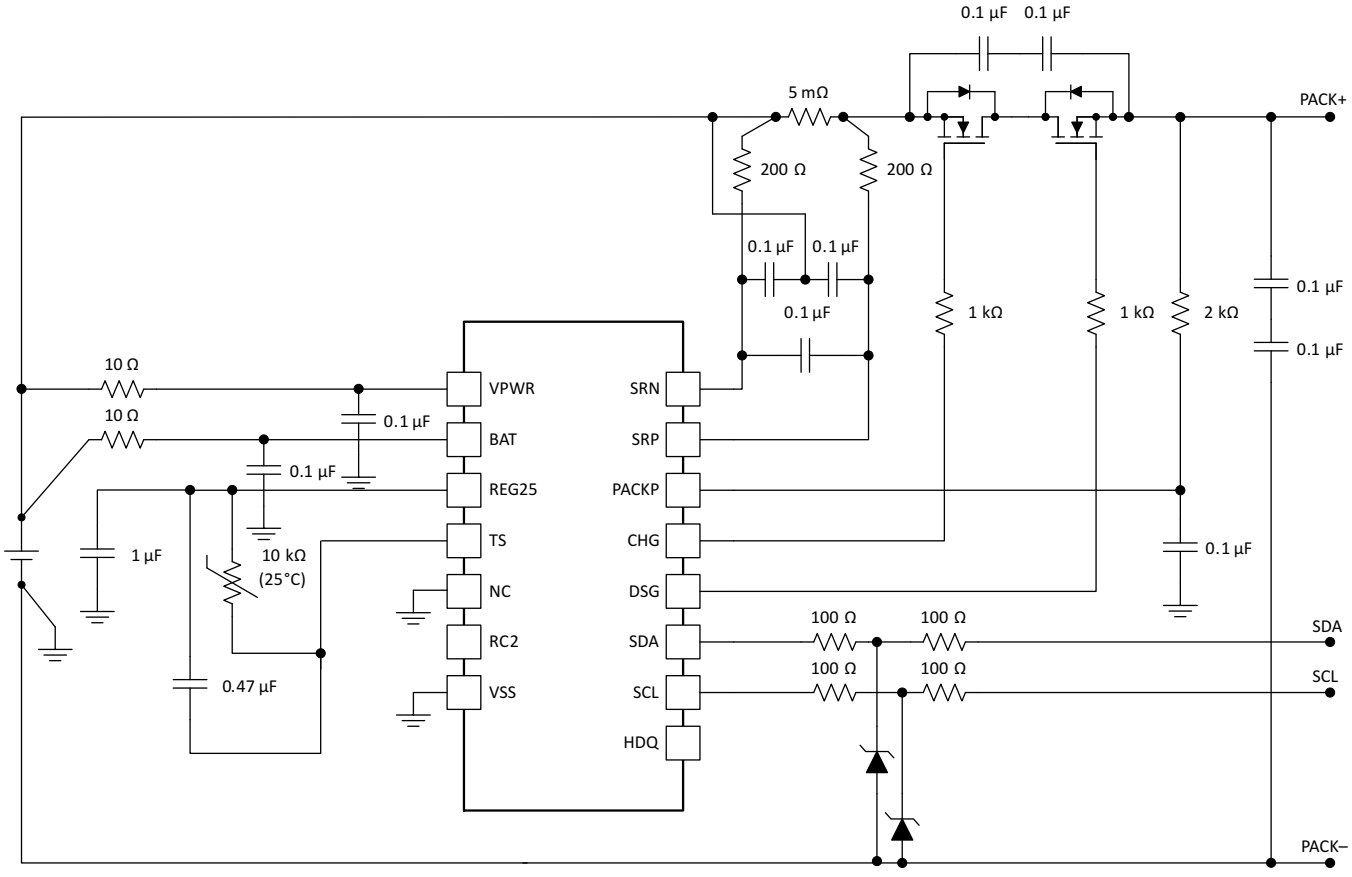


Figure 19. I²C Mode Schematic

Typical Applications (continued)

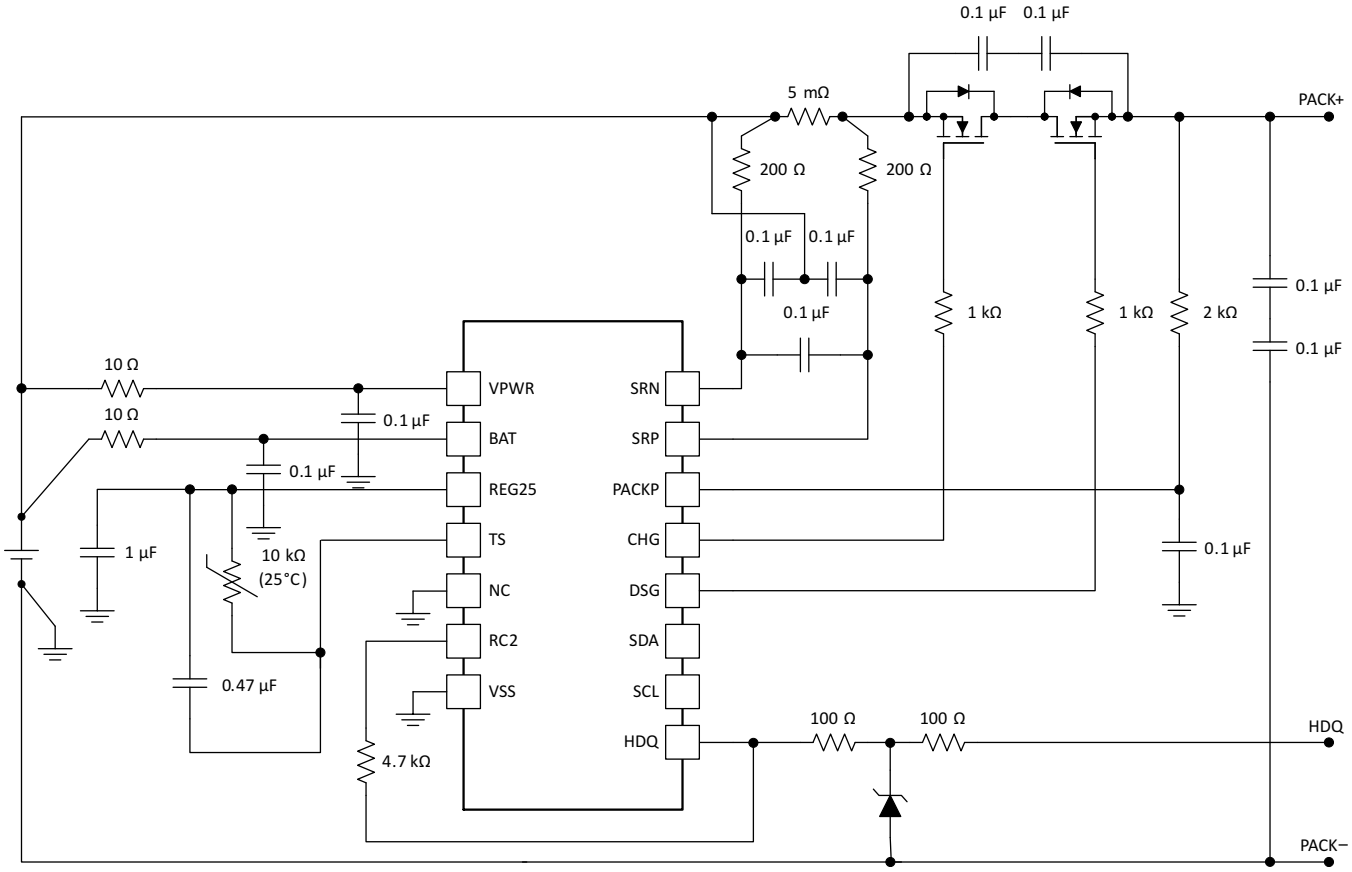


Figure 20. HDQ Mode Schematic

8.2.2 Design Requirements

Several key parameters must be updated to align with a given application's battery characteristics. For highest accuracy gauging, it is important to follow-up this initial configuration with a learning cycle to optimize resistance and maximum chemical capacity (Qmax) values prior to sealing and shipping packs to the field. Successful and accurate configuration of the fuel gauge for a target application can be used as the basis for creating a "golden" gas gauge (.GG) file that can be written to all production packs, assuming identical pack design and Li-Ion cell origin (chemistry, lot, etc.). Calibration data can be included as part of this golden GG file to cut down on battery pack production time. If going this route, it is recommended to average the calibration data from a large sample size and use these in the golden file. Ideally, it is recommended to calibrate all packs individually as this will lead to the highest performance and lowest measurement error in the end application on a per-pack basis. In addition, the integrated protection functionality should be correctly configured to ensure activation based on the fault protection needs of the target pack design, or else accidental trip could be possible if using defaults. Table 11, *Key Data Flash Parameters for Configuration*, shows the items that should be configured to achieve reliable protection and accurate gauging with minimal initial configuration.

Table 11. Key Data Flash Parameters for Configuration

NAME	DEFAULT	UNIT	RECOMMENDED SETTING
Design Capacity	1000	mAh	Set based on the nominal pack capacity as interpreted from cell manufacturer's datasheet. If multiple parallel cells are used, should be set to N * Cell Capacity.
Design Energy	3800	mWh	Set based on the nominal pack energy (nominal cell voltage * nominal cell capacity) as interpreted from the cell manufacturer's datasheet. If multiple parallel cells are used, should be set to N * Cell Energy.

Typical Applications (continued)

Table 11. Key Data Flash Parameters for Configuration (continued)

NAME	DEFAULT	UNIT	RECOMMENDED SETTING
Design Energy Scale	1	—	Set to 10 to convert all power values to cWh or to 1 for mWh. ***Design Energy*** is divided by this value.
Reserve Capacity	0	mAh	Set to desired runtime remaining (in seconds/3600) * typical applied load between reporting 0% SOC and reaching ***Terminate Voltage***, if needed.
Design Voltage	3800	mV	Set to nominal cell voltage per manufacturer datasheet.
Cycle Count Threshold	900	mAh	Set to 90% of configured ***Design Capacity***
Device Chemistry	0354	hex	Should be configured using TI-supplied Battery Management Studio software. Default open-circuit voltage and resistance tables are also updated in conjunction with this step. Do not attempt to manually update reported Device Chemistry as this does not change all chemistry information! Always update chemistry using the appropriate software tool (that is, BMS).
Load Mode	1	—	Set to applicable load model, 0 for constant current or 1 for constant power.
Load Select	1	—	Set to load profile which most closely matches typical system load.
Qmax Cell 0	1000	mAh	Set to initial configured value for Design Capacity. The gauge will update this parameter automatically after the optimization cycle and for every regular Qmax update thereafter.
V at Chg Term	4350	mV	Set to nominal cell voltage for a fully charged cell. The gauge will update this parameter automatically each time full charge termination is detected.
Terminate Voltage	3000	mV	Set to empty point reference of battery based on system needs. Typical is between 3000 and 3200 mV.
Ra Max Delta	43	mΩ	Set to 15% of Cell0 R_a 4 resistance after an optimization cycle is completed.
Charging Voltage	4350	mV	Set based on nominal charge voltage for the battery in normal conditions (25°C, etc). Used as the reference point for offsetting by ***Taper Voltage*** for full charge termination detection.
Taper Current	100	mA	Set to the nominal taper current of the charger + taper current tolerance to ensure that the gauge will reliably detect charge termination.
Taper Voltage	100	mV	Sets the voltage window for qualifying full charge termination. Can be set tighter to avoid or wider to ensure possibility of reporting 100% SOC in outer JEITA temperature ranges that use derated charging voltage.
Dsg Current Threshold	60	mA	Sets threshold for gauge detecting battery discharge. Should be set lower than minimal system load expected in the application and higher than ***Quit Current***.
Chg Current Threshold	75	mA	Sets the threshold for detecting battery charge. Can be set higher or lower depending on typical trickle charge current used. Also should be set higher than ***Quit Current***.
Quit Current	40	mA	Sets threshold for gauge detecting battery relaxation. Can be set higher or lower depending on typical standby current and exhibited in the end system.
Avg I Last Run	–299	mA	Current profile used in capacity simulations at onset of discharge or at all times if ***Load Select*** = 0. Should be set to nominal system load. Is automatically updated by the gauge every cycle.
Avg P Last Run	–1131	mW	Power profile used in capacity simulations at onset of discharge or at all times if ***Load Select*** = 0. Should be set to nominal system power. Is automatically updated by the gauge every cycle.
Sleep Current	15	mA	Sets the threshold at which the fuel gauge enters SLEEP Mode. Take care in setting above typical standby currents else entry to SLEEP may be unintentionally blocked.
Shutdown V	0	mV	If auto-shutdown of fuel gauge is required prior to protect against accidental discharge to undervoltage condition, set this to desired voltage threshold for completely powering down the fuel gauge. Recovery occurs when a charger is connected.
T1 Temp	0	°C	Sets the boundary between charging inhibit/suspend and charging with T1-T2 parameters. Defaults set based on recommended values from JEITA standard.
T2 Temp	10	°C	Sets the boundary between charging with T1-T2 or T2-T3 parameters. Defaults set based on recommended values from JEITA standard.
T3 Temp	45	°C	Sets the boundary between charging with T2-T3 or T3-T4 parameters. Defaults set based on recommended values from JEITA standard.

Typical Applications (continued)

Table 11. Key Data Flash Parameters for Configuration (continued)

NAME	DEFAULT	UNIT	RECOMMENDED SETTING
T4 Temp	50	°C	Sets the boundary between charging with T4-T5 or T4-T5 parameters. Also serves as charge inhibit boundary if initiating new charging event. Defaults set based on recommended values from JEITA standard.
T5 Temp	60	°C	Sets the boundary between charging suspend and charging with T4-T5 parameters. Refer to JEITA standard for compliance.
Temp Hys	1	°C	Adds temperature hysteresis for boundary crossings to avoid oscillation if temperature is changing by a degree or so on a given boundary.
T1-T2 Chg Voltage	4350	mV	Sets reported charge voltage when inside of ***T1 Temp*** and ***T2 Temp*** range. Defaults set based on recommended values from JEITA standard.
T2-T3 Chg Voltage	4350	mV	Sets reported charge voltage when inside of ***T2 Temp*** an d ***T3 Temp*** range. Defaults set based on recommended values from JEITA standard.
T3-T4 Chg Voltage	4300	mV	Sets reported charge voltage when inside of ***T3 Temp*** and ***T4 Temp*** range. Defaults set based on recommended values from JEITA standard.
T4-T5 Chg Voltage	4250	mV	Sets reported charge voltage when inside of ***T4 Temp*** and ***T5 Temp*** range. Defaults set based on recommended values from JEITA standard.
T1-T2 Chg Current	50	%	Sets reported charge current when inside of ***T1 Temp*** and ***T2 Temp*** range. Defaults set based on recommended values from JEITA standard.
T2-T3 Chg Current	80	%	Sets reported charge current when inside of ***T2 Temp*** and ***T3 Temp*** range. Defaults set based on recommended values from JEITA standard.
T3-T4 Chg Current	80	%	Sets reported charge current when inside of ***T3 Temp*** and ***T4 Temp*** range. Defaults set based on recommended values from JEITA standard.
T4-T5 Chg Current	80	%	Sets reported charge current when inside of ***T4 Temp*** and ***T5 Temp*** range. Defaults set based on recommended values from JEITA standard.
OV Prot Threshold	4390	mV	Set to maximum allowable cell voltage due to overcharge in normal operation.
OV Prot Delay	1	s	Set to required OVP duration prior to fault detection and FET disable. Setting of 0 disables firmware-based OVP feature. Default of 1s is recommended.
OV Prot Recovery	4290	mV	Set to desired OVP recovery threshold. 100 to 200 mV below OVP trip threshold is common.
OV Prot Threshold	2800	mV	Set to minimum allowable cell voltage due to overdischarge in normal operation.
OV Prot Delay	1	s	Set to required UVP duration prior to fault detection and FET disable. Setting of 0 disables firmware-based UVP feature. Default of 1s is recommended.
OV Prot Recovery	2900	mV	Set to desired UVP recovery threshold. 100 to 200 mV above UVP trip threshold is common.
Body Diode Current Threshold	60	mA	Varies based on FET selection. Use the max DC current for the forward-biased body diode from the FET datasheet and derate based on the operating temperature range to arrive at the minimum current value (and add some margin) that the fuel gauge should use to re-enable FET when disabled during a fault condition.
OT Chg	55.0	°C	Set to desired temperature at which charging is prohibited to prevent cell damage due to excessive ambient temperature.
OT Chg Time	5	s	Set to desired time before CHG FET is disabled based on overtemperature. Since temperature changes much more slowly than other fault conditions, the default setting is sufficient for most application.
OT Chg Recovery	50.0	°C	Set to the temperature threshold at which charging is no longer prohibited.
OT Dsg	60.0	°C	Set to desired temperature at which discharging is prohibited to prevent cell damage due to excessive ambient temperature.
OT Dsg Time	5	s	Set to desired time before DSG FET is disabled based on overtemperature. Since temperature changes much more slowly than other fault conditions, the default setting is sufficient for most application.
OT Dsg Recovery	55.0	°C	Set to the temperature threshold at which cell discharging is no longer prohibited.
Prot OC Config	0A	hex	Set based on required trip thresholds for overcurrent in charge, overcurrent in discharge, and short-circuit in discharge. When setting this parameter, be sure to account for charger tolerance and maximum load spikes expected in the end system to avoid accidental trip of these fault conditions

Typical Applications (continued)

Table 11. Key Data Flash Parameters for Configuration (continued)

NAME	DEFAULT	UNIT	RECOMMENDED SETTING
Prot OV Config	07	hex	Set to maximum tolerable cell voltage before cell is permanently damaged. Serves as a second level OVP protection mechanism.
Prot Checksum	11	hex	Set to sum of ***Prot OC Config*** and ***Prot OV Config***. Improper setting will cause FETs to open and warning flag assertion in *SafetyStatus()*, until corrected.
CC Gain	5	mΩ	Calibrate this parameter using TI-supplied BMS software and calibration procedure in the TRM. Determines conversion of coulomb counter measured sense resistor voltage to current.
CC Delta	5.074	mΩ	Calibrate this parameter using TI-supplied BMS software and calibration procedure in the TRM. Determines conversion of coulomb counter measured sense resistor voltage to passed charge.
CC Offset	6.874	mA	Calibrate this parameter using TI-supplied BMS software and calibration procedure in the TRM. Determines native offset of coulomb counter hardware that should be removed from conversions.
Board Offset	0.66	uA	Calibrate this parameter using TI-supplied BMS software and calibration procedure in the TRM. Determines native offset of the printed circuit board parasitics that should be removed from conversions.
Pack V Offset	0	mV	Calibrate this parameter using TI-supplied BMS software and calibration procedure in the TRM. Determines voltage offset between cell tab and ADC input node to incorporate back into or remove from measurement, depending on polarity.

8.2.3 Detailed Design Procedure

8.2.3.1 BAT Voltage Sense Input

A ceramic capacitor at the input to the BAT pin is used to bypass AC voltage ripple to ground, greatly reducing its influence on battery voltage measurements. It proves most effective in applications with load profiles that exhibit high frequency current pulses (that is, cell phones) but is recommended for use in all applications to reduce noise on this sensitive high impedance measurement node.

The series resistor between the battery and the BAT input is used to limit current that could be conducted through the chip-scale package's solder bumps in the event of an accidental short during the board assembly process. The resistor is not likely to survive a sustained short condition (depends on power rating), however, it sacrifices the much cheaper resistor component over suffering damage to the fuel gauge die itself.

8.2.3.2 SRP and SRN Current Sense Inputs

The filter network at the input to the coulomb counter is intended to improve differential mode rejection of voltage measured across the sense resistor. These components should be placed as close as possible to the coulomb counter inputs and the routing of the differential traces length-matched in order to best minimize impedance mismatch-induced measurement errors. The single-ended ceramic capacitors should be tied to the battery voltage node (preferably to a large copper pour connected to the SRN side of the sense resistor) in order to further improve common-mode noise rejection. The series resistors between the CC inputs and the sense resistor should be at least 200 Ω in order to mitigate SCR-induced latch-up due to possible ESD events.

8.2.3.3 Sense Resistor Selection

Any variation encountered in the resistance present between the SRP and SRN pins of the fuel gauge will affect the resulting differential voltage, and derived current, it senses. As such, it is recommended to select a sense resistor with minimal tolerance and temperature coefficient of resistance (TCR) characteristics. The standard recommendation based on best compromise between performance and price is a 1% tolerance, 50-ppm drift sense resistor with a 1-W power rating.

8.2.3.4 TS Temperature Sense Input

Similar to the BAT pin, a ceramic decoupling capacitor for the TS pin is used to bypass AC voltage ripple away from the high-impedance ADC input, minimizing measurement error. Another helpful advantage is that the capacitor provides additional ESD protection since most thermistors are handled and manually soldered to the PCB as a separate step in the factory production flow. As before, it should be placed as close as possible to the respective input pin for optimal filtering performance.

8.2.3.5 Thermistor Selection

The fuel gauge temperature sensing circuitry is designed to work with a negative temperature coefficient-type (NTC) thermistor with a characteristic 10-kΩ resistance at room temperature (25°C). The default curve-fitting coefficients configured in the fuel gauge specifically assume a 103AT-2 type thermistor profile and so that is the default recommendation for thermistor selection purposes. Moving to a separate thermistor resistance profile (for example, JT-2 or others) requires an update to the default thermistor coefficients in data flash to ensure highest accuracy temperature measurement performance.

8.2.3.6 VPWR Power Supply Input Filtering

A ceramic capacitor is placed at the input to the fuel gauge's internal LDO in order to increase power supply rejection (PSR) and improve effective line regulation. It ensures that voltage ripple is rejected to ground instead of coupling into the device's internal supply rails.

8.2.3.7 REG25 LDO Output Filtering

A ceramic capacitor is also needed at the output of the internal LDO in order to provide a current reservoir for fuel gauge load peaks during high peripheral utilization. It acts to stabilize the regulator output and reduce core voltage ripple inside of the device.

8.2.3.8 Communication Interface Lines

A protection network composed of resistors and zener diodes is recommended on each of the serial communication inputs to protect the fuel gauge from dangerous ESD transients. The Zener should be selected to break down at a voltage larger than the typical pullup voltage for these lines but less than the internal diode clamp breakdown voltage of the device inputs (~6 V). A zener voltage of 5.6 V is typically recommended. The series resistors are used to limit the current into the Zener diode and prevent component destruction due to thermal strain once it goes into breakdown. 100 Ω is typically recommended for these resistance values.

For HDQ-based designs, a pullup resistor is normally designed in on the battery pack PCB and can be connected to the RC2 input since a 1.8-V pullup voltage is readily available and provided by the fuel gauge.

8.2.3.9 PACKP Voltage Sense Input

Inclusion of a 2-kΩ series resistor on the PACKP input allows it to tolerate a charger overvoltage event up to 28 V without device damage. The resistor also protects the device in the event of a reverse polarity charger input, since the substrate diode will be forward biased and attempt to conduct charger current through the fuel gauge (as well as the high FETs). An external reverse charger input FET clamp can be added to short the DSG FET gate to its source terminal, forcing the conduction channel off when negative voltage is present at PACK+ input to the battery pack and preventing large battery discharge currents. A ceramic capacitor connected at the PACKP pin helps to filter voltage into the comparator sense lines used for checking charger and load presence. In addition, in the Low Voltage Charging State, the minimal circuit elements that are operational are powered from this input pin and require a stable supply.

8.2.3.10 CHG and DSG Charge Pump Voltage Outputs

The series resistors used at the DSG and CHG output pins serve to protect them from damaging ESD events or breakdown conditions, allowing the resistors to be sacrificed in place of the fuel gauge itself. An added bonus is that they also help to limit in-rush currents due to use of FETs with large gate capacitance, allowing smooth ramp of power-path connection turn-on to the system.

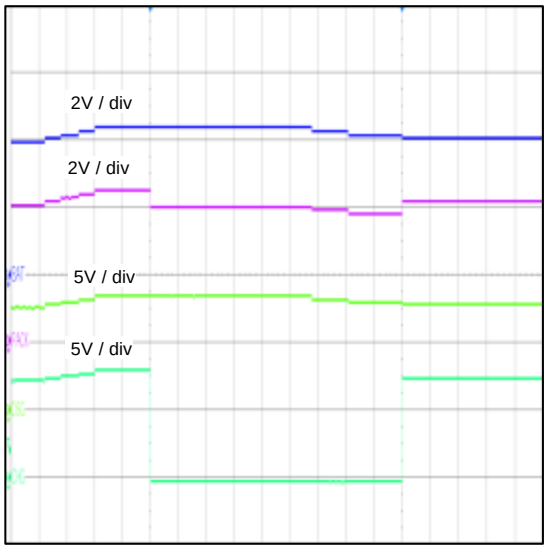
8.2.3.11 NFET Selection

The choice in NFETs for a single-cell battery pack design will depend on a variety of factors including package type, size, and device cost as well as performance metrics such as drain-to-source resistance ($r_{DS(on)}$), gate capacitance, maximum current and power handling, and similar. At a bare minimum, it is recommended that the selected FETs have a drain-to-source voltage (V_{DS}) and gate-to-source (V_{GS}) voltage tolerance of 12 V. Some FETs can are designed to handle as much as 24 V between the drain and source terminals and this would provide an increased safety margin for the pack design. Further, the DC current rating should be high enough to safely handle sustained current in charge or discharge direction just below the maximum threshold tolerances of the configured OCC and OCD protections and the lowest possible sense resistance value based on tolerance and TCR considerations, or vice-versa. This ensures that there is sufficient power dissipation margin given a worst case scenario for the fault detections. In addition, striving for minimal FET resistance at the expected gate bias as well as lowest gate capacitance will help reduce conduction losses and increase power efficiency as well as achieve faster turn-on and turn-off times for the FETs. Many of these FETs are now offered as dual, back-back NFETs in wafer-chip scale (WCSP) packaging, decreasing both BOM count and shrinking necessary board real estate to accommodate the components. Last, one should always refer to the safe operating area (SOA) curves of the target FETs to ensure that the boundaries are never violated based on all possible load conditions in the end application. The CSD83325L is an excellent example of a FET solution that meets all of the aforementioned criteria, offering $r_{DS(on)}$ of 10.3 mΩ and V_{DS} of 12 V with back-to-back NFETs in a chip-scale package, a perfect fit for battery pack designs.

8.2.3.12 Additional ESD Protection Components

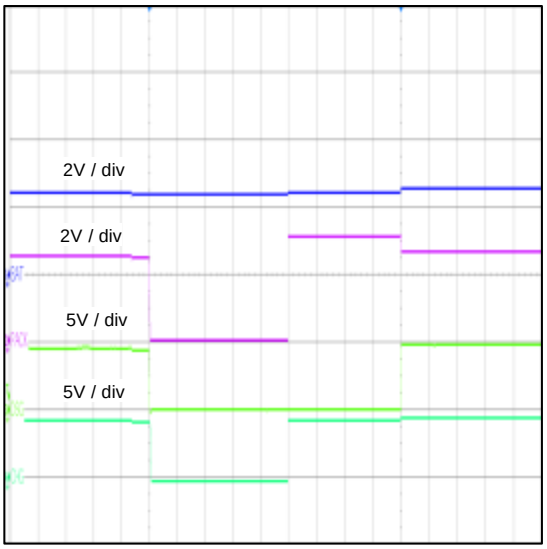
The additional capacitors placed across the CHG and DSF FET source pins as well as between PACK+ and ground help to bolster and greatly improve the ESD robustness of the pack design. The former components shunt damaging transients around the FETs and the latter components attempt to bypass such pulses to PACK– before they couple further into the battery pack PCB. Two series capacitors are used for each of these protection areas to prevent a battery short in the event of a single capacitor failure.

8.2.4 Application Curves



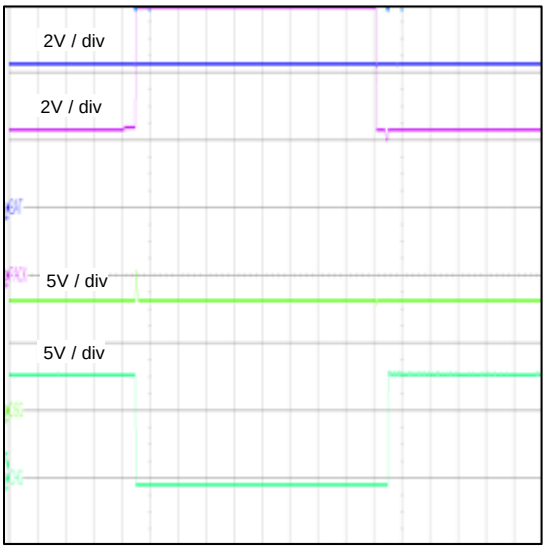
500ms / div

Figure 21. Overvoltage Protection Set and Clear



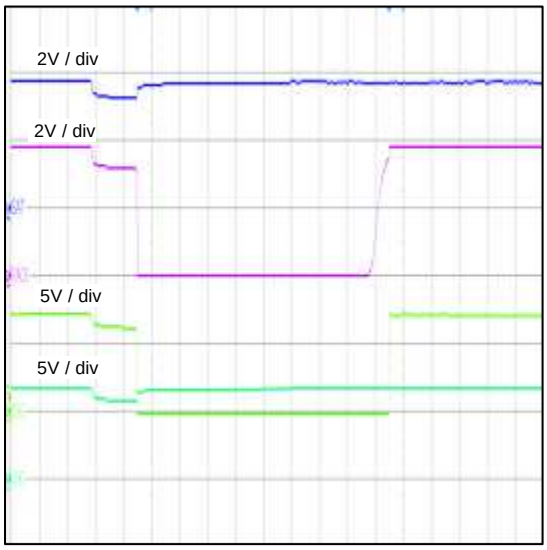
50ms / div

Figure 22. Undervoltage Protection Set and Clear



20ms / div

Figure 23. Overcurrent in Charge Protection Set and Clear



20ms / div

Figure 24. Overcurrent in Discharge Protection Set and Clear

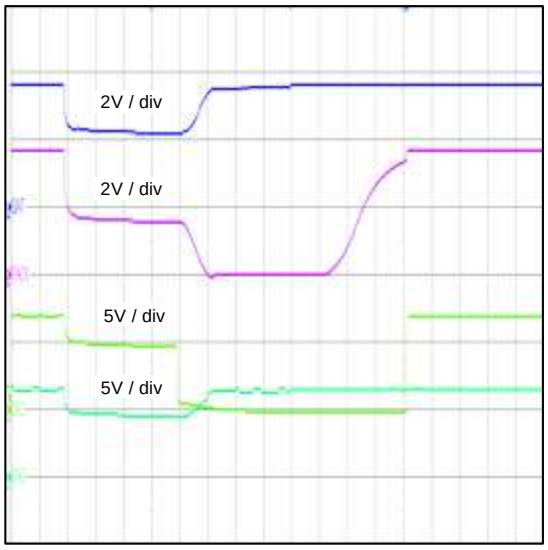


Figure 25. Short-Circuit in Discharge Protection Set and Clear

9 Power Supply Recommendation

9.1 Power Supply Decoupling

Both the VPWR input pin and the REG25 output pin require low equivalent series resistance (ESR) ceramic capacitors placed as closely as possible to the respective pins to optimize ripple rejection and provide a stable and dependable power rail that is resilient to line transients. A 0.1-µF capacitor at the VPWR and a 1-µF capacitor at REG25 will suffice for satisfactory device performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Li-Ion Cell Connections

For highest voltage measurement accuracy, it is critical to connect the BAT pin directly to the battery terminal PCB pad. This avoids measurement errors caused by IR drops when high charge or discharge currents are flowing. Connecting right at the positive battery terminal with a Kelvin connection ensures the elimination of parasitic resistance between the point of measurement and the actual battery terminal. Likewise the low current ground return for the fuel gauge and all related passive components should be star-connected right at the negative battery terminal. This technique minimizes measurement error due to current-induced ground offsets and also improves noise performance through prevention of ground bounce that could occur with high current and low current returns intersecting ahead of the battery ground. The bypass capacitor for this sense line needs to be placed as close as possible to the BAT input pin.

10.1.2 Sense Resistor Connections

Kelvin connections at the sense resistor are just as critical as those for the battery terminals themselves. The differential traces should be connected at the inside of the sense resistor pads and not anywhere along the high current trace path in order to prevent false increases to measured current that could result when measuring between the sum of the sense resistor and trace resistance between the tap points. In addition, the routing of these leads from the sense resistor to the input filter network and finally into the SRP and SRN pins needs to be as closely matched in length as possible else additional measurement offset could occur. It is further recommended to add copper trace or pour-based "guard rings" around the perimeter of the filter network and coulomb counter inputs to shield these sensitive pins from radiated EMI into the sense nodes. This prevents differential voltage shifts that could be interpreted as real current change to the fuel gauge. All of the filter components need to be placed as close as possible to the coulomb counter input pins.

10.1.3 Thermistor Connections

The thermistor sense input should include a ceramic bypass capacitor placed as close to the TS input pin as possible. The capacitor helps to filter measurements of any stray transients as the voltage bias circuit pulses periodically during temperature sensing windows.

10.1.4 FET Connections

The battery current transmission path through the FETs should be routed with large copper pours to provide the lowest resistance path possible to the system. Depending on package type, thermal vias can be placed in the package land pattern's thermal pad to reduce thermal impedance and improve heat dissipation from the package to the board, protecting the FETs during high system loading conditions. In addition, it is preferable to locate the FETs and other heat generating components away from the low power pack electronics to reduce the chance of temperature drift and associated impacts to data converter measurements. In the event of FET overheating, keeping reasonable distance between the most critical components, such as the fuel gauge, and the FETs helps to decrease the risk of thermal breakdown to the more fragile components.

10.1.5 ESD Component Connections

The ESD components included in the reference design that connect across the back-to-back FETs as well as from PACK+ to ground require trace connections that are as wide and short as possible in order to minimize loop inductance in their return path. This ensures impedance is lowest at the AC loop through the series capacitors and makes this route most attractive for ESD transients such that they are conducted away from the vulnerable low voltage, low power fuel gauge and passive components. The series resistors and Zener diodes connected to the serial communications lines should be placed as close as possible to the battery pack connector to keep large ESD currents confined to an area distant from the fuel gauge electronics. Further, all ESD components referred to ground should be single-point connected to the PACK– terminal if possible. This reduces the possibility of ESD coupling into other sensitive nodes well ahead of the PACK– ground return.

Layout Guidelines (continued)

10.1.6 High Current and Low Current Path Separation

For best possible noise performance, it is extremely important to separate the low current and high current loops to different areas of the board layout. The fuel gauge and all support components should be situated on one side of the boards and tap off of the high current loop (for measurement purposes) at the sense resistor. Routing the low current ground around instead of under high current traces will further help to improve noise rejection. Last, the high current path should be confined to a small loop from the battery, through the FETs, into the PACK connector, and back.

10.2 Layout Example

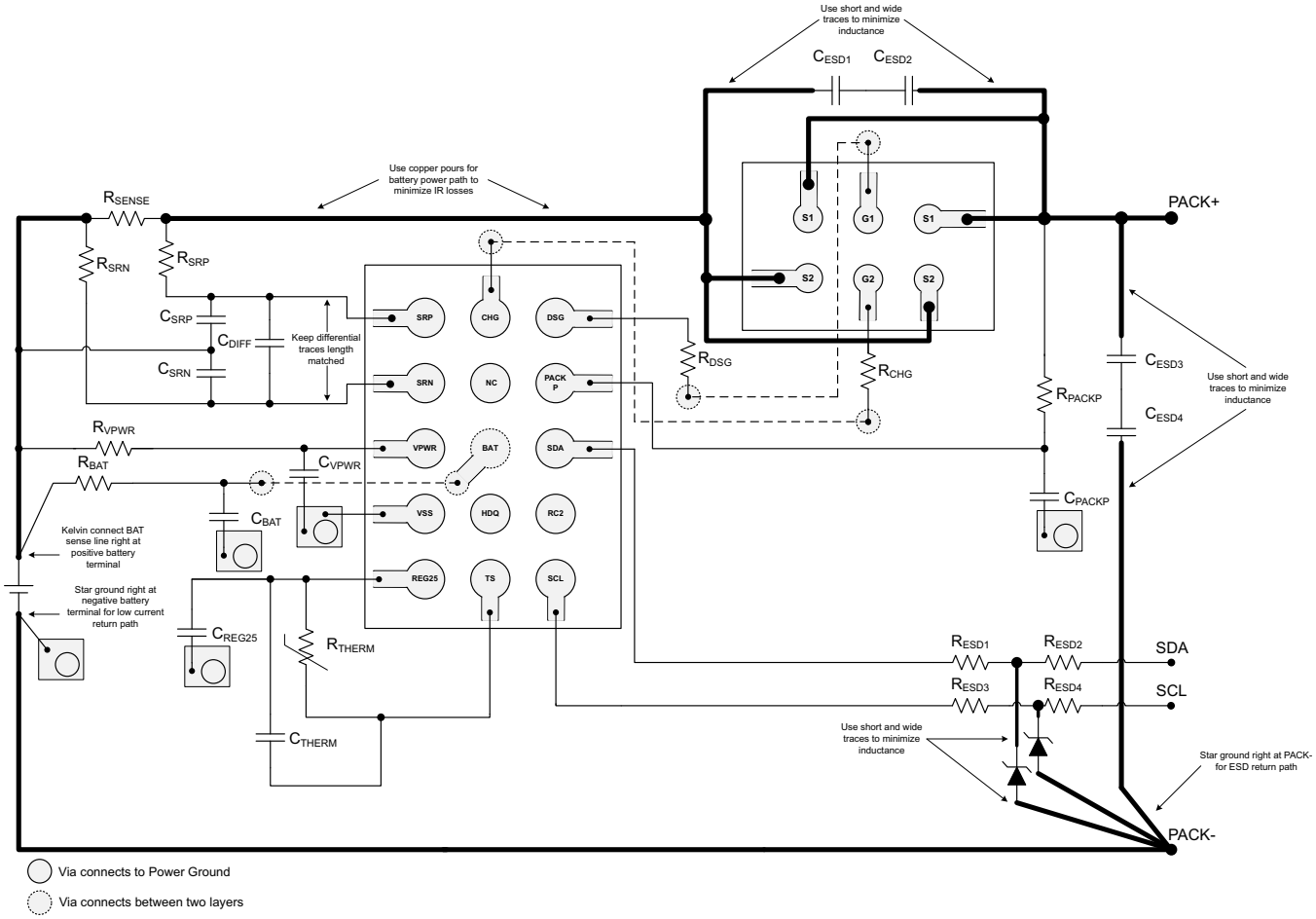


Figure 26. bq27742-G1 Board Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

1. *bq27742-G1 Single-Cell Impedance Track™ Battery Fuel Gauge with Programmable Hardware Protection Technical Reference Manual* (SLUUAX0)
2. *bq27742EVM Single Cell Impedance Track™ Technology Evaluation Module User's Guide* (SLUUAH1)

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ27742YZFR-G1	ACTIVE	DSBGA	YZF	15	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ27742	Samples
BQ27742YZFT-G1	ACTIVE	DSBGA	YZF	15	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ27742	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

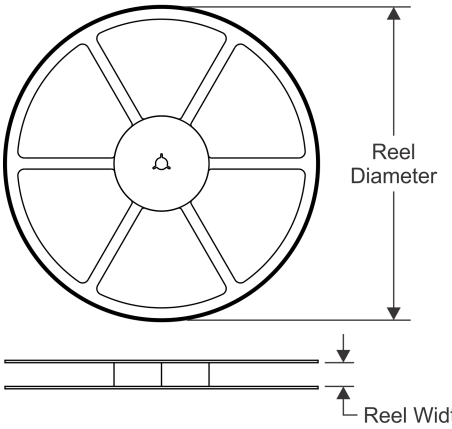
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

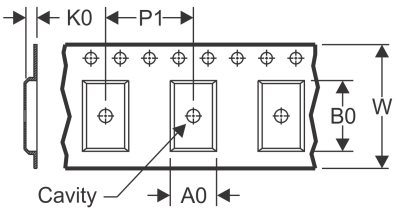
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

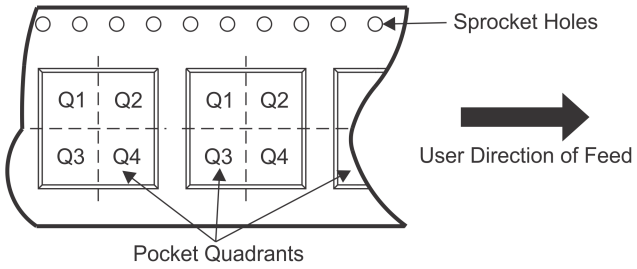


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

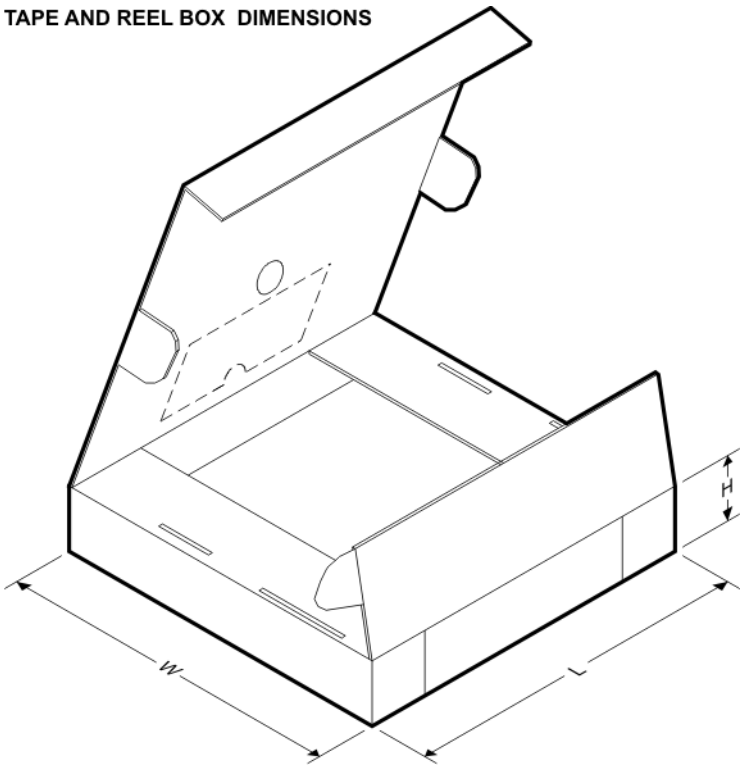
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ27742YZFR-G1	DSBGA	YZF	15	3000	180.0	8.4	2.06	2.88	0.69	4.0	8.0	Q1
BQ27742YZFT-G1	DSBGA	YZF	15	250	180.0	8.4	2.06	2.88	0.69	4.0	8.0	Q1

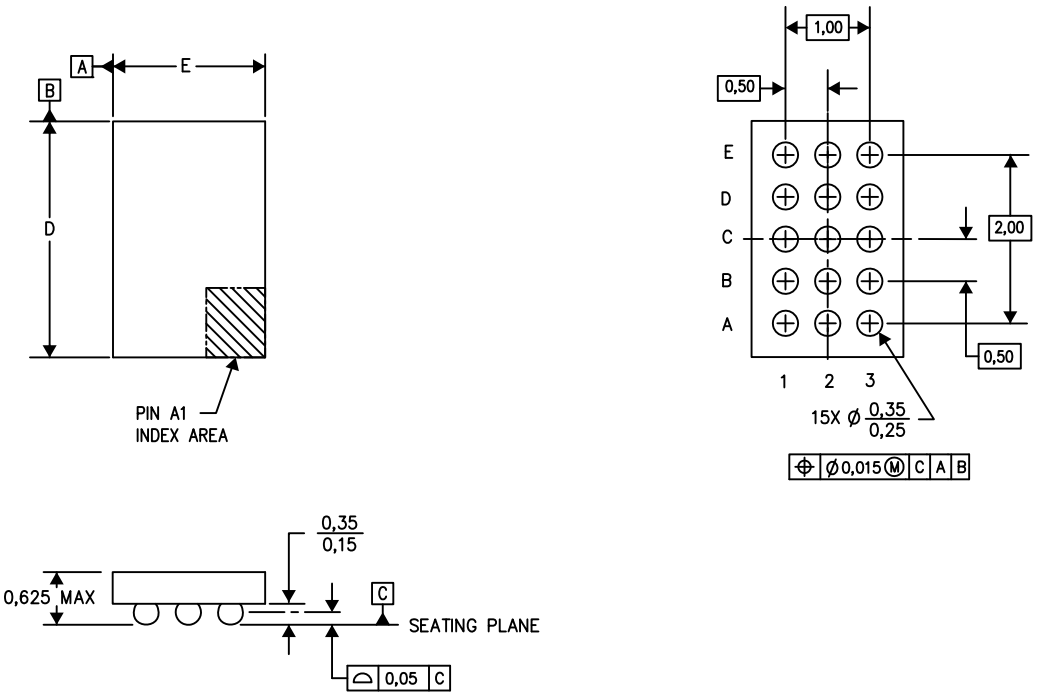
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ27742YZFR-G1	DSBGA	YZF	15	3000	182.0	182.0	20.0
BQ27742YZFT-G1	DSBGA	YZF	15	250	182.0	182.0	20.0

YZF (R–XBGA–N15) DIE–SIZE BALL GRID ARRAY



D: Max = 2.806 mm, Min =2.746 mm

E: Max = 1.986 mm, Min =1.926 mm

4205058–5/P 07/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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