

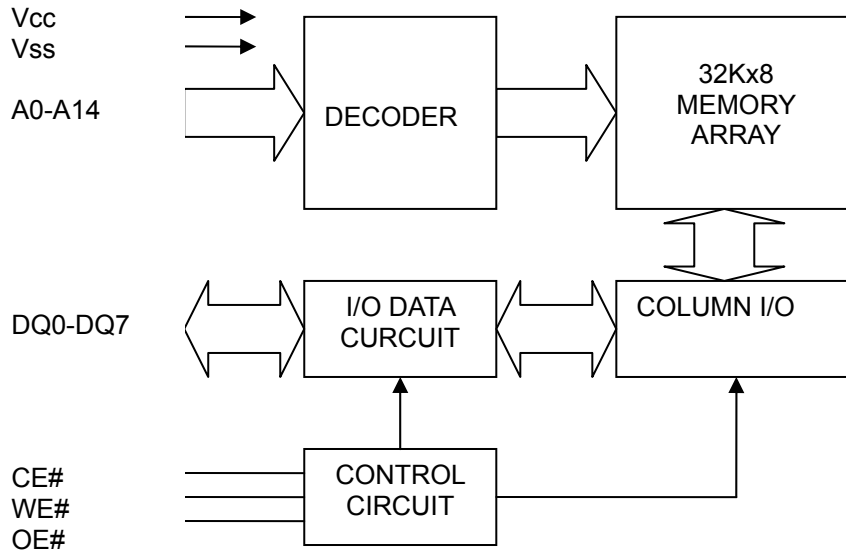
GENERAL DESCRIPTION

The EM6132K800W is a 262,144-bit low power CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature. The EM6132K800W is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application. The EM6132K800W operates from a single power supply of 2.7V ~ 5.5V and all inputs and outputs are fully TTL compatible

FEATURES

- Fast access time: 35/55/70ns
- Low power consumption:
Operating current:
20/15/10mA (TYP.), V_{CC} = 2.7 ~ 3.6V; 40/35/30mA (TYP.), V_{CC} = 4.5 ~ 5.5V
Standby current: -L/-LL version
1/0.5µA (TYP.), V_{CC} = 2.7 ~ 3.6V; 2/1µA (TYP.), V_{CC} = 4.5 ~ 5.5V
- Single 2.7V ~ 5.5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage: 2.0V (MIN.)
- Package: 28-pin 600 mil PDIP
28-pin 330 mil SOP
28-pin 8mm x 13.4mm STSOP

FUNCTIONAL BLOCK DIAGRAM

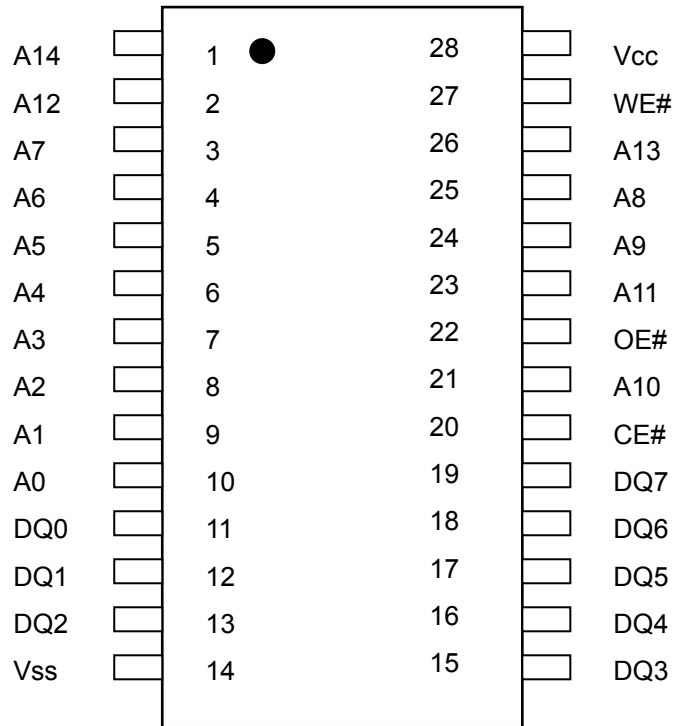


PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground

PIN CONFIGURATION

PDIP/SOP



STSOP Type I



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V _{SS}	V _{TERM}	-0.5 to 7.0	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA
Soldering Temperature (under 10 sec)	T _{SOLDER}	260	°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	High-Z	I _{CC} , I _{CC1}
Read	L	L	H	D _{OUT}	I _{CC} , I _{CC1}
Write	L	X	L	D _{IN}	I _{CC} , I _{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

I. V_{CC}=3.3V

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. *5	MAX.	UNIT	
Supply Voltage	V _{CC}		2.7	3.3	3.6	V	
Input High Voltage	V _{IH} *1		2.0	-	V _{CC} +0.5	V	
Input Low Voltage	V _{IL} *2		-0.5	-	0.6	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	-1	-	+1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	-1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.4	3.0	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V	
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} , I _{I/O} = 0mA	-35	-	20	40	mA
			-55	-	15	30	mA
			-70	-	10	20	mA
	I _{CC1}	Cycle time = 1μs CE# ≤ 0.2V and I _{I/O} = 0mA other pins at 0.2V or V _{CC} -0.2V	-	3	6	mA	
Standby Power Supply Current	I _{SB}	CE# = V _{IH}	-	1	3	mA	
	I _{SB1}	CE# V ≥ V _{CC} - 0.2V	-L	-	1	40	μA
			-LL		0.5	20*4	μA

II. V_{CC}=5V

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. *5	MAX.	UNIT	
Supply Voltage	V _{CC}		4.5	5.0	5.5	V	
Input High Voltage	V _{IH} *1		2.0	-	V _{CC} +0.5	V	
Input Low Voltage	V _{IL} *2		-0.5	-	0.8	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	-1	-	+1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	-1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.4	-	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V	
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} , I _{I/O} = 0mA	-35	-	40	50	mA
			-55	-	35	45	mA
			-70	-	30	40	mA
	I _{CC1}	Cycle time = 1μs CE# ≤ 0.2V and I _{I/O} = 0mA other pins at 0.2V or V _{CC} -0.2V	-	5	10	mA	
Standby Power Supply Current	I _{SB}	CE# = V _{IH}	-	1	3	mA	
	I _{SB1}	CE# V ≥ V _{CC} - 0.2V	-L	-	2	100	μA
			-LL	-	1	50*4	μA

Notes:

1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. 10μA for special request
5. Typical values are included for reference only and are not guaranteed or tested.
Typical valued are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 50pF + 1TTL, I _{OH} /I _{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS

READ CYCLE

PARAMETER	SYM.	-35		-55		70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	35	-	55	-	70	-	ns
Address Access Time	t _{AA}	-	35	-	55	-	70	ns
Chip Enable Access Time	t _{ACE}	-	35	-	55	-	70	ns
Output Enable Access Time	t _{OE}	-	25	-	30	-	35	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	10	-	10	-	10	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	5	-	5	-	5	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	15	-	20	-	25	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	15	-	20	-	25	ns
Output Hold from Address Change	t _{OH}	10	-	10	-	10	-	ns

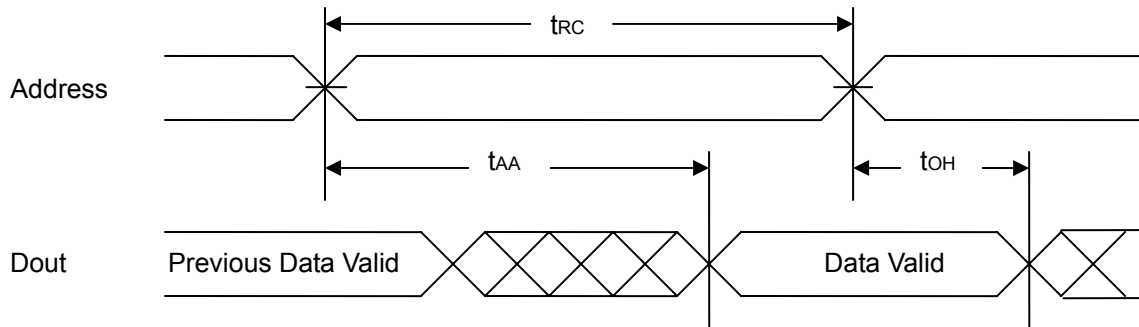
WRITE CYCLE

PARAMETER	SYM.	-35		-55		70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	35	-	55	-	70	-	ns
Address Valid to End of Write	t _{AW}	30	-	50	-	60	-	ns
Chip Enable to End of Write	t _{CW}	30	-	50	-	60	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t _{WP}	25	-	45	-	55	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	20	-	25	-	30	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	5	-	5	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	15	-	20	-	25	ns

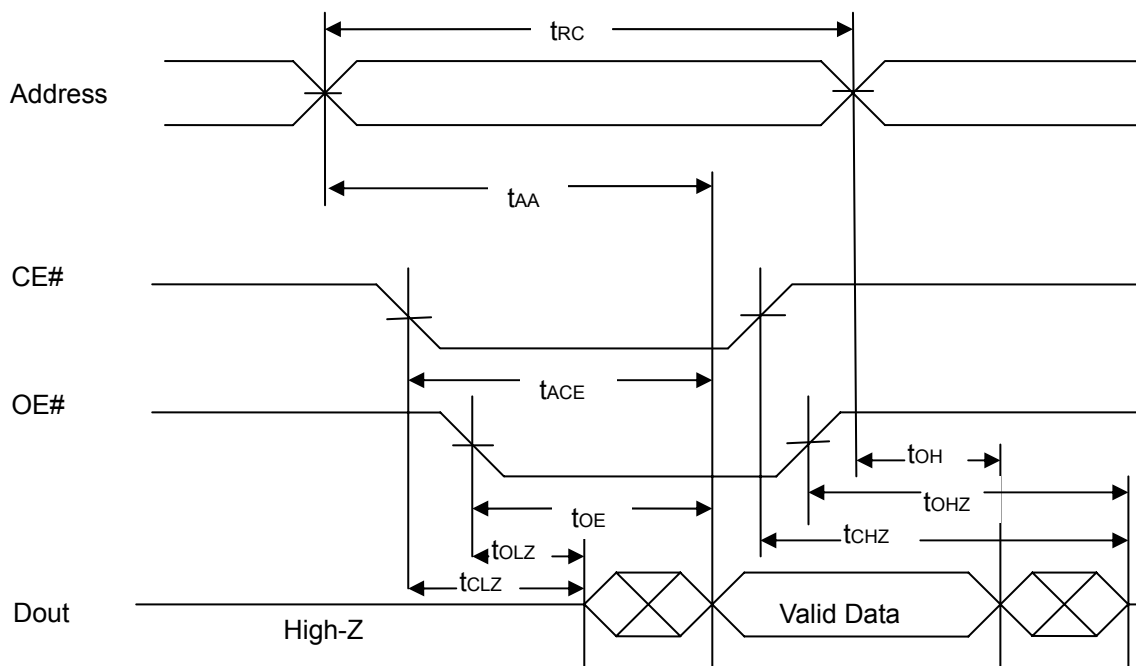
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



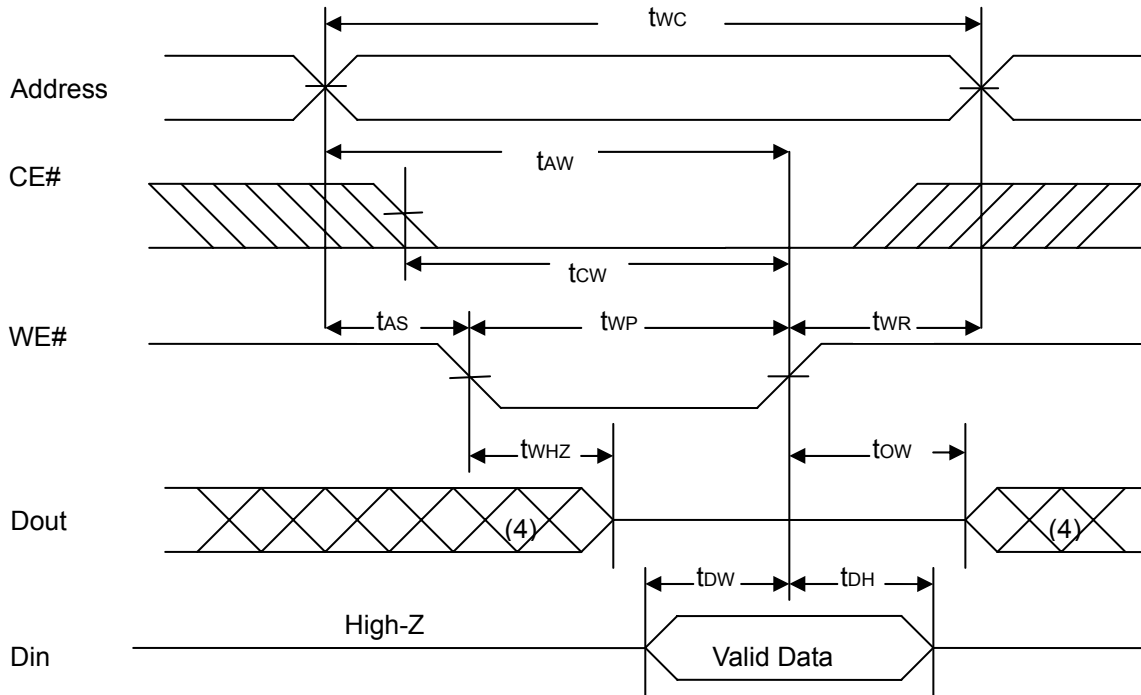
READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)



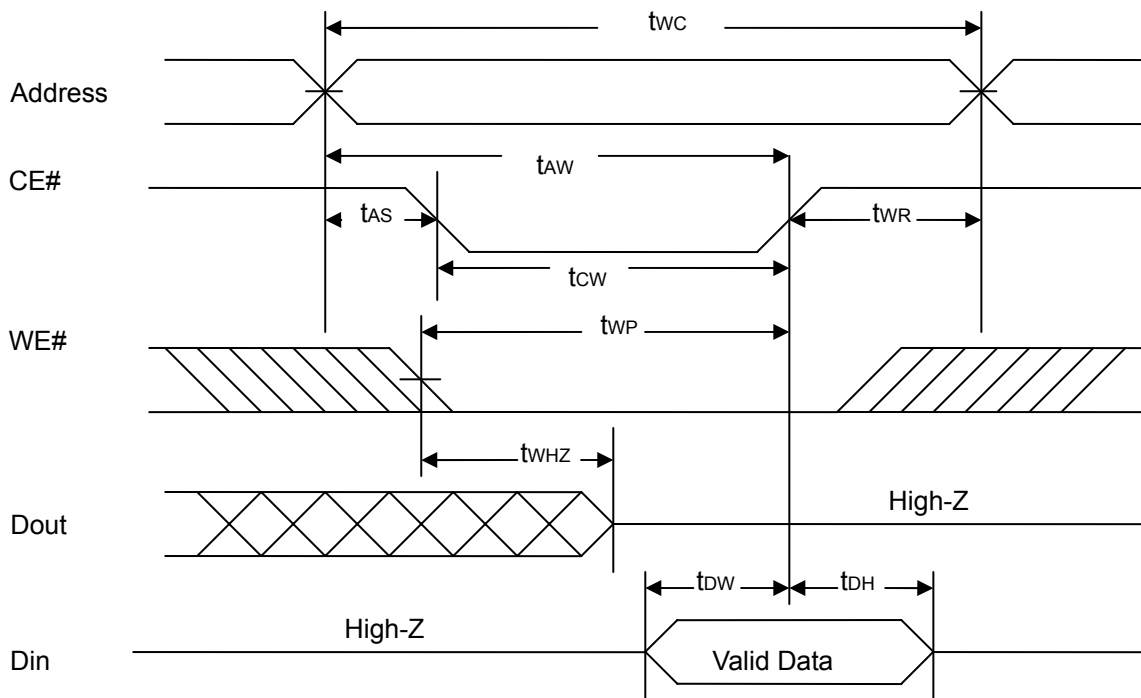
Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low,; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)



Notes :

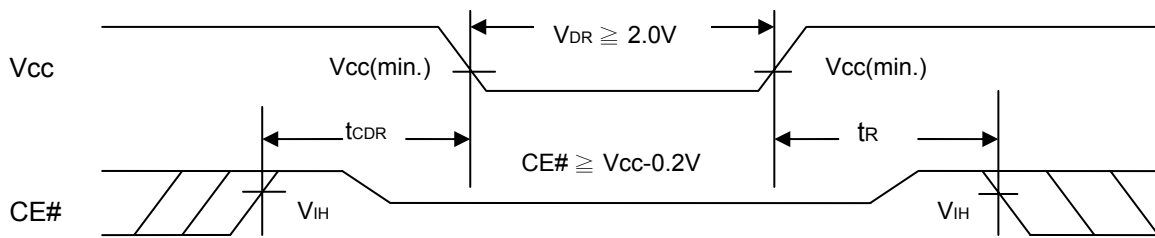
1. WE#, CE# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#.
3. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Vcc for Data Retention	V _{DR}	CE# V ≥ V _{CC} - 0.2V	2.0	-	5.5	V	
Data Retention Current	I _{DR}	V _{CC} = 1.5V CE# V ≥ V _{CC} - 0.2V	-L	-	1	50	μA
			-LL	-	0.5	20	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns	
Recovery Time	t _R		t _{RC} *			ns	

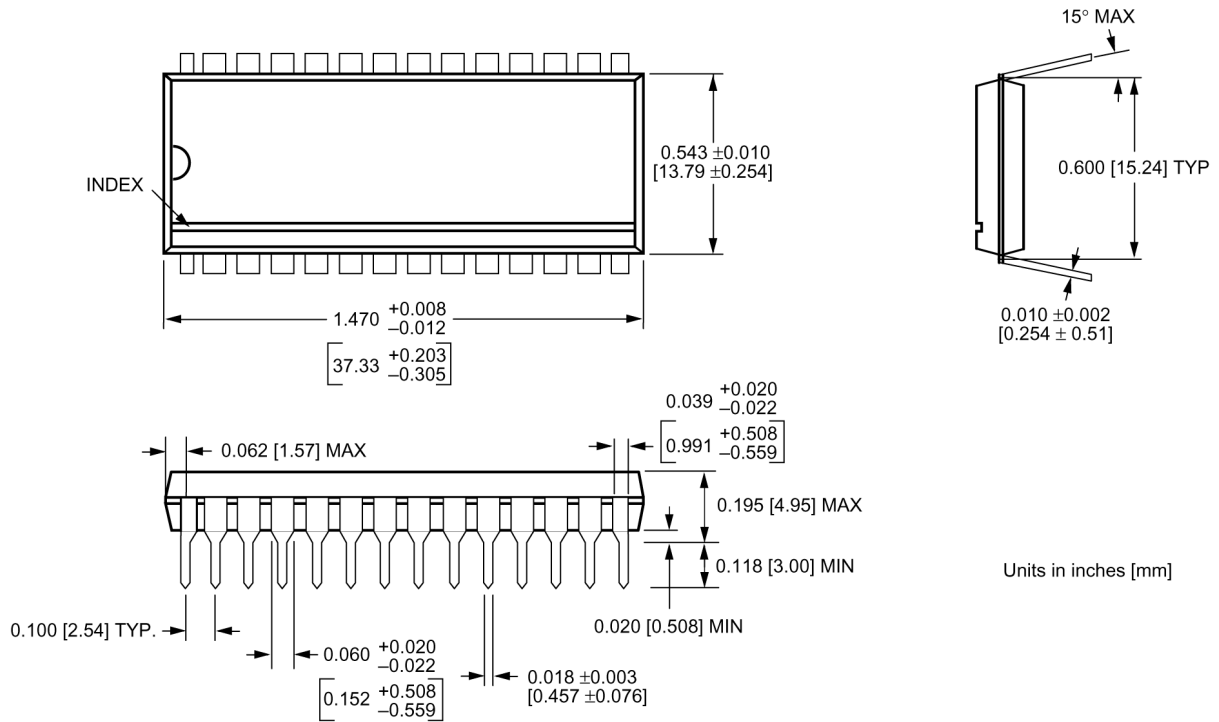
t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM

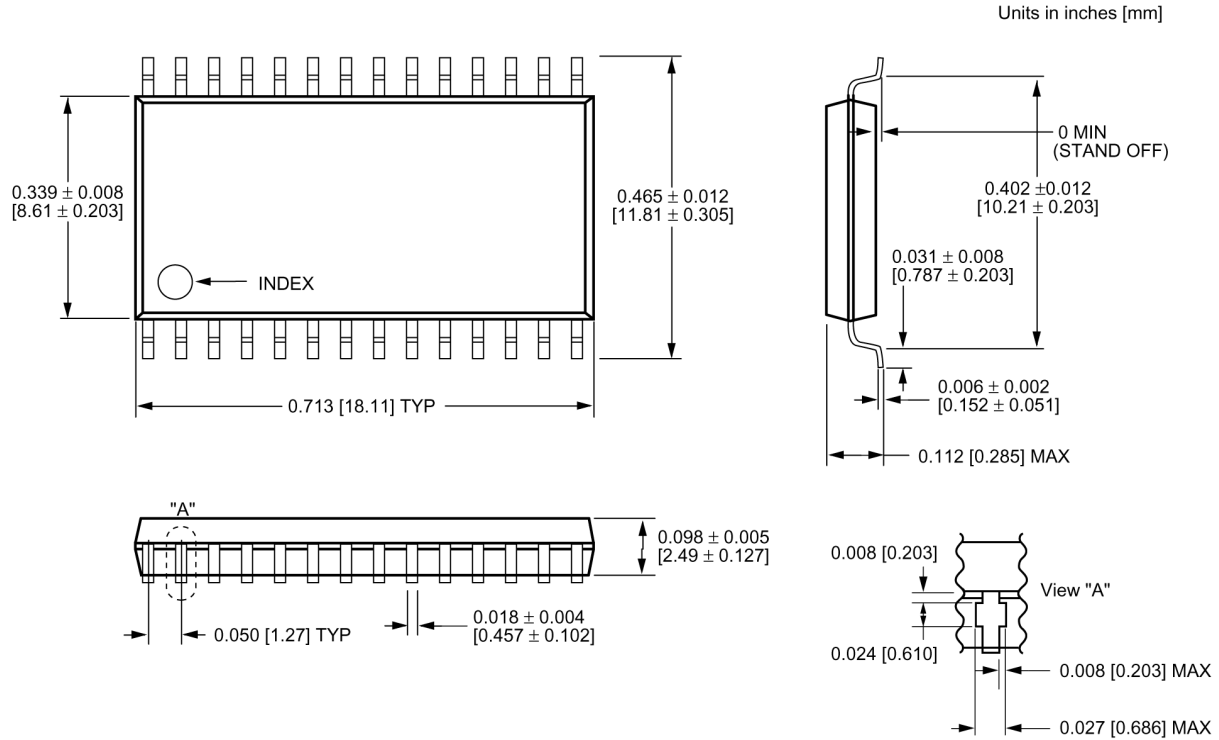


PACKAGE OUTLINE DIMENSION

28 pin 600 mil PDIP Package Outline Dimension



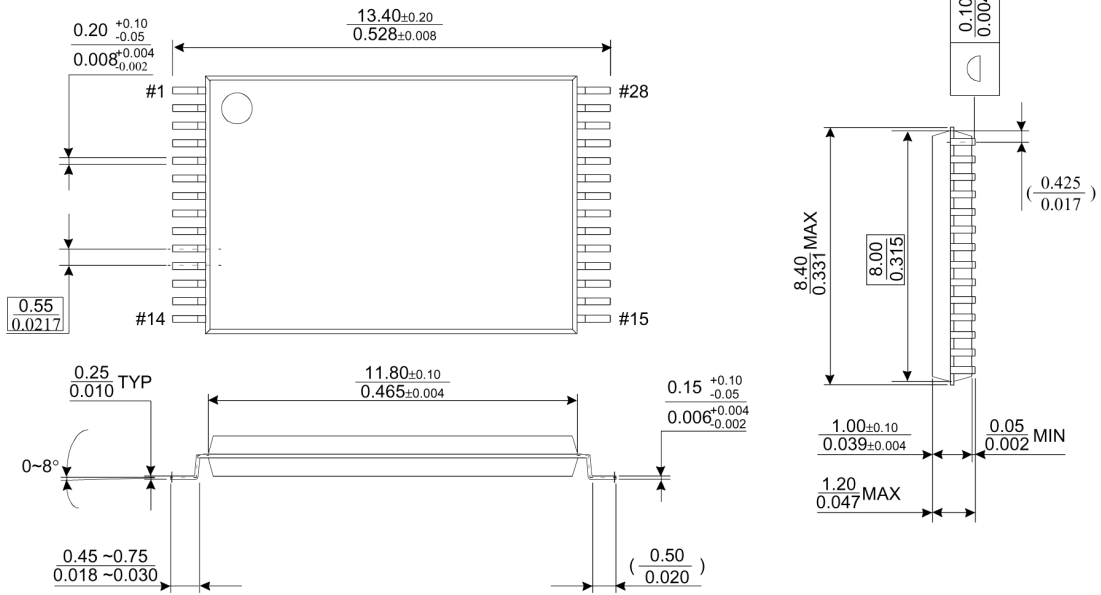
28 pin 330 mil SOP Package Outline Dimension



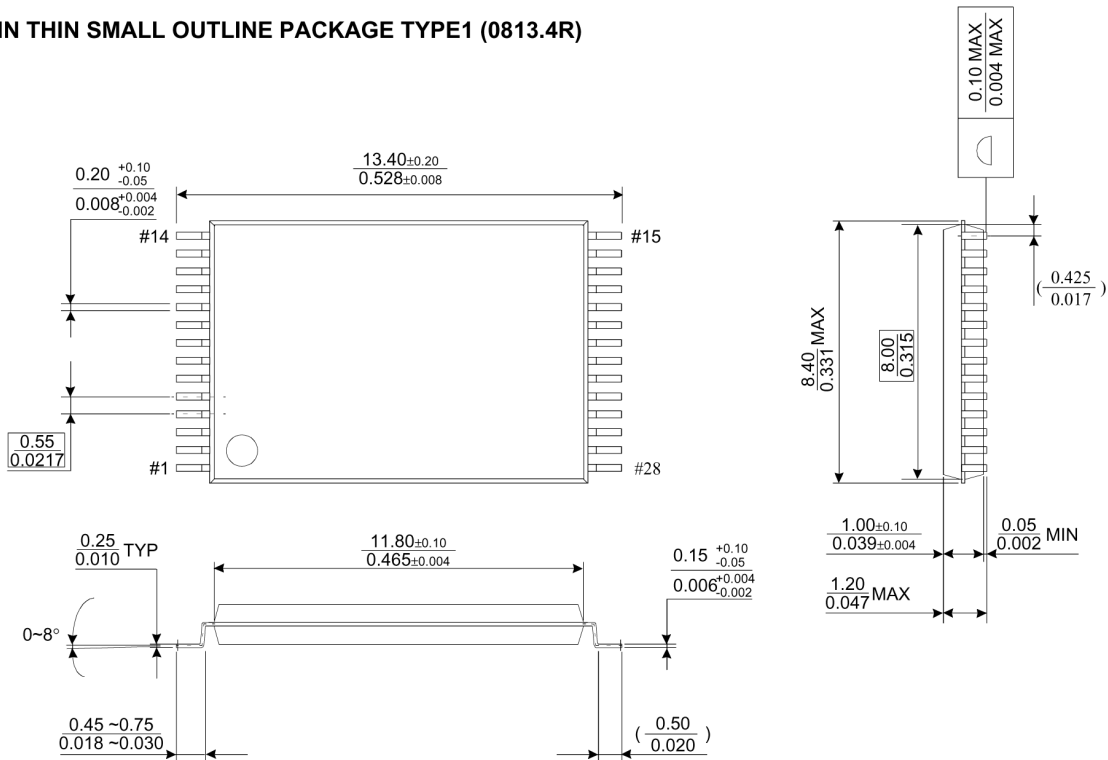
28 pin 8mm x 13.4mm STSOP Package Outline Dimension

28 PIN THIN SMALL OUTLINE PACKAGE TYPE1 (0813.4F)

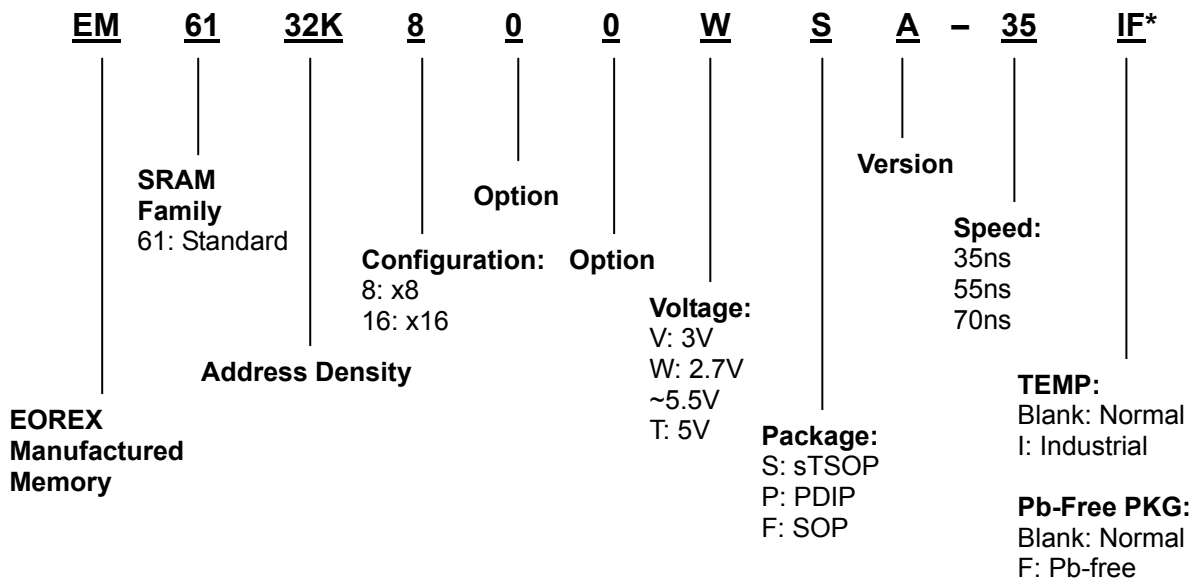
Units: millimeter(inch)



28 PIN THIN SMALL OUTLINE PACKAGE TYPE1 (0813.4R)



Product Number Information



* Product number example

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