T66H0004A

80 output LCD Segment/Common Driver IC

DESCRIPTION

The T66H0004A is a LCD driver LSI which is fabricated by low power CMOS high voltage process technology. In segment driver mode, it can be interfaced in 1-bit serial or 4-bit parallel method by the controller. In common driver mode, dual type mode is applicable. And in segment mode application, the power down function reduces power consumption.

FEATURES

- Power supply voltage: +5V±10% to +3V±10%
- Supply voltage for display: 6 to 28V(V_{DD}-V_{EE})
- 4 bit parallel/1 bit serial data processing (in segment mode)
- Single mode operation/dual mode operation (in common mode)
- Power down function (in segment mode)
- Applicable LCD duty:1/64 – 1/256
- High voltage CMOS process
- Bare die , QFP or TQFP available

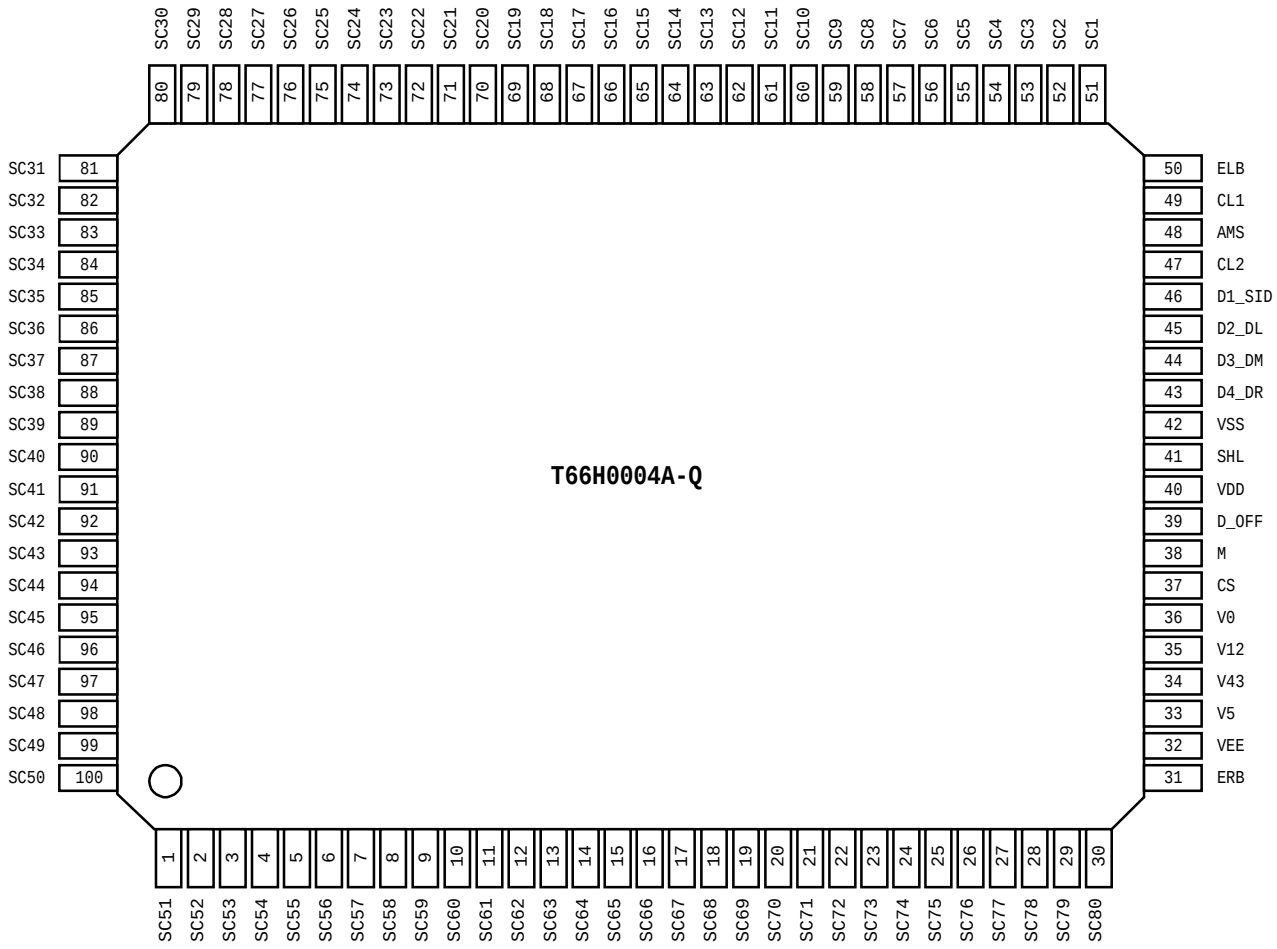
Ordering Information

Part No.	Pkg.	Description
T66H0004A-Q	QFP 100 pin	
T66H0004A-T	TQFP 100 pin	
T66H0004A1S	COG	Refer to **Pads List**

PACKAGE INFORMATION

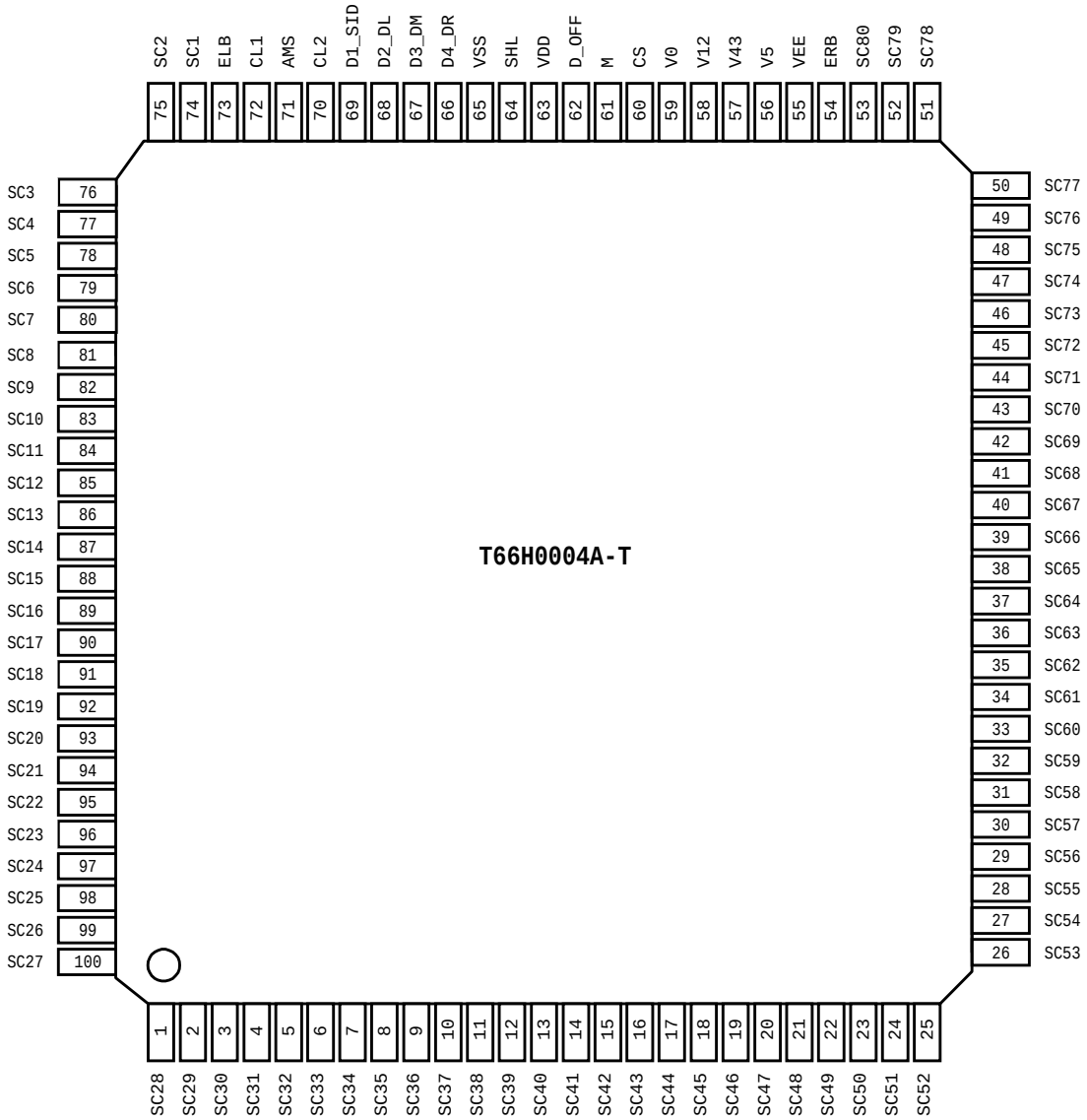
QFP

100QFP PACKAGE

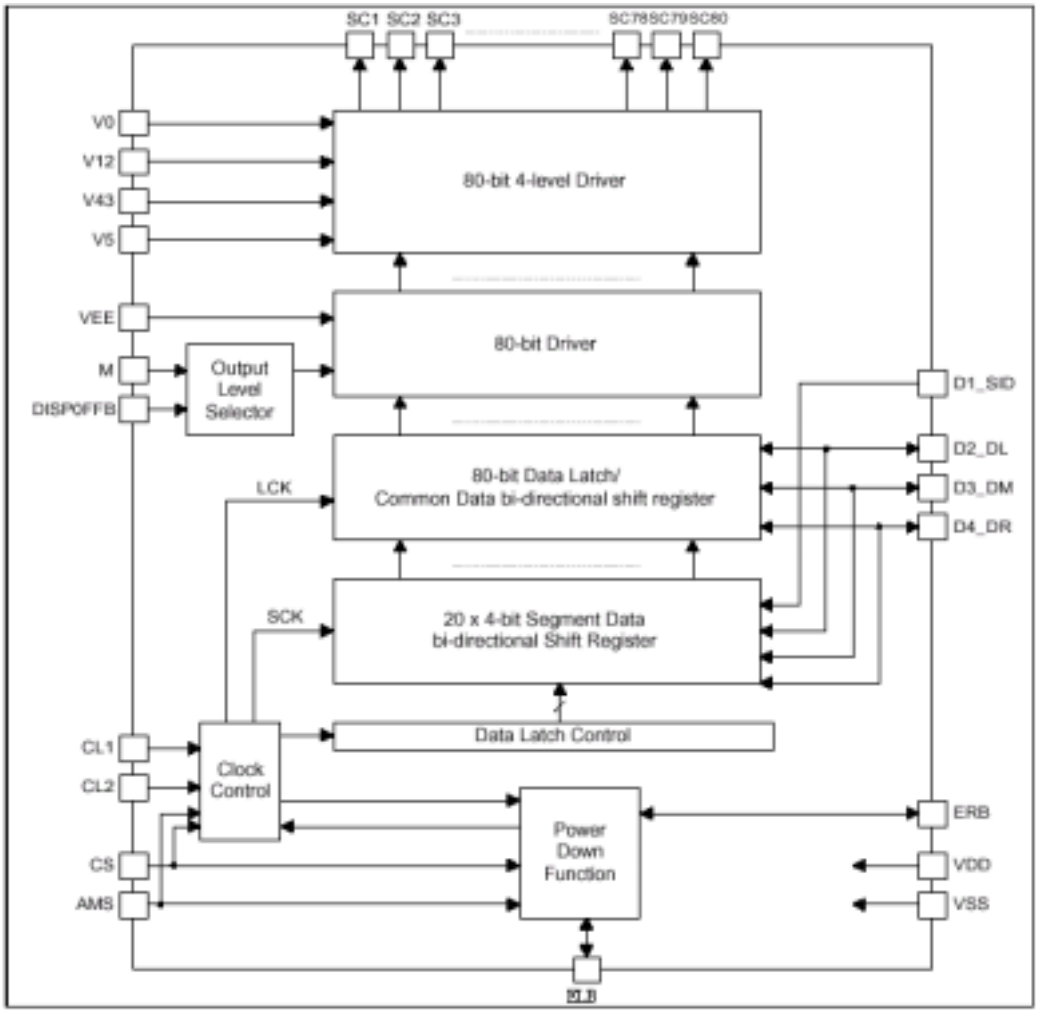


TQFP

100TQFP PACKAGE



BLOCK DIAGRAM



BLOCK DESCRIPTION

Name	Function	COM/SEG
Clock control	Generates latch clock (LCK),shift clock(SCK) and control clock timing according to the input of CL1,CL2 and control inputs(CS,AMS). In common driver application mode, this block generates the shift clock (LCK) for the common data Bi-directional shift register.	COM/SEG
Data latch control	Determines the direction of segment data shift, and input data of each Bi-directional shift register. In 4-bit segment data parallel transfer mode, data is shifted by 4-bit unit. In common driver application mode, data is transferred to the common data shift register directly, which disables this block.	SEG
Power down function	Controls the clock enable state of the current driver according to the input value of enable pin (ELB or ERB). If enable input value is ”Low”, every clock of the current driver is enabled and the clock control block works. But if enable input is “High”, current driver is disabled and the input data value has no effect on the output level. So power consumption can be lowered.	SEG
Output level selector	Controls the output voltage level according to the input control pin (M and DISPOFFB) (refer to PIN DESCRIPTION).	COM/SEG
20x4-bit segment data Bi-directional shift register	Stores output data value by shifting the input values. In 1-bit serial interface mode application, all 80 shift clocks (SCK) are needed to store all the display data. But in 4-bit parallel transfer mode application, only 20 clocks are needed. In common driver application mode, this block does not work.	SEG
80–bit data latch/common data Bi-directional shift register	In segment driver application mode, the data from the 20x4-bit segment data shift register are latched for segment driver output. In single-type common driver application, 1-bit input data (from DL or DR pin) is shifted and latched by the direction according to the SHL signal input. In dual-type common application mode, 80-bit registers are divided by two blocks and controlled independently (refer to NOTE 3).	COM/SEG
80-bit level shifter	Voltage level shifter block for high voltage part. The inputs of this block are of logical voltage level and the outputs of this block are at high voltage level value. These values are output to the driver.	SEG
80-bit 4-level driver	Selects the output voltage level according to M and latched data value. If the data value is “High” the driver output is at selected voltage level (V0 or V5), and in the reverse case the driver output value is at the non-selected level (V12 or V43). In segment driver application mode, non-selected output value is V2 or V3. And when in common driver application, this value becomes V1 or V4.	SEG

PIN DESCRIPTION

<table>
<tr><th>Pin</th><th>I/O</th><th>Name</th><th>Function</th><th>Interface</th></tr>
<tr><td>VDD</td><td rowspan="3"></td><td rowspan="3">Power supply</td><td>Logical “High” input port(+5V±10%,+3V±10%)</td><td rowspan="3">Power</td></tr>
<tr><td>Vss</td><td>0V(GND)</td></tr>
<tr><td>VEE</td><td>Logical “Low” for high voltage part</td></tr>
<tr><td>V0,V12, V43,V5</td><td>I</td><td>LCD driver output voltage level</td><td>Bias supply voltage input to drive the LCD. Bias voltage divided by the resistance is usually used as a supply voltage source (refer to NOTE 2).</td><td>Power</td></tr>
<tr><td>SC1-SC80</td><td>O</td><td>LCD driver output</td><td>Display data output pin which corresponds to the respective latch contents. One of V0, V12, V34 and V5 is selected as a display driving voltage source according to the combination of the latch data level and M signal (refer to NOTE 1).</td><td>LCD</td></tr>
<tr><td>CL2</td><td>I</td><td>Data shift clock</td><td>Clock pulse input for the bi-directional shift register.
- In segment driver application mode, the data is shifted to 20x4-bit segment data shift.
The clock pulse, which was input when the enable bit (ELB/ERB) is in not active condition, is invalid.
- In common driver application mode, the data is shifted to 80-bit common data bi-directional shift register by the CL1 clock.
Hence, this clock pin is not used (Open or connect this pin to VDD).</td><td>Controller</td></tr>
<tr><td>M</td><td>I</td><td>AC signal for LCD driver output</td><td>Alternate signal input pin for LCD driving.
Normal frame inversion signal is input in to this pin.</td><td>Controller</td></tr>
<tr><td>CL1</td><td>I</td><td>Data latch clock</td><td>- In segment driver application mode, this signal is used for latching the shift register contents at the falling edge of this clock pulse.
CL1 pulse “High” level initializes power-down function block.
- In common driver application mode, CL1 is used as a shifting clock of common output data.</td><td>Controller</td></tr>
<tr><td>DISPOFFB</td><td>I</td><td>Display OFF control</td><td>Control input pin to fix the driver output (SC1-SC80) to V0 level, during “Low” value input. LCD becomes non-selected by V0 level output from every output of segment drivers and every output of common drivers.</td><td>Controller</td></tr>
<tr><td>CS</td><td>I</td><td>COM/SEG mode control</td><td>When CS = ”Low”, T66H0004A is used as an 80-bit segment driver.
When CS = ”High”, T66H0004A is set to an 80-bit common driver.</td><td>VDD/VSS</td></tr>
<tr><td>AMS</td><td>I</td><td>Application mode select</td><td>According to the input value of the AMS and the CS pin, application mode of T66H0004A is differs as shown below.
<table>
<tr><th>CS</th><th>AMS</th><th>Application mode</th><th></th></tr>
<tr><td>0</td><td>0</td><td>4-bit parallel interface mode</td><td rowspan="2">SEG</td></tr>
<tr><td>0</td><td>1</td><td>1-bit serial interface mode</td></tr>
<tr><td>1</td><td>0</td><td>Single type application mode</td><td rowspan="2">COM</td></tr>
<tr><td>1</td><td>1</td><td>Dual type application mode</td></tr>
</table></td><td>VDD/VSS</td></tr>
<tr><td>D1_SID, D2_DL,</td><td>I/O</td><td>Display data input/serial</td><td>- In segment driver application mode, these pins are used as 4-bit data input pin (when 4-bit parallel</td><td>Controller</td></tr>
</table>

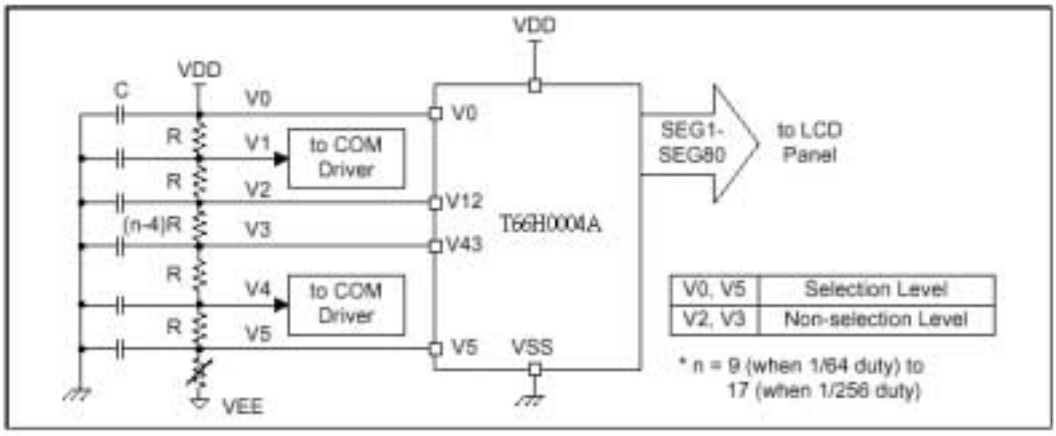
<table>
<tr><td>D3_DM,
D4_DR</td><td></td><td>input data/left, right data input output</td><td>interface mode: AMS = ”Low”), or D1_SID is used as serial data input pin and other pins are not used (connect these to VDD) (when 1-bit serial interface mode: AMS = ”High”).
- In common driver application mode, the data is shifted from D2_DL(D4_DR) to D4_DR (D2_DL),when in single type interface mode
(AMS = ”Low”). In dual-type application case, the data are shifted from D2_DL and D3_DM (D4_DR and D3_DM) to D4_DR(D2_DL). In each case the direction of the data shift and the connection of data pins are determined by SHL input (refer to NOTE3, NOTE4).</td><td></td></tr>
<tr><td>SHL</td><td>Input</td><td>Shift direction control</td><td>When SHL = ”Low”, data is shifted from left to right.
When SHL = ”High”, the direction is reversed.(refer to NOTE3)</td><td>VDD/VSS</td></tr>
<tr><td>ELB,ERB</td><td>I/O</td><td>Enable data input/output</td><td>- In segment driver application mode, the internal operation is enabled only when enable input (ELB or ERB) is “Low” (power down function). When several drivers are serially connected, the enable state of each driver is shifted according to the SHL input. Connect these pins as below.
<table>
<tr><td rowspan="2">SHL</td><td colspan="2">Segment Driver</td></tr>
<tr><td>ELB</td><td>ERB</td></tr>
<tr><td>L</td><td>Output(open)</td><td>Input(VSS)</td></tr>
<tr><td>H</td><td>Input(VSS)</td><td>Output(open)</td></tr>
</table>
- In common driver application mode, power down function is not used.
Open these pins.</td><td></td></tr>
</table>

NOTE 1. Output Level Control

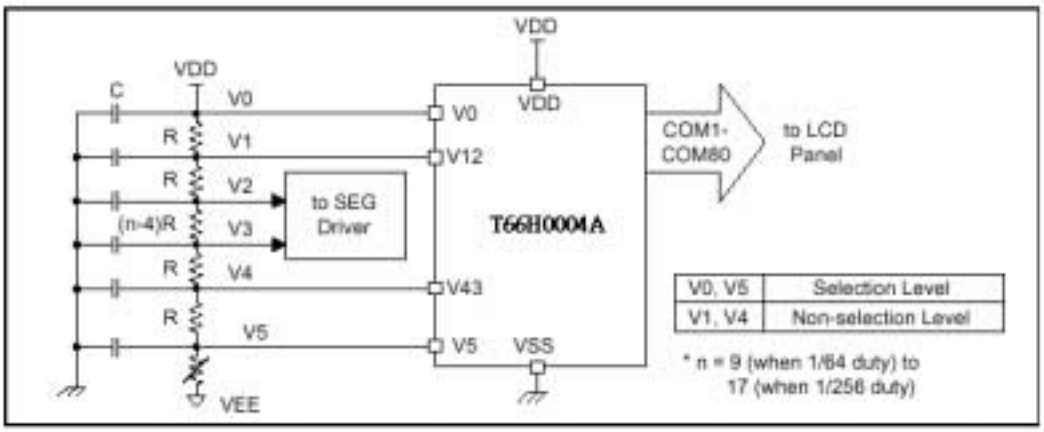
M	Latched data	DISPOFFB	Output level(SC1-SC80)	
			SEG Mode	COM Mode
L	L	H	V12(V2)	V12(V1)
L	H	H	V0	V5
H	L	H	V43(V3)	V43(V4)
H	H	H	V5	V0
X	X	L	V0	V0

NOTE 2. LCD Driving Voltage Application Circuit

(1) Segment driver application(CS = "Low")

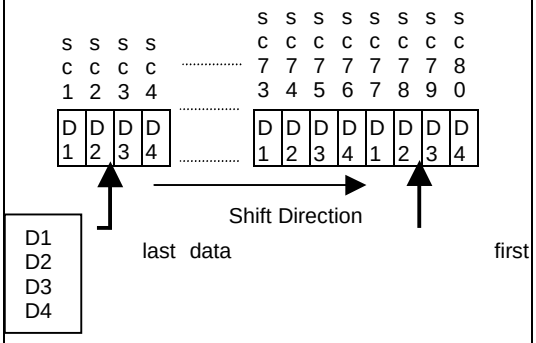
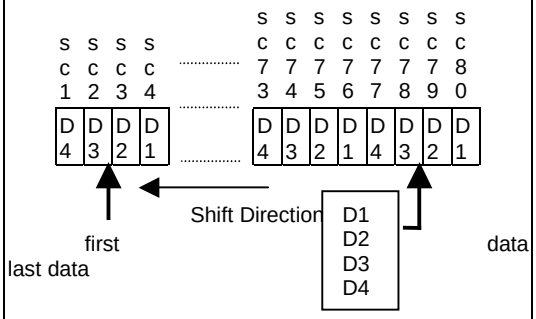
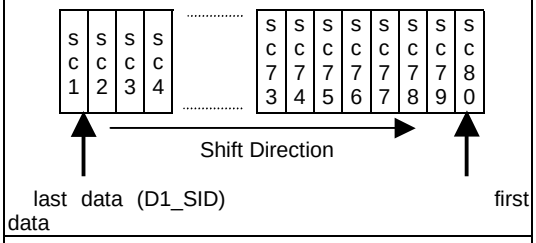
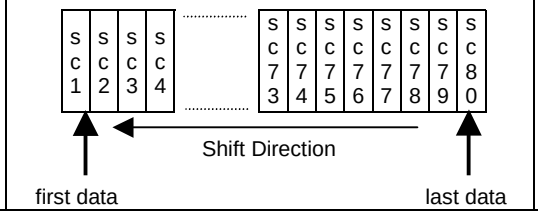


(2) Common driver application(CS = "High")

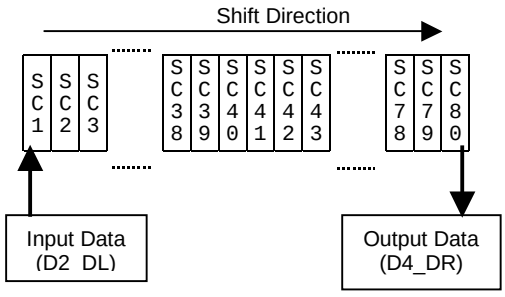
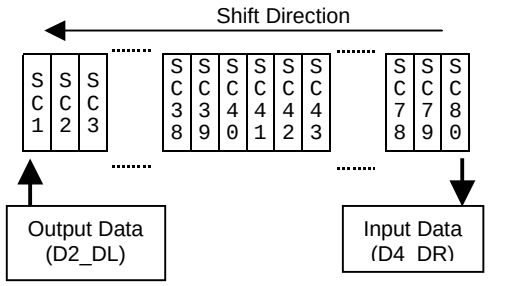
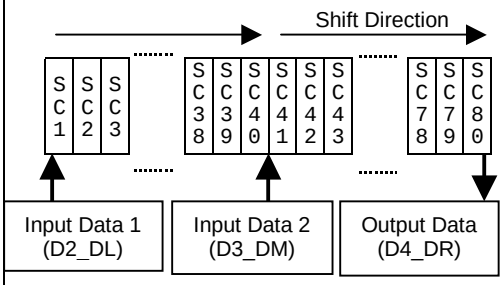
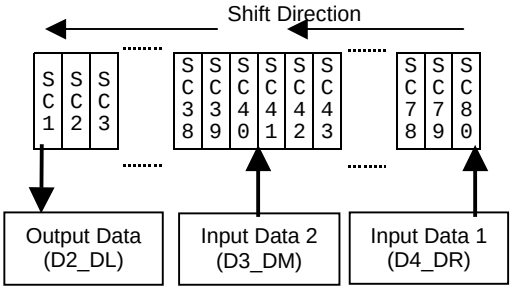


NOTE 3. Data Shift Direction according to Control Signals

(1) When CS = ”Low”(Segment driver application)

AMS	SHL	Application mode	Data Direction	Input Pin
L	L	4-Bit Parallel Data Transfer Mode(SEG)		D1_SID, D2_DL, D3_DM, D4_DR
	H			
H	L	1-Bit Serial Data Transfer Mode (SEG)		D1_SID
	H			

(2) When CS = ”High”(common driver application)

AMS	SHL	Application mode	Data Direction	Input Pin
L	L	Single-type Application Mode (COM)		D2_DL
	H			D4_DR
H	L	Dual-type Application Mode (COM)		D2_DL, D3_DM
	H			D4_DR, D3_DM

NOTE 4. Usage of Data Pins

COM/SEG (CS pin)	Application mode (AMS pin)	SHL	Data interface pin			
			D1_SID	D2_DL	D3_DM	D4_DR
SEG (CS = ”Low”)	4-bit parallel interface mode(AMS = ”Low”)	X	D1(input)	D2(input2)	D3(input3)	D4(input4)
	1-bit serial interface mode (AMS = ”High”)	X	SID(input)	Connect to VDD		
COM (CS = ”High”)	Single-type application mode(AMS = ”Low”)	L	Open	DL(input)	Open	DR(output)
		H		DL(output)		DR(input)
	Dual-type application mode (AMS = ”high”)	L	Open	DL(input1)	DM(input2)	DR(output2)
		H		DL(output2)	DM(input2)	DR(input1)

MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit
Power supply voltage	VDD	-0.3 to +7.0	V
Driver supply voltage	Vlcd	0 to +30	
Input voltage	Vin	-0.3 to VDD+0.3	
Operating temperature	Topr	-30 to +85	•
Storage temperature	Tstg	-55 to +150	

***NOTE:** Voltage greater than above may do damage to the circuit.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(1) Segment Driver Application

(Vss = 0V, Ta=-30 to +85°C)

Characteristic	Symbol	Test Condition		Min.	Typ.	Max.	Unit
Operating Voltage 1	V_{DD}	-		2.7	-	5.5	V
	V_{LCD}	$V_{IN} = V_{DD} - V_{EE}$		6	-	28	
Input voltage (1)	V_{IH}	-		$0.8V_{DD}$	-	V_{DD}	
	V_{IL}	-		0	-	$0.2\ V_{DD}$	
Output voltage (2)	V_{OH}	I_{OH} = -0.4mA		V_{DD}-0.4	-	-	V
	V_{OL}	I_{OL} = 0.4mA		-	-	0.4	
Input leakage current 1 (1)	I_{IL1}	$V_{IN} = V_{DD}$ to Vss		-10	-	10	uA
Input leakage current 2 (3)	I_{IL2}	$V_{IN} = V_{DD}$ to V_{EE}		-25	-	25	
On resistance (4)	R_{ON}	I_{ON} = 100uA		-	2	4	KOhm
Supply current (5)	I_{STBY}	F_{CL1} =32 KHz M=Vss	Vss pin	-	-	50	uA
	I_{DD}	F_{CL1} = 32KHz F_M = 80Hz	V_{DD}= 5V	-	-	5	mA
			V_{DD} = 3V	-	-	2	
	I_{EE}		V_{DD} =5V	-	-	500	uA

NOTES:

1. Applied to Cl1,CL2,ELB,ERB,D1_SID-D4_DR,SHL,DISPOFFB,M,CS,AMS pin
2. ELB,ERB pin
3. V0,V12,V43,V5 pin
4. $V_{LCD} = V_{DD} - V_{EE}$, $V0 = V_{DD}$ =5V, $V5 = V_{EE}$=-23V

   $V12 = V_{DD} - 2/n(V_{LCD})$, $V43 = V_{EE} + 2/n(V_{LCD})$, n=17(1/256 duty,1/17 bias)
5. $V0 = V_{DD}$, V12=1.71V(V_{DD} =5V) or –0.06V(V_{DD} =3V)

   V43=-19.71V(V_{DD} =5V) or –19.94V(V_{DD} =3V), $V5 = V_{EE}$=-23V, no-load condition (1/256 duty,1/17 bias)

   4-bit parallel interface mode.

   Istby: V_{DD} =5V, CL2=Vss, SHL=Vss, DISPOFFB= V_{DD}, M = Vss, display data pattern=0000

   I_{DD}: V_{DD} =3V, f_{CL2}=4MHz, display data pattern=0101

   V_{DD} = 5V, f_{CL2} f_{CL2}=5.12MHz, display data pattern=0101

   I_{EE}: V_{DD}=5V, f_{CL2}=5.12MHz, display data pattern=0101, V_{EE} pin

ELECTRICAL CHARACTERISTICS

(2) Common Driver Application

(Vss = 0V, Ta=-30 to +85°C)

Characteristic	Symbol	Test Condition		Min.	Typ.	Max.	Unit
Operating Voltage	V_{DD}	-		2.7	-	5.5	V
	V_{LCD}	V_{IN} = V_{DD} –V_{EE}		6	-	28	
Input voltage (1)	V_{IH}	-		0.8 V_{DD}	-	V_{DD}	
	V_{IL}	-		0	-	0.2 V_{DD}	
Output voltage (3)	V_{OH}	I_{OH} = -0.4mA		V_{DD} -0.4	-	-	V
	V_{OL}	I_{OL} = 0.4mA		-	-	0.4	
Input leakage current 1 (1)	I_{IL1}	V_{IN} = V_{DD} to Vss		-10	-	10	uA
Input leakage current 2 (2)	I_{IL2}	V_{IN}=0, V_{DD} =5V(PULL UP)		-50	-125	-250	
Input leakage current 3 (4)	I_{IL3}	V_{IN} = V_{DD} to V_{EE}		-25	-	25	
On resistance (5)	R_{ON}	I_{ON} = 100uA		-	2	4	KOhm
Supply current(6)	I_{STBY}	F_{CL1}=32KHz	Vss pin	-	-	50	uA
	I_{DD}	F_{CL1}=32KHz F_M=80Hz	V_{DD} =5V	-	-	200	
			V_{DD} =3V	-	-	120	
	I_{EE}		V_{DD} =5V	-	-	150	

NOTES:

1. Applied to CL1, D2_DL (SHL=LOW), D4_DR (SHL=HIGH), SHL, DISPOFFB, M, CS, AMS pin.
2. Pull-up input pins: CL2, D1_SID, D3_DM (AMS=HIGH), ELB (SHL=LOW), ERB (SHL= HIGH).
3. D2_DL (SHL = HIGH), D4_DR (SHL = LOW) pin.
4. V0, V12, V43, V5 pin
5. V_{LCD} = V_{DD} -V_{EE}, V0= V_{DD} =5V,V5=V_{EE}=-23V

   V12 = V_{DD} -1/n(V_{LCD}), V43= V_{EE} +1/n(V_{LCD}), n=17(1/256 duty, 1/17 bias)
6. V0= V_{DD}, V12=3.35V(V_{DD} =5V) or 1.47V(V_{DD} =3V),

   V43=-21.35V(V_{DD} =5V) or –21.47V(V_{DD} =3V), V5= V_{EE} =-23V, no-load condition (1/256 duty, 1/17 bias)Single-type mode operation: AMS = Vss, SHL = Vss,

   DISPOFFB = V_{DD} D1_SID=D3_DM=VDD, D4_DR=OPEN, ELB+ERB+OPEN,

   I_{STBY}: V_{DD} =5V, M=Vss, D2_DL=Vss

   I_{DD}: f_M=80Hz, D2_DL= V_{DD}

   V_{DD} =3V, display data pattern=10000000…,01000000…,00100000…,00010000…,…

   V_{DD} =5V.displat data pattern=10000000…,01000000…,00100000…,00010000…,…

   I_{EE}: f_M=80Hz,D2_DL= V_{DD}

   V_{DD} =5V, current through V_{EE} pin, display data

   pattern=100000000…,01000000…,00100000…,00010000…,…

AC CHARACTERRISTICS

(1) Segment Driver Application

(Vss = 0V, Ta=-30 to +85°C)

Characteristic	Symbol	Test Condition	(1) VDD=5V±10%			(2) VDD=3V±10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock cycle time	tcy	Duty=50%	125	-	-	250	-	-	ns
Clock pulse width	twck	-	45	-	-	95	-	-	
Clock rise/fall time	t_R/t_F	-	-	-	30	-	-	30	
Data set-up time	t_{DS}	-	30	-	-	65	-	-	
Data hold time	t_{DH}	-	30	-	-	65	-	-	
Clock set-up time	tcs	-	80	-	-	120	-	-	
Clock hold time	tch	-	80	-	-	120	-	-	
Propagation delay time	tphl	ELB Output	-	-	60	-	-	125	
		ERB Output			60			125	
ELB,ERB set-up time	tpsu	ELB Input	30	-	-	65	-	-	
		ERB Input	30			65			
DISPOFFB low pulse width	t_{WDL}	-	1.2	-	-	1.2	-	-	us
DISPOFFB clear time	tcd	-	100	-	-	100	-		ns
M-OUT propagation delay time	tpd1	C_L=15pF	-	-	1.0	-	-	1.2	us
CL1-OUT propagation delay time	tpd2		-	-	1.0	-	-	1.2	
DISPOFFB-OUT propagation delay time	tpd3		-	-	1.0	-	-	1.2	
Latch pulse rise to Shift clock rise time	t_{LS}		80	-	-	120	-	-	ns

AC CHARACTERISTICS

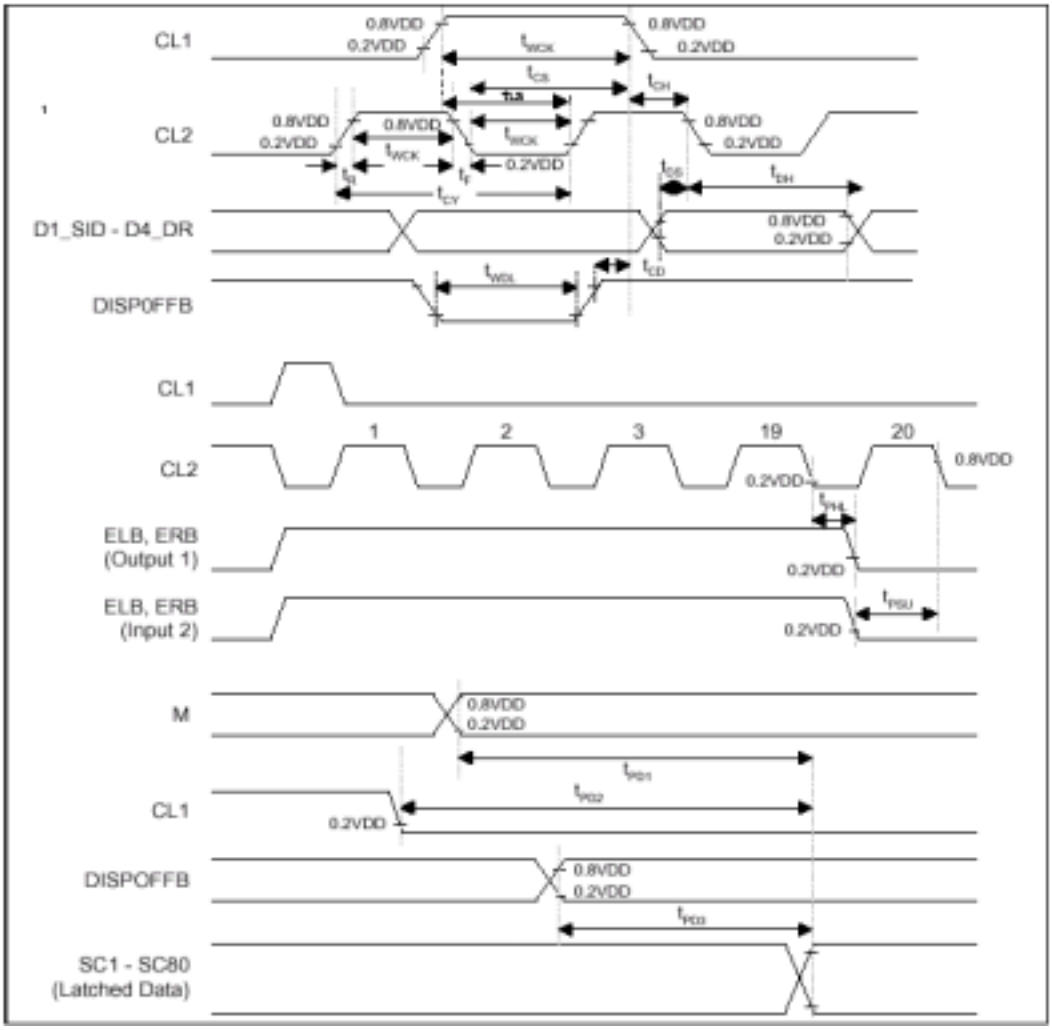
(2) Common Driver Application

(Vss = 0V, Ta=-30 to +85°C)

Characteristic	Symbol	Test Condition	(1) VDD=5V±10%			(2) VDD=3V±10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock cycle time	tcy	Duty=50%	250	-	-	500	-	-	ns
Clock pulse width	twck	-	45	-	-	95	-	-	
Clock rise/fall time	tR/tF	-	-	-	50	-	-	50	
Data set-up time	tDS	-	30	-	-	65	-	-	
Data hold time	tDH	-	30	-	-	65	-	-	
DISPOFFB low pulse width	twdl	-	1.2	-	-	1.2	-	-	us
DISPOFFB clear time	tcd	-	100	-	-	100	-		ns
Output delay time	tdl	CL=15pF	-	-	200	-	-	250	
M-OUT propagation delay time	tpd1		-	-	1.0	-	-	1.2	us
CL1-OUT propagation delay time	tpd2		-	-	1.0	-	-	1.2	
DISPOFFB-OUT propagation delay time	tpd3		-	-	1.0	-	-	1.2	

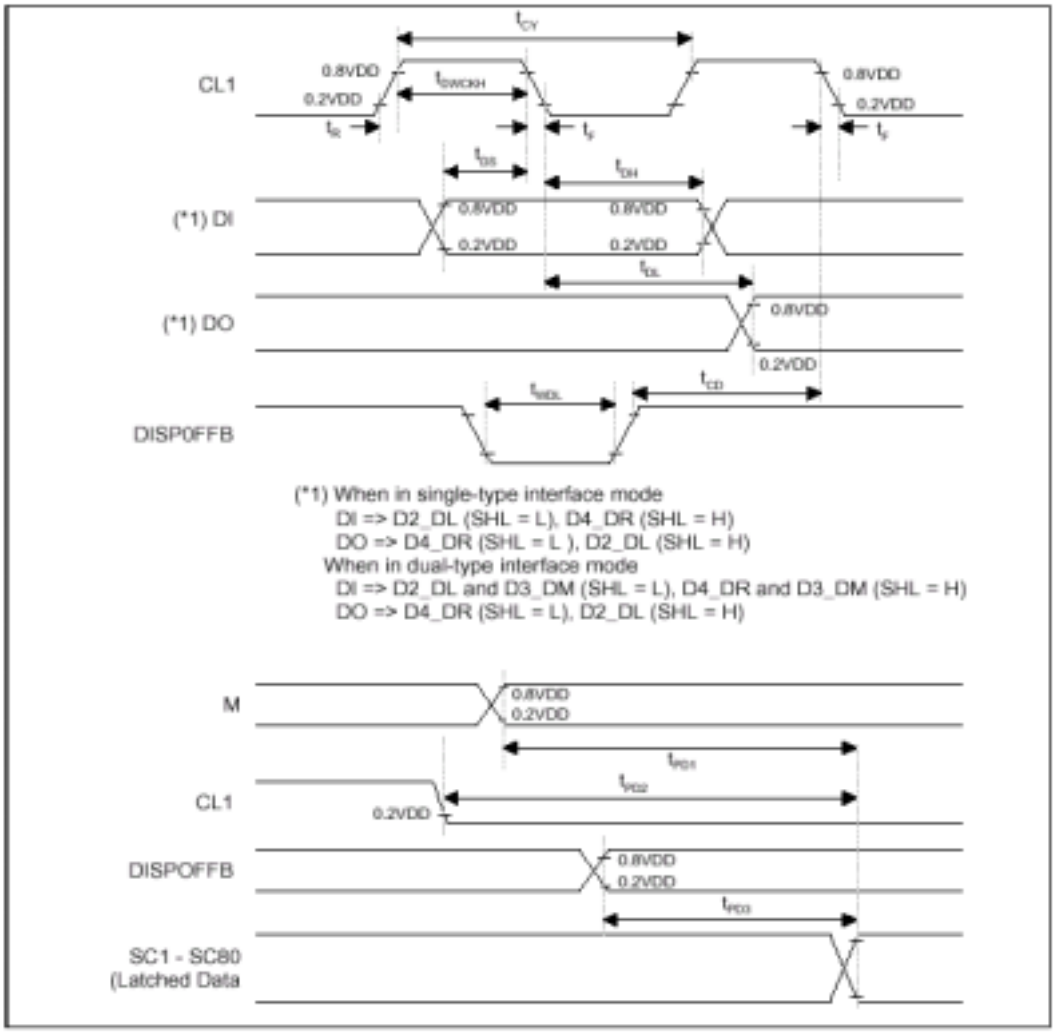
AC CHARACTERISTICS

(3) Segment Driver Application Timing



AC CHARACTERISTICS

(4) Common Driver Application Timing

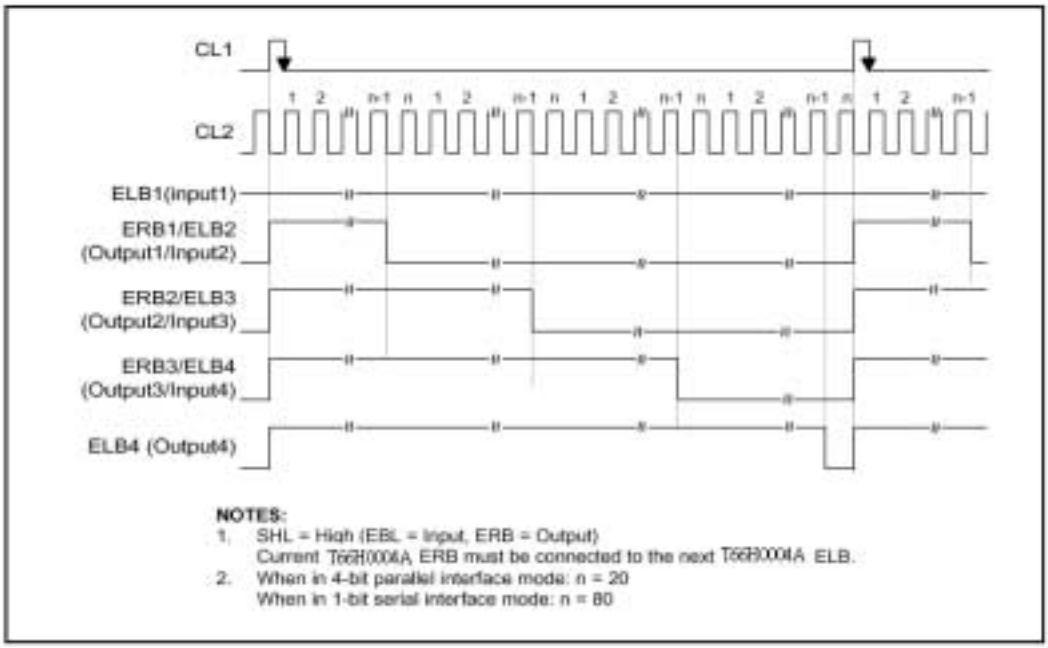


POWER DOWN FUNCTION

In the case of cascade connection of segment mode drivers,T66H0004A has a “power down function” In order to reduce the power consumption.

SHL	Enable input	Enable output	Current driver status	The other drivers status
L	ERB	ELB	While ERB = ”Low”, current driver is enabled.	Disabled
H	ELB	ERB	While ELB = ”Low”, current driver is enabled	Disabled

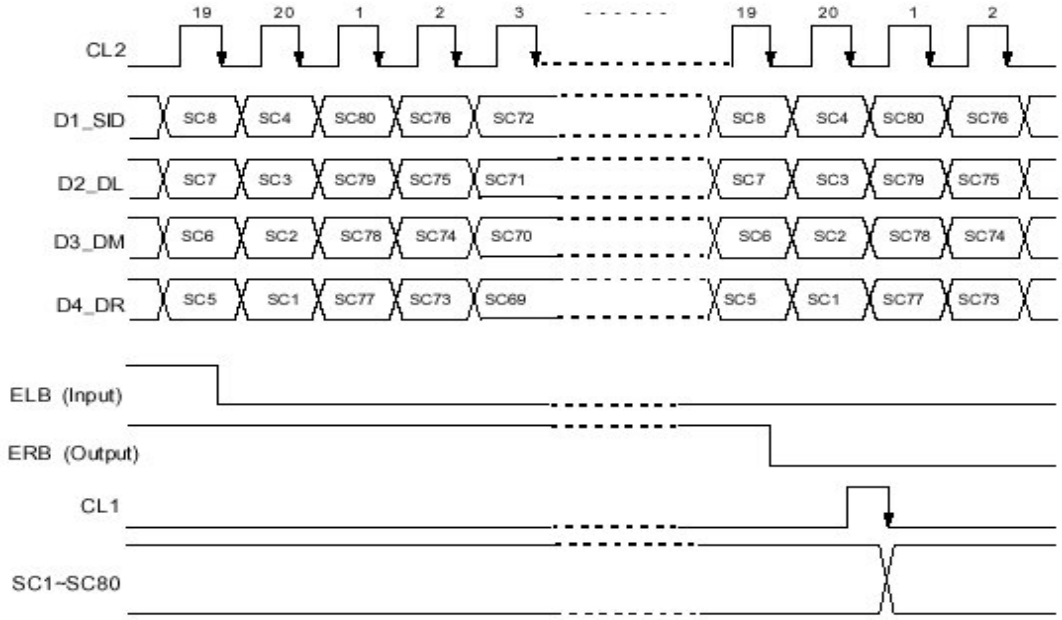
* In the case of common driver application, power down function dose not work.



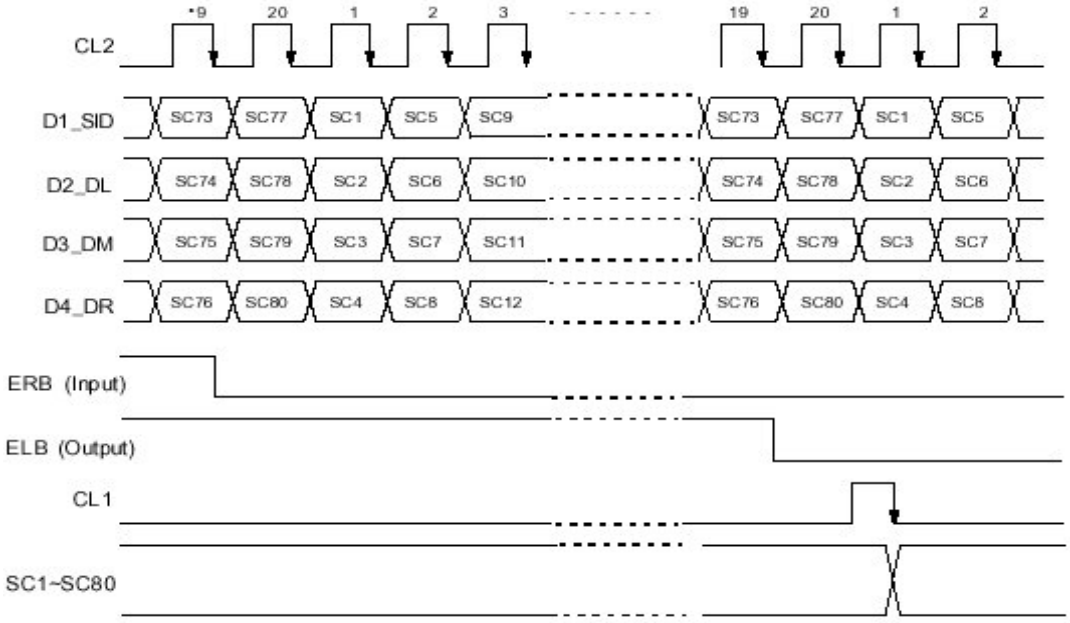
OPERATION TIMING DIAGRAM

(1) 4-bit Parallel Mode Interface Segment Driver

- When SHL = ”High”

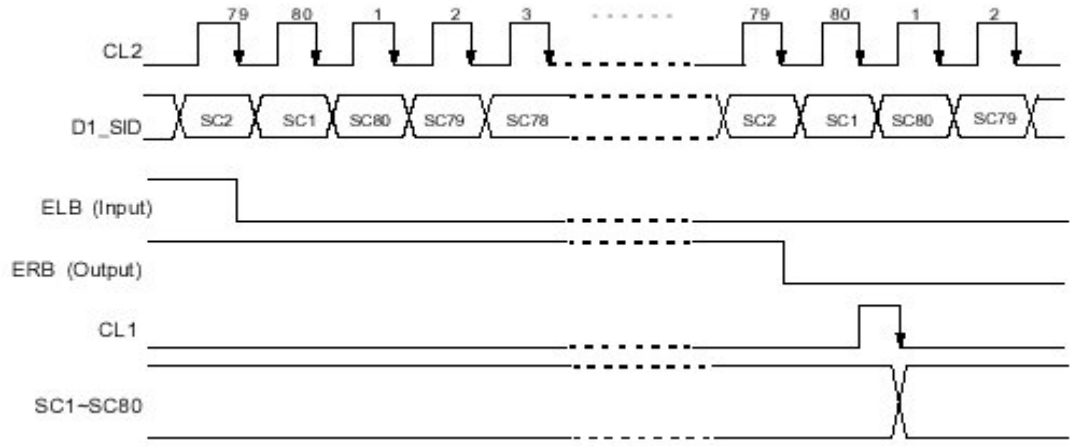


- When SHL = ”Low”

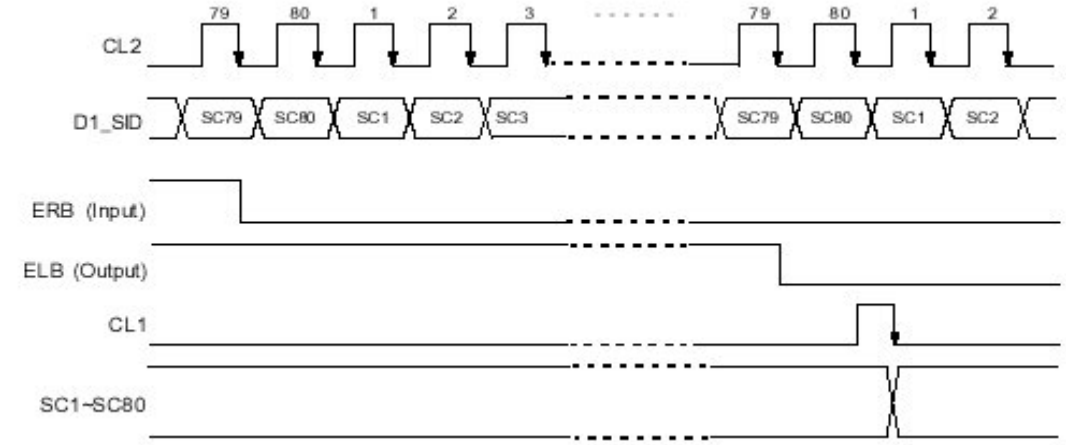


(2) 1-bit Serial Mode Interface Segment Driver

- When SHL = High”

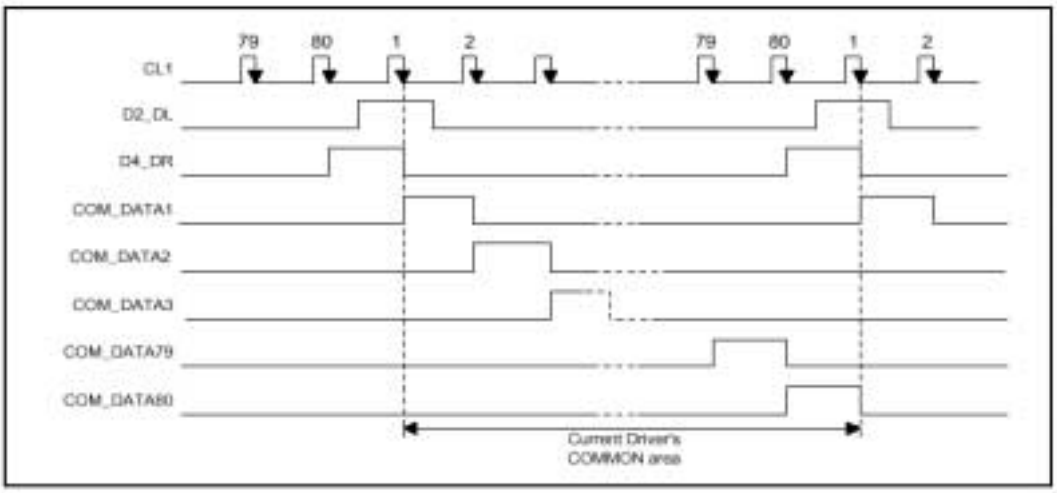


- When SHL = ”Low”

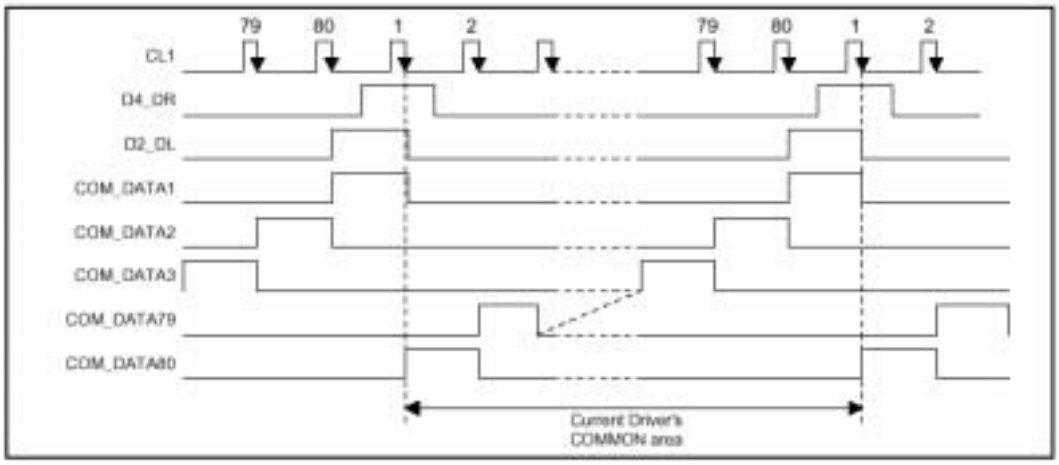


(3) Single-type Interface Mode Common Driver

- When SHL = ”Low”

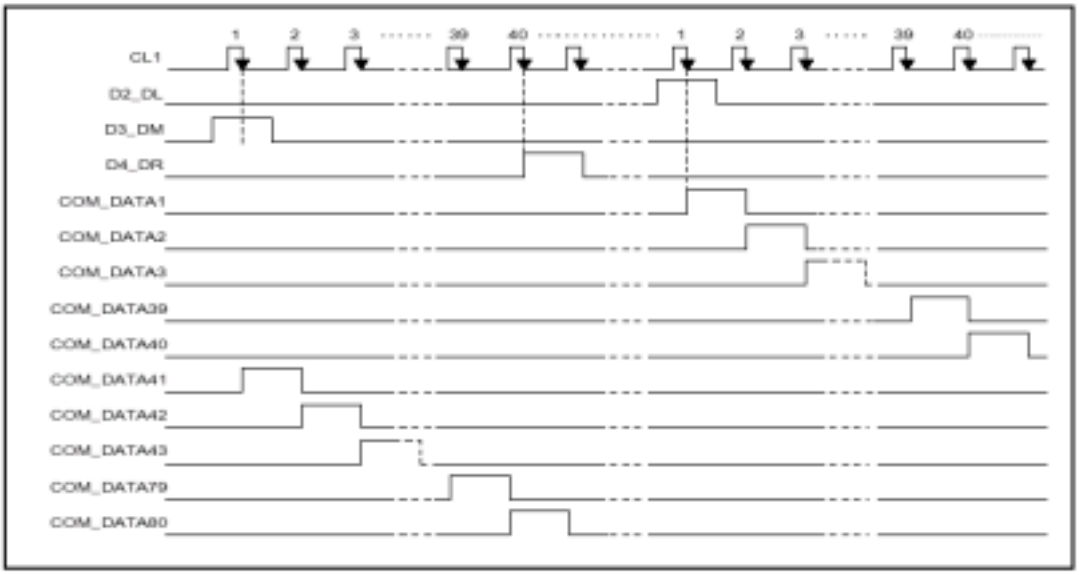


- When SHL = ”High”

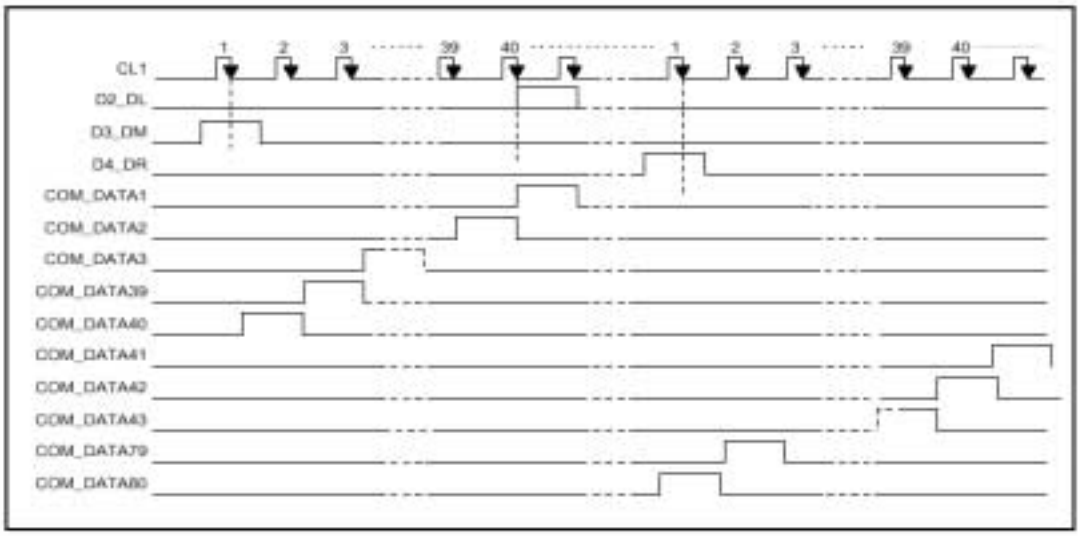


(4) DUAL-type Interface Mode Common Driver

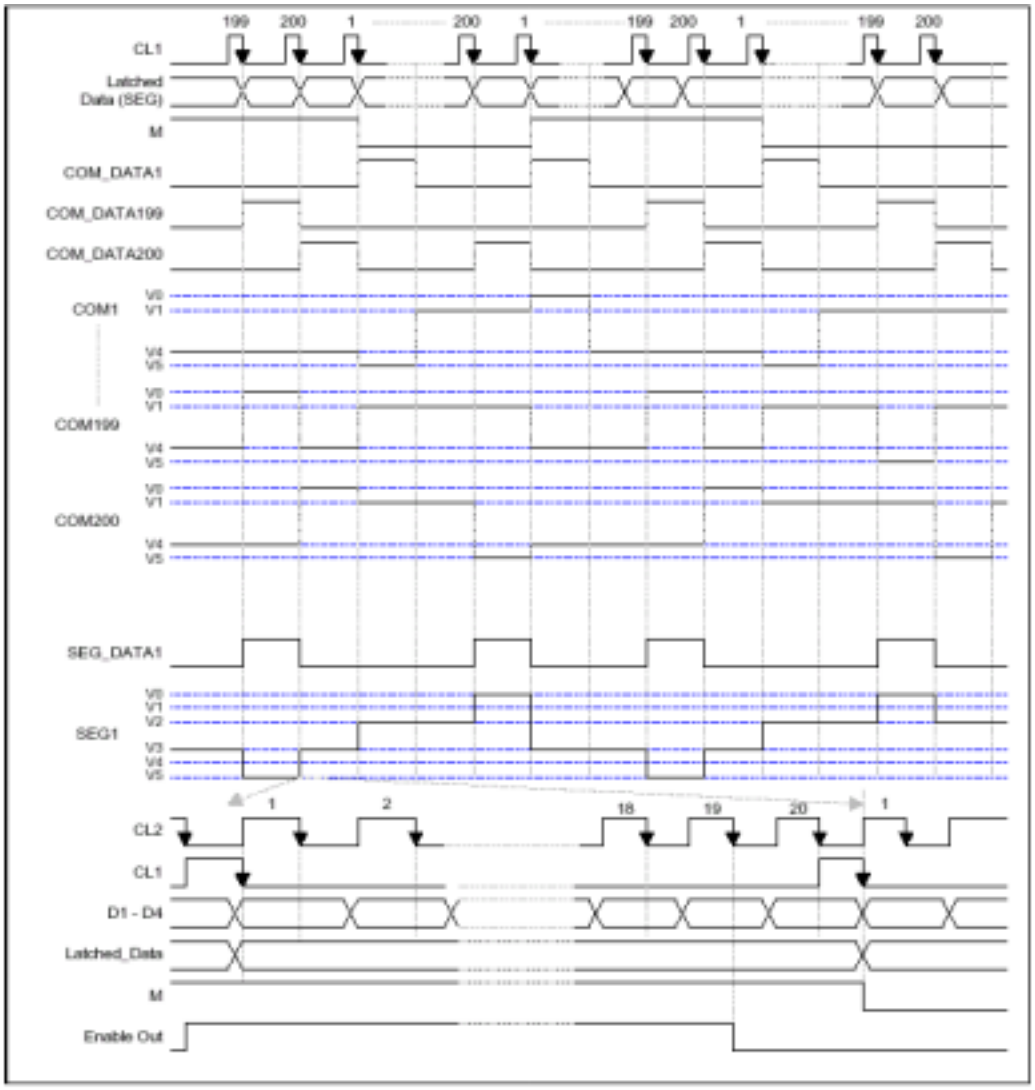
- When SHL = ”Low”



- When SHL = ”High”



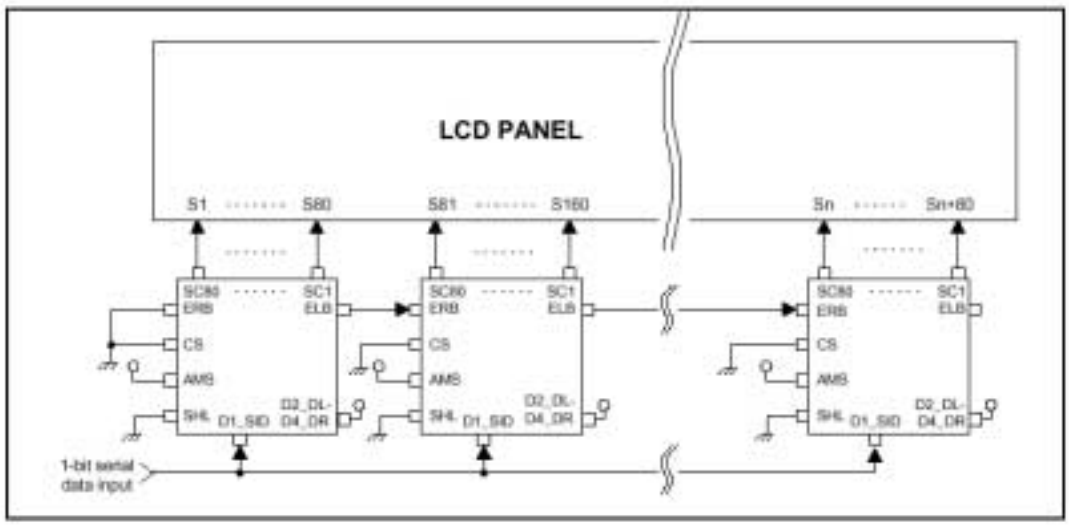
(5) Common/Segment driver Timing(1/200 DUTY)



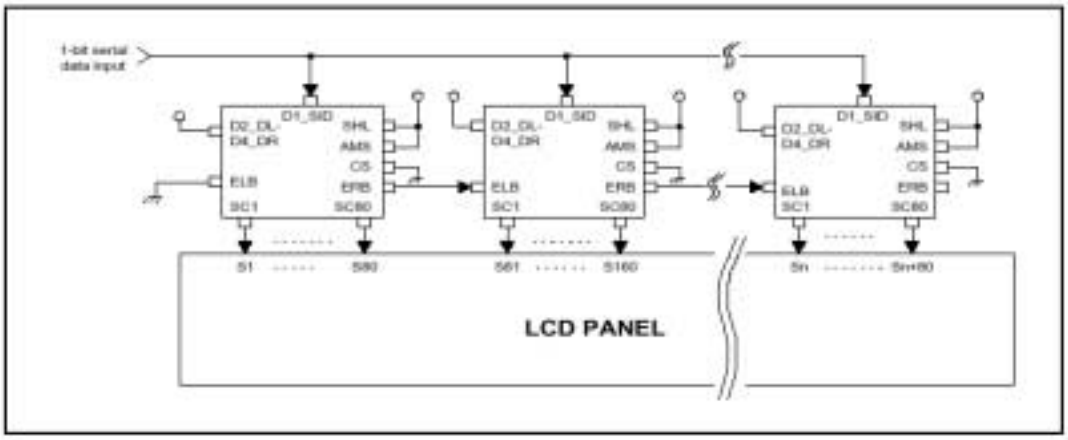
APPLICATION INFORMATION

1-bit Serial Interface Mode (80 output Segment Driver)

(a)Lower View(SHL = L , AMS = H)

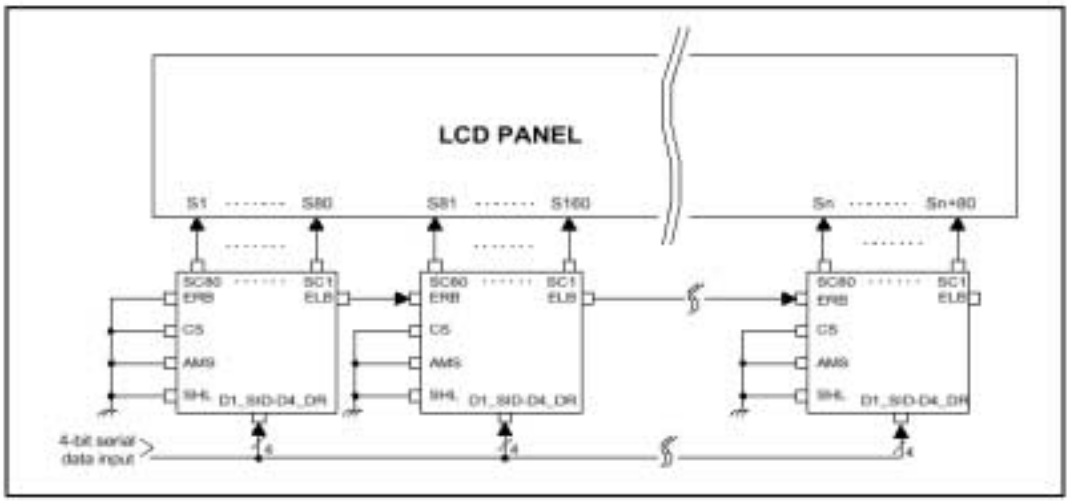


(b)Upper View (SHL = H, AMS = H)

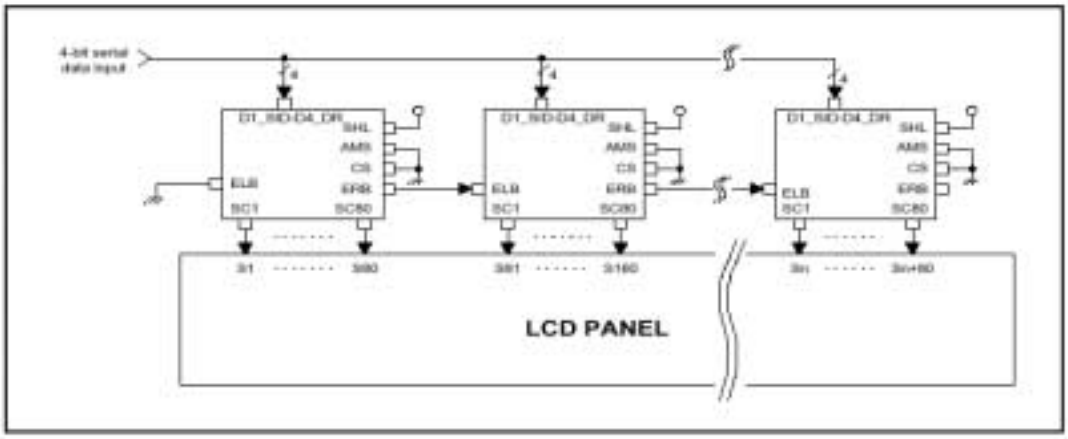


4-bit Parallel Interface Mode (80 output Segment Driver)

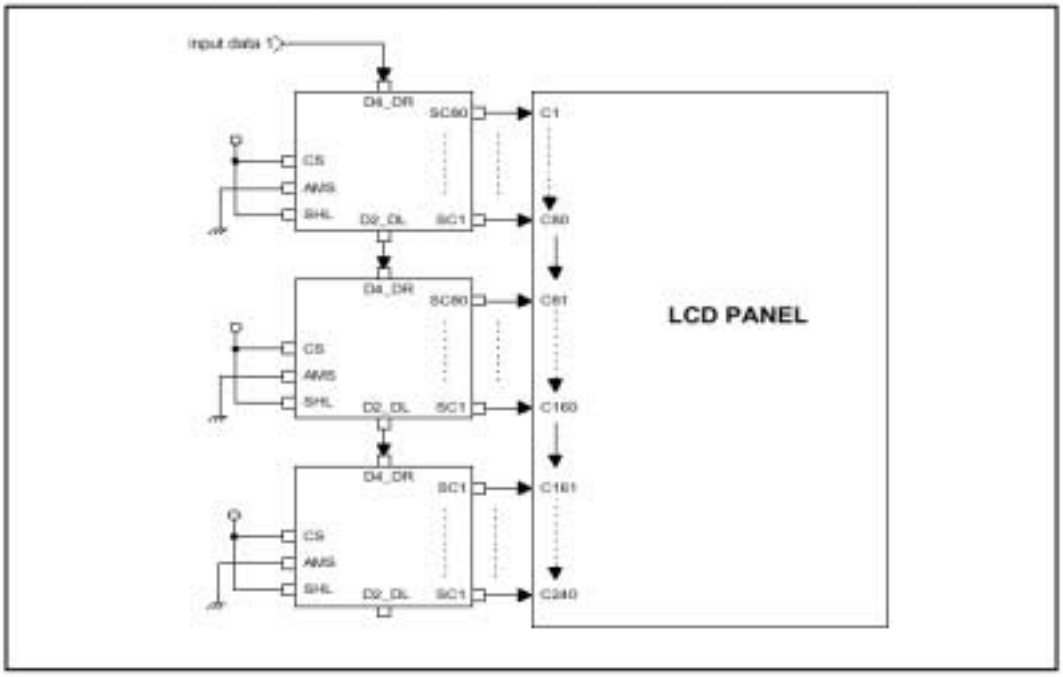
(a) Lower View(SHL = L , AMS = L)



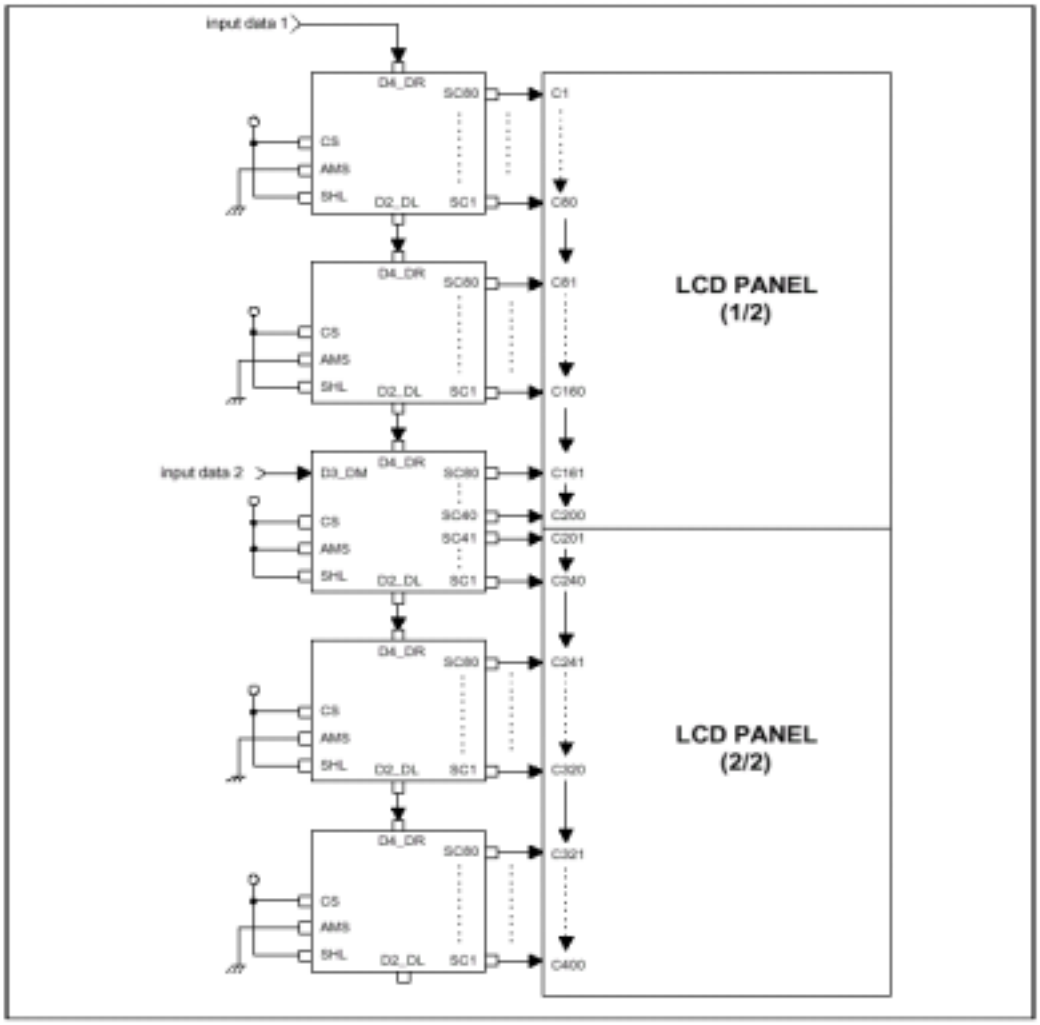
(b) Upper View (SHL = H , AMS = L)



Single-type Interface Mode (80 output Common Driver)

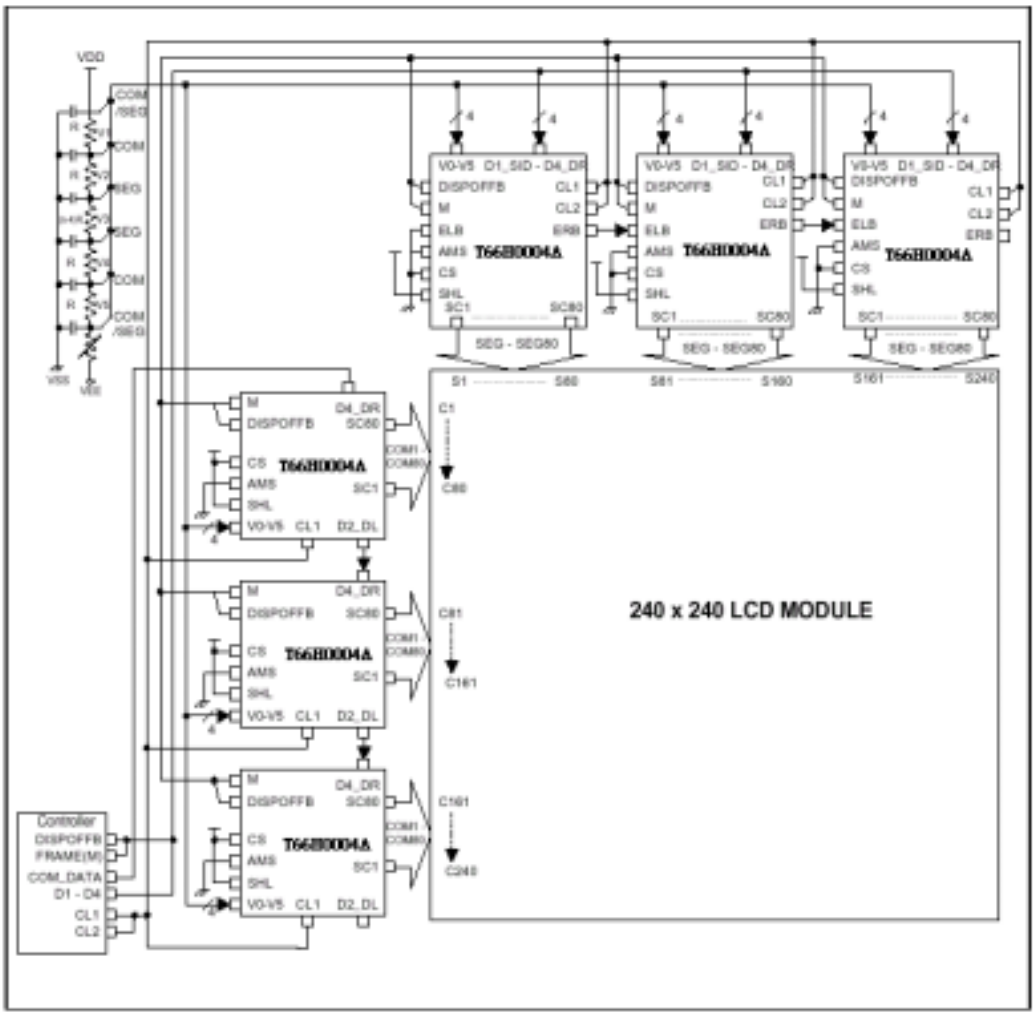


Dual-type Interface Mode (40 output Common Driver)



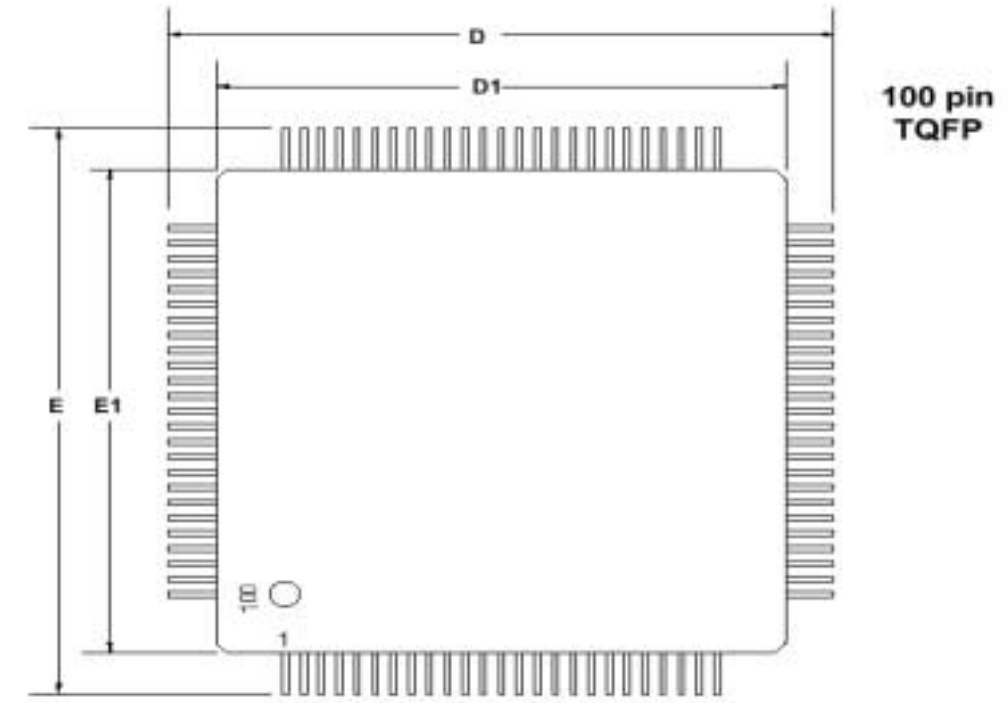
NOTE: Using this application mode (dual-type common mode), the duty ratio can be reduced to half. In case, 1/200 duty can be used to drive the 400 common LCD panel.

APPLICATION CIRCUIT EXAMPLE



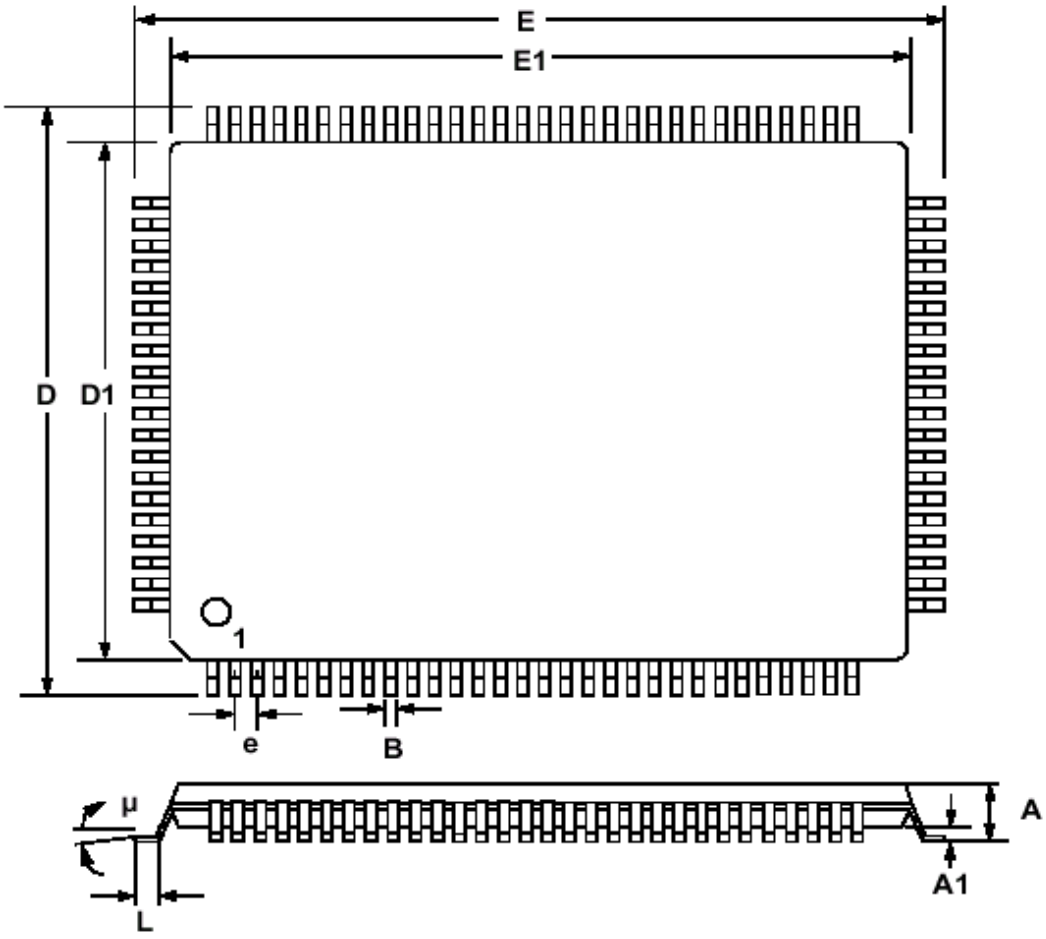
PACKAGE DIMENSION (Unit: mm)

100 pin TQFP



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.66	-	-	0.065
A1	0.00	-	-	0.000	-	-
B	0.14	0.20	0.26	0.006	0.008	0.010
C	0.40	0.51	0.60	0.016	0.020	0.024
D	15.70	16.00	16.30	0.618	0.630	0.642
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.70	16.00	16.30	0.618	0.630	0.642
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.375	0.5	0.625	0.015	0.020	0.025
L	0.30	0.51	0.70	0.012	0.020	0.028
∝	0°	-	12°	0°	-	12°
M	1.00 BSC			0.039 BSC		

100 pin QFP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.134	----	3.400
A1	0.010	0.014	0.250	0.350
B	0.009	0.015	0.220	0.380
D	0.667	0.687	16.950	17.450
D1	0.547	0.555	13.900	14.100
E	0.904	0.923	22.950	23.450
E1	0.783	0.791	19.900	20.100
e*	0.022	0.030	0.550	0.750
μ	0.000°	7.000°	0.000°	7.000°
L	0.018	0.030	0.450	0.750

* Nominal pin pitch is 0.65 mm

Pad List(For T66H0004A1S use)

Pad No.	Pin Name	X	Y
1	Y51	-1127.2	1473.25
2	Y52	-1127.2	1373.25
3	Y53	-1127.2	1273.25
4	Y54	-1127.2	1173.25
5	Y55	-1127.2	1073.25
6	Y56	-1127.2	973.25
7	Y57	-1127.2	873.25
8	Y58	-1127.2	773.25
9	Y59	-1127.2	673.25
10	Y60	-1127.2	573.25
11	Y61	-1127.2	473.25
12	Y62	-1127.2	373.25
13	Y63	-1127.2	273.25
14	Y64	-1127.2	173.25
15	Y65	-1127.2	73.25
16	Y66	-1127.2	-26.75
17	Y67	-1127.2	-126.75
18	Y68	-1127.2	-226.75
19	Y69	-1127.2	-326.75
20	Y70	-1127.2	-426.75
21	Y71	-1127.2	-526.75
22	Y72	-1127.2	-626.75
23	Y73	-1127.2	-726.75
24	Y74	-1127.2	-826.75
25	Y75	-1127.2	-926.75
26	Y76	-1127.2	-1026.75
27	Y77	-1127.2	-1126.75
28	Y78	-1127.2	-1226.75
29	Y79	-1127.2	-1326.75
30	Y80	-1127.2	-1426.75
31	ERB	-949.75	-1534.4
32	VEEP:G	-849.75	-1534.4

Pad No.	Pin Name	X	Y
36	VOP:P	-449.75	-1534.4
37	CS	-349.75	-1534.4
38	M	-249.75	-1534.4
39	DISSPO	-149.75	-1534.4
40	VDD	-49.75	-1534.4
41	SHL	50.25	-1534.4
42	VSS	150.25	-1534.4
43	D4_DR	250.25	-1534.4
44	D3_DM	350.25	-1534.4
45	D2_DL	450.25	-1534.4
46	D1_SID	550.25	-1534.4
47	CL2	650.25	-1534.4
48	AMS	750.25	-1534.4
49	CL1	850.25	-1534.4
50	ELB	950.25	-1534.4
51	Y1	1127.7	-1426.75
52	Y2	1127.7	-1326.75
53	Y3	1127.7	-1226.75
54	Y4	1127.7	-1126.75
55	Y5	1127.7	-1026.75
56	Y6	1127.7	-926.75
57	Y7	1127.7	-826.75
58	Y8	1127.7	-726.75
59	Y9	1127.7	-626.75
60	Y10	1127.7	-526.75
61	Y11	1127.7	-426.75
62	Y12	1127.7	-326.75
63	Y13	1127.7	-226.75
64	Y14	1127.7	-126.75
65	Y15	1127.7	-26.75
66	Y16	1127.7	73.25
67	Y17	1127.7	173.25

33	V5P	-749.75	-1534.4
34	V43P	-649.75	-1534.4
35	V12P	-549.75	-1534.4

68	Y18	1127.7	273.25
69	Y19	1127.7	373.25
70	Y20	1127.7	473.25

Pad No.	Pin Name	X	Y
71	Y21	1127.7	573.25
72	Y22	1127.7	673.25
73	Y23	1127.7	773.25
74	Y24	1127.7	873.25
75	Y25	1127.7	973.25
76	Y26	1127.7	1073.25
77	Y27	1127.7	1173.25
78	Y28	1127.7	1273.25
79	Y29	1127.7	1373.25
80	Y30	1127.7	1473.25
81	Y31	950.25	1534.4
82	Y32	850.25	1534.4
83	Y33	750.25	1534.4
84	Y34	650.25	1534.4
85	Y35	550.25	1534.4
86	Y36	450.25	1534.4
87	Y37	350.25	1534.4

88	Y38	250.25	1534.4
89	Y39	150.25	1534.4
90	Y40	50.25	1534.4
91	Y41	-49.75	1534.4
92	Y42	-149.75	1534.4
93	Y43	-249.75	1534.4
94	Y44	-349.75	1534.4
95	Y45	-449.75	1534.4
96	Y46	-549.75	1534.4
97	Y47	-649.75	1534.4
98	Y48	-749.75	1534.4
99	Y49	-849.75	1534.4
100	Y50	-949.75	1534.4

CHIP SIZE ==>
(2349.4,3163.8)

