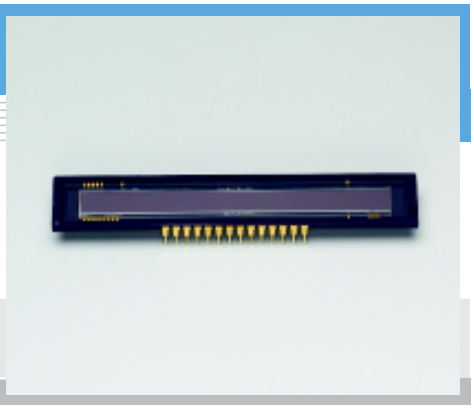
CCD area image sensor
S9979



TDI operation / large active area CCD

S9979 is a FFT-CCD area image sensor specifically designed for low-light-level detection in scientific applications. In particular, this image sensor is ideally suited for extremely low-light-level detection in such fields as spectroscopy and astronomy.
By operating this image sensor in MPP mode, the dark current can be exceedingly reduced. Moreover, use of the low-noise readout amplifier enables low-light-level detection and long integration time, thus achieving a wide dynamic range.
S9979 has an effective pixel size of 48 × 48 µm and is available in active area of 73.728 (H) × 6.144 (V) mm.

Features

- TDI (Time Delay Integration) operation
- 1536 (H) × 128 (V) pixel format
- Pixel size: 48 × 48 µm
- 100 % fill factor
- Wide dynamic range: 20000
- Low dark signal: 2 ke⁻/pixel/s Typ. (MPP mode)
- Low readout noise: 60 e⁻rms Typ.
- MPP operation

Applications

- Industrial inspection
- Low-light-level detection

■ Specification

Type No.	Cooling	Number of total pixels	Number of active pixels	Active area [mm (H) × mm(V)]
S9979	Non-cooled	1536 × 128	1536 × 128	73.728 × 6.144

■ General ratings

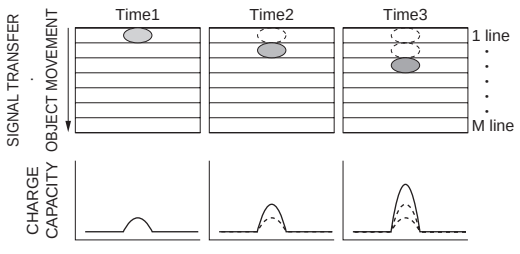
Parameter	Specification
CCD structure	Full frame transfer or TDI
Fill factor	100 %
Number of active pixels	1536 (H) × 128 (V)
Pixel size	48 (H) × 48 (V) µm
CCD active area	73.728 (H) × 6.144 (V) mm
Vertical clock phase	2 phase
Horizontal clock phase	2 phase
Output circuit	Two-stage MOSFET source follower with load resistance
Package	28-pin ceramic package
Window *1	Quartz window (standard) Temporarily attached window is available

*1: Temporary window type (ex. S9979N) and UV coat type (ex. S9979UV) are available upon request.
Temporary window is fixed by tape to protect the CCD chip and wire bonding.

What is TDI operation

In FFT-CCD, TDI operation performs continuous imaging of a fast-moving object, by transferring the signals at the same rate as the speed of the moving object. TDI operation allows acquiring continuous, clear images with high S/N and no frame breaks.
Since signals of all pixels in each row are accumulated, sensitivity variations can be drastically improved compared to two-dimensional operation.

● Signal integration by TDI operation



PRELIMINARY DATA
Sep. 2005

SOLID STATE DIVISION

■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-30	-	+30	°C
Storage temperature	Tstg	-30	-	+70	°C
OD voltage	V_{OD}	-0.5	-	+20	V
RD voltage	V_{RD}	-0.5	-	+18	V
ISV voltage	V_{ISV}	-0.5	-	+18	V
IGV voltage	V_{IGV}	-15	-	+15	V
IGH voltage	V_{IGH}	-15	-	+15	V
SG voltage	V_{SG}	-15	-	+15	V
OG voltage	V_{OG}	-15	-	+15	V
RG voltage	V_{RG}	-15	-	+15	V
TG voltage	V_{TG}	-15	-	+15	V
Vertical clock voltage	V_{P1AV}, V_{P2AV} V_{P1BV}, V_{P2BV}	-15	-	+15	V
Horizontal clock voltage	V_{P1AH}, V_{P2AH} V_{P1BH}, V_{P2BH}	-15	-	+15	V

■ Operating conditions (MPP mode, Ta=25 °C)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage			V_{OD}	12	15	-	V
Reset drain voltage			V_{RD}	12	13	14	V
Output gate voltage			V_{OG}	-0.5	2	5	V
Output transistor ground voltage			V_{SSA}	-	0	-	V
Substrate voltage			V_{SSD}	-5	0	-	V
Test point	Vertical input source		V_{ISV}	-	V_{RD}	-	V
	Vertical input gate		V_{IGV}	-8	0	-	
	Horizontal input gate		V_{IGH}	-8	0	-	
Vertical shift register clock voltage		High	V_{P1AVH}, V_{P2AVH} V_{P1BVH}, V_{P2BVH}	0	3	6	V
		Low	V_{P1AVL}, V_{P2AVL} V_{P1BVL}, V_{P2BVL}	-9	-8	-7	
Horizontal shift register clock voltage		High	V_{P1AHH}, V_{P2AHH} V_{P1BHH}, V_{P2BHH}	0	3	6	V
		Low	V_{P1AHL}, V_{P2AHL} V_{P1BHL}, V_{P2BHL}	-9	-8	-7	
Summing gate voltage		High	V_{SGH}	0	3	6	V
		Low	V_{SGL}	-9	-8	-7	
Reset gate voltage		High	V_{RGH}	0	3	6	V
		Low	V_{RGL}	-9	-8	-7	
Transfer gate voltage		High	V_{TGH}	0	3	6	V
		Low	V_{TGL}	-9	-8	-7	

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Remark	Min.	Typ.	Max.	Unit
Signal output frequency	fc		-	2	4	MHz
Reset clock frequency	frg		-	2	4	MHz
Vertical shift register capacitance	C_{P1AV}, C_{P2AV} C_{P1BV}, C_{P2BV}		-	15000	-	pF
Horizontal shift register capacitance	C_{P1AH}, C_{P2AH} C_{P1BH}, C_{P2BH}		-	500	-	pF
Summing gate capacitance	C_{SG}		-	15	-	pF
Reset gate capacitance	C_{RG}		-	10	-	pF
Transfer gate capacitance	C_{TG}		-	500	-	pF
Transfer efficiency	CTE	*2	0.99995	0.99999	-	
DC output level	Vout	*3	5	8	11	V
Output impedance	Zo	*3	-	500	-	Ω
Power dissipation	P	*3, *4	-	60	-	mW

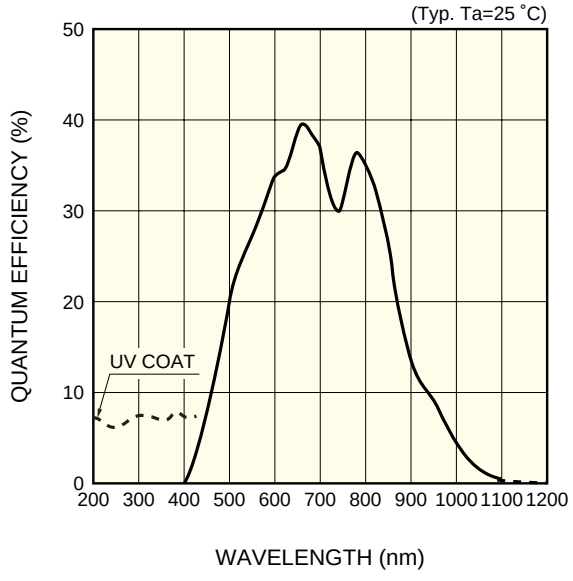
*2: Measured at half of the full well capacity. CTE is defined per pixel.
*3: V_{OD}=15 V
*4: Power dissipation of the on-chip amplifier

■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter			Symbol	Remark	Min.	Typ.	Max.	Unit
Saturation output voltage			Vsat		-	Fw × Sv	-	V
Full well capacity	Vertical		Fw		600	1200	-	ke^-
	Horizontal				600	1200	-	
	Summing				600	1200	-	
CCD node sensitivity			Sv	*5	0.45	0.6	-	$\mu V/e^-$
Dark current (MPP mode)			DS	*6	-	2	8	ke^-/pixel/s
Readout noise			Nr	*7	-	60	120	e^-rms
Dynamic range			DR	*8	5000	20000	-	
Photo response non-uniformity			PRNU	*9	-	±3	±10	%
Spectral response range			λ		-	400 to 1100	-	nm
Blemish	Point defects *10	White spots	-		-	-	0	-
		Black spots			-	-	0	
	Cluster defects			*11	-	-	0	
	Column defects			*12	-	-	0	

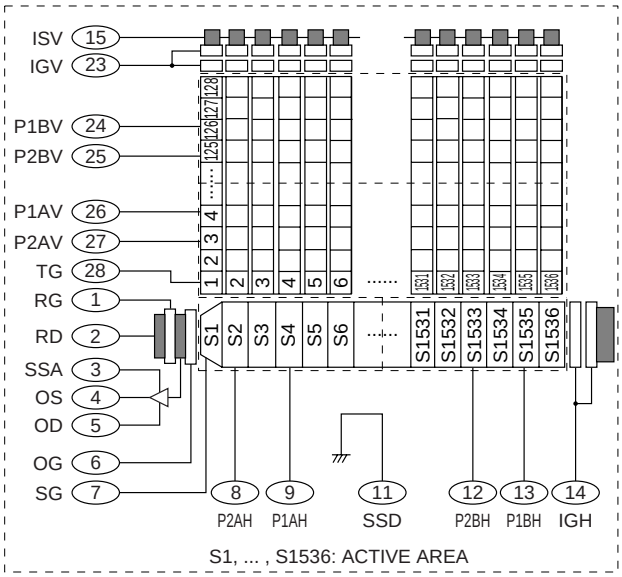
*5: V_{OD}=15 V.
*6: Dark current doubles for every 5 to 7 °C.
*7: -40 °C, operating frequency is 2 MHz.
*8: Dynamic range = Full well capacity / Readout noise
*9: Measured at the half of the full well capacity
PRNU (%) = Noise / Signal × 100
Noise: Fixed pattern noise (peak to peak)
*10: White spots > 20 times of Max. dark signal (8 ke^-/pixel/s).
Black spots
Pixels whose sensitivity is lower than one-half of the average pixel output (Measured with uniform light producing one-half of the saturation charge)
*11: 2 to 9 contiguous defective pixels.
*12: 10 or more contiguous defective pixels.

■ Spectral response (without window)



KMPDB0244EB

■ Device structure



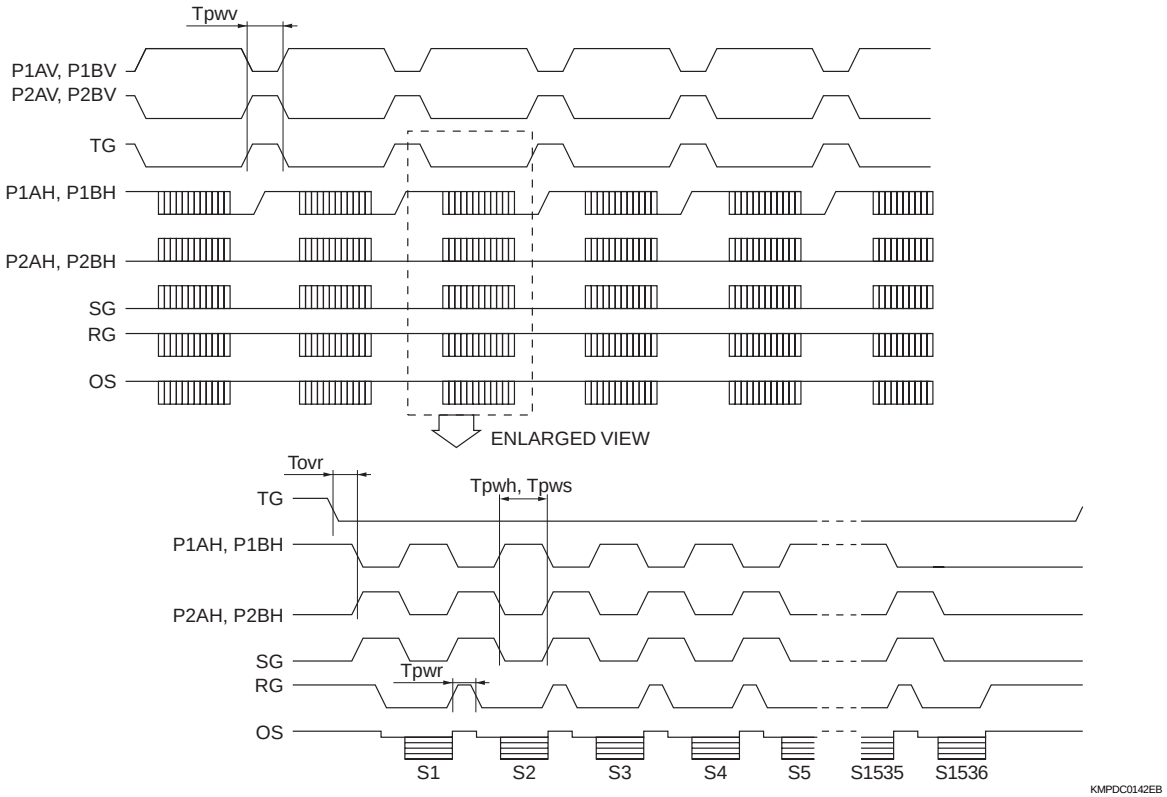
KMPDC0234EA

■ Pixel format

← Left Horizontal Direction → Right						
Blank	Optical black	Isolation	Effective	Isolation	Optical black	Blank
0	0	0	1536	0	0	0

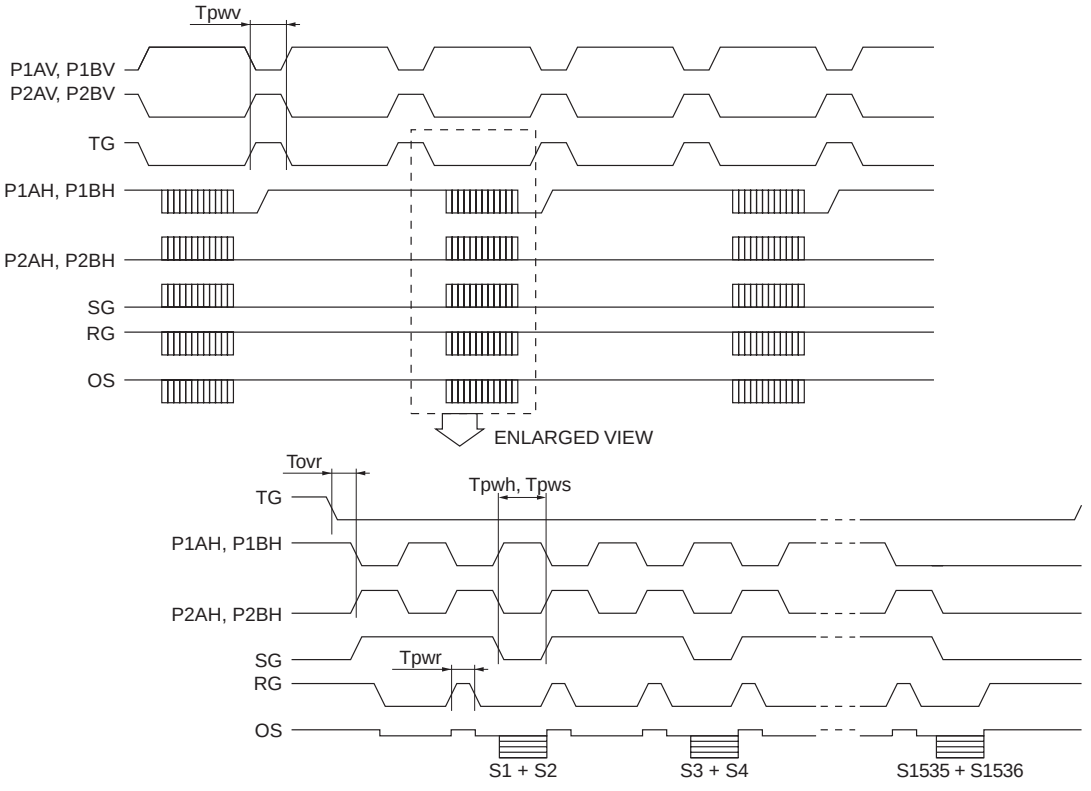
Top ← Vertical direction → Bottom		
Isolation	Effective	Isolation
0	128	0

■ Timing chart (TDI operation)



KMPDC0142EB

■ Timing chart (TDI operation, 2 × 2 pixel binning)

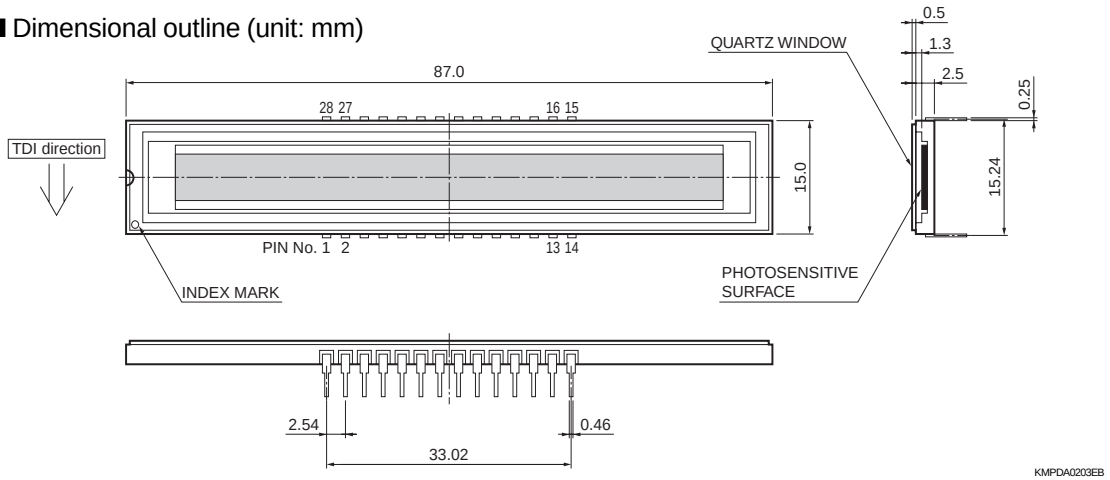


KMPDC0111EC

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1AV, P1BV, P2AV, P2BV, TG	Pulse width	tpwv	*13, *14	30	60	-	µs
	Rise and fall time	tprv, tpfv		200	-	-	ns
P1AH, P1BH, P2AH, P2BH	Pulse width	tpwh	*14	125	250	-	ns
	Rise and fall time	tprh, tpfh		10	-	-	ns
	Duty ratio			-	50	-	%
SG	Pulse width	tpws		125	250	-	ns
	Rise and fall time	tprs, tpfs		10	-	-	ns
	Duty ratio			-	50	-	%
RG	Pulse width	tpwr		10	50	-	ns
	Rise and fall time	tprr, tpfr		5	-	-	ns
TG-P1AH, P1BH	Overlap time	tovr		10	20	-	µs

*13: TG terminal can be short-circuited to P2AV terminal.
*14: The clock pulses should be overlapped at 50 % of clock pulse amplitude.

■ Dimensional outline (unit: mm)



■ Pin connections

Pin No.	Symbol	Description	Remark
1	RG	Reset gate	
2	RD	Reset drain	
3	SSA	Analog ground	
4	OS	Output transistor source	
5	OD	Output transistor drain	
6	OG	Output gate	
7	SG	Summing gate	
8	P2AH	CCD horizontal register clock A-2	
9	P1AH	CCD horizontal register clock A-1	
10	NC		
11	SSD	Digital ground	
12	P2BH	CCD horizontal register clock B-2	Same timing as P2AH
13	P1BH	CCD horizontal register clock B-1	Same timing as P1AH
14	IGH	Test point (Horizontal input gate)	
15	ISV	Test point (Vertical input source)	Shorted to RD
16 to 22	NC		
23	IGV	Test point (Vertical input gate)	
24	P1BV	CCD vertical register clock B-1	Same timing as P1AV
25	P2BV	CCD vertical register clock B-2	Same timing as P2AV
26	P1AV	CCD vertical register clock A-1	
27	P2AV	CCD vertical register clock A-2	
28	TG	Transfer gate	

■ Precautions for use (Electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

■ Element cooling/heating temperature incline rate

When cooling the CCD by an externally attached cooler, set the cooler operation so that the temperature gradient (rate of temperature change) for cooling or allowing the CCD to warm back is less than 5 K/minute.

Information described in this material is current as of March, 2011. Product specifications are subject to change without prior notice due to improvements or other reasons. Before assembly into final products, please contact us for the delivery specification sheet to check the latest information.
Type numbers of products listed in the delivery specification sheets or supplied as samples may have a suffix "(X)" which means preliminary specifications or a suffix "(Z)" which means developmental specifications.
The product warranty is valid for one year after delivery and is limited to product repair or replacement for defects discovered and reported to us within that one year period. However, even if within the warranty period we accept absolutely no liability for any loss caused by natural disasters or improper product use.
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