
eKTF5832

**8-Bit
Microcontroller**

IC Product Specification

DOC. VERSION 0.4

ELAN MICROELECTRONICS CORP.

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Specification Revision History

Version	Revision Description	Date
0.1	Initial Release Version	2015/01/13
0.2	Updated the format and corrected the error content	2015/03/24
0.3	Modified the package information	2016/03/24
0.4	Added some package type	2019/09/09

1 General Description

The eKTF5832 is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. It has a built-in 12K×16-bit programmable ROM and is equipped with touch sensors. The capacitive touchkey sensor uses plastic or glass substrate as cover.

The system controller converts fingertip position data into button presses, depending on finger location and human interface context. The eKTF5832 OCD can be used to develop user program for this microcontroller and several other ELAN Flash type ICs.

2 Features

- CPU configuration
 - Supports 12K×16 bits program ROM
 - (48+1024) bytes general purpose register.
 - 16-level stacks for subroutine nesting
 - Typical 1 μ A, during sleep mode
 - 3 programmable Level Volt Reset
LVR: 3.5V, 2.8V, 2.4V
 - 1 sets of 4 programmable Level Voltage Detector
LVD: 4V, 3.2V, 2.8V, 2.5V
 - Four CPU operation modes (Normal, Green, Idle, Sleep)
- I/O port configuration
 - Independent I/O_VDD for VOH and VIH/VIL
 - 4 bidirectional I/O ports: P5 ~ P8
 - 4 programmable pin change wake-up ports: P5~P8
 - 4 programmable pull-down I/O ports: P5~P8
 - 4 programmable pull-high I/O ports: P5~P8
 - 4 programmable open-drain I/O ports: P5~P8
 - 4 programmable high-sink/drive I/O ports: P5~P8
- Operating voltage range:
 - 2.8V~5.5V with IC LDO at -40°C~85°C (industrial)
- Operating frequency range (base on two clocks):

Main oscillator:

- IRC mode:
DC ~ 16 MHz at 3V; DC ~ 8 MHz at 2V

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~+85°C)	Voltage (2.8V~5.5V)	Process	Total
1 MHz	±2%	±1%	±1%	±4%
4 MHz	±2%	±1%	±1%	±4%
6 MHz	±2%	±1%	±1%	±4%
8 MHz	±2%	±1%	±1%	±4%
12 MHz	±2%	±1%	±1%	±4%
16 MHz	±2%	±1%	±1%	±4%

Sub oscillator:

- IRC mode: 16K/32K

Peripheral configuration

- 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
Three Pulse Width Modulation (PWMA, PWMB, PWMC) with 16-bit resolution shared with Timers A,B and C
- Provide the 24 sensor pins.
- 1-channel Digital-to-Analog converter for 256 steps
- Serial transmitter/receiver interface (SPI): 3-wire synchronous communication
- I²C function with 7/10 bits address and 8 bits data transmit/receive mode
- Power down (Sleep) mode
- Idle with scan mode
- 15 available interrupts: (2 external, 13 internal)
 - External interrupt: INT0, INT1
 - TCC overflow interrupt
 - Input-port status changed interrupt (wake up from sleep mode)
 - PWMA, PWMB, PWMC period match completion
 - I²C transfer/receive/stop interrupt
 - SPI interrupt
 - LVD interrupt
 - System hold interrupt
- Single instruction cycle commands
- Package Type:
 - 32 QFN(5x5x0.8mm) : eKTF5832QN32
 - 24 QFN(4x4x0.8mm) : eKTF5832QN24
 - 28 SOP(300mil) : eKTF5832SO28
 - 28 SSOP(209mil) : eKTF5832SS28
 - 24 SOP(300mil) : eKTF5832SO24

Note: These are all Green products which do not contain hazardous substances.

3 Pin Assignment

3.1 Package: QFN 32

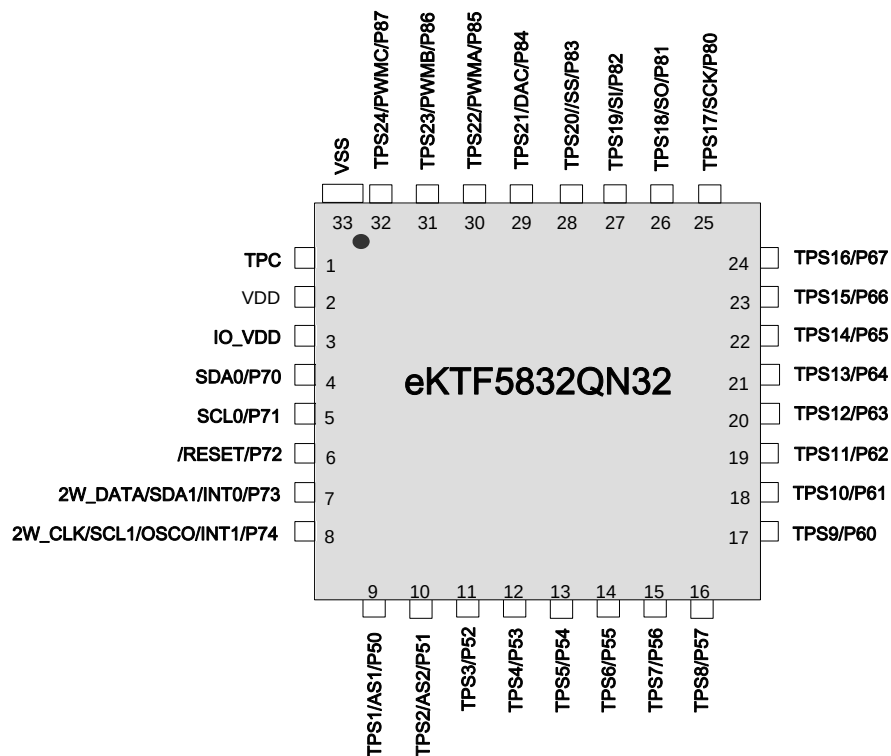


Figure 3-1 QFN-32 Pin Assignment

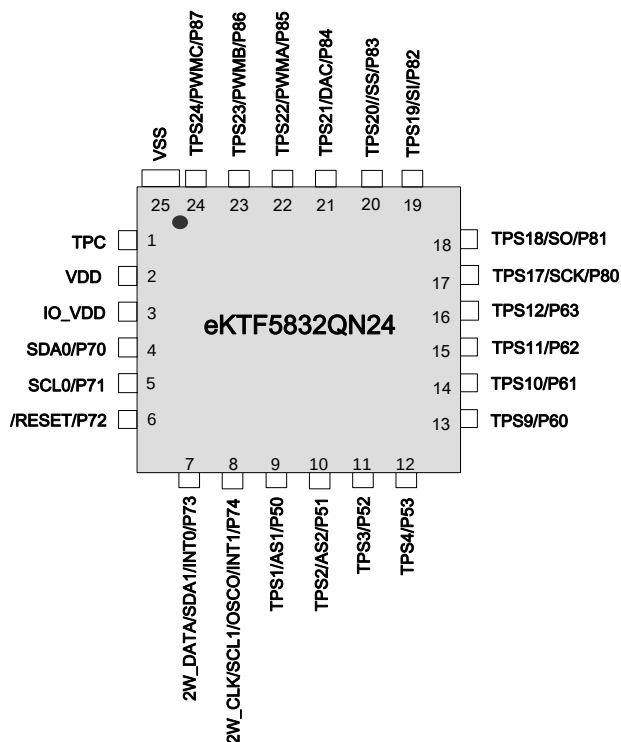


Figure 3-2 QFN-24 Pin Assignment

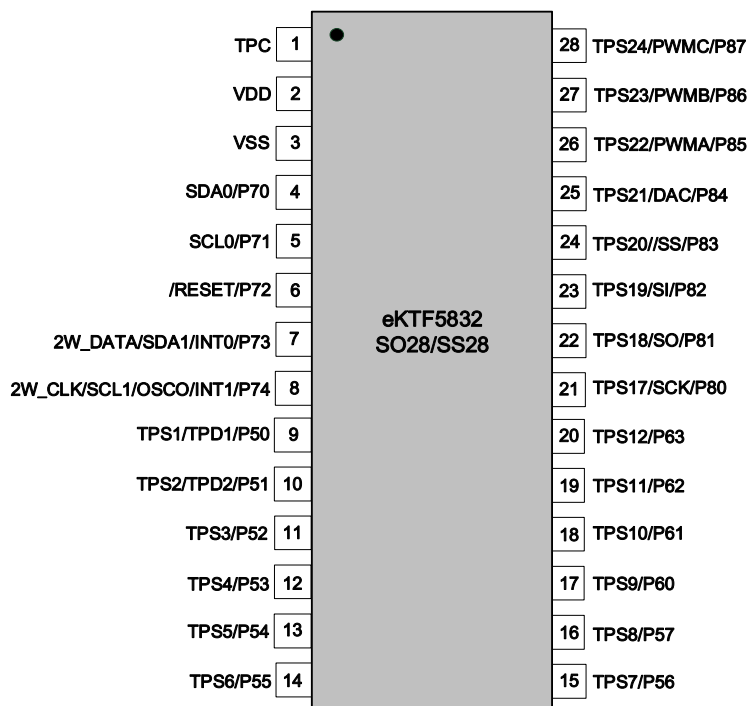


Figure 3-3 SOP-28/SSOP-28 Pin Assignment

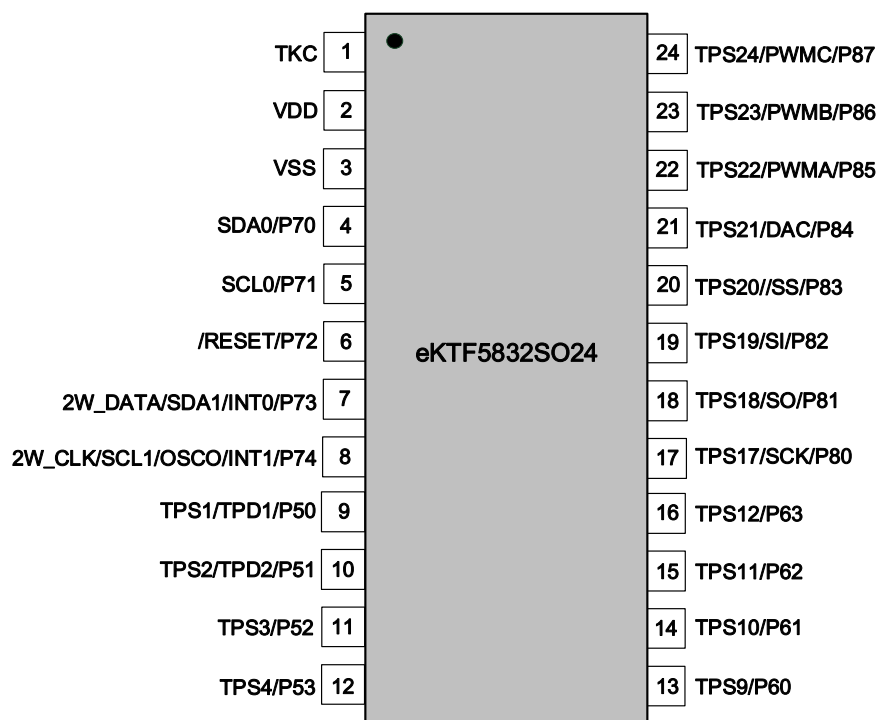


Figure 3-4 SOP-24 Pin Assignment

4 Pin Description

4.1 eKTF5832 Kernel Pin

Name	Function	Input Type	Output Type	Description
VDD	VDD	Power	–	Kernel Power
AVDD	TK VDD	Power	–	TK Power
IO_VDD	I/O VDD	Power	–	I/O Power (IOH, VIH, VIL)
VSS	VSS	Power	–	Ground
TPC	TPC	AN	–	Touch key external Capacitor pin
P50/TPS1/AS1	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS1	AN	–	TPS1 is a Touch Key Sensor pin
	AS1	AN	–	Active Shielding pin
P51/TPS2/AS2	P51	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS2	AN	–	TPS2 is a Touch Key Sensor pin
	AS2	AN	–	Active Shielding pin
P52/TPS3	P52	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS3	AN	–	TPS3 is a Touch Key Sensor pin
P53/TPS4	P53	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS4	AN	–	TPS4 is a Touch Key Sensor pin
P54/TPS5	P54	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS5	AN	–	TPS5 is a Touch Key Sensor pin
P55/TPS6	P55	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS6	AN	–	TPS6 is a Touch Key Sensor pin
P56/TPS7	P56	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS7	AN	–	TPS7 is a Touch Key Sensor pin

Name	Function	Input Type	Output Type	Description
P57/TPS8	P57	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS8	AN	–	TPS8 is a Touch Key Sensor pin
P60/TPS9	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS9	AN	–	TPS9 is a Touch Key Sensor pin
P61/TPS10	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS10	AN	–	TPS10 is a Touch Key Sensor pin
P62/TPS11	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS11	AN	–	TPS11 is a Touch Key Sensor pin
P63/TPS12	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS12	AN	–	TPS12 is a Touch Key Sensor pin
P64/TPS13	P64	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS13	AN	–	TPS13 is a Touch Key Sensor pin
P65/TPS14	P65	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS14	AN	–	TPS14 is a Touch Key Sensor pin
P66/TPS15	P66	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS15	AN	–	TPS15 is a Touch Key Sensor pin
P67/TPS16	P67	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS16	AN	–	TPS16 is a Touch Key Sensor pin
P70/SDA0	P70	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	SDA0	ST	CMOS	I ² C serial data line. It is open-drain

Name	Function	Input Type	Output Type	Description
P71/SCL0	P71	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	SCL0	ST	CMOS	I ² C serial clock line. It is open-drain.
P72//RESET	P72	–	–	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
	/RESET	ST	–	Internal pull-high reset pin
P73/SDA1/INT0 /2W_DATA	P73	–	–	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
	SDA1	ST	CMOS	I ² C serial data line. It is open-drain
	INT0	ST	–	External interrupt pin
	2W_DATA	ST	CMOS	OCD data line
P74/SCL1OSCO/INT1 /2W_CLK	P74	–	–	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain
	SCL1	ST	CMOS	I ² C serial clock line. It is open-drain.
	OSCO	–	CMOS	Clock output of internal RC oscillator
	INT1	ST	–	External interrupt pin
	2W_CLK	ST	CMOS	OCD clock line
P80/TPS17/SCK	P80	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS17	AN	–	TPS17 is a Touch Key Sensor pin
	SCK	ST	CMOS	SPI serial clock input/output
P81/TPS18/SO	P81	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS18	AN	–	TPS18 is a Touch Key Sensor pin
	SO	–	CMOS	SPI serial data output
P82/TPS19/SI	P82	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS19	AN	–	TPS19 is a Touch Key Sensor pin
	SI	ST	–	SPI serial data input
P83/TPS20//SS	P83	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS20	AN	–	TPS20 is a Touch Key Sensor pin
	/SS	ST	–	SPI slave mode enable

Name	Function	Input Type	Output Type	Description
P84/TPS21/DAC	P84	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS21	AN	–	TPS21 is a Touch Key Sensor pin
	DAC	AN	–	Digital to Analog Converter PIN
P85/TPS22/PWMA	P85	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS22	AN	–	TPS22 is a Touch Key Sensor pin
	PWMA	–	CMOS	PWMA output
P86/TPS23/PWMB	P86	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS23	AN	–	TPS23 is a Touch Key Sensor pin
	PWMB	–	CMOS	PWMB output
P87/TPS24/PWMC	P87	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	TPS24	AN	–	TPS24 is a Touch Key Sensor pin
	PWMC	–	CMOS	PWMC output

Note: OCD: On Chip Debug system

5 Functional Block Diagram

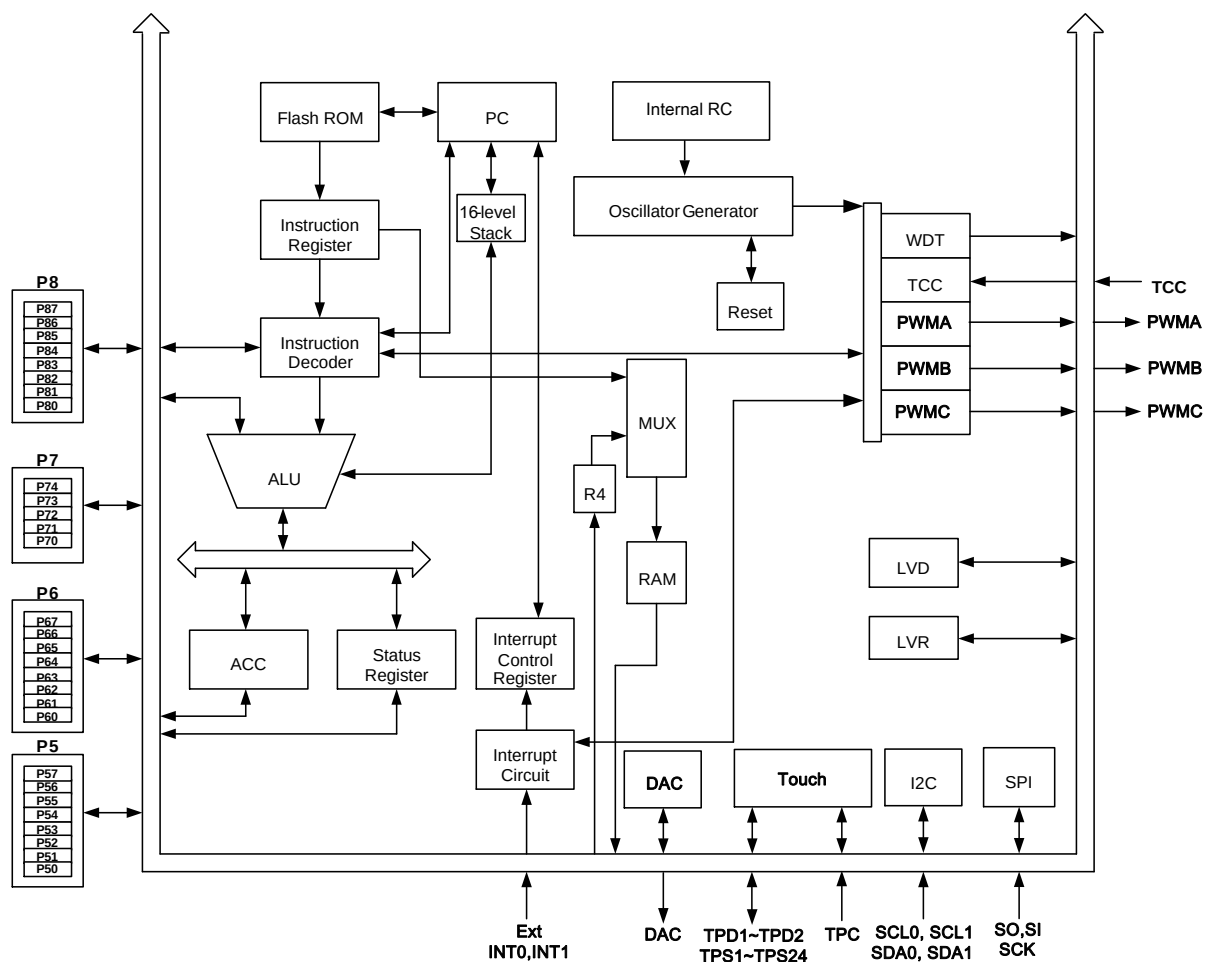


Figure 5-1 eKTF5832 Functional Block Diagram

6 Functional Description

6.1 Operational Registers

6.1.1 R0: IAR (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1: BSR (Bank Selection Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	SBS1	SBS0	-	GBS2	GBS1	GBS0
-	-	R/W	R/W	0	R/W	R/W	R/W

Bits 7~6: Not used. Set to “0” all the time.

Bits 5~4 (SBS1~SBS0): Special register bank select bit. It is used to select Banks 0/1/2 of Special Registers **R5~R4F**.

SBS1	SBS0	Special Register Bank
0	0	0
0	1	1
1	0	2
1	1	X

Bit 3: Not used. Set to “0” all the time.

Bits 2~0 (GBS2~GBS0): General register bank select bit. It is used to select Banks 0~7 of General Registers **R80~RFF**.

GBS2	GBS1	GBS0	RAM Bank
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

6.1.3 R2: PCL (Program Counter Low)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PC7~PC0): The low byte of program counter.

- Depending on the device type, R2 and hardware stack are 16-bits wide. The structure is depicted in Figure 6-1 *Program Counter Organization*.
- Generating 12K×16 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 4096 words long.
- R2 is set as all "0"s when under RESET condition.
- "JMP" instruction allows direct loading of the lower 12 program counter bits. Thus, "JMP" allows PC to go to any location within a page.
- "CALL" instruction loads the lower 12 bits of the PC, and the present PC value will add 1 and is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "LJMP" instruction allows direct loading of the lower 14 program counter bits. Therefore, "LJMP" allows PC to jump to any location within 12K (2^{14}).
- "LCALL" instruction loads the lower 14 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within 12K (2^{14}).
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and above bits of the PC won't be changed.
- Any instruction except "ADD R2,A" that is written to R2 (e.g. "MOV R2, A", "BC R2, 6", "INC R2", ...) will cause the ninth bit and the above bits (PC8~PC12) of the PC not change.
- All instructions are single instruction cycle ($F_{sys}/2$) except "LCALL", "CALL", "LJMP" and "JMP" instructions. The "LCALL" and "LJMP" instructions need two instruction cycles.

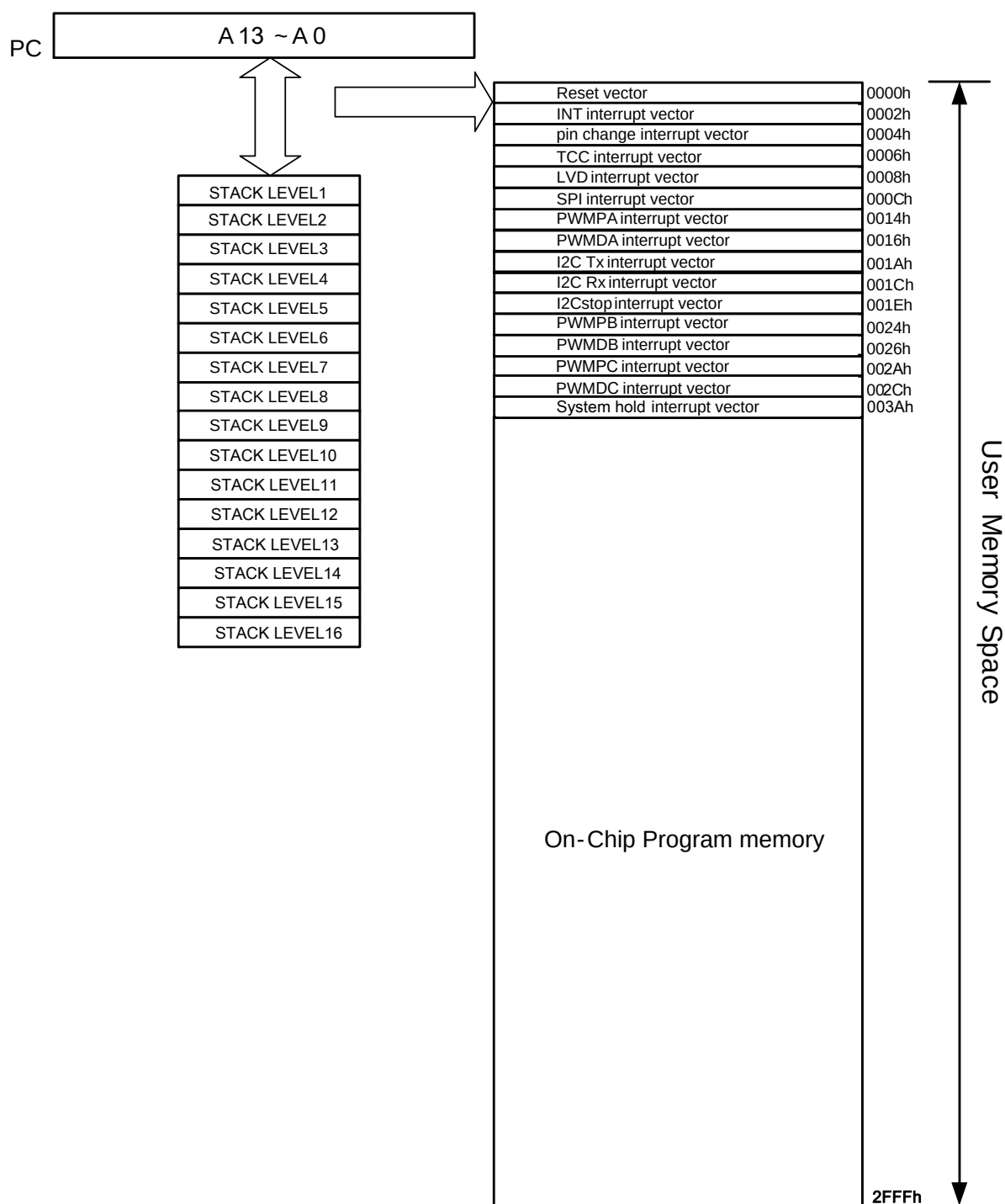


Figure 6-1 eKTF5832 Program Counter Organization

■ Data Memory Configuration

Address	BANK 0	BANK 1
0X00	IAR (Indirect Addressing Reg.)	
0X01	BSR (Bank Selection Control Reg.)	
0X02	PCL (Program Counter Low)	
0X03	SR (Status Reg.)	
0X04	RSR (RAM Selection Reg.)	
0X05	Port 5	IOCR8
0X06	Port 6	Unused
0X07	Port 7	Unused
0X08	Port 8	P5PHCR
0X09	Unused	P6PHCR
0X0A	Unused	P78PHCR
0X0B	IOCR5	P5PLCR
0X0C	IOCR6	P6PLCR
0X0D	IOCR7	P78PLCR
0X0E	OMCR (Operating Mode Control Register)	P5HDSCR
0X0F	EIESCR (External Interrupt Edge Selection Control Register)	P6HDSCR
0X10	WUCR1	P789AHDSCR
0X11	WUCR2	P5ODCR
0X12	WUCR3	P6ODCR
0X13	Unused	P78ODCR
0X14	SFR1 (Status Flag Register 1)	Unused
0X15	Unused	Unused
0X16	SFR3 (Status Flag Register 3)	PWMSCR
0X17	SFR4 (Status Flag Register 4)	PWMACR
0X18	Unused	PRDAL
0X19	SFR6 (Status Flag Register 6)	PRDAH
0X1A	Unused	DTAL
0X1B	IMR1 (Interrupt Mask Register 1)	DTAH
0X1C	Unused	TMRAL
0X1D	IMR3 (Interrupt Mask Register 3)	TMRAH
0X1E	IMR4 (Interrupt Mask Register 4)	PWMBCR
0X1F	Unused	PRDBL
0X20	IMR6 (Interrupt Mask Register 6)	PRDBH

0X21	WDTCR	DTBL
0X22	TCCCR	DTBH
0X23	TCCD	TMRBL
0X24	Unused	TMRBH
0X25	Unused	PWMCCR
0X26	Unused	PRDCL
0X27	Unused	PRDCH
0X28	Unused	DTCL
0X29	Unused	DTCH
0X2A	Unused	TMRCL
0x2B	Unused	TMRCH
0X2C	Unused	Unused
0X2D	Unused	Unused
0X2E	Unused	Unused
0X2F	Unused	Unused
0X30	I2CCR1	Unused
0X31	I2CCR2	Unused
0X32	I2CSA	Unused
0X33	I2CDB	Unused
0X34	I2CDAL	Unused
0X35	I2CDAH	Unused
0X36	SPICR	Unused
0X37	SPIS	Unused
0X38	SPIR	Unused
0X39	SPIW	Unused
0X3A	Unused	Unused
0x3B	Unused	Unused
0X3C	Unused	Unused
0X3D	Unused	Unused
0X3E	Unused	Unused
0X3F	Unused	Unused
0X40	Unused	Unused
0X41	Unused	Unused
0X42	Unused	Unused
0X43	Unused	Unused
0X44	Unused	Unused
0X45	Unused	TBPTL
0X46	Unused	TBPTH



0X47	Unused	STKMON						
0X48	Unused	PCH						
0X49	Unused	LVDCR						
0X4A	Unused	Unused						
0x4B	Unused	Unused						
0X4C	Unused	Unused						
0X4D	Unused	Unused						
0X4E	Unused	Unused						
0X4F	Unused	Unused						
0X50	GENERAL PURPOSE REGISTER							
0X51								
.								
.								
0X7F								
0X80	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
0X81								
.								
.								
.								
0XFE								
0XFF								

6.1.4 R3: SR (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT	N	OV	T	P	Z	DC	C
F	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (INT): Interrupt Enable flag

0: Interrupt masked by DISI or hardware interrupt

1: Interrupt enabled by ENI/RETI instructions

Bit 6 (N): Negative flag.

The negative flag stores the state of the most significant bit of the output result

0: The result of the operation is not negative.

1: The result of the operation is negative.

Bit 5 (OV): Overflow flag.

OV is set when a two's complement overflows occurs as a result of an operation

0: No overflow occurred.

1: Overflow occurred.

Bit 4 (T): Time-out bit.

Set to 1 with the "SLEP" and "WDTC" commands, or during power up and reset to 0 by WDT time-out.

Bit 3 (P): Power down bit.

Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 2 (Z): Zero flag.

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry or Borrow flag

C : C is set when a carry occurs and cleared when a borrow occurs during an arithmetic operation. The Carry Flag bit is set or cleared, depending on the operation that is performed

For ADD, ADC, INC, INCA instructions

0: No carry occurs.

1: Carry occurs.

For SUB, SUBB, DEC, DECA, NEG instructions

0: Borrow occurs.

1: No borrow occurs.

For RLC, RRC, RLCA, RRCA instructions

The Carry flag is used as a link between the least significant bit (LSB) and most significant bit

(MSB).

6.1.5 R4: RSR (RAM Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (RSR7~RSR0): These bits are used to select registers (Address 00 ~ FF) in indirect addressing mode. For more details, refer to the table on Data Memory Configuration in Section 6.1.3, R2: PCL (Program Counter Low).

6.1.6 Bank 0 R5 ~ R8: (Port 5 ~ Port 8)

R5, R6, R7, and R8 are I/O data registers.

6.1.7 Bank 0 R9 ~ RA: (Reserved)

6.1.8 Bank 0 RB~RD: (IOCR5 ~ IOCR7)

These registers are used to control the I/O port direction. They are both readable and writable.

0: Set the relative I/O pin as output

1: Set the relative I/O pin into high impedance

6.1.9 Bank 0 RE: OMCR (Operating Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPUS	IDLE	-	-	-	RCM2	RCM1	RCM0
R/W	R/W	-	-	-	R/W	R/W	R/W

Bit 7 (CPUS): CPU Oscillator Source Select.

0 : Fs: sub-oscillator

1 : Fm: main-oscillator (default)

When CPUS=0, the CPU oscillator select sub-oscillator and the main oscillator is stopped.

Bit 6 (IDLE): Idle Mode Enable Bit. This bit will decide SLEP instruction which mode to go.

0: "IDLE=0"+SLEP instruction → sleep mode

1: "IDLE=1"+SLEP instruction → idle mode (default)

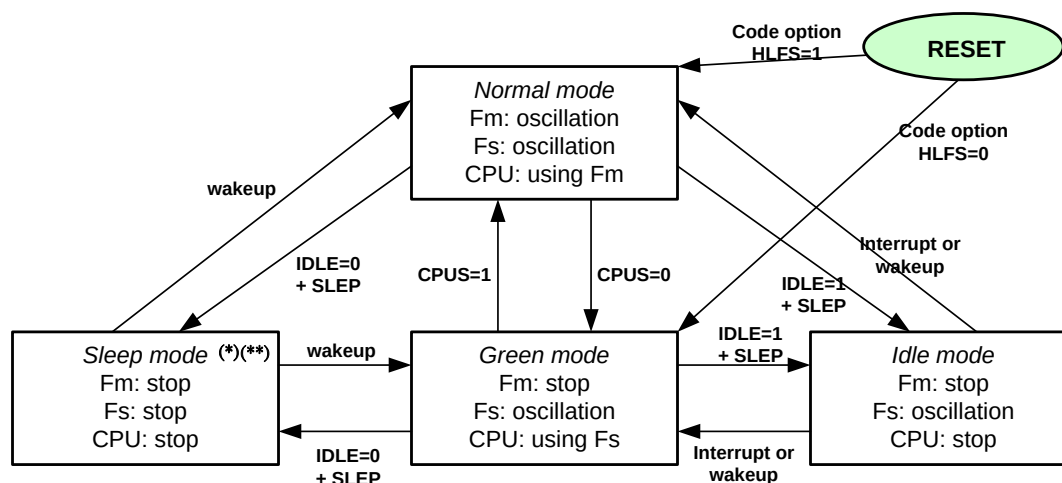


Figure 6-2 CPU Operation Mode

Note

(*)

If Watchdog function is enabled before into sleep mode, some circuits like timer (Its clock source is Fs) must stop counting.

If Watchdog function is enabled before into sleep mode, some circuits like timer (Its clock source is external pin) can still count and its interrupt flag can be active at matching condition as corresponding interrupt is enabled. But CPU cannot be wake up by this event.

(**)

Switching Operation Mode at sleep → Normal, Green → Normal:

If the clock source of timer is Fm, timer/counter must stop counting at sleep or green mode. Then, timer can continue to count until clock source is stable at normal mode. That clock source is stable means CPU starts to work at normal mode.

Switching Operation Mode at Sleep → green:

If the clock source of the timer is F_s , the timer must stop counting at sleep mode. Then, the timer can continue to count until the clock source is stable at green mode. That clock source is stable means that CPU starts to work at green mode.

Switching Operation Mode at Sleep → Normal:

If the clock source of the Timer is F_s , the timer must stop counting at sleep mode. Then, the timer can continue to count until the clock source is stable at normal mode. That clock source is stable means that CPU starts to work at normal mode.

CPU Mode Switch	IRC Frequency	Waiting Time before CPU starts to work
Sleep → Normal Idle → Normal	12M, 16M	WSTO + 32 clocks (main frequency)
Green → Normal	1M, 4M, 6M, 8M	WSTO + 8/32 clocks (main frequency)
Sleep → Green Idle → Green	32kHz	WSTO + 8 clocks (sub frequency)

WSTO: Waiting time of Start-to-Oscillation

Bits 5~3: Not used, set to "0" all the time

Bits 2~0 (RCM2~RCM0): Internal RC mode selection bits

*Default value corresponding code option Word1 RCM2~RCM0

*RCM2	*RCM1	*RCM0	Frequency (MHz)
0	0	0	4
0	0	1	1
0	1	0	6
0	1	1	8
1	0	0	12
1	0	1	16

6.1.10 Bank 0 RF: EIESCR (External Interrupt Edge Select Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	EIES1	EIES0	-	-
-	-	-	-	R/W	R/W	-	-

Bits 7~4: Not used, set to "0" all the time

Bits 3~2 (EIES1~0): external interrupt edge select bit

0: Falling edge interrupt

1: Rising edge interrupt

Bits 1~0: Not used, set to "0" all the time

6.1.11 Bank 0 R10: WUCR1 (Wake-up Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		LVDWK		INTWK1	INTWK0		
		R/W		R/W	R/W		

Bits 7~6, 4: Not used, set to "0" all the time

Bit 5 (LVDWK): Low Voltage Detect Wake-up Enable Bit

0: Disable Low Voltage Detect wake-up.

1: Enable Low Voltage Detect wake-up.

Bits 3~2 (INTWK1~0): External Interrupt (INT pin) Wake-up Function Enable Bit

0: Disable external interrupt wake-up

1: Enable external interrupt wake-up

When the External Interrupt status changed is used to enter interrupt vector or to wake-up IC from Sleep/Idle, the INTWK bits must be set to "enable".

Bits 1~0: Not used, set to "0" all the time

6.1.12 Bank 0 R11: WUCR2 (Wake-up Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	SPIWK	I2CWK	-	-
-	-	-	-	R/W	R/W	-	-

Bits 7~4: Not used. Set to "0" all the time.

Bit 3 (SPIWK): SPI wake-up enable bit. Applicable when SPI works in Slave mode.

0: Disable SPI wake-up

1: Enable SPI wake-up

Bit 2 (I2CWK): I²C wake-up enable bit. Applicable when I²C works in Slave mode.

0: Disable I²C wake-up

1: Enable I²C wake-up

NOTE

When I²C is in Slave mode, it cannot communicate with the MCU in Green mode. At the same time the SCL is on hold and kept at low level when the MCU is in Green mode. SCL is released when the MCU switches to Normal mode.

Bits 1~0: Not used. Set to "0" all the time.

6.1.13 Bank 0 R12: WUCR3 (Wake-up Control Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ICWKP8	ICWKP7	ICWKP6	ICWKP5	-	-	-	-
R/W	R/W	R/W	R/W	-	-	-	-

Bits 7~4 (ICWKP8~ICWKP5): Pin change Wake-up enable for Ports 8/7/6/5.

0: Disable wake-up function

1: Enable wake-up function

Bits 3~0: Not used. Set to "0" all the time.

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
Pin Change INT	ICWKP _x = 0, PxICIE = 0	Wake-up is invalid				Interrupt is invalid			
	ICWKP _x = 0, PxICIE = 1	Wake-up is invalid				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	ICWKP _x = 1, PxICIE = 0	Wake-up + Next Instruction				Interrupt is invalid			
	ICWKP _x = 1, PxICIE = 1	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Wake-up + Next Instruction	Wake-up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

NOTE

When the MCU wakes up from Sleep or Idle mode, the ICSF must be equal to 1. If ICSF is equal to 0, it means the pin status does not change or the pin change ICIE is disabled. Hence the MCU cannot wake-up.

6.1.14 Bank 0 R13: (Reserved)

6.1.15 Bank 0 R14: SFR1 (Status Flag Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		LVDSF		EXSF1	EXSF0		TCSF
		F		F	F		F

Each corresponding status flag is set to "1" when interrupt condition is triggered.

Bits 7~6, 4, 1: Not used, set to "0" all the time

Bit 5 (LVDSF): Low Voltage Detector status flag

LV DEN	LVDS1, LVDS0	LVD Voltage Interrupt Level	LVDSF
1	11	4.0V	1*
1	10	3.2V	1*
1	01	2.8V	1*
1	00	2.5V	1*
0	XX	NA	0

* If V_{dd} has crossover at the LVD voltage interrupt level as V_{dd} varies, LVDSF = 1.

Bits 3~2 (EXSF1~0): External interrupt status flag.

Bit 0 (TCSF): TCC overflow status flag. Set when TCC overflows, reset by software.

NOTE

If a function is enabled, the corresponding status flag would be active regardless of whether the interrupt mask is enabled or not.

6.1.16 Bank 0 R15: (Reserved)

6.1.17 Bank 0 R16: SFR3 (Status Flag Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		PWMCPSF	PWMCDSF	PWMBPSF	PWMBDSF	PWMA PSF	PWMADSF
		F	F	F	F	F	F

Bits 7~6: Not used, set to "0" all the time

Bit 5 (PWMCPSF): Status flag of period-matching for PWMC (Pulse Width Modulation). Set when a selected period is reached, reset by software.

Bit 4 (PWMCDSF): Status flag of duty-matching for PWMC (Pulse Width Modulation). Set when a selected duty is reached, reset by software.

Bit 3 (PWMBPSF): Status flag of period-matching for PWMB (Pulse Width Modulation). Set when a selected period is reached, reset by software.

Bit 2 (PWMBDSF): Status flag of duty-matching for PWMB (Pulse Width Modulation). Set when a selected duty is reached, reset by software.

Bit 1 (PWMAPSF): Status flag of period-matching for PWMA (Pulse Width Modulation). Set when a selected period is reached, reset by software.

Bit 0 (PWMA DSF): Status flag of duty-matching for PWMA (Pulse Width Modulation). Set when a selected duty is reached, reset by software.

NOTE

If a function is enabled, the corresponding status flag would be active whether the interrupt mask is enabled or not.

6.1.18 Bank 0 R17: SFR4 (Status Flag Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P8ICSF	P7ICSF	P6ICSF	P5ICSF	SPISF	I2CSTPSF	I2CRSF	I2CTSF
F	F	F	F	F	F	F	F

Bits 7~4 (P8ICSF~P5ICSF): Ports 5~8 input status change status flag. Set when Ports 5~8 input changes. Reset by software.

Bit 3 (SPISF): SPI mode status flag. Flag is cleared by software.

Bit 2 (I2CSTPSF): I²C stop status flag. Set when I²C stop signal occurs.

Bit 1 (I2CRSF): I²C receive status flag. Set when I²C receives 1byte data and responds ACK signal. Reset by firmware or I²C disable.

Bit 0 (I2CTSF): I²C transmit status flag. Set when I²C transmits a 1 byte data and receives a handshake signal (ACK or NACK). Reset by firmware or I²C disable.

NOTE

If a function is enabled, the corresponding status flag will be active regardless whether the interrupt mask is enabled or not.

6.1.19 Bank 0 R18: (Reserved)

6.1.20 Bank 0 R19: SFR6 (Status Flag Register 6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SHSF							
F							

Bit 7 (SHSF): System hold status flag, Set when system hold occur, reset by software.

Bits 6~0: Not used, set to "0" all the time

6.1.21 Bank 0 R1A: (Reserved)

6.1.22 Bank 0 R1B: IMR1 (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	LVDIE	-	EXIE1	EXIE0	-	TCIE
-	-	R/W	-	R/W	R/W	-	R/W

Bits 7~6, 4, 1: Not used, set to "0" all the time.

Bit 5 (LVDIE): LVDSF interrupt enable bit.

0: Disable LVDSF interrupt

1: Enable LVDSF interrupt

Bit 3 (EXIE1): EXSF1 interrupt enable and /INT1 function enable bit.

0: P74/INT1/SCL1/OSCO is P74/SCL1/OSCO pin, EXSF1 always equals 0.

1: Enable EXSF1 interrupt and P74/INT1/SCL1/OSCO is /INT1 pin

Bit 2 (EXIE0): EXSF0 interrupt enable and /INT0 function enable bit.

0: P73/INT0/SDA1 is P73/SDA1 pin, EXSF0 always equals 0.

1: Enable EXSF0 interrupt and P73/INT0/SDA1 is /INT0 pin

Bit 0 (TCIE): TCSF interrupt enable bit.

0: Disable TCSF interrupt

1: Enable TCSF interrupt

NOTE

If the interrupt mask and instruction "ENI" are enabled, the program counter will jump into the corresponding interrupt vector when the corresponding status flag is set.

6.1.23 Bank 0 R1C: (Reserved)

6.1.24 Bank 0 R1D: IMR3 (Interrupt Mask Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	PWMCPIE	PWMC DIE	PWMBPIE	PWMBDIE	PWMAPIE	PWMADIE
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6: Not used, set to "0" all the time.

Bit 5 (PWMCPIE): PWMCPSP interrupt enable bit.

0: Disable period-matching of PWMC interrupt

1: Enable period-matching of PWMC interrupt

Bit 4 (PWMC DIE): PWMCDSP interrupt enable bit.

0: Disable duty-matching of PWMC interrupt

1: Enable duty-matching of PWMC interrupt

Bit 3 (PWMBPIE): PWMBPSP interrupt enable bit.

0: Disable period-matching of PWMB interrupt

1: Enable period-matching of PWMB interrupt

Bit 2 (PWMBDIE): PWMBDSP interrupt enable bit.

0: Disable duty-matching of PWMB interrupt

1: Enable duty-matching of PWMB interrupt

Bit 1 (PWMAPIE): PWMA PPSF interrupt enable bit.

0: Disable period-matching of PWMA interrupt

1: Enable period-matching of PWMA interrupt

Bit 0 (PWMADIE): PWMADSP interrupt enable bit.

0: Disable duty-matching of PWMA interrupt

1: Enable duty-matching of PWMA interrupt

NOTE

If the interrupt mask and instruction "ENI" are enabled, the program counter will jump into the corresponding interrupt vector when the corresponding status flag is set.

6.1.23 Bank 0 R1E: IMR4 (Interrupt Mask Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P8ICIE	P7ICIE	P6ICIE	P5ICIE	SPIIE	I2CSTPIE	I2CRIE	I2CTIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~4 (P8ICIE~P5ICIE): PxICSF interrupt enable bit

0: Disable PxICSF interrupt

1: Enable PxICSF interrupt

Bit 3 (SPIIE): Interrupt enable bit

0: Disable SPSF interrupt

1: Enable SPSF interrupt

Bit 2 (I2CSTPIE): I²C stop interrupt enable bit.

0: Disable interrupt

1: Enable interrupt

Bit 1 (I2CRIE): I²C Interface Rx interrupt enable bit

0: Disable interrupt

1: Enable interrupt

Bit 0 (I2CTIE): I²C Interface Tx interrupt enable bit

0: Disable interrupt

1: Enable interrupt

NOTE

If the interrupt mask and instruction "ENI" are enabled, the program counter will jump into the corresponding interrupt vector when the corresponding status flag is set.

6.1.24 Bank 0 R1F: (Reserved)

6.1.24 Bank 0 R20: IMR6 (Interrupt Mask Register 6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SHIE							
R/W							

Bit 7 (SHIE): SHSF Interrupt Enable Bit.

0: Disable SHSF interrupt

1: Enable SHSF interrupt

Bits 6~0: Not used, set to "0" all the time.

6.1.25 Bank 0 R21: WDTCR (Watchdog Timer Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	-	-	-	PSWE	WPSR2	WPSR1	WPSR0
R/W	-	-	-	R/W	R/W	R/W	R/W

Bit 7 (WDTE): Watchdog Timer enable bit. WDTE is both readable and writable.

0: Disable WDT

1: Enable WDT

Bits 6~4: Not used. Set to "0" all the time.

Bit 3 (PSWE): Prescaler enable bit for WDT

0: Prescaler disable bit. WDT rate is 1:1.

1: Prescaler enable bit. The WDT rate is set at Bits 2~0.

Bits 2~0 (WPSR2~WPSR0): WDT Prescaler bits

WPSR2	WPSR1	WPSR0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.26 Bank 0 R22: TCCCR (TCC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	TCCS	-	-	PSTE	TPSR2	TPSR1	TPSR0
0	R/W	0	0	R/W	R/W	R/W	R/W

Bit 7: Not used. Set to “0” all the time.

Bit 6 (TCCS): TCC Clock Source select bit

0: Fs (sub clock)

1: Fm (main clock)

Bits 5~4: Not used. Set to “0” all the time.

Bit 3 (PSTE): Prescaler enable bit for TCC

0: Prescaler disable bit. TCC rate is 1:1.

1: Prescaler enable bit. TCC rate is set at Bit 2 ~ Bit 0.

Bits 2~0 (TPSR2~TPSR0): TCC Prescaler Bits

TPSR2	TPSR1	TPSR0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.27 Bank 0 R23: TCCD (TCC Data Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TCC7~TCC0): TCC data

Counter is increased by the instruction cycle clock. Writable and readable as any other registers.

6.1.28 Bank 0 R24 ~ R2F: (Reserved)

6.1.29 Bank 0 R30: I2CCR1 (I2C Status and Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Strobe/Pend	IMS	ISS	STOP	SAR_EMPTY	ACK	FULL	EMPTY
R/W	R/W	R/W	R/W	R	R	R	R

Bit 7 (Strobe/Pend): In Master mode, it is used as strobe signal to control I²C circuit in sending SCL clock. Automatically resets after receiving or transmitting handshake signal (ACK or NACK). In Slave mode, it is used as pending signal. User should clear it after writing data into Tx buffer or taking data from Rx buffer to inform Slave I²C circuit to release SCL signal.

Bit 6 (IMS): I²C Master/Slave mode select bit
0: Slave (Default)
1: Master

Bit 5 (ISS): I²C C Fast/Standard mode select bit (if Fm is 4 MHz and I2CTS1~0<0,0>)
0: Standard mode (100K bit/s)
1: Fast mode (400K bit/s)

Bit 4 (STOP): In Master mode, if STOP=1 and R/nW=1, then MCU must return nACK signal to Slave device before sending STOP signal. If STOP=1 and R/nW=0, then MCU sends STOP signal after receiving an ACK signal. MCU resets when it sends STOP signal to Slave device.
 In Slave mode, if STOP=1 and R/nW=0 then MCU must return nACK signal to Master device.

Bit 3 (SAR_EMPTY): Set when MCU transmits 1 byte data from I²C Slave Address Register and receive ACK (or nACK) signal. Reset when MCU writes 1 byte data to I²C Slave Address Register.

- Bit 2 (ACK):** The ACK condition bit is set to 1 by hardware when the device responds with an acknowledge (ACK). Resets when the device responds with a not-acknowledge (nACK) signal
- Bit 1 (FULL):** Set by hardware when I²C Receive Buffer register is full. Reset by hardware when the MCU reads data from the I²C Receive Buffer register.
- Bit 0 (EMPTY):** Set by hardware when I²C Transmit Buffer register is empty and ACK (or nACK) signal is received. Reset by hardware when the MCU writes new data into the I²C Transmit Buffer register.

6.1.30 Bank 0 R31: I2CCR2 (I2C Status and Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2CBF	GCEN	I2COPT	BBF	I2CTS2	I2CTS1	I2CTS0	I2CEN
R	R/W	R/W	R	R/W	R/W	R/W	R/W

Bit 7 (I2CBF): I2C Busy Flag Bit

0: clear to "0", in Slave mode, if receive STOP signal or I2C slave address not match.

1: set when I2C communicate with master in slave mode.

*Set when STAR signal, clear when I2C disable or STOP signal for Slave mode.

Bit 6 (GCEN): I2C General Call Function Enable Bit

0: Disable General Call Function

1: Enable General Call Function

Bit 5 (I2COPT): I2C pin optional bit. It is used to switch the pin position of I2C function.

0: Placed I2C pins in P70 (SDA0) and P71 (SCL0).

1: Placed I2C pins in P73 (SDA1) and P74 (SCL1).

*Default value corresponding code option Word 2 I2COPT

Bit 4 (BBF): Busy Flag Bit. I2C detection is busy in the master mode. Read only.

*Set when STAR signal, clear when STOP signal for Master mode.

Bits 3~1 (I2CTS2~I2CTS0): I2C Transmit Clock Select Bits. When using different operating frequency (Fm), these bits must be set correctly to let SCL clock fill in with standard/fast mode.

I2CCR1 Bit 5=1, Fast Mode

I2CTS2	I2CTS1	I2CTS0	SCL CLK	Operating Fm (MHz)
0	0	0	NA	NA
0	0	1	Fm/10	4
0	1	0	Fm/15	6
0	1	1	Fm/20	8
1	0	0	Fm/30	12
1	0	1	Fm/40	16

I2CCR1 Bit 5=0, Standard Mode

I2CTS2	I2CTS1	I2CTS0	SCL CLK	Operating Fm (MHz)
0	0	0	Fm/10	1
0	0	1	Fm/40	4
0	1	0	Fm/60	6
0	1	1	Fm/80	8
1	0	0	Fm/120	12
1	0	1	Fm/160	16
1	1	1	NA	NA

Bit 0 (I2CEN): I2C Enable Bit

0: Disable I2C mode (Default)

1: Enable I2C mode

6.1.31 Bank 0 R32: I2CSA (I2C Slave Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~1 (SA6~SA0): When the MCU is used as Master device for I²C application, these bits are the Slave Device Address register.

Bit 0 (IRW): When the MCU is used as Master device for I²C application, this bit is Read/Write transaction control bit.

0: Write

1: Read

6.1.32 Bank 0 R33: I2CDB (I2C Data Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DB7~DB0): I²C Receive/Transmit Data Buffer

6.1.33 Bank 0 R34: I2CDAL (I2C Device Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DA7~DA0): When the MCU is used as Slave device for I²C application, this register stores the MCU address. It is used to identify the data on the I²C bus to extract the message delivered to the MCU.

NOTE

Slave Address 0x77 is reserved for WTR use.

6.1.34 Bank 0 R35: I2CDAH (I2C Device Address Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	DA9	DA8
-	-	-	-	-	-	R/W	R/W

Bits 7~2: Not used. Set to "0" all the time.

Bits 1~0 (DA9~DA8): Device Address bits

6.1.35 Bank 0 R36: SPICR (SPI Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (CES): Clock Edge Select bit

0: Data shifted-out on a rising edge, and shift-in on a falling edge. Data is on hold during a low-level.

1: Data shifted-out on a falling edge, and shift-in on a rising edge. Data is on hold during a high-level.

Bit 6 (SPIE): SPI Enable bit

0: Disable SPI mode

1: Enable SPI mode

Bit 5 (SRO): SPI Read Overflow bit

0: No overflow

1: A new data is received while the previous data is still being held in the SPIR register. Under this condition, the data in the SPIS register is destroyed. To avoid setting this bit, user should read the SPIR register although only transmission is implemented. This can only occur in Slave mode.

Bit 4 (SSE): SPI Shift Enable bit

0: Reset as soon as the shifting is completed, and the next byte is read to shift.

1: Start to shift, and it remains at "1" while the current byte is still being transmitted.

Bit 3 (SDOC): SDO Output Status Control bit

0: After serial data output, the SDO remains high

1: After serial data output, the SDO remains low

Bits 2~0 (SBRS2~SBRS0): SPI Baud Rate Select bits

SBRS2	SBRS1	SBRS0	Mode	SPI Baud Rate
0	0	0	Master	Fosc/2
0	0	1	Master	Fosc/4
0	1	0	Master	Fosc/8
0	1	1	Master	Fosc/16
1	0	0	Master	Fosc/32
1	0	1	Master	Fosc/64
1	1	0	Slave	/SS enable
1	1	1	Slave	/SS disable

6.1.36 Bank 0 R37: SPIS (SPI Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DORD	TD1	TD0	0	OD3	OD4	0	RBF
R/W	R/W	R/W	-	R/W	R/W	-	R

Bit 7 (DORD): Data shift type control bit

0: Shift left (MSB first)

1: Shift right (LSB first)

Bits 6~5 (TD1~TD0): SDO status output delay time options (Normal mode only).

When the CPU oscillator source uses Fs, it will result to 1 CLK delay time.

NOTE

TD1~TD0 bits are applicable only to Normal mode → Normal mode. If under Sleep mode → Normal mode condition, then Wake-up time is "Warm up time + 1CLK".

TD1	TD0	Delay Time
0	0	8 CLK
0	1	16 CLK
1	0	24 CLK
1	1	32 CLK

Bit 4: Not used. Set to "0" all the time.

Bit 3 (OD3): Open-drain control bit

0: Open-drain disabled for SDO

1: Open-drain enabled for SDO

Bit 2 (OD4): Open-drain control bit

0: Open-drain disabled for SCK

1: Open-drain enabled for SCK

Bit 1: Not used. Set to “0” all the time.

Bit 0 (RBF): Read Buffer Full flag

0: Receiving is not completed, and SPIR has not fully exchanged data.

1: Receiving is completed, and SPIR has fully exchanged data.

6.1.37 Bank 0 R38: SPIR (SPI Read Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
R	R	R	R	R	R	R	R

Bits 7~0 (SRB7~SRB0): SPI Read Data Buffer

6.1.38 Bank 0 R39: SPIW (SPI Write Buffer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (SWB7~SWB0): SPI Write Data Buffer

6.1.39 Bank 0 R3A ~ R4F: (Reserved)

6.1.40 Bank 1 R5: IOCR8

These registers are used to control I/O port direction. They are both readable and writable.

1: Put the relative I/O pin into high impedance

0: Put the relative I/O pin as output

6.1.41 Bank 1 R6 ~ R7: (Reserved)

6.1.42 Bank 1 R8: P5PHCR (Port 5 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH57	PH56	PH55	PH54	PH53	PH52	PH51	PH50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PH57): Control bit used to enable pull-high of the P57 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (PH56): Control bit used to enable pull-high of the P56 pin

Bit 5 (PH55): Control bit used to enable pull-high of the P55 pin

Bit 4 (PH54): Control bit used to enable pull-high of the P54 pin

Bit 3 (PH53): Control bit used to enable pull-high of the P53 pin

Bit 2 (PH52): Control bit used to enable pull-high of the P52 pin

Bit 1 (PH51): Control bit used to enable pull-high of the P51 pin

Bit 0 (PH50): Control bit used to enable pull-high of the P50 pin

6.1.43 Bank 1 R9: P6PHCR (Port 6 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PH67): Control bit used to enable the pull high of P67 pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (PH66): Control bit used to enable the pull high of P66 pin

Bit 5 (PH65): Control bit used to enable the pull high of P65 pin

Bit 4 (PH64): Control bit used to enable the pull high of P64 pin

Bit 3 (PH63): Control bit used to enable the pull high of P63 pin

Bit 2 (PH62): Control bit used to enable the pull high of P62 pin

Bit 1 (PH61): Control bit used to enable the pull high of P61 pin

Bit 0 (PH60): Control bit used to enable the pull high of P60 pin

6.1.44 Bank 1 RA: P78PHCR (Ports 7~8 Pull-high Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				P8HPH	P8LPH	P7HPH	P7LPH
				R/W	R/W	R/W	R/W

Bits 7~4: Not used, set to "0" all the time.

Bit 3 (P8HPH): Control bit used to enable the pull high of Port 8 high nibble pin

0: Enable internal pull-high

1: Disable internal pull-high

Bit 2 (P8LPH): Control bit used to enable the pull high of Port8 low nibble pin

Bit 1 (P7HPH): Control bit used to enable the pull high of Port74 pin

Bit 0 (P7LPH): Control bit used to enable the pull high of Port7 low nibble pin

6.1.45 Bank 1 RB: P5PLCR (Port 5 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL57	PL56	PL55	PL54	PL53	PL52	PL51	PL50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PL57): Control bit used to enable pull-low of the P57 pin

0: Enable internal pull-low

1: Disable internal pull-low

Bit 6 (PL56): Control bit used to enable pull-low of the P56 pin

Bit 5 (PL55): Control bit used to enable pull-low of the P55 pin

Bit 4 (PL54): Control bit used to enable pull-low of the P54 pin

Bit 3 (PL53): Control bit used to enable pull low of the P53 pin

Bit 2 (PL52): Control bit used to enable pull-low of the P52 pin

Bit 1 (PL51): Control bit used to enable pull-low of the P51 pin

Bit 0 (PL50): Control bit used to enable pull-low of the P50 pin

6.1.46 Bank 1 RC: P6PLCR (Port 6 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (PL67): Control bit used to enable the pull low of P67 pin

0: Enable internal pull-low

1: Disable internal pull-low

Bit 6 (PL66): Control bit used to enable the pull low of P66 pin

Bit 5 (PL65): Control bit used to enable the pull low of P65 pin

Bit 4 (PL64): Control bit used to enable the pull low of P64 pin

Bit 3 (PL63): Control bit used to enable the pull low of P63 pin

Bit 2 (PL62): Control bit used to enable the pull low of P62 pin

Bit 1 (PL61): Control bit used to enable the pull low of P61 pin

Bit 0 (PL60): Control bit used to enable the pull low of P60 pin

6.1.47 Bank 1 RD: P78PLCR (Ports 7~8 Pull-low Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	P8HPL	P8LPL	P7HPL	P7LPL
-	-	-	-	R/W	R/W	R/W	R/W

Bits 7~4: Not used, set to "0" all the time.

Bit 3 (P8HPL): Control bit used to enable the pull low of Port 8 high nibble pin

0: Enable internal pull-low

1: Disable internal pull-low

Bit 2 (P8LPL): Control bit used to enable the pull low of Port 8 low nibble pin

Bit 1 (P7HPL): Control bit used to enable the pull low of Port 7 high nibble pin

Bit 0 (P7LPL): Control bit used to enable the pull low of Port 7 low nibble pin

6.1.48 Bank 1 RE: P5HDSCR (Port 5 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H57	H56	H55	H54	H53	H52	H51	H50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (H57~H50): P57~P50 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

6.1.49 Bank 1 RF: P6HDSCR (Port 6 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
H67	H66	H65	H64	H63	H62	H61	H60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~2, 0 (H67~H62,H60): P67~P60 high drive/sink current control bits

0: Enable high drive/sink

1: Disable high drive/sink

Bit 1: Not used. Set to "0" all the time.

6.1.50 Bank 1 R10: P78HDSCR (Port 7~8 High Drive/Sink Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	P8HHDS	P8LHDS	P7HHDS	P7LHDS
-	-	-	-	R/W	R/W	R/W	R/W

Bits 7~4: Not used, set to "0" all the time.

Bit 3 (P8HHDS): Control bit used to enable high drive/sink of Port8 high nibble pin

0: Enable high drive/sink

1: Disable high drive/sink

Bit 2 (P8LHDS): Control bit used to enable high drive/sink of Port8 low nibble pin

Bit 1 (P7HHDS): Control bit used to enable high drive/sink of Port7 high nibble pin

Bit 0 (P7LHDS): Control bit used to enable high drive/sink of Port7 low nibble pin

6.1.51 Bank 1 R11: P5ODCR (Port 5 Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (OD57~OD50): Open-Drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.1.52 Bank 1 R12: P6ODCR (Port 6 Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (OD67~OD60): Open-Drain control bits

0: Disable open-drain function

1: Enable open-drain function

6.1.53 Bank 1 R13: P78ODCR (Ports 7~8 Open-Drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	P8HOD	P8LOD	P7HOD	P7LOD
-	-	-	-	R/W	R/W	R/W	R/W

Bits 7~4: Not used, set to "0" all the time.

Bit 3 (P8HOD): Control bit used to enable open-drain of Port 8 high nibble pin

0: Disable open-drain function

1: Enable open-drain function

Bit 2 (P8LOD): Control bit used to enable open-drain of Port 8 low nibble pin

Bit 1 (P7HOD): Control bit used to enable open-drain of Port 7 high nibble pin

Bit 0 (P7LOD): Control bit used to enable open-drain of Port 7 low nibble pin

6.1.54 Bank 1 R14 ~ R15: (Reserved)

6.1.55 Bank 1 R16: PWMSCR (PWM Source Clock Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	PWMCS	PWMBS	PWMAS
-	-	-	-	-	R/W	R/W	R/W

Bits 7~3: Not used, set to "0" all the time.

Bit 2 (PWMCS): Clock selection for PWMC timer

0: Fs (default)

1: Fm

Bit 1 (PWMBS): Clock selection for PWMB timer

0: Fs (default)

1: Fm

Bit 0 (PWMAS): Clock selection for PWMA timer

0: Fs (default)

1: Fm

6.1.56 Bank 1 R17: PWMACR (PWM1 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMAE	-	-	-	TAEN	TAP2	TAP1	TAP0
R/W	-	-	-	R/W	R/W	R/W	R/W

Bit 7 (PWMAE): PWMA enable bit

0: Disable (default)

1: Enable. The compound pin is used as PWMA pin

Bits 6~4: Not used, set to "0" all the time.

Bit 3 (TAEN): TMRA enable bit. All PWM function is valid only as this bit is set

0: TMRA is off (default value)

1: TMRA is on

PWMXEN	TXEN	Function description
0	0	Not used as PWM function; I/O pin or other functional pin.
0	1	Timer function; I/O pin or other function pin.
1	0	PWM function, the waveform keeps at low level.
1	1	PWM function, the normal PWM output waveform.

Bits 2~0 (TAP2~TAP0): TMRA clock prescaler option bits

TAP2	TAP1	TAP0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.57 Bank 1 R18: PRDAL (Low Byte of PWMA Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDA7	PRDA6	PRDA5	PRDA4	PRDA3	PRDA2	PRDA1	PRDA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PRDA7~0): The contents of the register are low bytes of the PWMA period.

NOTE

If the PWMA duty/period needs to reload, the PRDAL register must be updated.

6.1.58 Bank 1 R19: PRDAH (High Byte of PWMA Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDA15	PRDA14	PRDA13	PRDA12	PRDA11	PRDA10	PRDA9	PRDA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PRDA15~8): The contents of the register are high bytes of PWMA period

6.1.59 Bank 1 R1A: DTAL (Low Byte of PMWA Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTA7	DTA6	DTA5	DTA4	DTA3	DTA2	DTA1	DTA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DTA7~0): The contents of the register are low bytes of the PWMA duty.

6.1.60 Bank 1 R1B: DTAH (High Byte of PMWA Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTA15	DTA14	DTA13	DTA12	DTA11	DTA10	DTA9	DTA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DTA15~8): The contents of the register are high bytes of the PWMA duty.

6.1.61 Bank 1 R1C: TMRAL (Low Byte of Timer 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRA7	TMRA6	TMRA5	TMRA4	TMRA3	TMRA2	TMRA1	TMRA0
R	R	R	R	R	R	R	R

Bits 7~0 (TMRA7~0): The contents of the register are low bytes of the PWMA timer which is counting. This is read-only.

6.1.62 Bank 1 R1D: TMRAH (High Byte of Timer 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRA15	TMRA14	TMRA13	TMRA12	TMRA11	TMRA10	TMRA9	TMRA8
R	R	R	R	R	R	R	R

Bits 7~0 (TMRA15~8): The contents of the register are high bytes of the PWMA timer which is counting. This is read-only.

6.1.63 Bank 1 R1E: PWMB CR (PWMB Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMBE	-	-	-	TBEN	TBP2	TBP1	TBP0
R/W	-	-	-	R/W	R/W	R/W	R/W

Bit 7 (PWMBE): PWMB enable bit

0: Disable (default)

1: Enable. The compound pin is used as PWMB pin

Bits 6~4: Not used, set to "0" all the time.

Bit 3 (TBEN): TMRB enable bit. All PWM function is valid only as this bit is set

0: TMRB is off (default value)

1: TMRB is on

Bits 2~0 (TBP2~TBP0): TMRB clock prescaler option bits

TBP2	TBP1	TBP0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.64 Bank 1 R1F: PRDBL (Low Byte of PWMB Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDB7	PRDB6	PRDB5	PRDB4	PRDB3	PRDB2	PRDB1	PRDB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PRDB7~0): The contents of the register are low byte of the PWMB period

NOTE

If the PWMB duty/period needs to reload, the PRDBL register must be updated.

6.1.65 Bank 1 R20: PRDBH (High Byte of PWMB Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDB15	PRDB14	PRDB13	PRDB12	PRDB11	PRDB10	PRDB9	PRDB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PRDB15~8): The contents of the register are high byte of PWMB period

6.1.66 Bank 1 R21: DTBL (Low Byte of PMWB Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTB7	DTB6	DTB5	DTB4	DTB3	DTB2	DTB1	DTB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DTB7~0): The contents of the register are low byte of the PWMB duty

6.1.67 Bank 1 R22: DTBH (High Byte of PMW2 Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTB15	DTB14	DTB13	DTB12	DTB11	DTB10	DTB9	DTB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DTB15~8): The contents of the register are high byte of the PWMB duty

6.1.68 Bank 1 R23: TMRBL (Low Byte of Timer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRB7	TMRB6	TMRB5	TMRB4	TMRB3	TMRB2	TMRB1	TMRB0
R	R	R	R	R	R	R	R

Bits 7~0 (TMRB7~0): The contents of the register are low byte of the PWMB timer which is counting. This is read-only

6.1.69 Bank 1 R24: TMRBH (High Byte of Timer 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRB15	TMRB14	TMRB13	TMRB12	TMRB11	TMRB10	TMRB9	TMRB8
R	R	R	R	R	R	R	R

Bits 7~0 (TMRB15~8): The contents of the register are high byte of the PWMB timer which is counting. This is read-only

6.1.70 Bank 1 R25: PWMCCR (PWMC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCE	-	-	-	TCEN	TCP2	TCP1	TCP0
R/W	-	-	-	R/W	R/W	R/W	R/W

Bit 7 (PWMCE): PWMC enable bit

0: Disable (default)

1: Enable. The compound pin is used as PWMC pin

Bits 6~4: Not used, set to "0" all the time.

Bit 3 (TCEN): TMRC enable bit. All PWM function is valid only as this bit is set

0: TMRC is off (default value)

1: TMRC is on

Bits 2~0 (TCP2~TCP0): TMRC clock prescaler option bits

TCP2	TCP1	TCP0	Prescale
0	0	0	1:1 (default)
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.71 Bank 1 R26: PRDCL (Low byte of PWM Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDC7	PRDC6	PRDC5	PRDC4	PRDC3	PRDC2	PRDC1	PRDC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PRDC7~0): The contents of the register are low byte of the PWM period

*PWM duty/period reload for PRDCL register update.

6.1.72 Bank 1 R27: PRDCH (High Byte of PWM Period)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRDC15	PRDC14	PRDC13	PRDC12	PRDC11	PRDC10	PRDC9	PRDC8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PRDC15~8): The contents of the register are high byte of PWM period

6.1.73 Bank 1 R28: DTCL (Low Byte of PWM Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTC7	DTC6	DTC5	DTC4	DTC3	DTC2	DTC1	DTC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DTC7~0): The contents of the register are low byte of the PWM duty

6.1.74 Bank 1 R29: DTCH (High Byte of PMWC Duty)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DTC15	DTC14	DTC13	DTC12	DTC11	DTC10	DTC9	DTC8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DTC15~8): The contents of the register are high byte of the PWM duty

6.1.75 Bank 1 R2A: TMRCL (Low byte of Timer C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRC7	TMRC6	TMRC5	TMRC4	TMRC3	TMRC2	TMRC1	TMRC0
R	R	R	R	R	R	R	R

Bits 7~0 (TMRC7~0): The contents of the register are low byte of the PWM timer which is counting. This is read-only

6.1.76 Bank 1 R2B: TMRCH (High byte of Timer C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMRC15	TMRC14	TMRC13	TMRC12	TMRC11	TMRC10	TMRC9	TMRC8
R	R	R	R	R	R	R	R

Bits 7~0 (TMRC15~8): The contents of the register are high byte of the PWM timer which is counting. This is read-only

6.1.77 Bank 1 R2C ~ R44: (Reserved)

6.1.78 Bank 1 R45: TBPTL (Table Point Low Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (TB7~TB0): Table Point Address Bits 7~0.

6.1.79 Bank 1 R46: TBPTH (Table Point High Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HLB	RDS	TB13	TB12	TB11	TB10	TB9	TB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (HLB): Obtain MLB or LSB at machine code of ROM or Data area.

0: the address of read byte value is Bit7 ~Bit0

1: the address of read byte value is Bit15~Bit8

Bit 6 (RDS): ROM / Data select bit, read machine code information area select.

0: ROM (default)

1: Data area (Data Address 000~17F)

HLB	RDS	Read to Register Data Value Description
0	0	Read byte value is Bit 7 ~ Bit 0 from machine code.
0	1	Read byte value is Bit 7 ~ Bit 0 from Data area.
1	0	Read byte value is— Highest bit fixed at “0” and Bit 15 ~ Bit 8 from machine code.
1	1	Read byte value is Bit 15 ~ Bit 8 from Data area.

Bits 5~0 (TB13~TB8): Table point Address Bits 13~8.

6.1.80 Bank 1 R47: STKMON (Stack Pointer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STOV	-	-	STL4	STL3	STL2	STL1	STL0
R	-	-	R	R	R	R	R

Bit 7 (STOV): Stack pointer overflow indicator bit. Read only.

Bits 4~0 (STL4~0): Stack pointer number. Read only.

6.1.81 Bank 1 R48: PCH (Program Counter High)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	PC13	PC12	PC11	PC10	PC9	PC8
-	-	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~6: Not used. Set to “0” all the time.

Bits 5~0 (PC13~PC8): The high byte of program counter

6.1.82 Bank 1 R49: LVDCR (Low Voltage Detector Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDEN		LVDS1	LVDS0	LVDB			
R/W		R/W	R/W	R			

Bit 7 (LVDEN): Low Voltage Detector Enable Bit

0: Disable low voltage detector

1: Enable low voltage detector

Bits 5~4 (LVDS1~LVDS0): Low Voltage Detector Level Bits.

LV DEN	LVDS1, LVDS0	LVD Voltage Interrupt Level	LVDB
1	00	VDD <2.5V	0
		VDD >2.7V	1
1	01	VDD <2.8V	0
		VDD >3.0V	1
1	10	VDD <3.2V	0
		VDD >3.4V	1
1	11	VDD <4V	0
		VDD >4.2V	1
0	XX	NA	1

Bit 3 (LVDB): Low Voltage Detector State Bit. This is a read only bit. When the VDD pin voltage is lower than LVD voltage interrupt level (selected by LVDS1 ~ LVDS0), this bit will be cleared.

0: Low voltage is detected.

1: Low voltage is not detected or LVD function is disabled.

Bits 6, 2~0: Not used, set to "0" all the time.

6.1.83 Bank 1 R4A~ R4F: (Reserved)

6.1.84 Bank 2 R5 ~ R46: (Reserved)

6.1.85 Bank 2 R47: DACR (DAC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	DAE
-	-	-	-	-	-	-	R/W

Bits 7~1: not used bits, fixed to "0" all the time.

Bits 0 (DAE): DAC enable bit of P84 pin.

0: Disable DAC, P84/TPS21/DAC act as P84/TPS21 pin.

1: Enable DAC to act as analog output pin.

6.1.86 Bank 2 R48: DACD (Digital to Analog Converter Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DAD0[7]	DAD0[6]	DAD0[5]	DAD0[4]	DAD0[3]	DAD0[2]	DAD0[1]	DAD0[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (DAD0[7]~DAD0[0]): DAC Data Buffer.

6.1.87 Bank 2 R49 ~ R4F: (Reserved)

6.1.88 R50~R7F, Banks 0~3 R80~RFF

These are all 8-bit general-purpose registers.

6.2 TCC/WDT and Prescaler

Two 8-bit counters are available as prescalers for the TCC and WDT. The TPSR0~TPSR2 bits of the TCCCR register (Bank 0 R22) are used to determine the ratio of the TCC prescaler. Likewise, the WPSR0~WPSR2 bits of the WDTCR register (Section 6.1.25 Bank 0 R21) are used to determine the WDT prescaler. The prescaler counter is cleared by the instructions each time they are written into TCC. The WDT and prescaler are cleared by the “WDTC” and “SLEP” instructions. Figure 6-3 below depicts the circuit diagram of TCC/WDT.

The TCCD (Section 6.1.27 TCC Data Register) is an 8-bit timer/counter. The TCC clock source is from the internal clock only and TCC will be incremented by 1 at Fc clock (without prescaler). **The TCC will stop running when Sleep mode occurs.**

The Watchdog Timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e., in Sleep mode). During Normal operation or Sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during Normal mode by software programming (see WDTE bit of WDTCR (Section 6.1.25 Bank 0 R21) register). With no prescaler, the WDT time-out period is approximately 18 ms¹ (one oscillator start-up timer period).

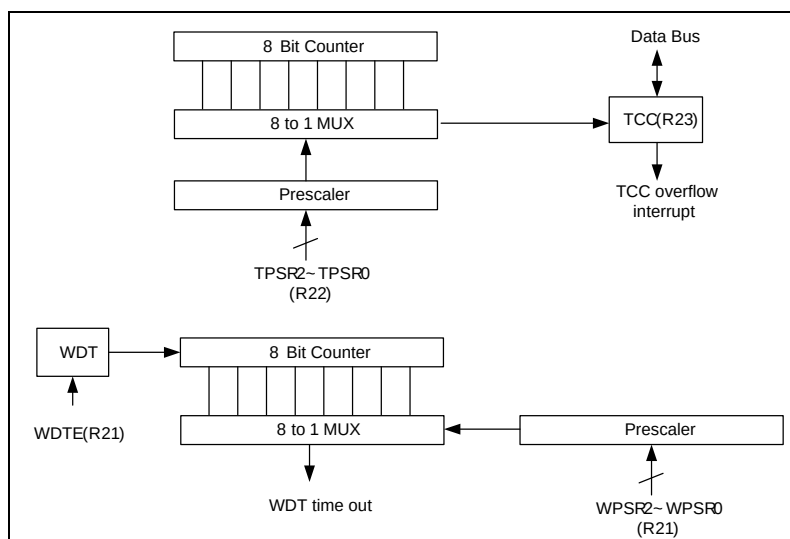


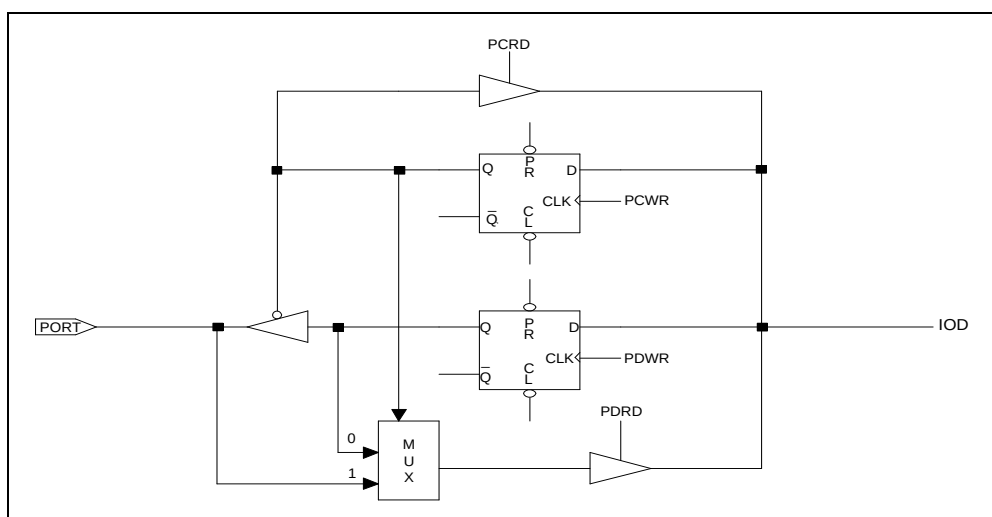
Figure 6-3 TCC and WDT Block Diagram

¹ VDD=5V, WDT time-out period = 16.5ms ± 8%.
VDD=3V, WDT time-out period = 18ms ± 8%.

6.3 I/O Ports

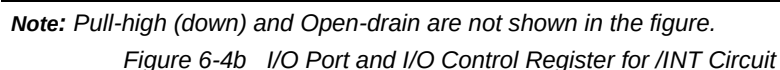
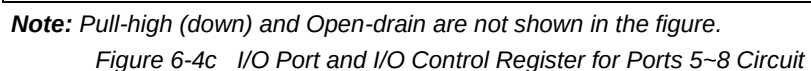
The I/O registers, Port 5~Port 8 are bidirectional tri-state I/O ports. All can be pulled high and pulled low internally by software. Furthermore, they can also be set as open-drain output and high sink/drive by software. Ports 5~8 features wake-up and interrupt function as well as input status change interrupt function. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC8).

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 ~ Port 8 are shown in the following Figure 6-4a to 6-4d.



Note: Pull-down is not shown in the figure.

Figure 6-4a I/O Port and I/O Control Register for Port 5~8 Circuit Diagram



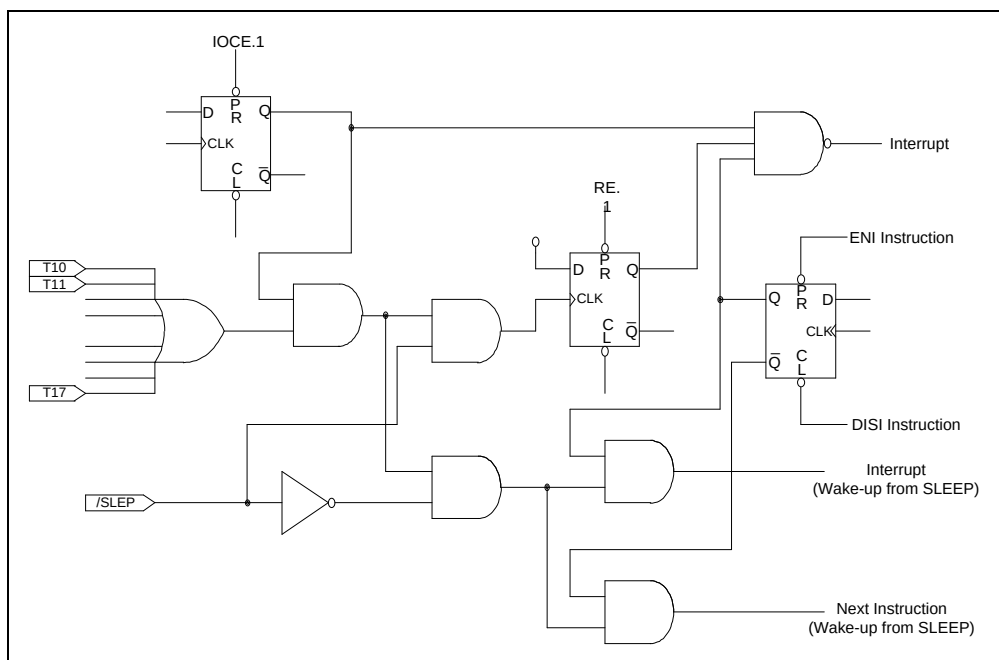


Figure 6-4d I/O Port 5~8 with Input Change Interrupt/Wake-up Block Diagram

6.3.1 Usage of Ports 5~8 Input Change Wake-up/Interrupt Function

1. Wake-up

a) Before Sleep:

- 1) Disable WDT
- 2) Read I/O Port (MOV R6,R6)
- 3) Execute "ENI" or "DISI"
- 4) Enable Wake-up bit (Set ICWKP_x = 1)
- 5) Execute "SLEP" instruction

b) After Wake-up:

→ Next instruction

2. Wake-up and Interrupt

a) Before SLEEP

- 1) Disable WDT
- 2) Read I/O Port (MOV R6,R6)
- 3) Execute "ENI" or "DISI"
- 4) Enable Wake-up bit (Set ICWKP_x = 1)
- 5) Enable interrupt (Set PxICIE = 1)
- 6) Execute "SLEP" instruction

b) After Wake-up

- 1) IF "ENI" → Interrupt vector (0006H)
- 2) IF "DISI" → Next instruction

6.4 Reset and Wake-up

A Reset is initiated by one of the following events:

- 1) Power-on reset
- 2) /RESET pin input "low"
- 3) WDT time-out (if enabled)
- 4) LVR (if enabled)

The device is kept in a Reset condition for a period of approximately 18ms² (one oscillator start-up timer period) after a reset is detected. If the /Reset pin goes "low" or the WDT time-out is active, a reset is generated. In IRC mode, the reset time is 8-/32 clocks. Once a Reset occurs, the following functions are performed (see Figure 6-5 below):

- The oscillator is continuously running, or will be started.
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog Timer and prescaler are cleared.
- The control register bits are set as shown in the table below under Section 6.4.3, *Summary of Register Initial Values after Reset*.

The Sleep (power down) mode is asserted by executing the "SLEP" instruction. While entering Sleep mode, WDT (if enabled) is cleared but keeps on running. Wake-up is then generated (in IRC mode the wake-up time is 8-/32 clocks). The controller can be awakened by any of the following events:

- 1) External reset input on /RESET pin
- 2) WDT time-out (if enabled)
- 3) External (/INT) pin changes (if INTWE is enabled)
- 4) Port input status changes (if ICWKPx is enabled)
- 5) SPI receives data while it serves as Slave device (if SPIWK is enabled)
- 6) I²C receives data while it serves as Slave device (if I2CWK is enabled)
- 7) TCC Counter mode overflow occur.(if TCIE is enable)

The first two events (1 and 2) will cause the eKTF5832 to reset. The T and P flags of R3 are used to determine the source of the reset (Wake-up). Events 3 to 7 are considered as continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 0x02~0x40 after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up.

² Vdd = 5V, set up time period = 16.5ms ± 8%
Vdd = 3V, set up time period = 16.5ms ± 8%

Only one of Events 3 to 6 can be enabled before entering into Sleep mode. That is:

- If WDT is enabled before SLEEP, the eKTF5832 can wake-up only when Events 1 or 2 occurs. Refer to the Section 6.5 *Interrupt*, for further details.
- If External (/INT) pin change is used to wake-up the eKTF5832 and the EXWE bit is enabled before SLEEP (with WDT disabled). Hence, the eKTF5832 can wake-up only when Event 3 occurs.
- If Port Input Status Change is used to wake-up the eKTF5832 and the corresponding wake-up setting is enabled before SLEEP (with WDT disabled), the eKTF5832 can wake-up only when Event 4 occurs.
- With SPI serving as Slave device and the SPIWK bit of Bank0 R11 register is enabled before SLEEP (with WDT disabled), the SPI will wake-up the eKTF5832 after it receives data. Hence, the eKTF5832 can wake-up only when Event 5 occurs.
- When I²C serving as Slave device and I2CWB bit of Bank 0 R11 register is enabled before SLEEP (with WDT disabled), the I²C will wake-up the eKTF5832 after it receives data. Hence, the eKTF5832 can be waken-up only by Event 6.

6.4.1 Summary of Wake-up and Interrupt Mode Operation

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
External INT	INTWK = 0, EXIE = 0	/INT pin Disable							
	INTWK = 0, EXIE = 1	Wake-up is invalid.				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	INTWK = 1, EXIE = 0	/INT pin Disable							
	INTWK = 1, EXIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TCC INT	TCIE = 0	Wake-up is invalid.				Interrupt is invalid.			
	TCIE = 1	Wake-up is invalid.		Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
PWMA/B/C (When TimerA/B/C Match PRD or DT)	PWMxPIE = 0	Wake-up is invalid.				Interrupt is invalid.			
	PWMxPIE = 1	Wake-up is invalid.		Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Pin Change INT	WKPxH/L = 0, PxICIE = 0	Wake-up is invalid.				Interrupt is invalid.			
	WKPxH/L = 0, PxICIE = 1	Wake-up is invalid.				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

	WKPxH/L = 1, PxICIE = 0	Wake up + Next Instruction				Interrupt is invalid.			
	WKPxH/L = 1, PxICIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Low Voltage Detector	LVDWK = 0, LVDIE = 0	Wake-up is invalid.				Interrupt is invalid.			
	LVDWK = 0, LVDIE = 1	Wake-up is invalid.				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	LVDWK = 1, LVDIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid.			
	LVDWK = 1, LVDIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
I2C (Slave mode)	I2CWK = 0, I2CxIE = 0	Wake-up is invalid.				I2C Can't use		Interrupt is invalid.	
	I2CWK = 0, I2CxIE = 1	Wake-up is invalid.				I2C Can't use		Next Instruction	Interrupt + Interrupt Vector
	I2CWK = 1, I2CxIE = 0	Wake up + Next Instruction I2C must be slave mode				I2C Can't use		Interrupt is invalid.	
	I2CWK = 1, I2CxIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	I2C Can't use		Next Instruction	Interrupt + Interrupt Vector
SPI (Slave mode)	SPIWK = 0, SPIE = 0	Wake-up is invalid.				Interrupt is invalid.			
	SPIWK = 0, SPIE = 1	Wake-up is invalid.				Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	SPIWK = 1, SPIE = 0	Wake up + Next Instruction				Interrupt is invalid.			
	SPIWK = 1, SPIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
WDT time out		RESET	RESET	RESET	RESET	RESET	RESET	RESET	RESET

NOTE

After wake up:

1. If interrupt enable → interrupt+ next instruction
2. If interrupt disable → next instruction

6.4.2 The Status of RST, T, and P of the Status Register

A reset condition is initiated by one of the following events:

- 1) Power-on condition
- 2) High-low-high pulse on the /RESET pin
- 3) Watchdog timer time-out
- 4) When LVR occurs

The values of T and P, as listed in the following table are used to check how the MCU wakes up. The next table shows the events that may affect the status of T and P.

■ Values of RST, T and P after Reset:

Reset Type	T	P
Power-on	1	1
/RESET during Operation mode	P*	P*
/RESET Wake-up during Sleep mode	1	0
WDT during Operation mode	0	P*
WDT Wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

* P: Previous status before reset

■ Status of T and P being affected by Events:

Event	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin change during Sleep mode	1	0

* P: Previous value before reset

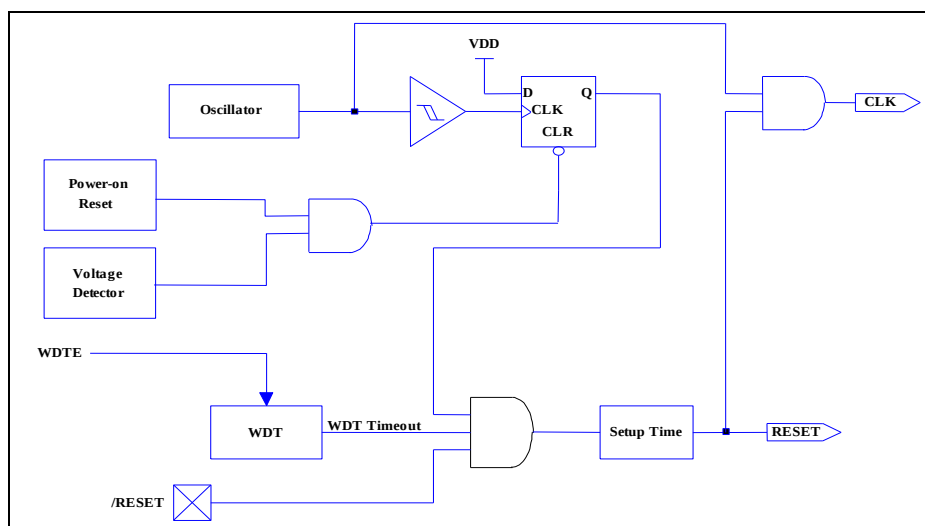


Figure 6-5 Block Diagram of Controller Reset

6.4.3 Summary of Register Initial Values after Reset

Legend: *U*: Unknown or don't care *P*: Previous value before reset
C: Same with Code option *t*: Check tables under Section 6.4.2

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x01	R1 (BSR)	Bit Name	0	0	SBS1	SBS0	0	GBS2	GBS1	GBS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	P	0	P	P	P
0x02	R2 (PCL)	Bit Name	-	-	-	-	-	-	-	-
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x03	R3 (SR)	Bit Name	INT	N	OV	T	P	Z	DC	C
		Power-On	0	U	U	1	1	U	U	U
		/RESET and WDT	0	P	P	t	t	P	P	P
		Wake-up from Sleep/Idle	P	P	P	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	RSR7	RSR6	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X05	Bank 0, R5 (Port 5)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x06	Bank 0, R6 (Port 6)	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x07	Bank 0, R7 (Port 7)	Bit Name				P74	P73	P72	P71	P70
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	P	P	P	P	P
0x08	Bank 0, R8 (Port 8)	Bit Name	P87	P86	P85	P84	P83	P82	P81	P80
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0B	Bank 0, RB (IOCR5)	Bit Name	IOC57	IOC56	IOC55	IOC54	IOC53	IOC52	IOC51	IOC50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x0C	Bank 0, RC (IOCR6)	Bit Name	IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0D	Bank 0, RD (IOCR7)	Bit Name				IOC74	IOC73	IOC72	IOC71	IOC70
		Power-On	0	0	0	1	1	1	1	1
		/RESET and WDT	0	0	0	1	1	1	1	1
		Wake-up from Sleep/Idle	0	0	0	P	P	P	P	P
0x0E	Bank 0, RE (OMCR)	Bit Name	CPUS	IDLE				RCM2	RCM1	RCM0
		Power-On	Code option (HLFS)	1	0	0	0	Code option (RCM2)	Code option (RCM1)	Code option (RCM0)
		/RESET and WDT	Code option (HLFS)	1	0	0	0	P	P	P
		Wake-up from Sleep/Idle	P	P	0	0	0	P	P	P
0X0F	Bank 0, RF EIESCR	Bit Name					EIES1	EIES0		
		Power-On	0	0	0	0	1	1	0	0
		/RESET and WDT	0	0	0	0	1	1	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	0	0

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x10	Bank 0, R10 (WUCR1)	Bit Name			LVDWK		INTWK 1	INTWK 0		
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	0	P	P	0	0
0x11	Bank 0, R11 WUCR2	Bit Name					SPIWK	I2CWK		
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	P	P	0	0
0x12	Bank 0, R12 WUCR3	Bit Name	ICWKP 8	ICWKP 7	ICWKP6	ICWKP 5				
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	0	0	0	0
0x14	Bank 0, R14 SFR1	-			LVD SF		EXSF1	EXSF0		TCSF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	0	P	P	0	P
0x16	Bank 0, R16 SFR3	Bit Name			PWMCP SF	PWMC DSF	PWMB PSF	PWMB DSF	PWMA PSF	PWMA DSF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	P	P	P	P	P
0x17	Bank 0, R17 SFR4	Bit Name	P8ICSF	P7ICSF	P6ICSF	P5ICSF	SPISF	I2CSTP SF	I2CRSF	I2CTSF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x19	Bank 0, R19 SFR6	Bit Name	SHSF							
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0x1B	Bank 0, R1B IMR1	Bit Name			LVDIE		EXIE1	EXIE0		TCIE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	0	P	P	0	P
0x1D	BANK 0, R1D IMR3	Bit Name			PWMCPIE	PWMC DIE	PWMB PIE	PWMB DIE	PWMA PIE	PWMA DIE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X1E	Bank 0, R1E IMR4	Bit Name	P8ICIE	P7ICIE	P6ICIE	P5ICIE	SPIIE	I2CSTP IE	I2CRIE	I2CTIE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X20	Bank 0, R20 IMR6	Bit Name	SHIE							
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	P	0	P	P
0X21	Bank 0, R21 WDTCR	Bit Name	WDTE				PSWE	WPSR2	WPSR1	WPSR0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	P	P	P	P
0X22	Bank 0, R22 TCCCR	Bit Name		TCCS			PSTE	TPSR2	TPSR1	TPSR0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	P	P	P	P	P	P	P
0X23	Bank 0, R23 TCCD	Bit Name	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X30	Bank 0, R30 I2CCR1	Bit Name	Strobe/ Pend	IMS	ISS	STOP	SAR_E MPTY	ACK	FULL	EMPTY
		Power-On	0	0	0	0	1	0	0	1
		/RESET and WDT	0	0	0	0	1	0	0	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X31	Bank 0, R31 I2CCR2	Bit Name	I2CBF	GCEN	I2COPT	BBF	I2CTS2	I2CTS1	I2CTS0	I2CEN
		Power-On	0	0	Code option (I2COPT)	0	0	0	0	1
		/RESET and WDT	0	0	P	0	0	0	0	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X32	Bank 0, R32 I2CSA	Bit Name	SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X33	Bank 0, R33 I2CDB	Bit Name	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X34	Bank 0, R34 I2CDAL	Bit Name	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X35	Bank 0, R35 I2CDAH	Bit Name							DA9	DA8
		Power-On	0	0	0	0	0	0	1	1
		/RESET and WDT	0	0	0	0	0	0	1	1
		Wake-up from Sleep/Idle	0	0	0	0	0	0	P	P
0X36	Bank 0, R36 SPICR	Bit Name	CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X37	Bank 0, R37 SPIS	Bit Name	DORD	TD1	TD0		OD3	OD4		RBF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	0	P	P	0	P
0X38	Bank 0, R38 SPIR	Bit Name	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
		Power-On	U*	U*	U*	U*	U*	U*	U*	U*
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X39	BANK 0, R39 SPIW	Bit Name	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
		Power-On	U*	U*	U*	U*	U*	U*	U*	U*
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X05	Bank 1, R5 IOCR8	Bit Name	IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X08	Bank 1, R8 P5PHCR	Bit Name	PH57	PH56	PH55	PH54	PH53	PH52	PH51	PH50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X09	Bank 1, R9 P6PHCR	Bit Name	PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0A	Bank 1, RA P78PHCR	Bit Name					P8HPH	P8LPH	P7HPH	P7LPH
		Power-On	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0B	Bank 1, RB P5PLCR	Bit Name	PL57	PL56	PL55	PL54	PL53	PL52	PL51	PL50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0C	Bank 1, RC P6PLCR	Bit Name	PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0D	Bank 1, RD P78PLCR	Bit Name					P8HPL	P8LPL	P7HPL	P7LPL
		Power-On	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P
0X0E	Bank 1, RE P5HDSCR	Bit Name	H57	H56	H55	H54	H53	H52	H51	H50
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X0F	Bank 1, RF P6HDSCR	Bit Name	H67	H66	H65	H64	H63	H62	H61	H60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X10	Bank 1, R10 P78HDSCR	Bit Name					P8HHD S	P8LHD S	P7HHD S	P7LHD S
		Power-On	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P
0X11	Bank 1, R11 P5ODCR	Bit Name	OD57	OD56	OD55	OD54	OD53	OD52	OD51	OD50
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X12	Bank 1, R12 P6ODCR	Bit Name	OD67	OD66	OD65	OD64	OD63	OD62	OD61	OD60
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X13	Bank 1, R13 P78ODCR	Bit Name					P8HOD	P8LOD	P7HOD	P7LOD
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P
0X16	Bank 1, R16 PWMSCR	Bit Name						PWMC S	PWMB S	PWMA S
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	0	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X17	Bank 1, R17 PWMA CR	Bit Name	PWMA E				TAEN	TAP2	TAP1	TAP0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	P	P	P	P
0X18	Bank 1, R18 PRDAL	Bit Name	PRDA7	PRDA 6	PRDA5	PRDA 4	PRDA3	PRDA2	PRDA1	PRDA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X19	Bank 1, R19 PRDAH	Bit Name	PRDA1 5	PRDA 14	PRDA13	PRDA 12	PRDA1 1	PRDA1 0	PRDA9	PRDA8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1A	Bank 1, R1A DTAL	Bit Name	DTA7	DTA6	DTA5	DTA4	DTA3	DTA2	DTA1	DTA0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1B	Bank 1, R1B DTAH	Bit Name	DTA15	DTA14	DTA13	DTA12	DTA11	DTA10	DTA9	DTA8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1C	Bank 1, R1C TMRAL	Bit Name	TMRA7	TMRA 6	TMRA5	TMRA 4	TMRA3	TMRA2	TMRA1	TMRA0
		Power-On	0	0	0	0	0	0	0	1
		/RESET and WDT	0	0	0	0	0	0	0	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1D	Bank 1, R1D TMRAH	Bit Name	TMRA1 5	TMRA 14	TMRA13	TMRA 12	TMRA1 1	TMRA1 0	TMRA9	TMRA8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X1E	BANK 1, R1E PWMB CR	Bit Name	PWMB E				TBEN	TBP2	TBP1	TBP0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	0	0	0	P	P	P	P
0X1F	Bank 1, R1F PRDBL	Bit Name	PRDB7	PRDB 6	PRDB5	PRDB 4	PRDB3	PRDB2	PRDB1	PRDB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X20	Bank 1, R20 PRDBH	Bit Name	PRDB1 5	PRDB 14	PRDB13	PRDB 12	PRDB1 1	PRDB1 0	PRDB9	PRDB8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X21	Bank 1, R21 DTBL	Bit Name	DTB7	DTB6	DTB5	DTB4	DTB3	DTB2	DTB1	DTB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X22	Bank 1, R22 DTBH	Bit Name	DTB15	DTB14	DTB13	DTB12	DTB11	DTB10	DTB9	DTB8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X23	Bank 1, R23 TMRBL	Bit Name	TMRB7	TMRB6	TMRB5	TMRB4	TMRB3	TMRB2	TMRB1	TMRB0
		Power-On	0	0	0	0	0	0	0	1
		/RESET and WDT	0	0	0	0	0	0	0	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X24	Bank 1, R24 TMRBH	Bit Name	TMRB15	TMRB14	TMRB13	TMRB12	TMRB11	TMRB10	TMRB9	TMRB8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X25	Bank 1, R25 PWMCCR	Bit Name	PWMC E				TCEN	TCP2	TCP1	TCP0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	P	P	P	P
0X26	Bank 1, R26 PRDCL	Bit Name	PRDC7	PRDC6	PRDC5	PRDC4	PRDC3	PRDC2	PRDC1	PRDC0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X27	Bank 1, R27 PRDCH	Bit Name	PRDC15	PRDC14	PRDC13	PRDC12	PRDC11	PRDC10	PRDC9	PRDC8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	P	P	P	P	P	P	P	P
0X28	Bank 1, R28 DTCL	Bit Name	DTC7	DTC6	DTC5	DTC4	DTC3	DTC2	DTC1	DTC0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X29	Bank 1, R29 DTCH	Bit Name	DTC15	DTC14	DTC13	DTC12	DTC11	DTC10	DTC9	DTC8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P

Address	Bank Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X2A	Bank 1, R2A TMRCL	Bit Name	TMRC7	TMRC6	TMRC5	TMRC4	TMRC3	TMRC2	TMRC1	TMRC0
		Power-On	0	0	0	0	0	0	0	1
		/RESET and WDT	0	0	0	0	0	0	0	1
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X2B	Bank 1, R2B TMRCH	Bit Name	TMRC15	TMRC14	TMRC13	TMRC12	TMRC11	TMRC10	TMRC9	TMRC8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X45	Bank 1, R45 TBPTL	Bit Name	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X46	Bank 1, R46 TBP TH	Bit Name	HLB	RDS	TB13	TB12	TB11	TB10	TB9	TB8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	P	P	P	P	P	P	P
0X47	Bank 1, R47 STKMON	Bit Name	STOV			STL4	STL3	STL2	STL1	STL0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	P	0	0	0	P	P	P	P
0X48	Bank 1, R48 PCH	Bit Name			PC13	PC12	PC11	PC10	PC9	PC8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	P	P	P	P	P	P
0X49	Bank 1, R49 LVDCR	Bit Name	LV DEN		LVDS1	LVDS0	LVDB			
		Power-On	0	0	0	0	1	0	0	0
		/RESET and WDT	0	0	0	0	1	0	0	0
		Wake-up from Sleep/Idle	P	0	P	P	P	0	0	0
0X47	Bank 2, R47 DACR	Bit Name								DAE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Sleep/Idle	0	0	0	0	0	0	0	P
0X48	Bank 2, R48 DACD	Bit Name	DAD0[7]	DAD0[6]	DAD0[5]	DAD0[4]	DAD0[3]	DAD0[2]	DAD0[1]	DAD0[0]
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Sleep/Idle	0	0	0	0	P	P	P	P

6.5 Interrupt

The eKTF5832 has 15 interrupts (External, Internal) as listed below:

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal / External	Reset	-	-	0	High 0
External	INT	ENI + EXIE=1	EXSF	2	1
External	Pin change	ENI + ICIE=1	ICSF	4	2
Internal	TCC	ENI + TCIE=1	TCSF	6	3
Internal	LVD	ENI+LVDEN & LVDIE=1	LVDSF	8	4
Internal	SPI	ENI + SPIIE=1	SPISF	C	5
Internal	PWMPA	ENI+PWMAPIE=1	PWMAPIE=1	14	6
Internal	PWMDA	ENI+PWMDIE=1	PWMDIE=1	16	7
Internal	I2C Transmit	ENI+ I2CTIE	I2CTSF	1A	8
Internal	I2C Receive	ENI+ I2CRIE	I2CRSF	1C	9
Internal	I2CSTOP	ENI+ I2CSTPIE	I2CSTPSF	1E	10
Internal	PWMPB	ENI+PWMBPIE=1	PWMBPIE=1	24	11
Internal	PWMDB	ENI+PWMBDIE=1	PWMBDIE=1	26	12
Internal	PWMPB	ENI+PWMCPIE=1	PWMCPIE=1	2A	13
Internal	PWMDC	ENI+PWMCPIE=1	PWMCPIE=1	2C	14
Internal	System hold	ENI+SHIE	SHSF	3A	15

Bank 0 R14~R19 are the interrupt status registers that record the interrupt requests in the relative flags/bits. Bank0 R1B~R20 are the interrupt Mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the enabled interrupts occurs, the next instruction will be fetched from individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICSF bit which is set to "0") in the Interrupt Status Register is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

External interrupt is equipped with digital noise rejection circuit (input pulse of less than **4 System Clock Time** is eliminated as noise). When an interrupt (Falling edge) is generated by the External interrupt (if enabled), the next instruction will be fetched from Address 002H.

Before the interrupt subroutine is executed, the contents of ACC and the R3 (Bit 0~Bit 6) and R4 registers are saved by hardware. If another interrupt occurs, the ACC, R3 (Bit 0~Bit 4), and R4 will be replaced by the new interrupt. After the interrupt service routine is completed, ACC, R3 (Bit 0~Bit 6), and R4 restored.

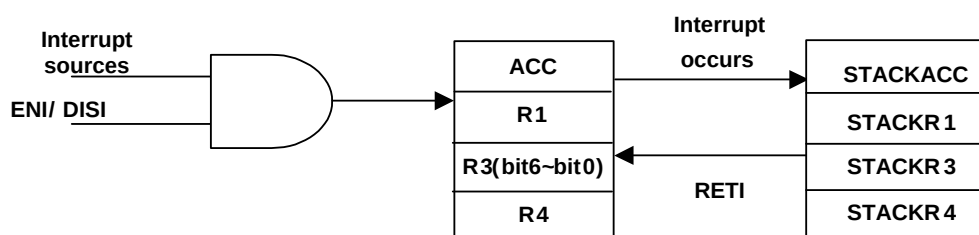


Figure 6-6a Interrupt Backup Diagram

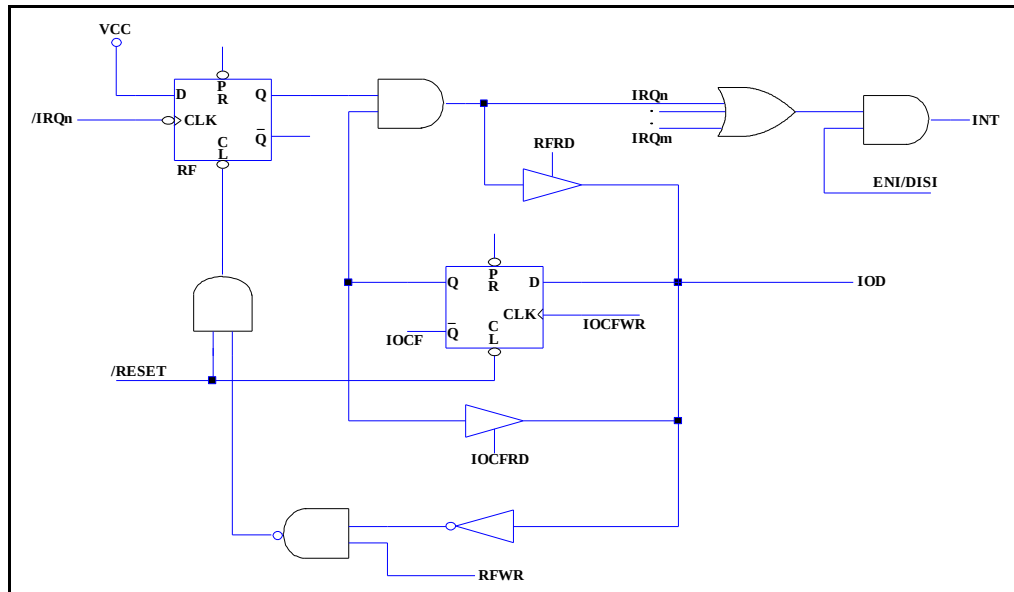


Figure 6-6b Interrupt Input Circuit

6.6.2 Control Register

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x16	SFR3	-	-	PWMCPS F	PWMCDS F	PWMBPSF	PWMBDSF	PWMAFSF	PWMADSF
			-	-	F	F	F	F	F	F
Bank 0	0x1D	IMR3	-	-	PWMCPIE	PWMCDEIE	PWMBPIE	PWMBDIE	PWMAPIE	PWMADIE
			-	-	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x16	PWMSC R	-	-	-	-	-	PWMCS	PWMBS	PWMAS
			-	-	-	-	-	R/W	R/W	R/W
Bank 1	0x17	PWMA R	PWMAE	-	-	-	TAEN	TAP2	TAP1	TAP0
			R/W	-	-	-	R/W	R/W	R/W	R/W
Bank 1	0x18	PRDAL	PRDA7	PRDA6	PRDA5	PRDA4	PRDA3	PRDA2	PRDA1	PRDA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x19	PRDAH	PRDA15	PRDA14	PRDA13	PRDA12	PRDA11	PRDA10	PRDA9	PRDA8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1A	DTAL	DTA7	DTA6	DTA5	DTA4	DTA3	DTA2	DTA1	DTA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1B	DTAH	DTA15	DTA14	DTA13	DTA12	DTA11	DTA10	DTA9	DTA8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1C	TMRAL	TMRA7	TMRA6	TMRA5	TMRA4	TMRA3	TMRA2	TMRA1	TMRA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1D	TMRAH	TMRA15	TMRA14	TMRA13	TMRA12	TMRA11	TMRA10	TMRA9	TMRA8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x1E	PWMBC R	PWMBE	-	-	-	TBEN	TBP2	TBP1	TBP0
			R/W	-	-	-	R/W	R/W	R/W	R/W
Bank 1	0x1F	PRDBL	PRDB7	PRDB6	PRDB5	PRDB4	PRDB3	PRDB2	PRDB1	PRDB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x20	PRDBH	PRDB15	PRDB14	PRDB13	PRDB12	PRDB11	PRDB10	PRDB9	PRDB8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x21	DTBL	DTB7	DTB6	DTB5	DTB4	DTB3	DTB2	DTB1	DTB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x22	DTBH	DTB15	DTB14	DTB13	DTB12	DTB11	DTB10	DTB9	DTB8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x23	TMRBL	TMRB7	TMRB6	TMRB5	TMRB4	TMRB3	TMRB2	TMRB1	TMRB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x24	TMRBH	TMRB15	TMRB14	TMRB13	TMRB12	TMRB11	TMRB10	TMRB9	TMRB8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x25	PWMCC R	PWMCE	-	-	-	TCEN	TCP2	TCP1	TCP0
			R/W	-	-	-	R/W	R/W	R/W	R/W
Bank 1	0x26	PRDCL	PRDC7	PRDC6	PRDC5	PRDC4	PRDC3	PRDC2	PRDC1	PRDC0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 1	0x27	PRDCH	PRDC15	PRDC14	PRDC13	PRDC12	PRDC11	PRDC10	PRDC9	PRDC8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x28	DTCL	DTC7	DTC6	DTC5	DTC4	DTC3	DTC2	DTC1	DTC0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x29	DTCH	DTC15	DTC14	DTC13	DTC12	DTC11	DTC10	DTC9	DTC8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x2A	TMRCL	TMRC7	TMRC6	TMRC5	TMRC4	TMRC3	TMRC2	TMRC1	TMRC0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 1	0x2B	TMRCH	TMRC15	TMRC14	TMRC13	TMRC12	TMRC11	TMRC10	TMRC9	TMRC8
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.6.3 Increment Timer Counter (TMRX: TMRxH/TMRxL)

TMRX's are 16-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMR can be read only. If employed, they can be turned off for power saving by setting the TxEN Bit to "0". TMRA, TMRB and TMRC, are internal designs and cannot be read.

6.6.4 PWM Time Period (PRDX: PRDxL/H)

The PWM time period has a 16-bit resolution and is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

- 1) TMRX is cleared
- 2) The PWMX pin is set to "1"

NOTE

The PWM output cannot be set if the duty cycle is "0."

- 3) The PWMXPSF bit is set to "1"

To calculate the PWM time period, use the following formula:

Example:

PRDX = 49; Fosc = 4 MHz; TMRX (0, 0, 0) = 1 : 1;

Then

$$Period = (49 + 1) \times \left(\frac{1}{4M} \right) \times 1 = 12.5\mu s$$

6.6.5 PWM Duty Cycle (DTX: DTxH/DT1L)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded anytime. However, it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula shows how to calculate the PWM duty cycle:

$$\text{Duty cycle} = (\text{DTX}) \times \left(\frac{1}{F_{OSC}} \right) \times (\text{TMRX prescale value})$$

Example:

DTX = 10; Fosc = 4 MHz; TMRX (0, 0, 0) = 1 : 1;

Then

$$\text{Duty cycle} = (10) \times \left(\frac{1}{4M} \right) \times 1 = 2.5\mu s$$

6.6.6 PWM Programming Process/Steps

- 1) Load the PWM duty cycle to DT
- 2) Load the PWM time period to PRD
- 3) Enable the interrupt function by writing Bank0-R1D, if required
- 4) Load a desired value for the timer prescaler
- 5) Enable PWMX function, i.e., enable PWMXE control bit
- 6) Finally, enable TMRX function, i.e., enable TXEN control bit

If the application needs to change PWM duty and period cycle at run time, refer to the following programming steps:

- 1) Load new duty cycle (if using dual PWM function) at any time.
- 2) Load new period cycle. You must take note of the order of loading period cycle. As the low byte of PWM period cycle is assigned a value, the new PWM cycle is loaded into circuit.
- 3) The circuit will automatically update the new duty and period cycles to generate new PWM waveform at the next PWM cycle.

6.7 SPI (Serial Peripheral Interface)

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0X36	SPICR	CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0
			R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Bank 0	0X37	SPIS	DORD	TD1	TD0	-	OD3	OD4	-	RBF
			R/W	R/W	R	-	R/W	R/W	-	R/W
Bank 0	0X38	SPIR	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
			R	R	R	R	R	R	R	R
Bank 0	0X39	SPIW	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0X18	SFR4	-	-	-	-	SPSF	-	-	-
			-	-	-	-	R/W	-	-	-
Bank 0	0X1E	IMR4	-	-	-	-	SPIE	-	-	-
			-	-	-	-	R/W	-	-	-

6.7.1 Overview and Features

■ Overview:

Figures 6-8a and 6-8b show how the eKTF5832 communicates with other devices through SPI module. If the eKTF5832 is the Master controller, it will send clock through the SCK pin. A couple of 8-bit data are transmitted and received at the same time. However, if the eKTF5832 is defined as a Slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted based on both clock rate and the selected edge. User can also set the –

- SPIS Bit 7 (DORD) to determine the SPI transmission order,
- SPICR Bit 3 (SDOC) to control SDO pin after serial data output status,
- SPIS Bit 6 (TD1) and Bit 5 (TD0) determine the SDO status output delay times.

■ Features:

- 1) Operation in either Master mode or Slave mode
- 2) Three-wire or four-wire full duplex synchronous communication
- 3) Programmable baud rates of communication
- 4) Programmable clock polarity, (Bank 0 R36 Bit 7)
- 5) Interrupt flag available for read buffer full
- 6) SPI transmission order
- 7) SDO status select after serial data output
- 8) SDO status output delay time
- 9) SPI handshake pin
- 10) Up to 8 MHz (maximum) bit frequency

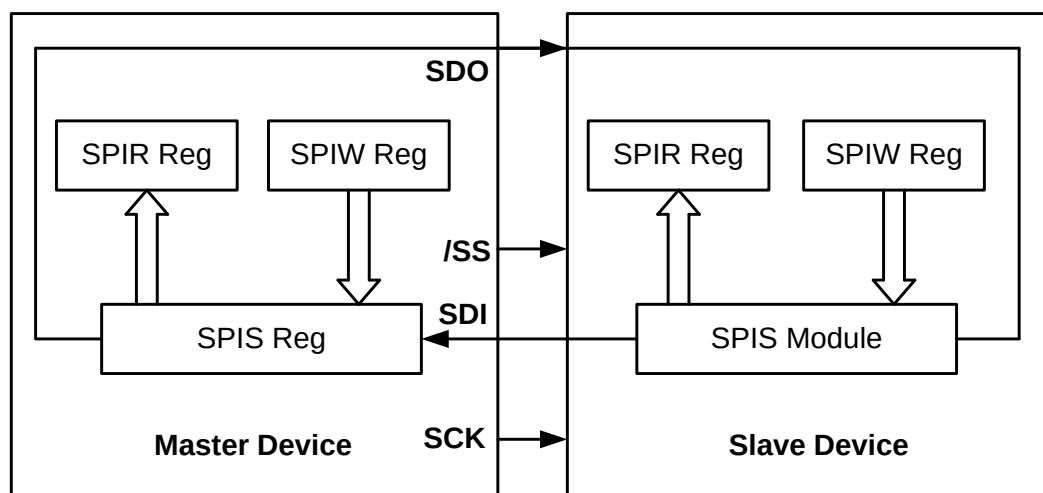


Figure 6-8a SPI Master/Slave Communication Block Diagram

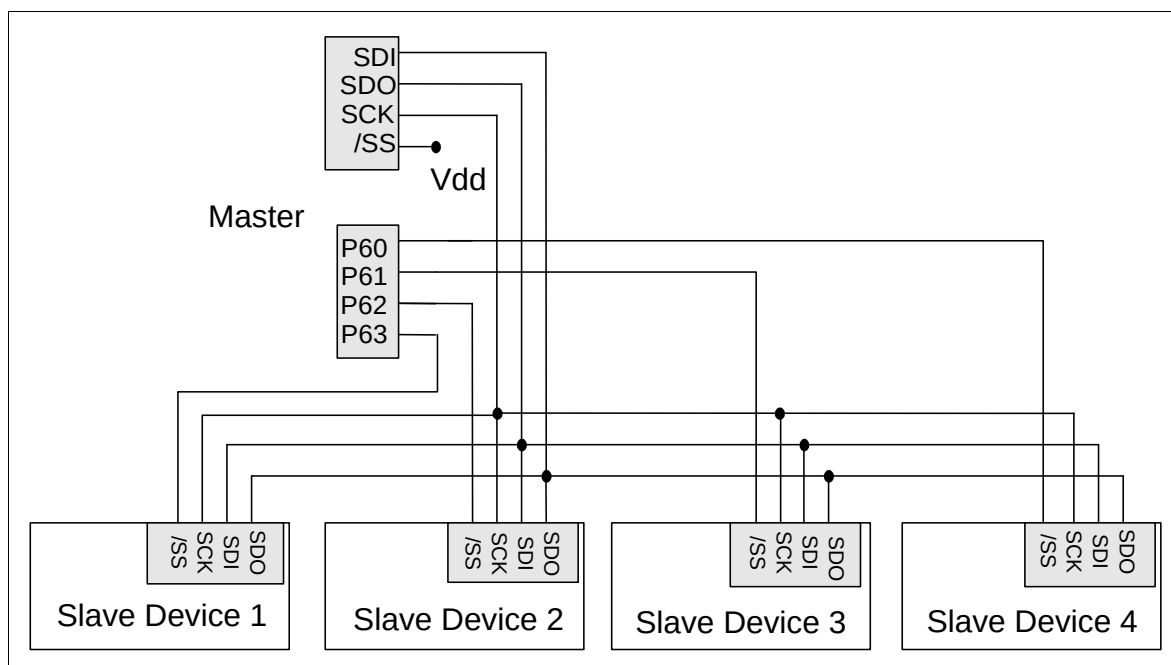


Figure 6-8b Single-Master and Multi-Slave SPI Configuration

6.7.2 SPI Function Description

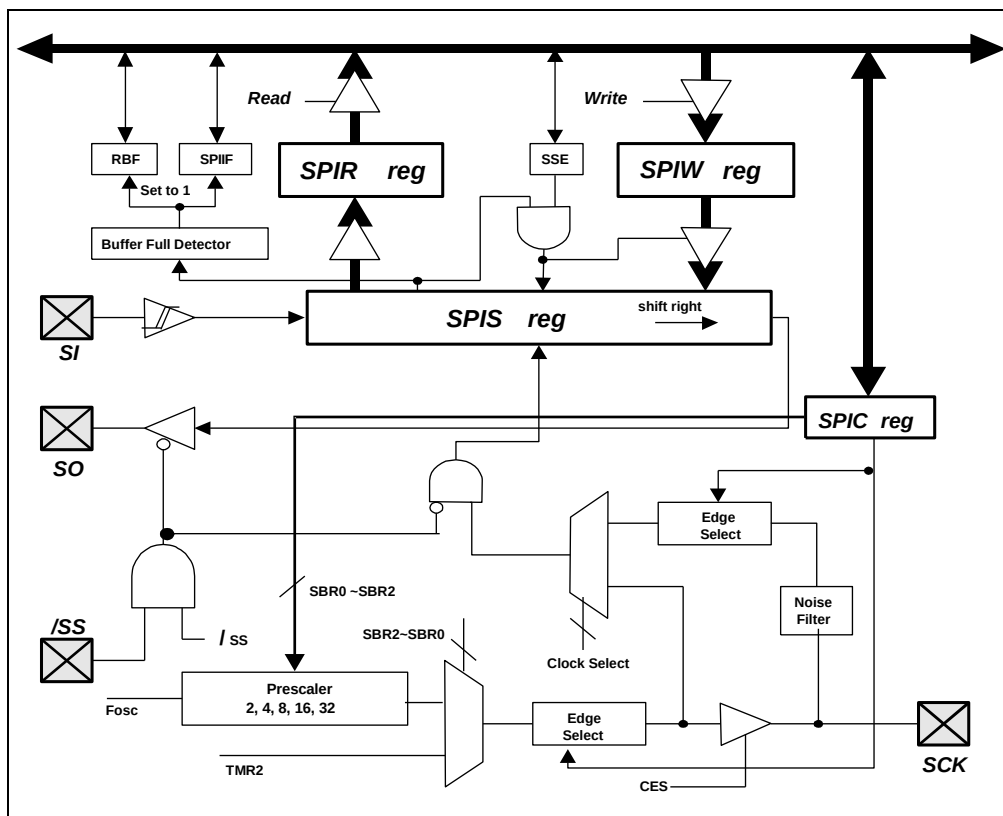


Figure 6-9a SPI Function Block Diagram

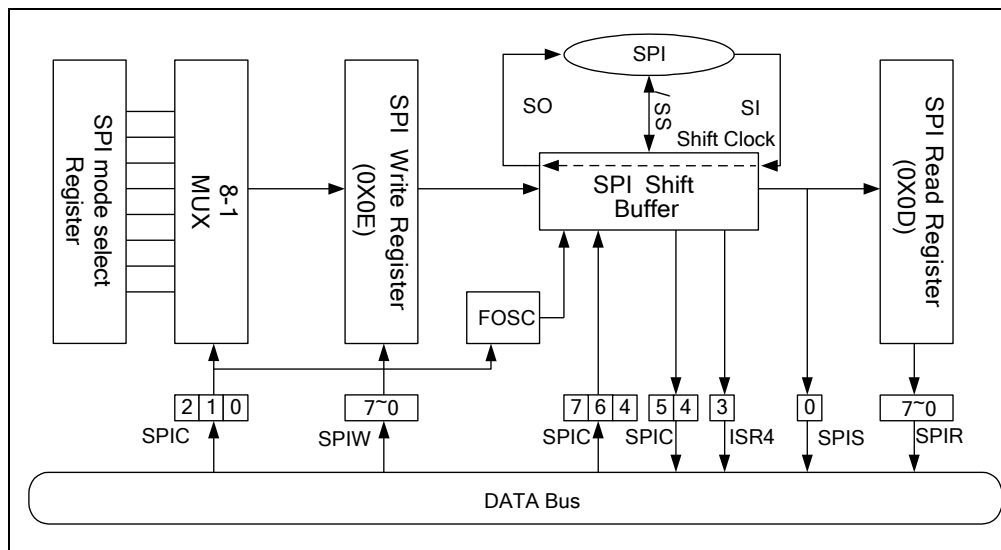


Figure 6-9b SPI Transmission Function Block Diagram

The following explains the functions of each block in the above figures as SPI carries out communication with the depicted signals:

- **P52/SI/TPA2:** Serial Data In
- **P51/SO/TPA1:** Serial Data Out
- **P53/SCK/TPA3:** Serial Clock
- **P50//SS/TPA0:** /Slave Select (Option). This pin (/SS) may be required during Slave mode.
- **RBF:** Set by Buffer Full Detector
- **Buffer Full Detector:** Set to 1 when an 8-bit shifting is completed.
- **SSE:** Loads the data in SPIS register, and begin to shift. The SSE bit will be kept in “1” if the communication is still undergoing. This flag must be cleared as shifting is completed. You can determine if the next write attempt is available.
- **SPIS reg.:** Shifting byte in and out. The MSB is shifted first. Both the SPIR and the SPIW registers are shifted at the same time. Once data are written, SPIS starts transmitting / receiving. The data received will be moved to the SPIR register as the shifting of the 8-bit data is completed. The RBF (Read Buffer Full) flag and the SPI SF (SPI Interrupt) flag are then set.
- **SPIR reg.:** Read buffer. The buffer is updated as the 8-bit shifting is completed. The data must be read before the next reception is completed. The RBF flag is cleared as the SPIR register reads.
- **SPIW reg.:** Write buffer. The buffer will deny any attempts to write until the 8-bit shifting is completed.
- **SBRS2~SBRS0:** Programming of the clock frequency/rates and sources.
- **Clock Select:** Select either the internal or the external clock as shifting clock.
- **Edge Select:** Select the appropriate clock edges by programming the CES bit

6.7.3 SPI Signal and Pin Description

The detailed functions of the four pins, SI, SO, SCK, and /SS are as follows:

- **P52/SI/TPA2:**
 - Serial Data In
 - Receive sequentially, the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last.
 - Defined as high-impedance if not selected.

- Program the same clock rate and clock edge to latch on both the Master and Slave devices.
- The byte received will update the transmitted byte.
- The RBF will be set as the SPI operation is completed.
- Timing is shown in Figures 6-10a and 6-10b below.

■ **P51/SO/TPA1:**

- Serial Data Out
- Transmit sequentially; the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last.
- Program the same clock rate and clock edge to latch on both the Master and Slave devices.
- The received byte will update the transmitted byte.
- The CES bit is reset, as the SPI operation is completed.
- Timing is shown in Figures 6-10a and 6-10b.

■ **P53/SCK/TPA3:**

- Serial Clock
- Generated by a Master device
- Synchronize the data communication on both the SI and SO pins.
- The CES is used to select the edge to communicate.
- The SBR0~SBR2 is used to determine the baud rate of communication.
- The CES, SBR0, SBR1, and SBR2 bits have no effect in Slave mode.
- Timing is shown in Figures 6-10a and 6-10b.

■ **P50//SS/TPA0:**

- Slave Select; negative logic.
- Generated by a Master device to indicate the Slave(s) has to receive data.
- Goes low before the first cycle of SCK occurs, and remains low until the last (8th) cycle is completed
- Ignore the data on the SI and SO pins when /SS is high, because SO is no longer driven
- Timing is shown in Figures 6-10a and 6-10b.

6.7.4 SPI Mode Timing

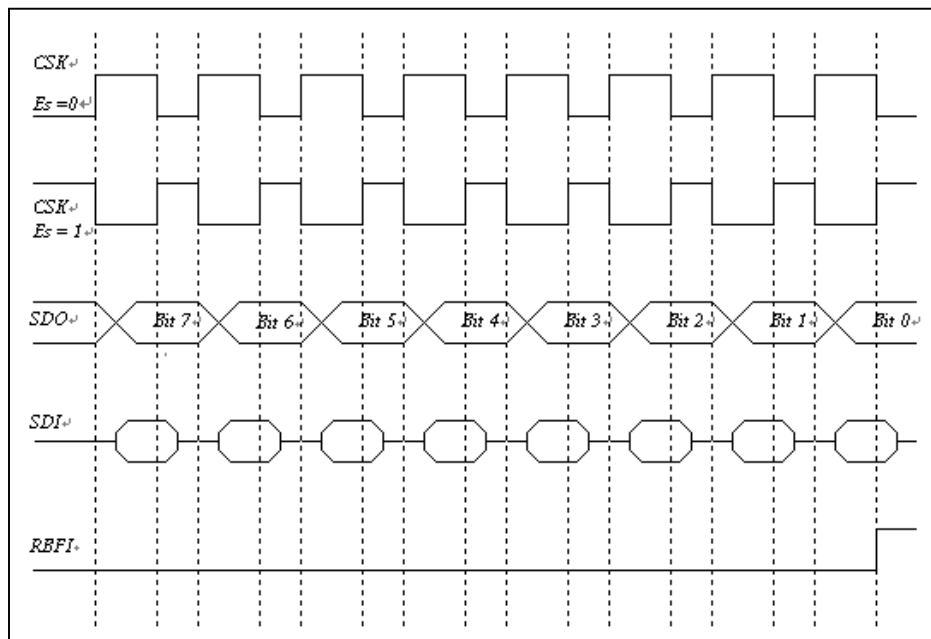


Figure 6-10a SPI Mode with /SS Disabled Timing Diagram

The SCK edge is selected by programming the bit CES. The waveform shown in Figure 6-10a above, is applicable regardless of whether the eKTF5832 is in Master or Slave mode with /SS disabled. However, the waveform in Figure 6-10b below can only be implemented in Slave mode with /SS enabled.

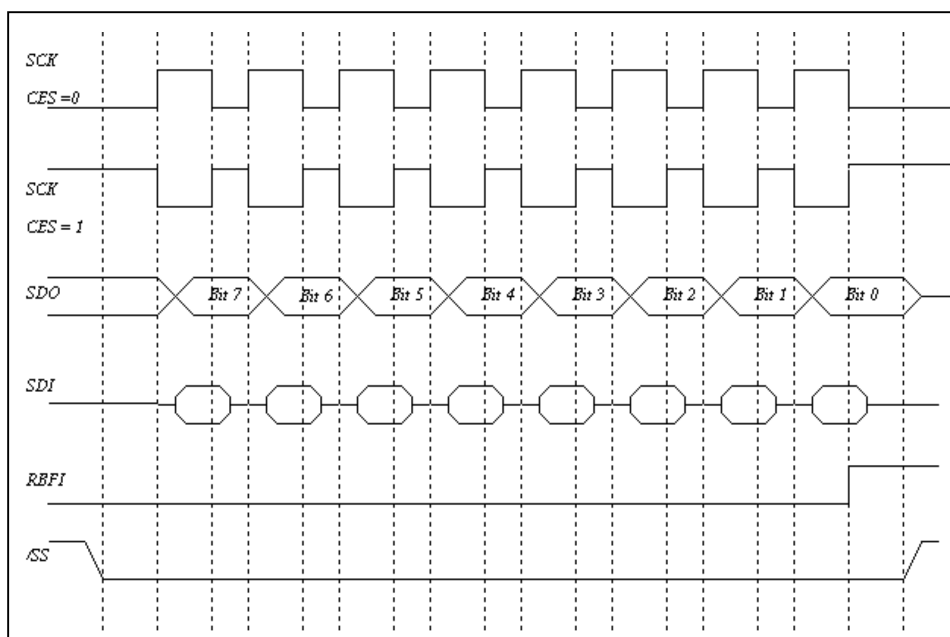


Figure 6-10b SPI Mode with /SS Enabled Timing Diagram

6.8 I²C Function

The I²C function and transmit/receive pin are enabled by default when eKTF5832 is powered-on.

■ Registers for I²C circuit:

R_BANK	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 0	0x30	I2CCR1	Strobe /Pend	IMS	ISS	STOP	SAR_EMPTY	ACK	FULL	EMPTY
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x31	I2CCR2	I2CBF	GCEN	I2COPT	BBF	I2CTS2	I2CTS1	I2CTS0	I2CEN
			R	R/W	R/W	R	R/W	R/W	R/W	R/W
Bank 0	0x32	I2CSA	SA6	SA5	SA4	SA3	SA2	SA1	SA0	IRW
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x33	I2CDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x34	I2CDAL	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bank 0	0x35	I2CDAH	-	-	-	-	-	-	DA9	DA8
			-	-	-	-	-	-	R/W	R/W
Bank 0	0x18	SFR4	-	-	-	-	-	I2CSTPIF	I2CRSF	I2CTSF
			-	-	-	-	-	R/W	R/W	R/W
Bank 0	0x1E	IMR4	-	-	-	-	-	I2CSTPIE	I2CRIE	I2CTIE
			-	-	-	-	-	R/W	R/W	R/W

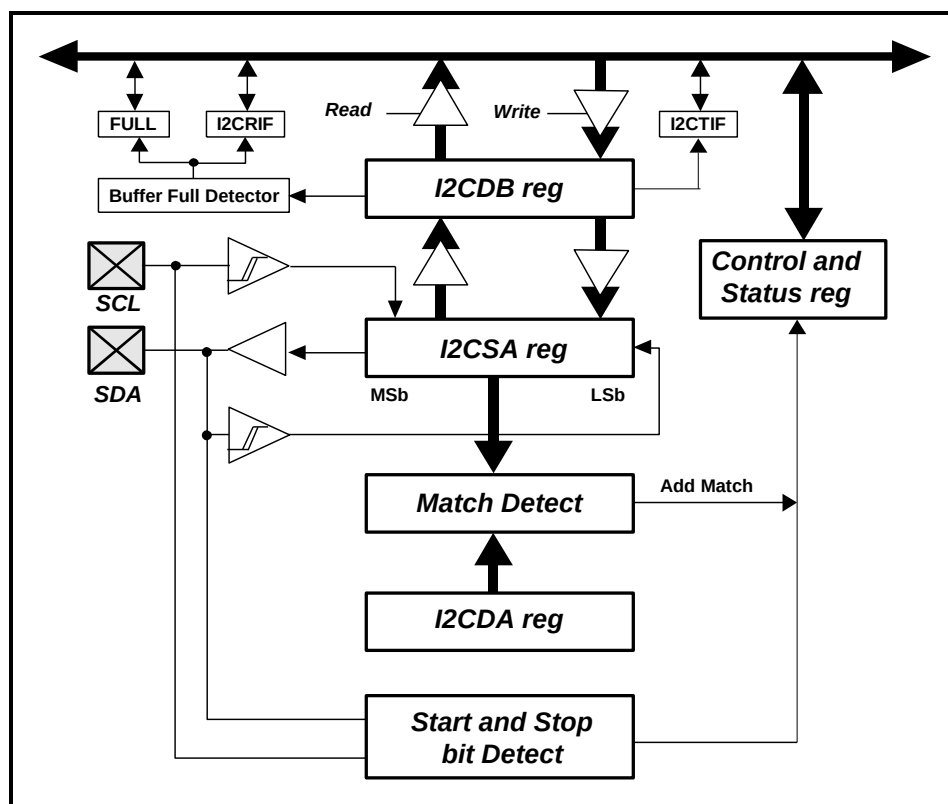


Figure 6-11 eKTF5832 I²C Block Diagram

The eKTF5832 supports a bidirectional, 2-wire bus, 7/10-bit addressing, and data transmission protocol. A device that sends data to the bus is defined as transmitter, while a device receiving the data is defined as a receiver. The bus has to be controlled by a Master device which generates the Serial Clock (SCL), controls the bus access, and generates the Start and Stop conditions. Both Master and Slave can operate as transmitter or receiver, but the Master device determines which mode is activated.

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are HIGH. The output stages of the devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the I²C-bus can be transferred at the rates of up to 100 kbit/sec in Standard-mode or up to 400 kbit/sec in Fast-mode.

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW.

The I²C interrupt occurs as describe below:

Condition	Master/Slave	Transmit Address	Transmit Data	Stop
Master Transmitter (transmits to Slave-Receiver)	Master	Transmit interrupt	Transmit interrupt	Stop interrupt
	Slave	Receive interrupt	Receive interrupt	Stop interrupt
Master Receiver (read Slave- Transmitter)	Master	Transmit interrupt	Receive interrupt	Stop interrupt
	Slave	Transmit interrupt	Transmit interrupt	Stop interrupt

Within the procedure of the I²C bus, unique situations could arise which are defined as START (S) and STOP (P) conditions.

A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition.

A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

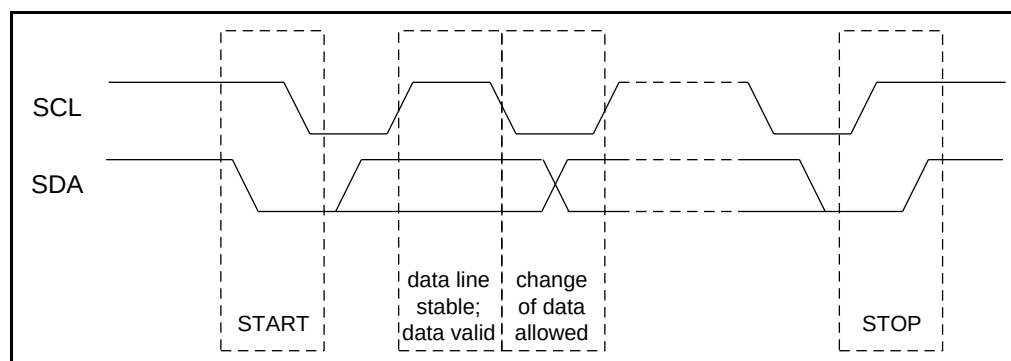


Figure 6-12 I²C Transfer Condition

6.8.1 7-Bit Slave Address

Master-transmitter transmits to Slave-receiver. The transfer direction is not changed.

Master reads Slave immediately after first byte. At the moment of the first acknowledgement, the Master-transmitter becomes a Master-receiver and the Slave-receiver becomes a Slave-transmitter. This first acknowledgement is still generated by the Slave. The STOP condition is generated by the Master, which has previously sent a Not-Acknowledge (A). The difference between Master-transmitter and Master-receiver is only in their R/W bit. If the R/W bit is "0", the Master device would be transmitter. Otherwise, the Master device would be the receiver (R/W Bit = "1").

Communications between the Master-transmitter/receiver and Slave-transmitter/receiver are illustrated in the following Figures 6-13a and 6-13b.

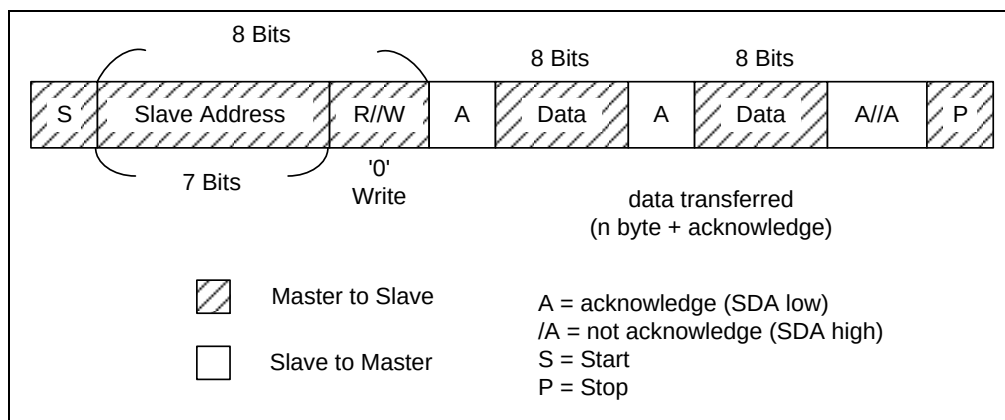


Figure 6-13a Master-Transmitter Transmits to Slave-Receiver with 7-Bit Slave Address

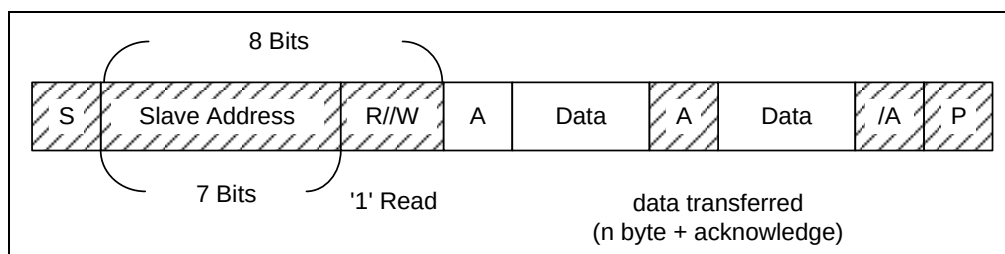


Figure 6-13b Master-Receiver Reads from Slave-Transmitter with 7-Bit Slave Address

6.8.2 10-Bit Slave Address

In 10-Bit Slave address mode, using 10-bit for addressing exploits the reserved combination 11110XX for the first seven bits of the first byte following a START(S) or repeated START (Sr) condition. The first seven bits of the first byte are the combination 11110XX of which the last two bits (XX) are the two most-significant bits of the 10-bit address. If the R/W bit is "0", the second byte after acknowledge would be the eight address bits of 10-bits Slave address. Otherwise, the second byte would just be the next transmitted data from a Slave to Master device. The first byte 11110XX is transmitted by using the Slave address register (I2CSA), and the second byte XXXXXXXX is transmitted by using the data buffer (I2CDB).

The possible data transfer formats for 10-bit Slave address mode are explained in the following paragraphs and Figures 6-14a ~ 6-14e.

■ Master-Transmitter Transmits to Slave-Receiver with a 10-bit Slave Address

When the Slave receives the first byte after START bit from Master, each Slave device will compare the first seven bits of the first byte (11110XX) with their own address and check the 8th bit (R/W). If the R/W bit is “0”, a Slave or more, will return an Acknowledge (A1). Then all Slave devices will continue to compare the second address (XXXXXXX). If a Slave device finds a match, that particular Slave device will be the only one to return an Acknowledge (A2). The matched Slave device will remain addressed by the Master until it receives the STOP condition or until a repeated START condition followed by the different Slave address is received.

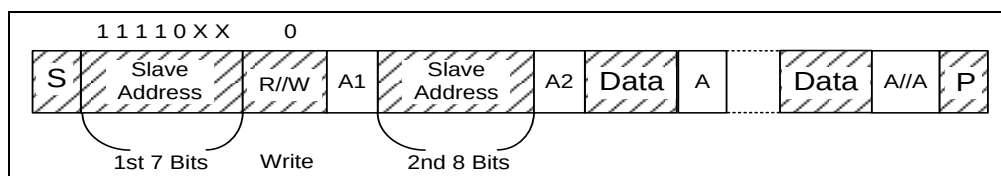


Figure 6-14a Master-Transmitter Transmits to Slave-Receiver with a 10-Bit Slave Address

■ Master-Receiver Read Slave-Transmitter with a 10-bit Slave Address

Up to, and including Acknowledge Bit A2, the procedure is the same as that described above for Master-Transmitter addressing a Slave-Receiver. After the Acknowledge (A2), a repeated START condition (Sr) takes place followed by seven bits Slave address (11110XX), but the 8th bit R/W is “1.” The addressed Slave device will then return the Acknowledge (A3). If the repeated START (Sr) condition occurs and the seven bits of first byte (11110XX) are received by Slave device, all the Slave devices will compare with their own address and check the 8th bit (R/W). However, none of the Slave devices can return an acknowledgement because R/W=1.

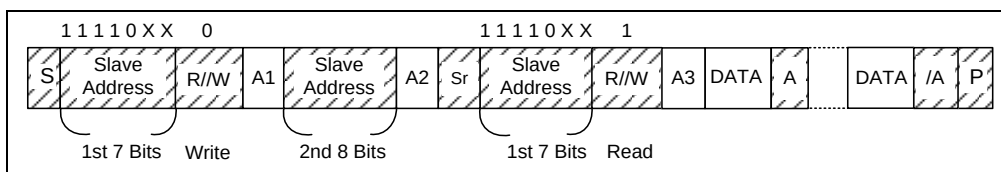


Figure 6-14b Master-Receiver reads Slave-Transmitter with a 10-Bit Slave Address

■ Master Transmits and Receives Data to and from the Same Slave Device with 10-Bit Addresses

The initial operation of this data transfer format is the same as explained in the above paragraph on “Master-Transmitter transmits to Slave-Receiver with a 10-bit Slave Address.” Then the Master device starts to transmit the data to the Slave device. When the Slave device receives the Acknowledge or None-Acknowledge that is followed by repeat START (Sr), the above operation under “Master-Receiver Reads Slave-Transmitter with a 10-Bit Slave Address” is repeatedly performed.

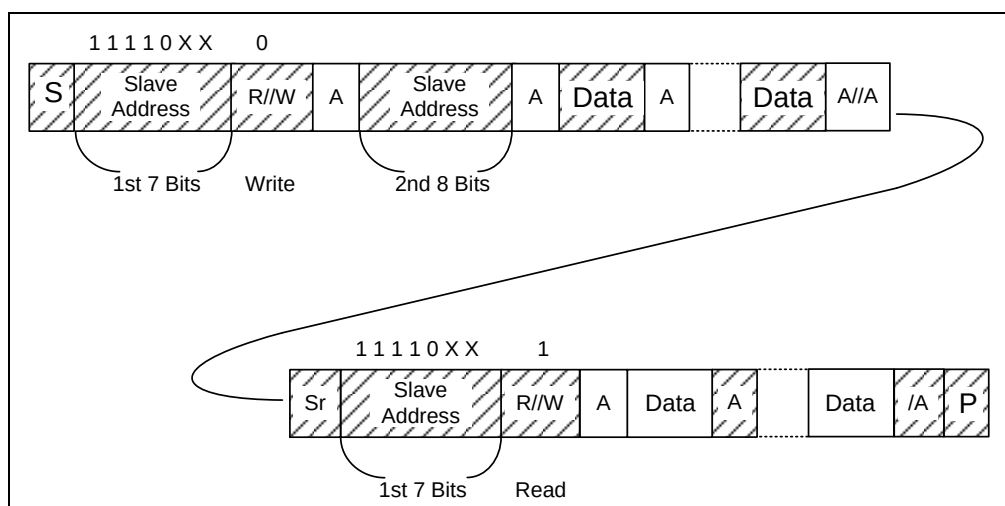


Figure 6-14c Master Addresses a Slave with 10-Bit Addresses Transmits and Receives Data with the Same Slave Device

■ Master Device Transmits Data to Two or More Slave Devices with 10 & 7 Bits Slave Address

For 10-bit address, the initial operation of this data transfer format is the same as explained in the above paragraph on “Master-Transmitter transmits to Slave-Receiver with a 10-bit Slave Address,” which describes how to transmit data to Slave device. After the Master device completes the initial transmittal, and wants to continue transmitting data to another device, the Master needs to address each of the new Slave devices by repeating the initial operation mentioned above. If the Master device wants to transmit the data in 7-bit and 10-bit Slave address modes successively, this could be done after the Start or repeat Start conditions as illustrated in the following figures.

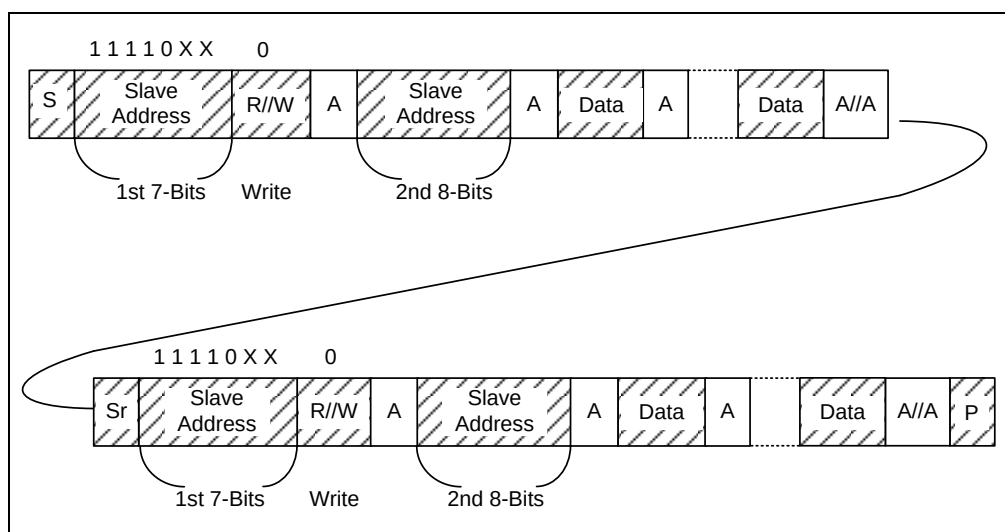


Figure 6-14d Master Transmitting to More than One Slave Devices with 10-Bit Slave Address

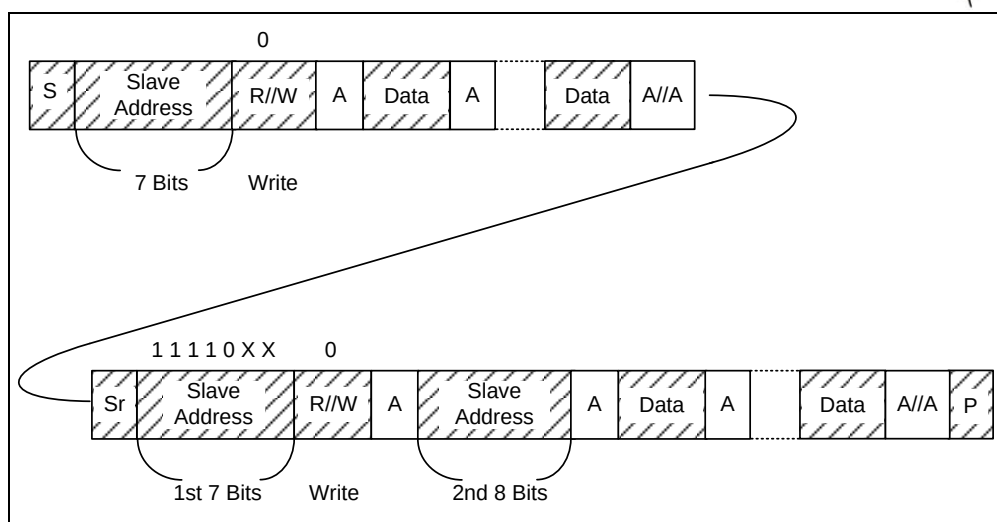


Figure 6-14e Master Successively Transmitting to 7-Bit and 10-Bit Slave Address

6.8.3 Master Mode

In transmitting (receiving) serial data, the I²C is carried on as follows:

- 1) Set I2CTS1~0, I2CCS, and ISS bits to select I²C transmit clock source.
- 2) Set I2CEN and IMS bits to enable THE I²C Master function.
- 3) Write Slave address into the I2CSA register and IRW bit to select read or write.
- 4) Set strobe bit to start transmitting and then check I2CTS_F (I2CRSF) bit.
- 5) Write 1st data into the I2CDB register, set strobe bit, and check I2CTS_F (I2CRSF) bit.
- 6) Write 2nd data into the I2CDB register, set strobe bit, STOP bit, and check I2CTS_F (I2CRSF) bit.

6.8.4 Slave Mode I2C Transmit

In receiving (transmitting) serial data, the I²C is carried on as follows:

- 1) Set I2CTS1~0, I2CCS, and ISS bits to select I²C transmit clock source.
- 2) Set I2CEN and IMS bits to enable I²C Slave function.
- 3) Write device address into the I2CDA register.
- 4) Check I2CRSF (I2CTS_F) bit, read I2CDB register (address), and then clear the Pend bit.
- 5) Check I2CRSF (I2CTS_F) bit, read I2CDB register (1st data), and then clear the Pend bit.
- 6) Check I2CRSF (I2CTS_F) bit, read I2CDB register (2nd data), and then clear the Pend bit.
- 7) Check the I2CSTPSF bit, end transmission.

6.9 Oscillator

6.9.1 Oscillator Modes

The eKTF5832 can be operated in the one oscillator mode, i.e., Internal RC oscillator mode (IRC). You need to set the main-oscillator modes by selecting the OSC0, and set sub-oscillator modes by selecting the FSS in the Code Option register to complete the overall oscillator mode setting.

■ Main-Oscillator Modes Defined By OSC0

Main-Oscillator Mode	OSC0
IRC (Internal RC oscillator mode; default) RCOUT (P74) acts as I/O pin	1
IRC (Internal RC oscillator mode) RCOUT (P74) acts as clock output pin	0

■ Summary of Maximum Operating Speeds

Conditions	VDD	Fxt Max. (MHz)
Two cycles with two clocks	2.4	4.0
	3	8.0
	4	12.0
	5	16.0

6.9.2 Internal RC Oscillator Mode

The eKTF5832 offers a versatile internal RC mode with default frequency value of 4 MHz. The Internal RC oscillator mode has other frequencies (16 MHz, 12 MHz, 8 MHz, 6 MHz, and 1 MHz) that can be set by Code Option; RCM2~RCM0. The Table below describes a typical drift rate of the calibration.

■ Internal RC Drift Rate (Ta=25°C, VDD=3.6V±5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~+85°C)	Voltage (2.8V~5.5V)	Process	Total
1MHz	±2%	±1%	±1%	±4%
4MHz	±2%	±1%	±1%	±4%
6MHz	±2%	±1%	±1%	±4%
8MHz	±2%	±1%	±1%	±4%
12MHz	±2%	±1%	±1%	±4%
16MHz	±2%	±1%	±1%	±4%

Note: These are theoretical values intended for reference only. Actual values may vary depending on actual conditions.

6.10 Power-On Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply reaches its steady state. The eKTF5832 is equipped with a Power-on Voltage Detector (POVD) with a detection level of 2.2V. It will work well if V_{DD} rises fast enough (50 ms or less). However, in critical applications, extra devices are still required to assist in solving power-up problems.

6.11 External Power-on Reset Circuit

The circuit diagram in Figure 6-15 implements an external RC to generate the reset pulse. The pulse width (time constant) should be kept long enough for V_{DD} to reach minimum operational voltage. Apply this circuit when the power supply has slow rise time. Since the current leakage from the /RESET pin is about $\pm 5 \mu\text{A}$, it is recommended that R should not be greater than 40K Ω in order for the /RESET pin voltage to remain at below 0.2V. The diode (D) functions as a short circuit at the instant of power down. The capacitor (C) will discharge rapidly and fully. The current-limited resistor (R_{in}) will prevent high current or ESD (electrostatic discharge) from flowing into /RESET pin.

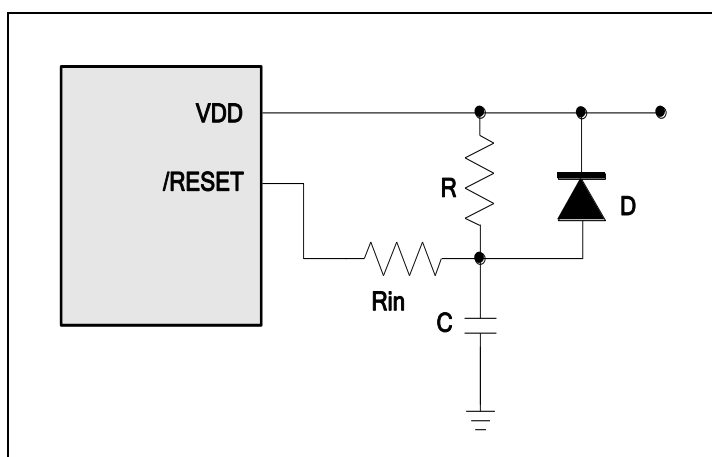


Figure 6-15 External Power-Up Reset Circuit

6.12 Residue-Voltage Protection

When the battery is replaced, device power (V_{DD}) is taken off but residue-voltage remains. The residue-voltage may trip below V_{DD} minimum, but not to zero. This condition may cause a poor power-on reset. Figures 6-16a and 6-16b show how to accomplish a proper residue-voltage protection circuit.

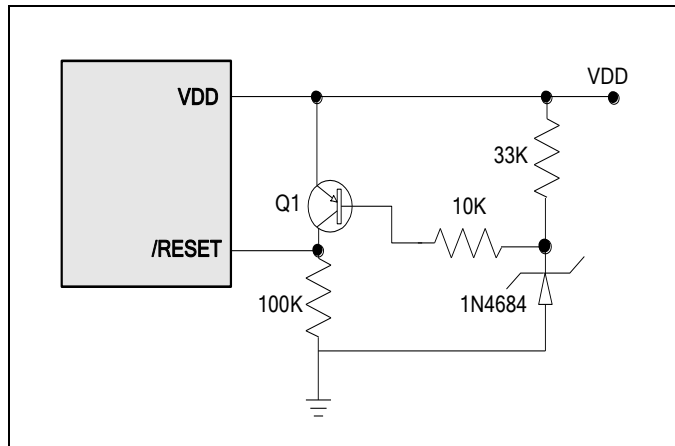


Figure 6-16a Circuit 1 for Residue Voltage Protection

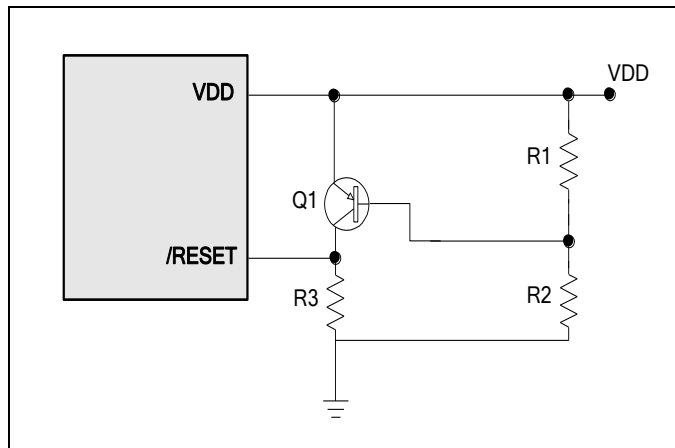


Figure 6-16b Circuit 2 for Residue Voltage Protection

6.13 Code Option

6.13.1 Code Option Register (Word 0)

Word 0								
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Mnemonic	-	-	IRCWUT	-	-	HLFS	HLP	LVR1
1	High	High	32 clks	High	High	Green	Low	High
0	Low	Low	8 clks	Low	Low	Normal	High	Low
Default	0	0	0	1	0	0	0	0
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	LVR0	RESETEN	ENWDT	NRHL	NRE	-	-	-
1	High	/RST	Enable	8/fc	Disable	High	High	High
0	Low	P72	Disable	32/fc	Enable	Low	Low	Low
Default	0	0	0	0	0	0	0	0

Bits 15~14, 11: Not used, set to "0" all the time.

Bit 13 (IRCWUT): IRC Warm Up time (Support IRC Frequency 1 MHz~8 MHz)

1: 32 clocks

0: 8 clocks (default)

CPU mode switch	IRC Frequency	Waiting time before CPU starting to work
Sleep → Normal Idle → Normal Green → Normal	12M, 16M	WSTO + 32 clocks (main frequency)
	1M, 4M, 6M, 8M	WSTO + 8/32 clocks (main frequency)
Sleep → Green Idle → Green	32kHz	WSTO + 8 clocks (sub frequency)

Bits 12: Not used, set to "1" all the time.

Bit 10 (HLFS): Reset to Normal or Green Mode Select Bit

1: CPU is selected as Green mode when a reset occurs.

0: CPU is selected as Normal mode when a reset occurs (default)

Bit 9 (HLP): Power Consumption Selection

1: Low power consumption, apply to working frequency at 4 MHz or below

0: High power consumption, apply to working frequency above 4 MHz

Bits 8~7 (LVR1~LVR0): Low voltage reset enable bit.

LVR1, LVR0	*VDD Reset Level	VDD Release Level
00	NA (Power on reset) (default)	
01	2.4V	2.6V
10	2.8V	3.0V
11	3.5V	3.7V

Note *: If VDD < 2.4V and keep about 5μs, IC will be reset.

If VDD < 2.8V and keep about 5μs, IC will be reset.

If VDD < 3.5V and keep about 5μs, IC will be reset.

Bit 6 (RESETEN): P72//RESET pin selection bit

- 1:** Enable, /RESET pin.
- 0:** Disable, P72 pin (default)

Bit 5 (ENWDT): WDT enable bit

- 1:** Enable
- 0:** Disable (default)

Bit 4 (NRHL): noise rejection high/low pulse defined bit.

- 1:** pulses equal to 8/fc [s] is regarded as signal
- 0:** pulses equal to 32/fc [s] is regarded as signal (default)

Bit 3 (NRE): noise rejection enable bit

- 1:** Disable.
- 0:** Enable (default) **In Green, Idle, and Sleep modes the noise rejection circuit is always disabled.**

Bits 2~0: Not used, set to "0" all the time.

6.13.2 Code Option Register (Word 1)

Word 1								
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Mnemonic	-	-	FSS					
1	High	High	32K	High	High	High	High	High
0	Low	Low	16K	Low	Low	Low	Low	Low
Default	0	0	0	0	0	0	0	0
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	-	RCM2	RCM1	RCM0			OSC0	RCOUT
1	High	High	High	High	High	High	High	High
0	Low	Low	Low	Low	Low	Low	Low	Low
Default	0	0	1	1	0	0	0	0

Bits 15~14: Not used, set to "0" all the time.

Bits 13 (FSS): Sub-oscillator mode selection bits

- 1:** Fs is 32kHz
- 0:** Fs is 16kHz

Note: WDT frequency is always 16kHz whatever the FSS bits are set.

Bits 12~7: Not used, set to "0" all the time.

Bits 6~4 (RCM2~RCM0): IRC frequency selection.

* Corresponding with control register Bank0 RE RCM2~RCM0

RCM2	RCM1	RCM0	Frequency (MHz)
0	0	0	4
0	0	1	1
0	1	0	6
0	1	1	8 (default)
1	0	0	12
1	0	1	16

Bits 3~2: Not used, set to "0" all the time.

Bit 1 (OSC0): Main-oscillator mode selection bits.

Main-Oscillator Mode	OSC0
IRC (Internal RC oscillator mode) (default) RCOUT (P74) acts as I/O pin	0
IRC (Internal RC oscillator mode) RCOUT (P74) acts as clock output pin	1

Bit 0 (RCOUT): System Clock Output Enable Bit in IRC mode

1: OSCO pin is open drain

0: OSCO output instruction cycle time (default)

6.13.3 Code Option Register (Word 2)

Word 2								
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Mnemonic	-	SHEN	SHCLK1	SHCLK0	BOREN	BORT2	BORT1	BORT0
1	High	Disable	High	High	Disable	High	High	High
0	Low	Enable	Low	Low	Enable	Low	Low	Low
Default	0	0	0	0	1	0	0	0
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	-	-	-	I2COPT	TPPSB	TPECS	-	-
1	High	High	High	High	VDD	Internal	High	High
0	Low	Low	Low	Low	LDO	External	Low	Low
Default	0	0	0	0	0	0	1	1

Bit 15: Not used, set to "0" all the time.

Bit 14 (SHEN): System hold enable bit.

1: Disable

0: Enable

Bits 13~12 (SHCLK1~SHCLK0): System hold clock selection bits (extra 32kHz source)

SHCLK1~0	System Hold Clock
00	4 clocks (default)
01	2 clocks
10	8 clocks
11	16 clocks

Bit 11 (BOREN): BOR Enable bit

1: BOR Disable (default)

0: BOR Enable

Bits 10~8 (BORT2~ BORT0)

BORT 2~0	BOR Sample Time (μ s)
000	Always On (default)
001	16000
010	8000
011	4000
100	2000
101	1000
110	500
111	250

Bit 7~5: Not used, set to "0" all the time.

Bit 4 (I2COPT): I2C pin optional bit. It is used to switch the pin position of I2C function.

1: Placed I2C pins in P73 (SDA1) and P74 (SCL1).

0: Placed I2C pins in P70 (SDA0) and P71 (SCL0) (default)

*Corresponding with control register Bank 0 R31 I2COPT

Bit 3 (TPPSB): TK power source select bit.

1: TK power source from VDD

0: TK power source from LDO (default)

Bit 2 (TPECS): TPC external capacitor select bit

1: Internal, TPC pin floating.

0: External, TPC pin connect a capacitor to GND. (default)

Bits 1~0: Not used, set to "1" all the time.

6.13.4 Code Option Register (Word 3)

Word 3								
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Mnemonic	-	-	-	-	-	-	-	-
1	High	High	High	High	High	High	High	High
0	Low	Low	Low	Low	Low	Low	Low	Low
Default	0	0	0	0	0	0	0	0
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	-	-	ID5	ID4	ID3	ID2	ID1	ID0
1	High	High	Customer ID					
0	Low	Low						
Default	0	1						

Bits 15~7: Not used, set to "0" all the time

Bit 6: Not used, set to "1" all the time

Bits 5~0 (ID5~ID0): Customer's ID Code

6.14 Instruction Set

Each instruction in the instruction set is a 15-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2, A", "ADD R2, A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2, A", "BS(C) R2, 6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

- "LCALL", "LJMP", "JMP", "CALL", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Moreover, the instruction set has the following features:

- 1) Every bit of any register can be directly set, cleared, or tested.
- 2) The I/O register can be considered as general register. That is; the same instruction can operate on I/O register.

■ Instruction Set Table:

In the following Instruction Set table, the following symbols are used:

"R" represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction.

"b" represents a bit field designator that selects the value for the bit which is located in the register "R", and affects operation.

"k" represents an 8 or 10-bit constant or literal value.

Mnemonic	Operation	Status Affected
NOP	No Operation	None
DAA	Decimal Adjust A	C
SLEP	0 → WDT, Stop oscillator	T,P
WDTC	0 → WDT	T,P
ENI	Enable Interrupt	None
DISI	Disable Interrupt	None
RET	[Top of Stack] → PC	None
RETI	[Top of Stack] → PC, Enable Interrupt	None
RESET	Software Device Reset	ALL Registers = Reset Value Flags* = Reset Value
TBWR	Table Writer Start instruction	None
INT k	PC+1 → [SP], k*2 → PC	None
BTG R,b	Bit Toggle R ; /(R)->R *Range R5~RA	None
MOV R,A	A → R	None
CLRA	0 → A	Z
CLR R	0 → R	Z
SUB A,R	R-A → A	Z,C,DC,OV,N
SUB R,A	R-A → R	Z,C,DC,OV,N
DECA R	R-1 → A	Z,C,DC,OV,N
DEC R	R-1 → R	Z,C,DC,OV,N
OR A,R	A ∨ R → A	Z,N
OR R,A	A ∨ R → R	Z,N
AND A,R	A & R → A	Z,N
AND R,A	A & R → R	Z,N
XOR A,R	A ⊕ R → A	Z,N
XOR R,A	A ⊕ R → R	Z,N
ADD A,R	A + R → A	Z,C,DC,OV,N
ADD R,A	A + R → R	Z,C,DC,OV,N

Mnemonic	Operation	Status Affected
MOV A,R	$R \rightarrow A$	Z
MOV R,R	$R \rightarrow R$	Z
COMA R	$/R \rightarrow A$	Z,N
COM R	$/R \rightarrow R$	Z,N
INCA R	$R+1 \rightarrow A$	Z,C,DC,OV,N
INC R	$R+1 \rightarrow R$	Z,C,DC,OV,N
DJZA R	$R-1 \rightarrow A$, skip if zero	None
DJZ R	$R-1 \rightarrow R$, skip if zero	None
RRCA R	$R(n) \rightarrow A(n-1)$, $R(0) \rightarrow C$, $C \rightarrow A(7)$	C, N
RRC R	$R(n) \rightarrow R(n-1)$, $R(0) \rightarrow C$, $C \rightarrow R(7)$	C, N
RLCA R	$R(n) \rightarrow A(n+1)$, $R(7) \rightarrow C$, $C \rightarrow A(0)$	C, N
RLC R	$R(n) \rightarrow R(n+1)$, $R(7) \rightarrow C$, $C \rightarrow R(0)$	C,N
SWAPA R	$R(0-3) \rightarrow A(4-7)$, $R(4-7) \rightarrow A(0-3)$	None
SWAP R	$R(0-3) \leftrightarrow R(4-7)$	None
JZA R	$R+1 \rightarrow A$, skip if zero	None
JZ R	$R+1 \rightarrow R$, skip if zero	None
BC R,b	$0 \rightarrow R(b)$	None <Note2>
BS R,b	$1 \rightarrow R(b)$	None <Note3>
JBC R,b	if $R(b)=0$, skip	None
JBS R,b	if $R(b)=1$, skip	None
CALL k	$PC+1 \rightarrow [SP]$, (Page, k) $\rightarrow PC$	None
JMP k	(Page, k) $\rightarrow PC$	None
MOV A,k	$k \rightarrow A$	None
JE R	Compare R with ACC, Skip =	None
JGE R	Compare R with ACC, Skip >	None
JLE R	Compare R with ACC Skip <	None
OR A,k	$A \vee k \rightarrow A$	Z,N
JE k	Compare K with ACC, Skip =	None
TBRDA R	$ROM[(TABPTR)] \rightarrow R$, A $A \leftarrow$ program code (low byte) ; $R \leftarrow$ program code (high byte)	None
AND A,k	$A \& k \rightarrow A$	Z,N

Mnemonic	Operation	Status Affected
SJC k	Short jump to K if Carry if C=1 PC+1+offset → PC *offset = -128 ≤ k ≤ 127	None
SJNC k	Short jump to K if Not Carry if C=0 PC+1+offset → PC *offset = -128 ≤ k ≤ 127	None
SJZ k	Short jump to K if Zero if Z=1 PC+1+offset → PC *offset = -128 ≤ k ≤ 127	None
XOR A,k	$A \oplus k \rightarrow A$	Z,N
SJNZ k	Short jump to K if Not Zero if Z=0 PC+1+offset → PC *offset = -128 ≤ k ≤ 127	None
RRA R	$R(n) \rightarrow A(n-1), R(0) \rightarrow A(7)$	N
RR R	$R(n) \rightarrow R(n-1), R(0) \rightarrow R(7)$	N
RETL k	$k \rightarrow A,$ $[Top\ of\ Stack] \rightarrow PC$	None
XCH R	$R \longleftrightarrow A$	None
RLA R	$R(n) \rightarrow A(n+1), R(7) \rightarrow A(0)$	N
RL R	$R(n) \rightarrow R(n+1), R(7) \rightarrow R(0)$	N
SUB A,k	$k-A \rightarrow A$	Z,C,DC,OV,N
SUBB A,R	$R-A-/C \rightarrow A$	Z, C, DC, OV, N
SUBB R,A	$R-A-/C \rightarrow R$	Z, C, DC, OV, N
SBANK k	$K \rightarrow R1(4)$	None
GBANK k	$K \rightarrow R1(3:0)$	None
LCALL k	Next instruction : k kkkk kkkk kkkk $PC+1 \rightarrow [SP], k \rightarrow PC$	None
LJMP k	Next instruction : k kkkk kkkk kkkk $K \rightarrow PC$	None
TBRD R	$ROM[(TABPTR)] \rightarrow R$	None
ADD A,k	$k+A \rightarrow A$	Z,C,DC,OV,N
NEG R	2's complement, $/R +1 \rightarrow R$	Z,C,DC,OV,N
ADC A,R	$A+R+C \rightarrow A$	Z,C,DC,OV,N
ADC R,A	$A+R+C \rightarrow R$	Z,C,DC,OV,N

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	V _{SS} -0.3V	to	V _{DD} +0.3V
Output voltage	V _{SS} -0.3V	to	V _{DD} +0.3V
Working Voltage	2.0V	to	5.5V
Working Frequency	DC	to	16 MHz

8 DC Electrical Characteristics

(Ta=25 °C, V_{DD}=5.0V±5%, V_{SS}=0V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Fxt	IRC: VDD to 5 V	1 MHz, 6 MHz, 8 MHz, 12 MHz, 16 MHz, 4 MHz		F		Hz
IRCE	Internal RC oscillator error per stage			±1		%
IRC1	IRC:VDD to 5V	RCM2~RCM1=000		4		MHz
IRC2	IRC:VDD to 5V	RCM2~RCM1=001		1		MHz
IRC3	IRC:VDD to 5V	RCM2~RCM1=010		6		MHz
IRC4	IRC:VDD to 5V	RCM2~RCM1=011		8		MHz
IRC5	IRC:VDD to 5V	RCM2~RCM1=100		12		MHz
IRC6	IRC:VDD to 5V	RCM2~RCM1=101		16		MHz
IIL	Input Leakage Current for input pins	V _{IN} = V _{DD} , V _{SS}	-1	0	1	μA
VIH1	Input High Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	0.56 IO_VDD		IO_VDD +0.3V	V
VIL1	Input Low Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	-0.3V		0.44 IO_VDD	V
VIHT1	Input High Threshold Voltage (Schmitt trigger)	/RESET	0.56 IO_VDD		IO_VDD +0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-0.3V		0.44 IO_VDD	V
VIHT2	Input High Threshold Voltage (Schmitt trigger)	TCC,INT	0.56 IO_VDD		IO_VDD +0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt trigger)	TCC,INT	-0.3V		0.44 IO_VDD	V
IOH1	Output High Voltage (Port 72)	VOH = IO_VDD-0.1IO_VDD	-2.5			mA
IOH2	Output High Voltage (Ports 5, 6, 7, 8)	VOH = IO_VDD-0.1IO_VDD	-3			mA
IOH2	Output High Voltage (high drive) (Ports 5, 6, 7, 8)	VOH = IO_VDD-0.1IO_VDD	11			mA
IOL1	Output Low Voltage (Port 72)	VOL = GND+0.1IO_VDD	12			mA
IOL2	Output Low Voltage (Ports 5, 6, 7, 8)	VOL = GND+0.1IO_VDD	14			mA
IOL2	Output Low Voltage (high sink) (Ports 5, 6, 7, 8)	VOL = GND+0.1IO_VDD	30			mA
IPH	Pull-high current	Pull-high active, input pin at V _{SS}		-80		μA
IPL	Pull-low current	Pull-low active, input pin at IO_VDD		30		μA
ISB1	Power down current	/RESET= 'High', Fm & Fs off		2		μA

	(Sleep mode)	All input and I/O pins at VDD, output pin floating, WDT disabled				
ISB2	Power down current (Sleep mode)	/RESET= 'High', Fm & Fs off All input and I/O pins at VDD, output pin floating, WDT enabled		4		μA
ISB3	Power down current (Idle mode)	/RESET= 'High', Fm off, Fs=32K/16KHz (IRC type) output pin floating, WDT disabled,		4		μA
ISB4	Power down current (Idle mode)	/RESET= 'High', Fm off, Fs=32K/16KHz (IRC type), output pin floating, WDT enabled		4		μA
ICC1	Operating supply current (Green mode)	/RESET= 'High', Fm off, Fs=32K/16KHz (IRC type), output pin floating, WDT disabled		30		μA
ICC2	Operating supply current (Green mode)	/RESET= 'High', Fm off, Fs=32K/16KHz (IRC type), output pin floating, WDT enabled		30		μA
ICC4	Operating supply current (Normal mode)	/RESET= 'High', Fm=1MHz, Fs on, output pin floating, WDT enabled		500		μA

NOTE

- The above parameters are theoretical values only and have not been tested or verified.
- Data under the "Min.", "Typ.", and "Max." columns are based on theoretical results at 25°C. These data are for design reference only and have not been tested or verified.

9 AC Electrical Characteristics

■ (eKTF5832 $-40 \leq T_a \leq 85^\circ\text{C}$, $V_{DD}=5.5\text{V}$, $V_{SS}=0\text{V}$)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	-	45	50	55	%
Tins	Instruction cycle time	RC type	500	-	DC	ns
Ttcc	TCC input period	-	$(T_{ins}+20)/N^*$	-	-	ns
Tdrh	Device reset hold time	-	11.3	16.2	21.6	ms
Trst	/RESET pulse width	$T_a = 25^\circ\text{C}$	2000	-	-	ns
Twtd	Watchdog timer period	$T_a = 25^\circ\text{C}$	11.3	16.2	21.6	ms
Tset	Input pin setup time	-	-	0		ns
Thold	Input pin hold time	-	15	20	25	ns
Tdelay	Output pin delay time	Cload=20pF	45	50	55	ns

* N : Selected prescaler ratio

NOTE

- The above parameters are theoretical values only and have not been tested or verified.
- Data under the "Min.", "Typ.", and "Max." columns are based on theoretical results at 25°C . These data are for design reference only and have not been tested or verified.

APPENDIX

A Package Type

MCU	Package Type	Pin Count	Package Size
eKTF5832QN32	QFN	32 pins	5x5x0.8 mm
eKTF5832QN24	QFN	24 pins	4x4x0.8 mm
eKTF5832SO28	SOP	28 pins	300 mil
eKTF5832SS28	SSOP	28 pins	209mil
eKTF5832SO24	SOP	24 pins	300 mil

These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

The Pb contents are less 100ppm and comply with Sony specifications.

Part No.	eKTF5832 S/J
Electroplate type	Pure Tin
Ingredient (%)	Sn: 100%
Melting point(°C)	232°C
Electrical resistivity ($\mu\Omega$ -cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

B Package Information

B.1 eKTF5832QN32

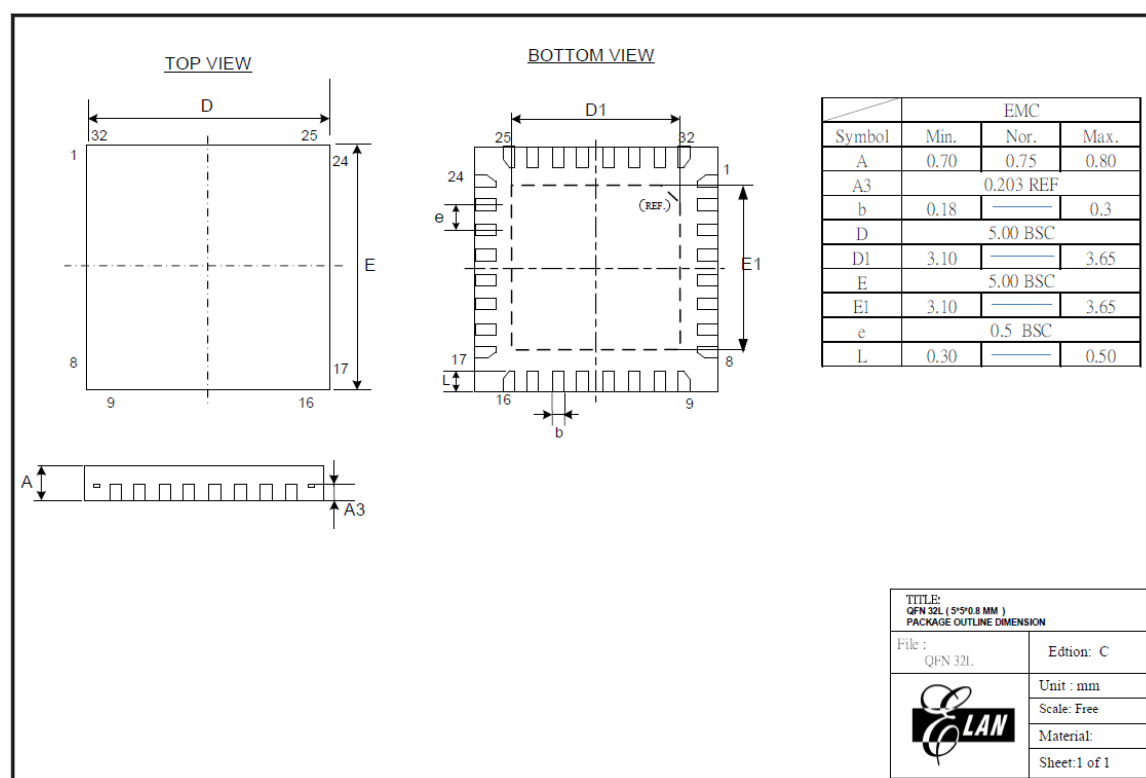


Figure B-1 eKTF5832 32-pin QFN Package Type

B.2 eKTF5832QN24

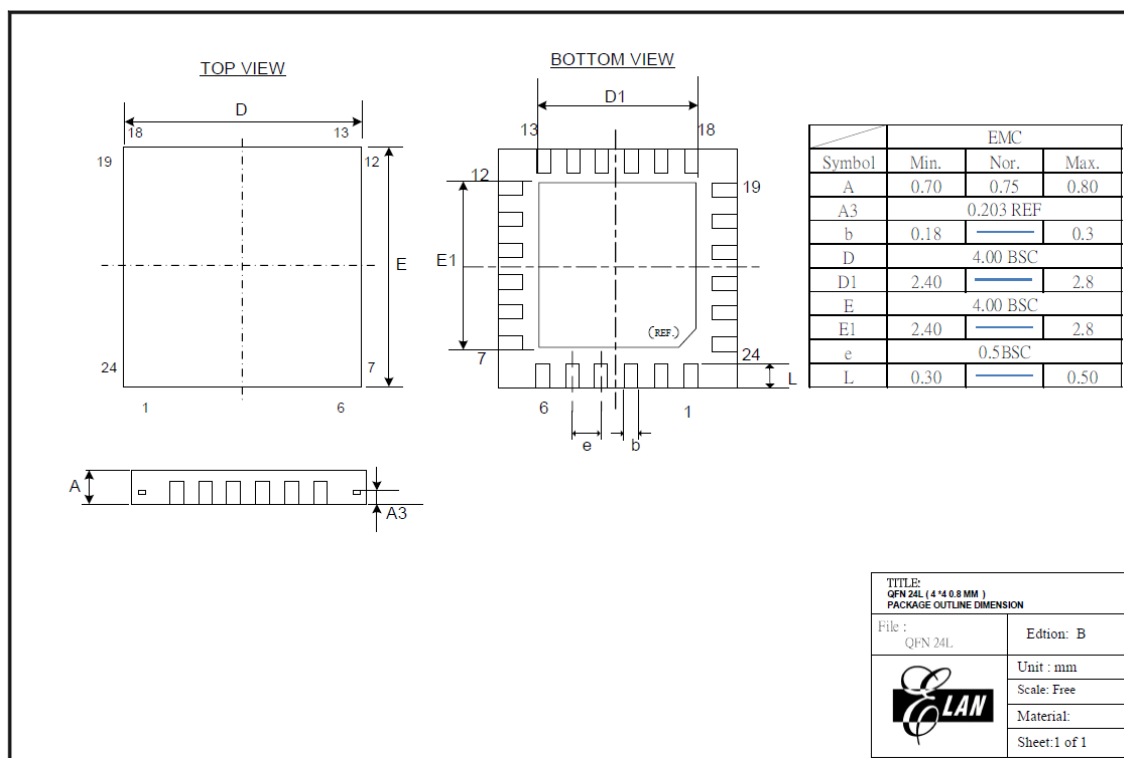


Figure B-2 eKTF5832 24-pin QFN Package Type

B.3 eKTF5832SO28

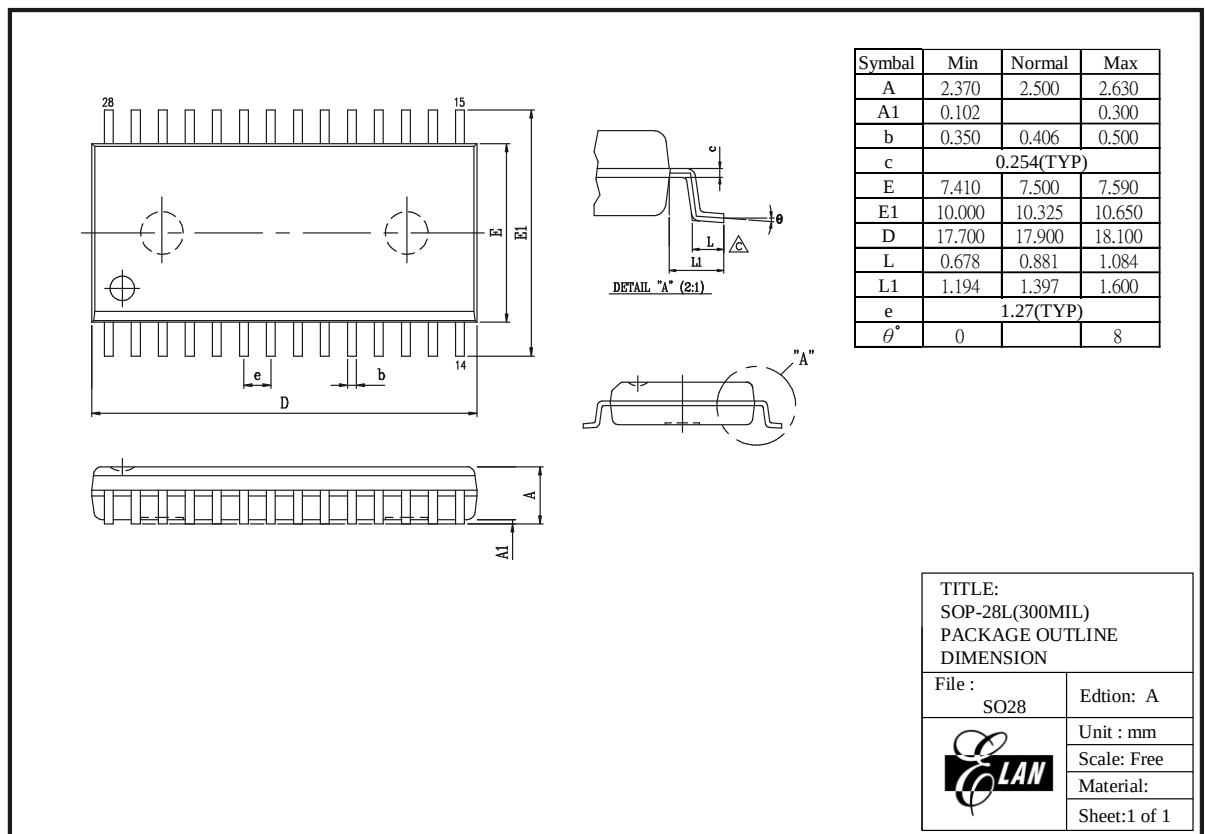


Figure B-3 eKTF5832 28-pin SOP Package Type

B.4 eKTF5832SS28

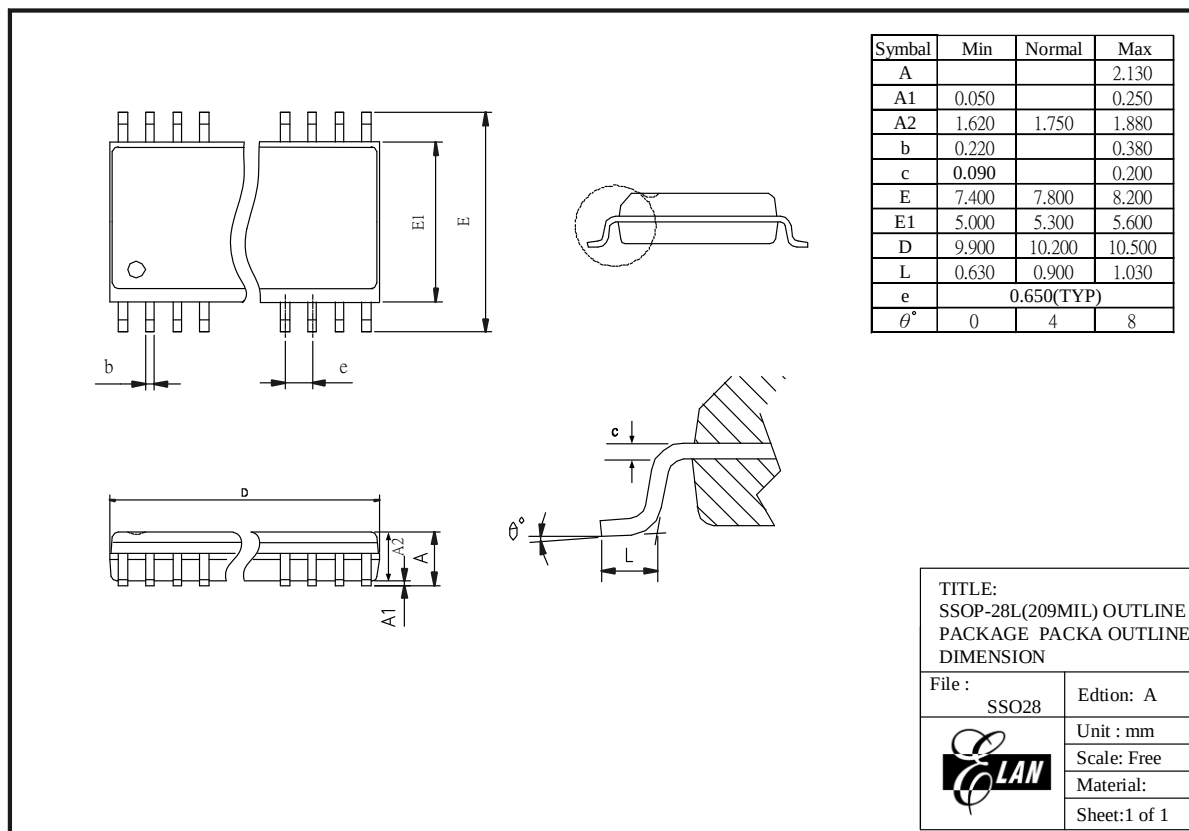


Figure B-3 eKTF5832 28-pin SSOP Package Type

B.5 eKTF5832SO24

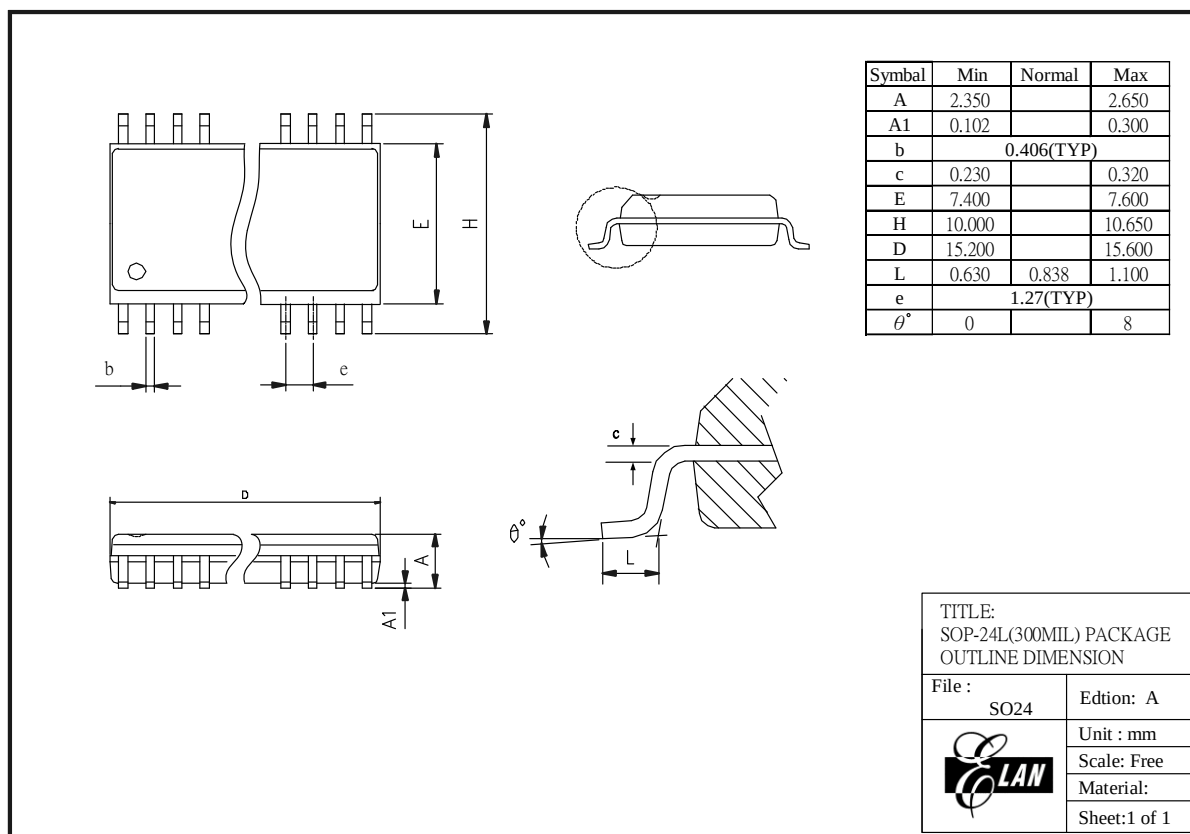
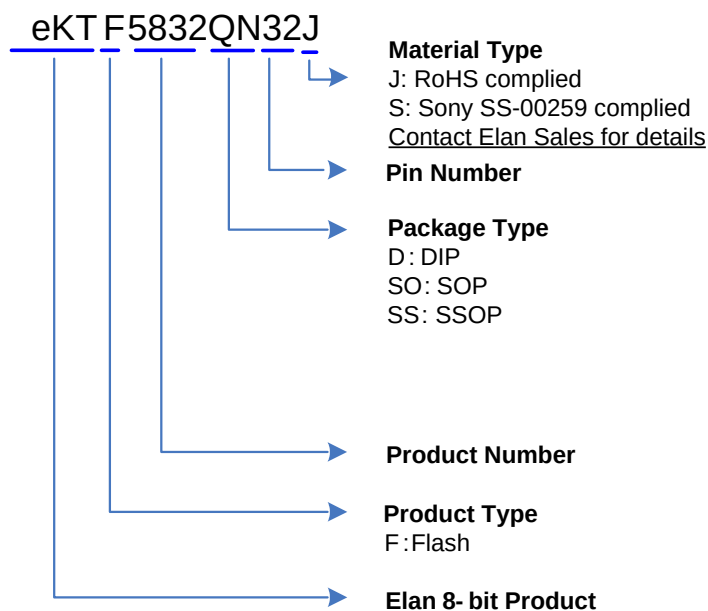


Figure B-3 eKTF5832 24-pin SOP Package Type

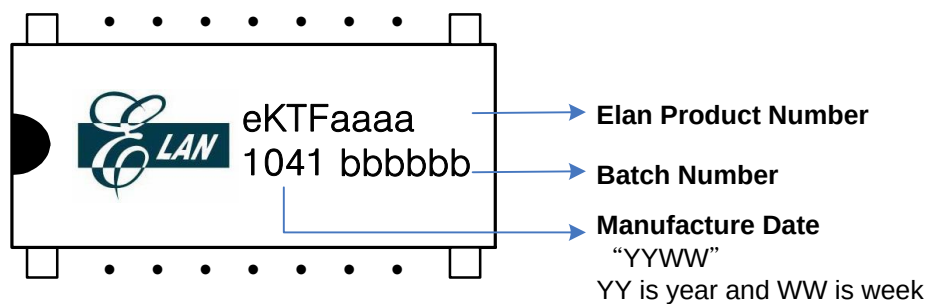
C Ordering and Manufacturing Information



For example

eKTF5832QN32J

is eKTF5832 with Flash program memory , in 32-pin QFN package



Ordering Code

KTF5832QN32J

