PCI-Express Clock Generator IC, PLL Core, Dividers, Two Outputs

AD9573

FEATURES

- **Fully integrated VCO/PLL core**
  - **0.54 ps rms jitter from 12 kHz to 20 MHz**
  - **Input crystal frequency of 25 MHz**
- **Preset divide ratios for 100 MHz, 33.33 MHz**
- **LVDS/LVCMOS output format**
- **Integrated loop filter**
- **Space saving 4.4 mm × 5.0 mm TSSOP**
- **0.235 W power dissipation**
- **3.3 V operation**

APPLICATIONS

- **Line cards, switches, and routers**
- **CPU/PCIe applications**
- **Low jitter, low phase noise clock generation**

GENERAL DESCRIPTION

The AD9573 provides a highly integrated, dual output clock generator function including an on-chip PLL core that is optimized for PCI-e applications. The integer-N PLL design is based on the Analog Devices, Inc., proven portfolio of high performance, low jitter frequency synthesizers to maximize line card performance. Other applications with demanding phase noise and jitter requirements also benefit from this part.

The PLL section consists of a low noise phase frequency detector (PFD), a precision charge pump, a low phase noise voltage controlled oscillator (VCO), and a preprogrammed feedback divider and output divider.

By connecting an external 25 MHz crystal, output frequencies of 100 MHz and 33.33 MHz can be locked to the input reference. The output divider and feedback divider ratios are preprogrammed for the required output rates. No external loop filter components are required, thus conserving valuable design time and board space.

The AD9573 is available in a 16-lead 4.4 mm × 5.0 mm TSSOP and can be operated from a single 3.3 V supply. The temperature range is −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

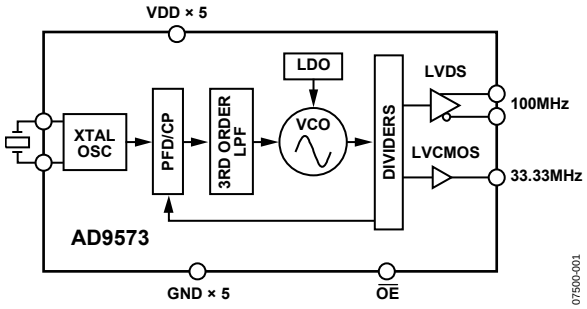


Figure 1.

Rev. 0

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REVISION HISTORY

7/09—Revision 0: Initial Version

SPECIFICATIONS

Typical (typ) is given for V_{DD} = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum (min) and maximum (max) values are given over full V_{DD} and T_A (−40°C to +85°C) variation.

PLL CHARACTERISTICS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
NOISE CHARACTERISTICS					
PLL Noise (100 MHz Output)					
@ 1 kHz		−121		dBc/Hz	
@ 10 kHz		−128		dBc/Hz	
@ 100 kHz		−131		dBc/Hz	
@ 1 MHz		−144		dBc/Hz	
@ 10 MHz		−150		dBc/Hz	
@ 30 MHz		−151		dBc/Hz	
PLL Noise (33.33 MHz Output)					
@ 1 kHz		−131		dBc/Hz	
@ 10 kHz		−137		dBc/Hz	
@ 100 kHz		−140		dBc/Hz	
@ 1 MHz		−150		dBc/Hz	
@ 5 MHz		−151		dBc/Hz	
Spurious Content		−70		dBc	
PLL Figure of Merit		−217.5		dBc/Hz	

CLOCK OUTPUT JITTER

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS OUTPUT ABSOLUTE TIME JITTER					
RMS Jitter (100 MHz Output)		540		fsec	12 kHz to 20 MHz

CLOCK OUTPUTS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS CLOCK OUTPUT					Termination = 100 Ω differential
Output Frequency			100	MHz	
Differential Output Voltage (V_{OD})	500	640	700	mV	
Delta V_{OD}			25	mV	
Output Offset Voltage (V_{OS})	1.125	1.25	1.375	V	
Delta V_{OS}			25	mV	
Short-Circuit Current (I_{SA}, I_{SB})		14	24	mA	Output shorted to GND
Duty Cycle	45		55	%	
LVCMOS CLOCK OUTPUT					
Output Frequency			33.33	MHz	
Output High Voltage (V_{OH})	V_S − 0.1			V	Sourcing 1.0 mA current
Output Low Voltage (V_{OL})			0.1	V	Sinking 1.0 mA current
Duty Cycle	45		55	%	

TIMING CHARACTERISTICS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS					Termination = 100 Ω differential; C_{LOAD} = 0 pF
Output Rise Time, t_{RL}	140	200	260	ps	20% to 80%, measured differentially
Output Fall Time, t_{FL}	140	200	260	ps	80% to 20%, measured differentially
LVCMOS					Termination = open
Output Rise Time, t_{RC}	0.25	0.60	2.5	ns	20% to 80%; C_{LOAD} = 5 pF
Output Fall Time, t_{FC}	0.25	0.80	2.5	ns	80% to 20%; C_{LOAD} = 5 pF

CONTROL PINS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT CHARACTERISTICS					
$\overline{OE}$ Pin					$\overline{OE}$ has a 50 kΩ pull-down resistor.
Logic 1 Voltage	2.5			V	
Logic 0 Voltage			0.8	V	
Logic 1 Current			120	µA	
Logic 0 Current			1.0	µA	

POWER

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Power Supply	3.0	3.3	3.6	V	
Power Dissipation		235	285	mW	

CRYSTAL OSCILLATOR

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CRYSTAL SPECIFICATION					Parallel resonant/fundamental mode
Frequency		25		MHz	
ESR			40	Ω	
Load Capacitance		18		pF	
Phase Noise		−138		dBc/Hz	@ 1 kHz offset
Stability	−30		+30	ppm	

TIMING DIAGRAMS

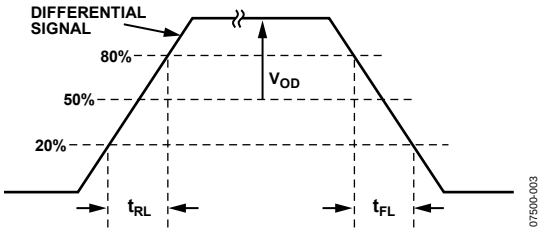


Figure 2. LVDS Timing, Differential

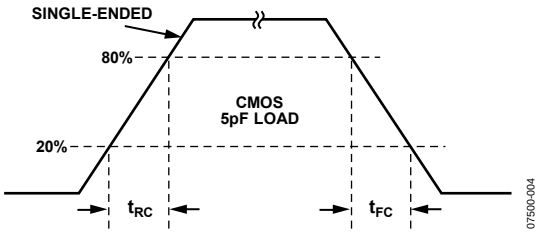


Figure 3. LVCMOS Timing

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
VDD, VDDA, VDDX, and VDD33 to GND	−0.3 V to +3.6 V
XO1, XO2 to GND	−0.3 V to V_S + 0.3 V
100M, $\overline{100M}$, 33M to GND	−0.3 V to V_S + 0.3 V
Junction Temperature[1]	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 sec)	300°C

[1] See Table 9 for θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. Thermal impedance measurements were taken on a 4-layer board in still air in accordance with EIA/JESD51-7.

Table 9. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead TSSOP	90.3	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

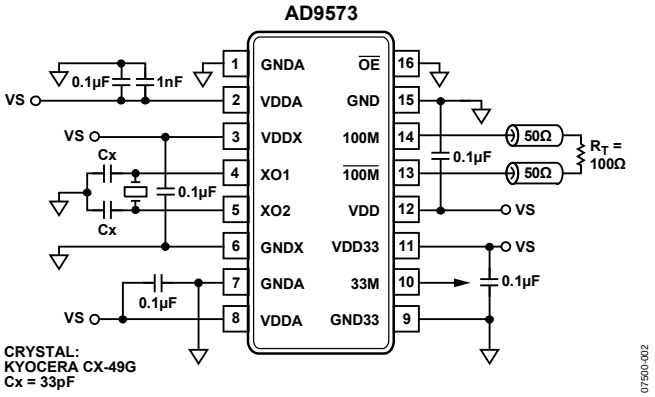


Figure 4. Typical Application

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

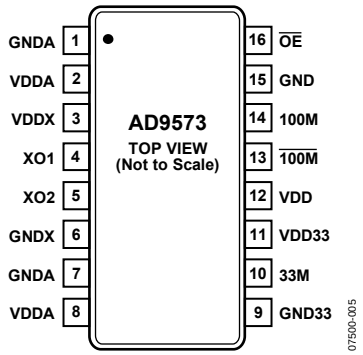


Figure 5. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 7	GNDA	Analog Ground.
2, 8	VDDA	Analog Power Supply (3.3 V).
3	VDDX	Crystal Oscillator Power Supply.
4, 5	XO1, XO2	External 25 MHz Crystal.
6	GNDX	Crystal Oscillator Ground.
9	GND33	Ground for LVCMOS Output.
10	33M	LVCMOS Output at 33.33 MHz.
11	VDD33	Power Supply for LVCMOS Output.
12	VDD	Power Supply for LVDS Output.
13	$\overline{100M}$	Complementary LVDS Output at 100 MHz.
14	100M	LVDS Output at 100 MHz.
15	GND	Ground for LVDS Output.
16	$\overline{OE}$	Output Enable (Active Low). Places both outputs in a high impedance state when high. This pin has a 50 kΩ internal pull-down resistor.

TYPICAL PERFORMANCE CHARACTERISTICS

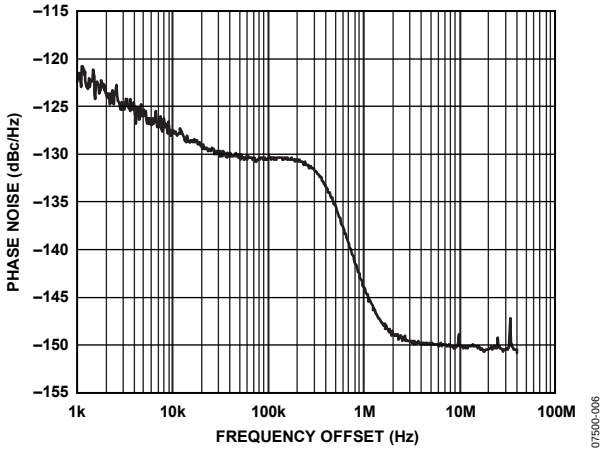


Figure 6. 100 MHz Phase Noise

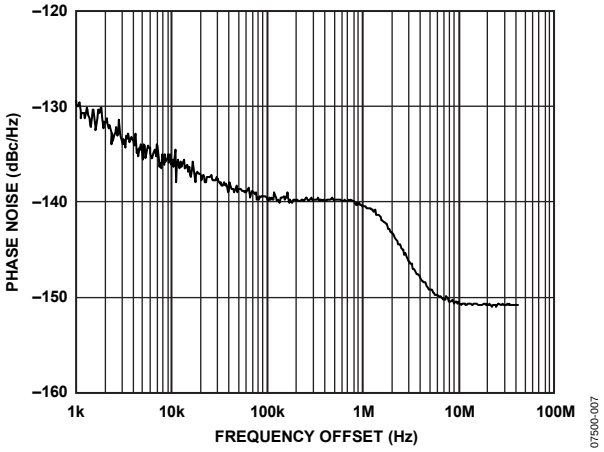


Figure 7. 33.33 MHz Phase Noise

TERMINOLOGY

Phase Jitter

An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0 degrees to 360 degrees for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is called phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as gaussian (normal) in distribution.

This phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in dB) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

Phase Noise

When the total power contained within some interval of offset frequencies (for example, 12 kHz to 20 MHz) is integrated, it is called the integrated phase noise over that frequency offset interval, and it can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on error rate performance by increasing eye closure at the transmitter output and reducing the jitter tolerance/sensitivity of the receiver.

Time Jitter

Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings is seen to vary. In a square wave, the time jitter is seen as a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in units of seconds root mean square (rms) or 1 sigma of the gaussian distribution.

Additive Phase Noise

Additive phase noise is the amount of phase noise that is attributable to the device or subsystem being measured. The phase noise of any external oscillators or clock sources has been subtracted. This makes it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise.

Additive Time Jitter

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THEORY OF OPERATION

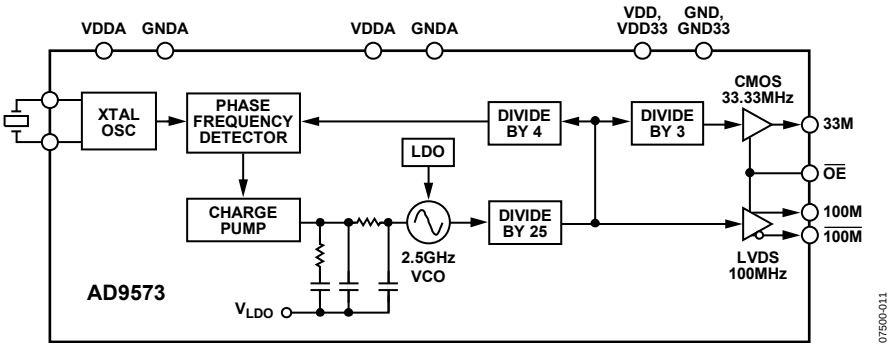


Figure 8. Detailed Block Diagram

Figure 8 shows a block diagram of the AD9573. The chip features a PLL core, which is configured to generate the specific clock frequencies required for PCI-express, without any user programming. This PLL is based on proven Analog Devices synthesizer technology, noted for its exceptional phase noise performance. The AD9573 is highly integrated and includes the loop filter, a regulator for supply noise immunity, all the necessary dividers, output buffers, and a crystal oscillator. A user need only supply a 25 MHz external crystal to implement an entire PCIe clocking solution, which does not require any processor intervention.

OUTPUTS

Table 11 provides a summary of the outputs available.

Table 11. Output Formats

Frequency	Format	Copies
100 MHz	LVDS	1
33.33 MHz	LVCMOS	1

The simplified equivalent circuit of the LVDS output is shown in Figure 9. The 100 MHz output is described as LVDS because it uses an LVDS driver topology. However, the levels are HCSL compatible, and therefore do not meet the LVDS standard. The output current has been increased to provide a larger output swing than standard LVDS.

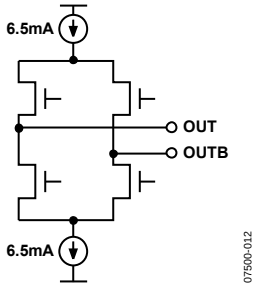


Figure 9. LVDS Output Simplified Equivalent Circuit

Both outputs can be placed in a high impedance state by connecting the $\overline{OE}$ pin according to Table 12. This pin has a 50 kΩ pull-down resistor.

Table 12. Output Enable Pin Function

$\overline{OE}$ State	Output State
0	Enabled
1	High impedance

Phase Frequency Detector (PFD) and Charge Pump

The PFD takes inputs from the reference clock and feedback divider to produce an output proportional to the phase and frequency difference between them. Figure 10 shows a simplified schematic.

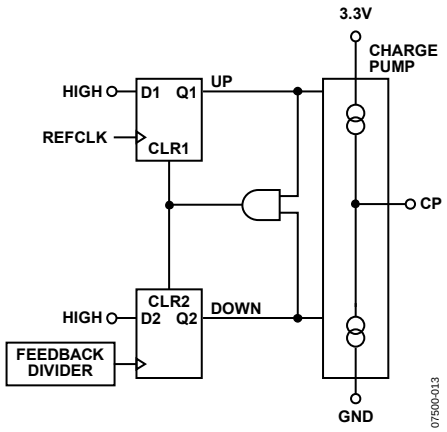


Figure 10. PFD Simplified Schematic and Timing (in Lock)

POWER SUPPLY

The AD9573 requires a 3.3 V ± 10% power supply for VDD. The tables in the Specifications section give the performance expected from the AD9573 with the power supply voltage within this range. The absolute maximum range of (−0.3 V) – (+3.6 V), with respect to GND, must never be exceeded on the VDD or VDDA pins.

Good engineering practice should be followed in the layout of power supply traces and the ground plane of the PCB. The power supply should be bypassed on the PCB with adequate capacitance (>10 µF). The AD9573 should be decoupled with adequate capacitors (0.1 µF) at all power pins as close as possible to these power pins. The layout of the AD9573

evaluation board shows a good example (see the Ordering Guide for information about the evaluation board).

LVDS CLOCK DISTRIBUTION

Low voltage differential signaling (LVDS) is the differential output for the AD9573. LVDS uses a current mode output stage with a factory programmed current level. The normal value (default) for this current is 6.5 mA, which yields a 650 mV output swing across a 100 Ω resistor.

The typical termination circuit for the LVDS outputs is shown in Figure 11.

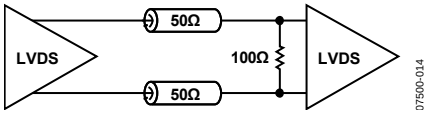


Figure 11. LVDS Output Termination

An alternative method of terminating the output to preserve output swing but also minimize reflections is shown in Figure 12.

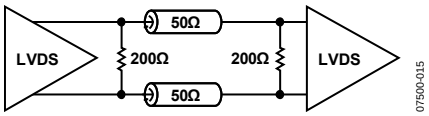


Figure 12. Alternative LVDS Output Termination

CMOS CLOCK DISTRIBUTION

The AD9573 provides a 33.33 MHz clock output, which is a dedicated CMOS level. Whenever single-ended CMOS clocking is used, some of the following general guidelines should be followed.

Point-to-point nets should be designed such that a driver has one receiver only on the net, if possible. This allows for simple termination schemes and minimizes ringing due to possible mismatched impedances on the net. Series termination at the source is generally required to provide transmission line matching and/or to reduce current transients at the driver. The value of the resistor is dependent on the board design and timing requirements (typically 10 Ω to 100 Ω is used). CMOS outputs are limited in terms of the capacitive load or trace length that they can drive. Typically, trace lengths less than 6 inches are recommended to preserve signal rise/fall times and preserve signal integrity.

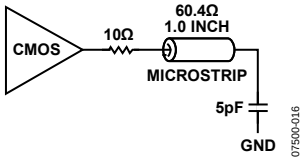


Figure 13. Series Termination of CMOS Output

Termination at the far end of the PCB trace is a second option. The CMOS output of the AD9573 does not supply enough current to provide a full voltage swing with a low impedance resistive, far end termination, as shown in Figure 14. The far end termination network should match the PCB trace impedance and provide the desired switching point.

The reduced signal swing may still meet receiver input requirements in some applications. This can be useful when driving long trace lengths on less critical nets.

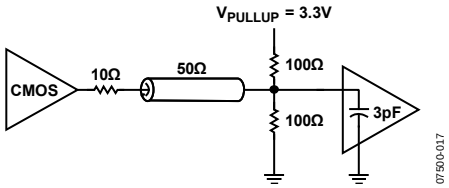


Figure 14. CMOS Output with Far-End Termination

POWER AND GROUNDING CONSIDERATIONS AND POWER SUPPLY REJECTION

Many applications seek high speed and performance under less than ideal operating conditions. In these application circuits, the implementation and construction of the PCB is as important as the circuit design. Proper RF techniques must be used for device selection, placement, and routing, as well as for power supply decoupling and grounding to ensure optimum performance.

OUTLINE DIMENSIONS

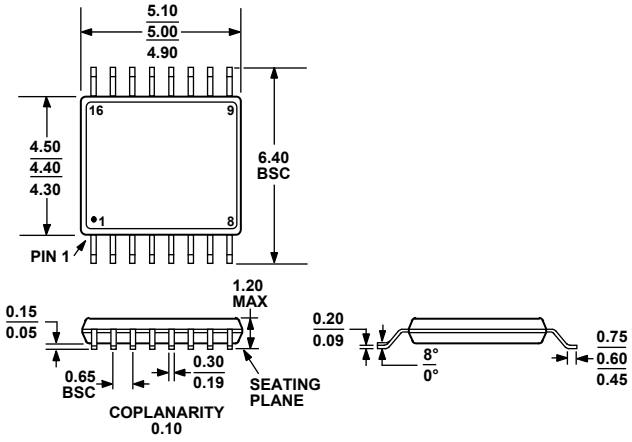


Figure 15. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9573ARUZ[1]	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD9573-EVALZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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